FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13743-5E

16-Bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90880 Series

MB90882(S)/F882A(S)/F883B(S)/F883BH(S)/F883C(S)/ MB90F884B(S)/F884BH(S)/F884C(S)/V880A-101/102

■ DESCRIPTION

The MB90880 series is a general-purpose 16-bit microcontroller, designed by FUJITSU MICROELECTRONICS, for process control of devices such as consumer appliances, which require high-speed real-time processing capabilities.

The instruction set of the F²MC-16LX CPU core retains the same AT architecture as the F²MC* family, with further refinements including high-level language instructions, an expanded addressing mode, enhanced multiplier-divider instructions and bit processing. In addition, a 32-bit accumulator is built in to enable long word processing.

As its peripheral resources, the MB90880 series has a 16-bit PPG, multi-function serial interface (software switch over enabled for SIO, UART and I²C) , 10-bit A/D converter, 16-bit I/O timer, 8/16-bit up-down counter, base timer (software switch over enabled for 16-bit reload timer, PWC timer, PPG timer and PWM timer), DTP / external interrupt and chip select pins.

* : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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■ FEATURES

- Clock
  Minimum instruction execution time : 30.3 ns / 4.125 MHz source oscillation × eight times
  (in internal operation : 33 MHz)
  PLL clock multiplication system
- Maximum memory space
  16 Mbytes
- Instruction set optimized for control applications
  Supported data types : bit, byte, word and long word
  Standard addressing modes : 23 types
  Enhanced high-precision calculation realized by 32-bit accumulator
  Signed multiplication/division instructions and extended RETI instruction functions
- Instruction set supporting high-level language (C language) and multi-task operations
  Introduction of system stack pointer
  Symmetrical instruction set and barrel shift instructions
- Improved execution speed
  4-byte queue
- Powerful interrupt functions
  Eight priority levels programmable; External interrupts : 24
- Data transfer functions (μDMAC)
  Up to 16 channels
- Built-in ROM
  Flash memory product : 256, 384 and 512 Kbytes; Mask ROM product : 256 Kbytes only
- Built-in RAM
  Flash memory product : 16, 24 and 30 Kbytes; Mask ROM product : 16 Kbytes only
- General-purpose ports
  Dual clock product : up to 81 channels; Single clock product : up to 83 channels
- A/D converter
  RC successive approximation conversion type : 20 channels (Resolution : 8 or 10 bits)
- Multi-function serial interface
  7 channels (software switchable between for SIO, UART and I^2C)
- 16-bit PPG
  8 channels
- 8/16-bit up-down counter/timer
  Event input pins : 6
  8-bit up-down counters : 2
  8-bit reload/compare registers : 2
- Base timer
  4 channels (software switchable between 16-bit reload timer, PWC timer, PPG timer, and PWM timer)
- 16-bit I/O timer
  Input capture × 2 channels, output compare × 6 channels, free run timer × 1 channel
- Built-in dual clock generator
- Low power consumption modes
  Stop mode, sleep mode, CPU intermittent operation mode, watch timer, time base timer mode
- Package
  QFP-100/LQFP-100
- Process
  CMOS technology
- Power supply voltage
  3V : Single power supply operation

■ PRODUCT LINEUP

Part number / Parameter	MB90882(S)	MB90F882A(S)	MB90F883B(S)/ MB90F883BH(S)/ MB90F883C(S)	MB90F884B(S)/ MB90F884BH(S)/ MB90F884C(S)	MB90V880A-101/ MB90V880A-102
Type	MASK ROM product	Flash memory product			Evaluation product
ROM size	256 Kbytes	256 Kbytes	384 Kbytes	512 Kbytes	—
RAM size	16 Kbytes	16 Kbytes	24 Kbytes	30 Kbytes	30 Kbytes
CPU functions	Number of instructions : 351 Instruction bit length : 8 bits, 16 bits Instruction length : 1 to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits Minimum execution time : 30.3 ns (machine clock : 33 MHz) The maximum operating frequency of MB90F883B(S), MB90F884B(S) is 25 MHz.				
Ports	General-purpose I/O ports : up to 81 for dual clock model, up to 83 for single clock model Pins X0A and X1A cannot be used as I/O ports in dual clock model General-purpose I/O ports (CMOS output)				
Multi-function serial interface	7 channels (software switchable between SIO, UART and I²C)				
16-bit PPG timer	8 channels				
8/16-bit up-down counter/timer	Event input pins : 6 8-bit up-down counters : 2 8-bit reload/compare registers : 2				
16-bit I/O timer — 16-bit free run timer	Number of channels : 1 Overflow interrupt				
16-bit I/O timer — Output compare (OCU)	Number of channels : 6 Pin input source : Match signal of compare register				
16-bit I/O timer — Input capture (ICU)	Number of channels : 2 Rewriting register by pin input (rising, falling or both edges)				
DTP/external interrupt circuit	External interrupt pins : 24 channels (edge/level support)				
Base timer	4 channels (software switchable between 16-bit reload timer, PWC timer, PPG timer, and PWM timer)				
Time base timer	18-bit counter Interrupt interval : 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (source oscillation : 4 MHz)				
A/D converter	Conversion accuracy : 8 or 10 bits can be switched Single conversion mode (Selected channel converted only once) Scan conversion mode (Multiple successive channels converted) Successive conversion mode (Selected channel converted repeatedly) Stop conversion mode (Selected channel converted and stopped repeatedly)				
Watchdog timer	Reset generation interval : 3.58 ms, 14.33 ms, 57.23ms, 458.75 ms (source oscillation : 4 MHz, minimum value)				

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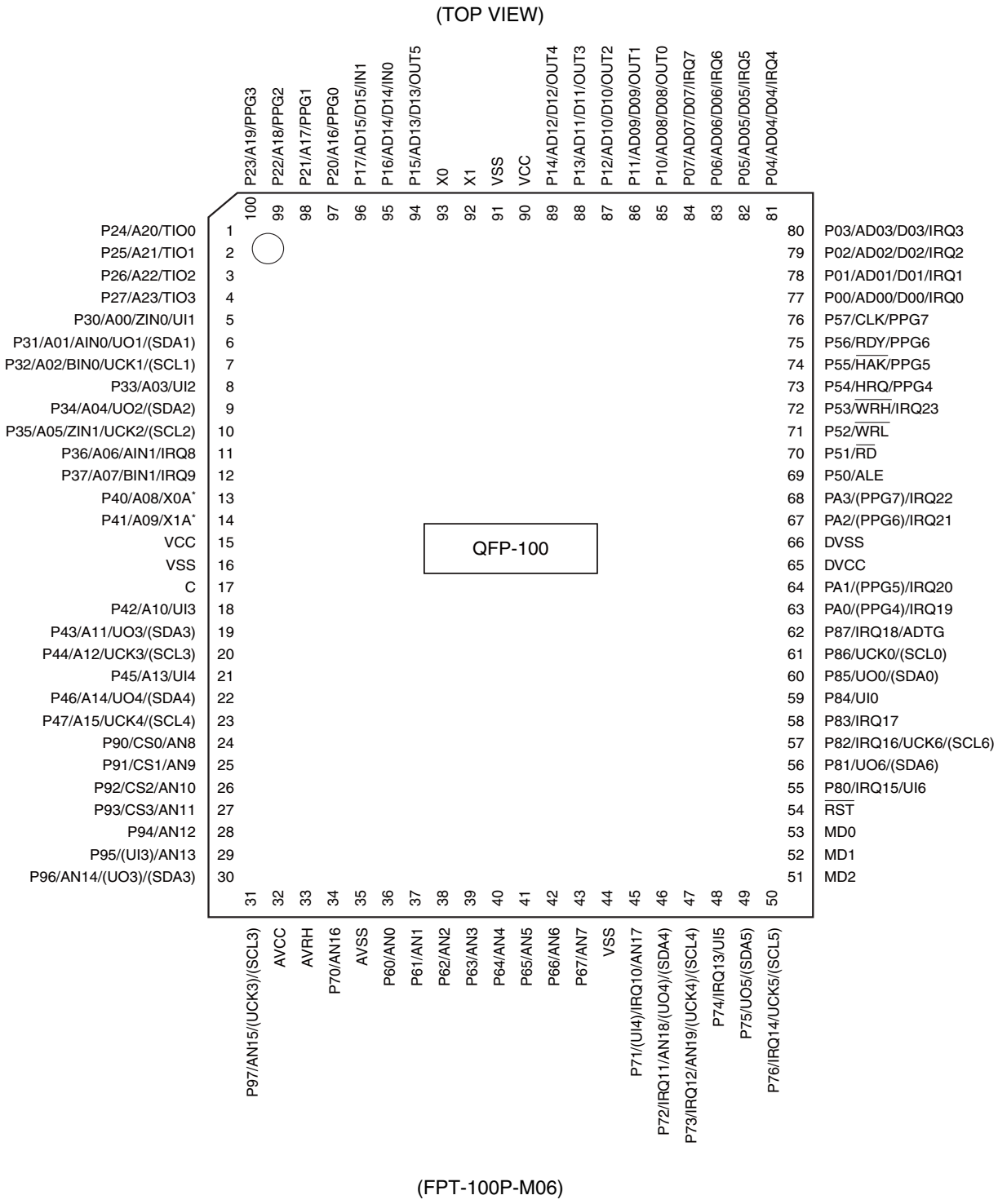
Part number / Parameter	MB90882(S)	MB90F882A(S)	MB90F883B(S)/ MB90F883BH(S)/ MB90F883C(S)	MB90F884B(S)/ MB90F884BH(S)/ MB90F884C(S)	MB90V880A-101/ MB90V880A-102
Low power consumption (standby) modes	Sleep, stop, CPU intermittent operation, watch timer, time base timer				
Flash memory	—	Flash security function/ accidental write prevention function (not available in MB90F883B(S), MB90F884B(S), MB90F883BH(S), MB90F884BH(S))			—
Process	CMOS technology				
Emulator-specific power supply*	—				Yes

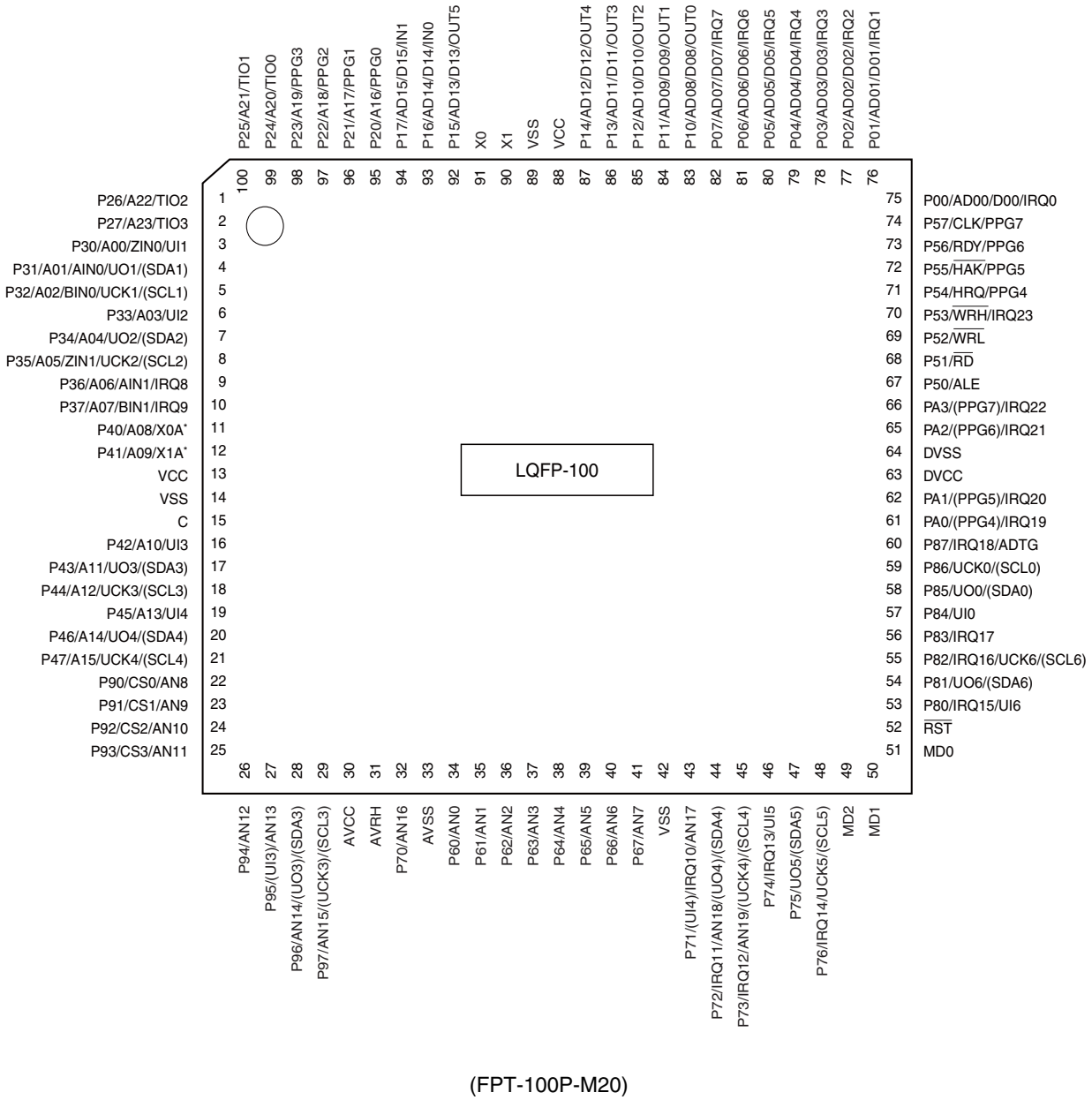
* : It is setting of Jumper switch (TOOL VCC) when emulator is used. Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

■ PIN ASSIGNMENTS



(FPT-100P-M06)

* : Dual clock product is sub clock oscillation pin.
Single clock product is P40/A08 and P41/A09 pins.



(FPT-100P-M20)

* : Dual clock product is sub clock oscillation pin.
Single clock product is P40/A08 and P41/A09 pins.

■ PIN DESCRIPTIONS

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
1	3	P26	D	General-purpose I/O port
		A22		Higher address output pin (A22) when corresponding bit in external address output control register (HACR) is set to "0".
		TIO2		Base timer I/O pin (ch.2)
2	4	P27	D	General-purpose I/O port
		A23		Higher address output pin (A23) when corresponding bit in external address output control register (HACR) is set to "0".
		TIO3		Base timer I/O pin (ch.3)
3	5	P30	E	General-purpose I/O port
		A00		External address pin in non-multiplex mode.
		ZIN0		8/16-bit up-down counter/timer input pin (ch.0)
		UI1		Multi-function serial input pin
4	6	P31	E	General-purpose I/O port
		A01		External address pin in non-multiplex mode.
		AIN0		8/16-bit up-down counter/timer input pin (ch.0)
		UO1/ (SDA1)		Multi-function serial output pin This pin operates as UO1 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA1 when it is used in an I²C (operation mode 4).
5	7	P32	E	General-purpose I/O port
		A02		External address pin in non-multiplex mode.
		BIN0		8/16-bit up-down counter/timer input pin (ch.0)
		UCK1/ (SCL1)		Multi-function serial clock I/O pin This pin operates as UCK1 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL1 when it is used in an I²C (operation mode 4).
6	8	P33	E	General-purpose I/O port
		A03		External address pin in non-multiplex mode.
		UI2		Multi-function serial input pin
7	9	P34	E	General-purpose I/O port
		A04		External address pin in non-multiplex mode.
		UO2/ (SDA2)		Multi-function serial output pin This pin operates as UO2 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA2 when it is used in an I²C (operation mode 4).

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
8	10	P35	E	General-purpose I/O port
		A05		External address pin in non-multiplex mode.
		ZIN1		8/16-bit up-down counter/timer input pin (ch.1)
		UCK2/ (SCL2)		Multi-function serial clock I/O pin This pin operates as UCK2 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL2 when it is used in an I²C (operation mode 4).
9	11	P36	D	General-purpose I/O port
		A06		External address pin in non-multiplex mode.
		AIN1		8/16-bit up-down counter/timer input pin (ch.1)
		IRQ8		External interrupt input pin
10	12	P37	D	General-purpose I/O port
		A07		External address pin in non-multiplex mode.
		BIN1		8/16-bit up-down counter/timer input pin (ch.1)
		IRQ9		External interrupt input pin
11	13	P40	A/D	General-purpose I/O port (Only for single clock model)
		A08		External address pin in non-multiplex mode. (Only for single clock model)
		X0A		32 kHz oscillator connecting pin (Only for dual clock model)
12	14	P41	A/D	General-purpose I/O port (Only for single clock model)
		A09		External address pin in non-multiplex mode. (Only for single clock model)
		X1A		32 kHz oscillator connecting pin (Only for dual clock model)
13	15	VCC	—	Power supply pin
14	16	VSS	—	Power supply pin (GND)
15	17	C	—	Regulator stabilization capacity connecting pin It should be connected to a 0.47µF ceramic capacitor.
16	18	P42	E	General-purpose I/O port
		A10		External address pin in non-multiplex mode.
		UI3		Multi-function serial input pin
17	19	P43	E	General-purpose I/O port
		A11		External address pin in non-multiplex mode.
		UO3/ (SDA3)		Multi-function serial output pin This pin operates as UO3 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA3 when it is used in an I²C (operation mode 4).

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
18	20	P44	E	General-purpose I/O port
		A12		External address pin in non-multiplex mode.
		UCK3/ (SCL3)		Multi-function serial clock I/O pin This pin operates as UCK3 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL3 when it is used in an I²C (operation mode 4).
19	21	P45	E	General-purpose I/O port
		A13		External address pin in non-multiplex mode.
		UI4		Multi-function serial input pin
20	22	P46	E	General-purpose I/O port
		A14		External address pin in non-multiplex mode.
		UO4/ (SDA4)		Multi-function serial output pin This pin operates as UO4 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA4 when it is used in an I²C (operation mode 4).
21	23	P47	E	General-purpose I/O port
		A15		External address pin in non-multiplex mode.
		UCK4/ (SCL4)		Multi-function serial clock I/O pin This pin operates as UCK4 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL4 when it is used in an I²C (operation mode 4).
22	24	P90	H	General-purpose I/O port
		CS0		Chip select 0 output pin
		AN8		Analog input pin
23	25	P91	H	General-purpose I/O port
		CS1		Chip select 1 output pin
		AN9		Analog input pin
24	26	P92	H	General-purpose I/O port
		CS2		Chip select 2 output pin
		AN10		Analog input pin
25	27	P93	H	General-purpose I/O port
		CS3		Chip select 3 output pin
		AN11		Analog input pin
26	28	P94	H	General-purpose I/O port
		AN12		Analog input pin
27	29	P95	K	General-purpose I/O port
		AN13		Analog input pin
		(UI3)		Multi-function serial input pin (when the P95FS bit in P9FSR register is “1”)

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
28	30	P96	K	General-purpose I/O port
		AN14		Analog input pin
		(UO3)/ (SDA3)		Multi-function serial output pin This pin operates as UO3 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA3 when it is used in an I²C (operation mode 4). (when the P96FS bit in P9FSR register is “1”)
29	31	P97	K	General-purpose I/O port
		AN15		Analog input pin
		(UCK3)/ (SCL3)		Multi-function serial clock I/O pin This pin operates as UCK3 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL3 when it is used in an I²C (operation mode 4). (when the P97FS bit in P9FSR register is “1”)
30	32	AVCC	—	A/D converter power supply pin
31	33	AVRH	—	Reference voltage input pin for A/D converter This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AVCC.
32	34	P70	H	General-purpose I/O port
		AN16		Analog input pin
33	35	AVSS	-	A/D converter analog GND pin
34	36	P60	H	General-purpose I/O port
		AN0		Analog input pin
35	37	P61	H	General-purpose I/O port
		AN1		Analog input pin
36	38	P62	H	General-purpose I/O port
		AN2		Analog input pin
37	39	P63	H	General-purpose I/O port
		AN3		Analog input pin
38	40	P64	H	General-purpose I/O port
		AN4		Analog input pin
39	41	P65	H	General-purpose I/O port
		AN5		Analog input pin
40	42	P66	H	General-purpose I/O port
		AN6		Analog input pin
41	43	P67	H	General-purpose I/O port
		AN7		Analog input pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
42	44	VSS	—	Power supply pin (GND)
43	45	P71	K	General-purpose I/O port
		IRQ10		External interrupt input pin
		AN17		Analog input pin
		(UI4)		Multi-function serial input pin (when the P71FS bit in P7FSR register is “1”)
44	46	P72	K	General-purpose I/O port
		IRQ11		External interrupt input pin
		AN18		Analog input pin
		(UO4)/ (SDA4)		Multi-function serial output pin This pin operates as UO4 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA4 when it is used in an I²C (operation mode 4). (when the P72FS bit in P7FSR register is “1”)
45	47	P73	K	General-purpose I/O port
		IRQ12		External interrupt input pin
		AN19		Analog input pin
		(UCK4)/ (SCL4)		Multi-function serial clock I/O pin This pin operates as UCK4 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL4 when it is used in an I²C (operation mode 4). (when the P73FS bit in P7FSR register is “1”)
46	48	P74	G	General-purpose I/O port
		IRQ13		External interrupt input pin
		UI5		Multi-function serial input pin
47	49	P75	G	General-purpose I/O port
		UO5/ (SDA5)		Multi-function serial output pin This pin operates as UO5 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).
48	50	P76	G	General-purpose I/O port
		IRQ14		External interrupt input pin
		UCK5/ (SCL5)		Multi-function serial clock I/O pin This pin operates as UCK5 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL5 when it is used in an I²C (operation mode 4).
49	51	MD2	M	Operation mode specification input pin
50	52	MD1	L	Operation mode specification input pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
51	53	MD0	L	Operation mode specification input pin
52	54	$\overline{RST}$	B	Reset input pin
53	55	P80	G	General-purpose I/O port
		IRQ15		External interrupt input pin
		UI6		Multi-function serial input pin
54	56	P81	G	General-purpose I/O port
		UO6/ (SDA6)		Multi-function serial output pin This pin operates as UO6 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).
55	57	P82	G	General-purpose I/O port
		IRQ16		External interrupt input pin
		UCK6/ (SCL6)		Multi-function serial clock I/O pin This pin operates as UCK6 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL6 when it is used in an I²C (operation mode 4).
56	58	P83	I	General-purpose I/O port
		IRQ17		External interrupt input pin
57	59	P84	G	General-purpose I/O port
		UI0		Multi-function serial input pin
58	60	P85	G	General-purpose I/O port
		UO0/ (SDA0)		Multi-function serial output pin This pin operates as UO0 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SDA0 when it is used in an I²C (operation mode 4).
59	61	P86	G	General-purpose I/O port
		UCK0/ (SCL0)		Multi-function serial clock I/O pin This pin operates as UCK0 when it is used in a UART/CSIO/LIN-UART (operation modes 0 to 3) and as SCL0 when it is used in an I²C (operation mode 4).
60	62	P87	I	General-purpose I/O port
		IRQ18		External interrupt input pin
		ADTG		External trigger input pin, when A/D converter is used.
61	63	PA0	J	General-purpose I/O port
		IRQ19		External interrupt input pin
		(PPG4)		PPG timer output pin (when the PA0FS bit in PAFSR register is “1”)

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
62	64	PA1	J	General-purpose I/O port
		IRQ20		External interrupt input pin
		(PPG5)		PPG timer output pin (when the PA1FS bit in PAFSR register is "1")
63	65	DVCC	—	PA port power supply pin
64	66	DVSS	—	PA port power supply pin (GND)
65	67	PA2	J	General-purpose I/O port
		IRQ21		External interrupt input pin
		(PPG6)		PPG timer output pin (when the PA2FS bit in PAFSR register is "1")
66	68	PA3	J	General-purpose I/O port
		IRQ22		External interrupt input pin
		(PPG7)		PPG timer output pin (when the PA3FS bit in PAFSR register is "1")
67	69	P50	F	General-purpose I/O port
		ALE		Address latch enable signal (ALE) pin in external bus mode.
68	70	P51	F	General-purpose I/O port
		$\overline{RD}$		Read strobe output ($\overline{RD}$) pin in external bus mode.
69	71	P52	F	General-purpose I/O port
		$\overline{WRL}$		Lower data write strobe output ($\overline{WRL}$) pin in external bus mode, and serves as a general-purpose I/O port when WRE bit in EPCR register is "0".
70	72	P53	F	General-purpose I/O port
		$\overline{WRH}$		Higher data write strobe output ($\overline{WRH}$) pin in external bus mode with 16-bit bus width, and serves as a general-purpose I/O port when WRE bit in EPCR register is "0".
		IRQ23		External interrupt input pin
71	73	P54	F	General-purpose I/O port
		HRQ		Hold request input (HRQ) pin in external bus mode, and serves as a general-purpose I/O port when HDE bit in EPCR register is "0".
		PPG4		PPG timer output pin
72	74	P55	F	General-purpose I/O port
		$\overline{HAK}$		Hold acknowledge output ($\overline{HAK}$) pin in external bus mode, and serves as a general-purpose I/O port when HDE bit in EPCR register is "0".
		PPG5		PPG timer output pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
73	75	P56	F	General-purpose I/O port
		RDY		External ready input (RDY) pin in external bus mode, and serves as a general-purpose I/O port when RYE bit in EPCR register is "0".
		PPG6		PPG timer output pin
74	76	P57	F	General-purpose I/O port
		CLK		Machine cycle clock output (CLK) pin in external bus mode, and serves as a general-purpose I/O port when CKE bit in EPCR register is "0".
		PPG7		PPG timer output pin
75	77	P00	C	General-purpose I/O port
		AD00/ D00		Lower external address/data bus I/O pin (AD00) in multiplex mode.
				Lower external data bus output pin (D00) in non-multiplex mode.
		IRQ0		External interrupt input pin
76	78	P01	C	General-purpose I/O port
		AD01/ D01		External address/lower data bus I/O pin (AD01) in multiplex mode.
				Lower external data bus output pin (D01) in non-multiplex mode.
		IRQ1		External interrupt input pin
77	79	P02	C	General-purpose I/O port
		AD02/ D02		External address/lower data bus I/O pin (AD02) in multiplex mode.
				Lower external data bus output pin (D02) in non-multiplex mode.
		IRQ2		External interrupt input pin
78	80	P03	C	General-purpose I/O port
		AD03/ D03		External address/lower data bus I/O pin (AD03) in multiplex mode.
				Lower external data bus output pin (D03) in non-multiplex mode.
		IRQ3		External interrupt input pin
79	81	P04	C	General-purpose I/O port
		AD04/ D04		Lower external address/data bus I/O pin (AD04) in multiplex mode.
				Lower external data bus output pin (D04) in non-multiplex mode.
		IRQ4		External interrupt input pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
80	82	P05	C	General-purpose I/O port
		AD05/ D05		Lower external address/data bus I/O pin (AD05) in multiplex mode.
				Lower external data bus output pin (D05) in non-multiplex mode.
		IRQ5		External interrupt input pin
81	83	P06	C	General-purpose I/O port
		AD06/ D06		Lower external address/data bus I/O pin (AD06) in multiplex mode.
				Lower external data bus output pin (D06) in non-multiplex mode.
		IRQ6		External interrupt input pin
82	84	P07	C	General-purpose I/O port
		AD07/ D07		Lower external address/data bus I/O pin (AD07) in multiplex mode.
				Lower external data bus output pin (D07) in non-multiplex mode.
		IRQ7		External interrupt input pin
83	85	P10	C	General-purpose I/O port
		AD08/ D08		Higher external address/data bus I/O pin (AD08) in multiplex mode.
				Higher external data output pin (D08) in non-multiplex mode.
		OUT0		Output compare event output pin
84	86	P11	C	General-purpose I/O port
		AD09/ D09		Higher external address/data bus I/O pin (AD09) in multiplex mode.
				Higher external data output pin (D09) in non-multiplex mode.
		OUT1		Output compare event output pin
85	87	P12	C	General-purpose I/O port
		AD10/ D10		Higher external address/data bus I/O pin (AD10) in multiplex mode.
				Higher external data output pin (D10) in non-multiplex mode.
		OUT2		Output compare event output pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
86	88	P13	C	General-purpose I/O port
		AD11/ D11		Higher external address/data bus I/O pin (AD11) in multiplex mode.
				Higher external data output pin (D11) in non-multiplex mode.
		OUT3		Output compare event output pin
87	89	P14	C	General-purpose I/O port
		AD12/ D12		Higher external address/data bus I/O pin (AD12) in multiplex mode.
				Higher external data output pin (D12) in non-multiplex mode.
		OUT4		Output compare event output pin
88	90	VCC	—	Power supply pin
89	91	VSS	—	Power supply pin (GND)
90	92	X1	A	Main oscillator connecting pin
91	93	X0	A	Main oscillator connecting pin
92	94	P15	C	General-purpose I/O port
		AD13/ D13		Higher external address/data bus I/O pin (AD13) in multiplex mode.
				Higher external data output pin (D13) in non-multiplex mode.
		OUT5		Output compare event output pin
93	95	P16	C	General-purpose I/O port
		AD14/ D14		Higher external address/data bus I/O pin (AD14) in multiplex mode.
				Higher external data output pin (D14) in non-multiplex mode.
		IN0		Trigger input pin for input capture ch.0
94	96	P17	C	General-purpose I/O port
		AD15/ D15		Higher external address/data bus I/O pin (AD15) in multiplex mode.
				Higher external data output pin (D15) in non-multiplex mode.
		IN1		Trigger input pin for input capture ch.1
95	97	P20	D	General-purpose I/O port
		A16		Higher address output pin (A16) when corresponding bit in external address output control register (HACR) is set to "0".
		PPG0		PPG timer output pin

(Continued)

(Continued)

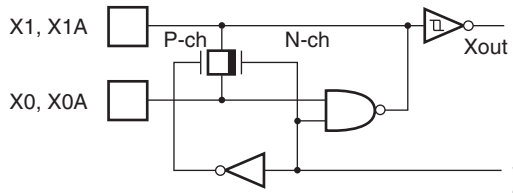
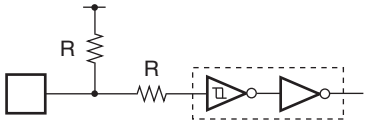
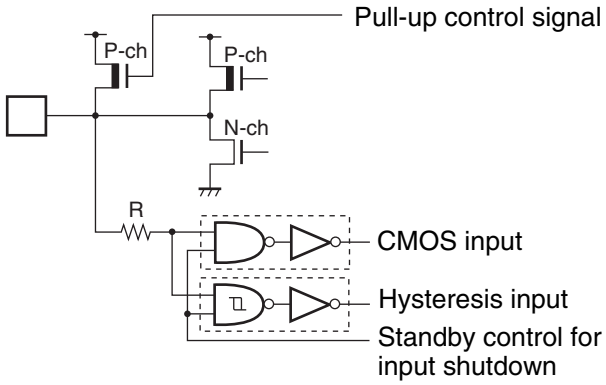
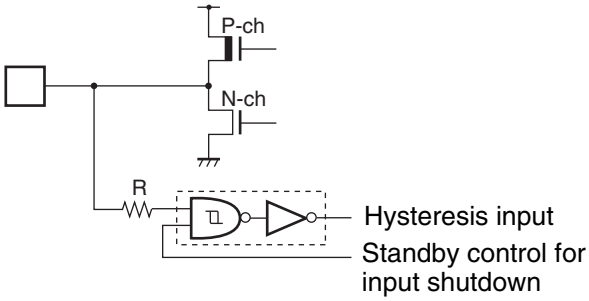
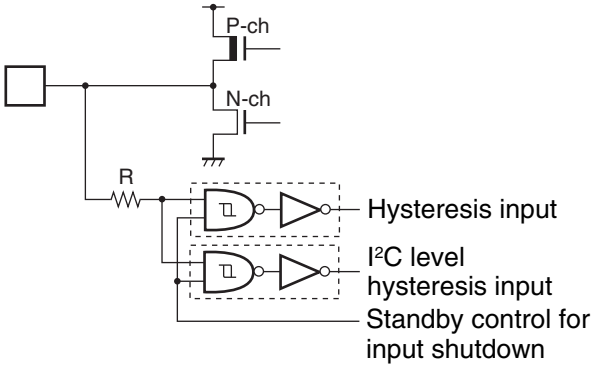
Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
96	98	P21	D	General-purpose I/O port
		A17		Higher address output pin (A17) when corresponding bit in external address output control register (HACR) is set to "0".
		PPG1		PPG timer output pin
97	99	P22	D	General-purpose I/O port
		A18		Higher address output pin (A18) when corresponding bit in external address output control register (HACR) is set to "0".
		PPG2		PPG timer output pin
98	100	P23	D	General-purpose I/O port
		A19		Higher address output pin (A19) when corresponding bit in external address output control register (HACR) is set to "0".
		PPG3		PPG timer output pin
99	1	P24	D	General-purpose I/O port
		A20		Higher address output pin (A20) when corresponding bit in external address output control register (HACR) is set to "0".
		TIO0		Base timer I/O pin (ch.0)
100	2	P25	D	General-purpose I/O port
		A21		Higher address output pin (A21) when corresponding bit in external address output control register (HACR) is set to "0".
		TIO1		Base timer I/O pin (ch.1)

*1 : LQFP : FPT-100P-M20

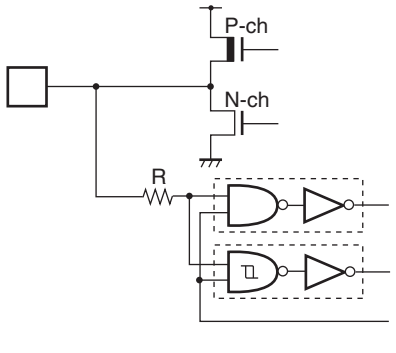
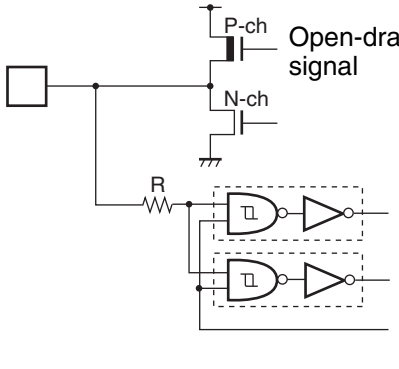
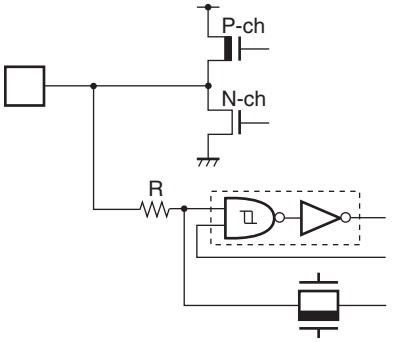
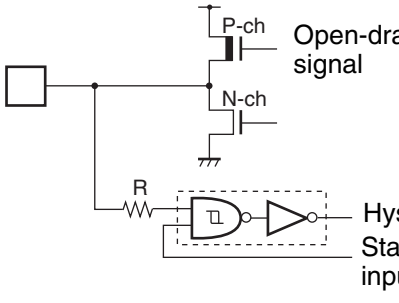
*2 : QFP : FPT-100P-M06

*3 : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

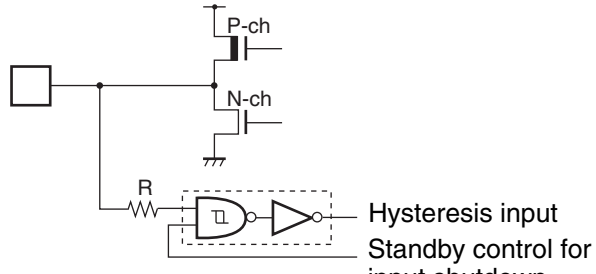
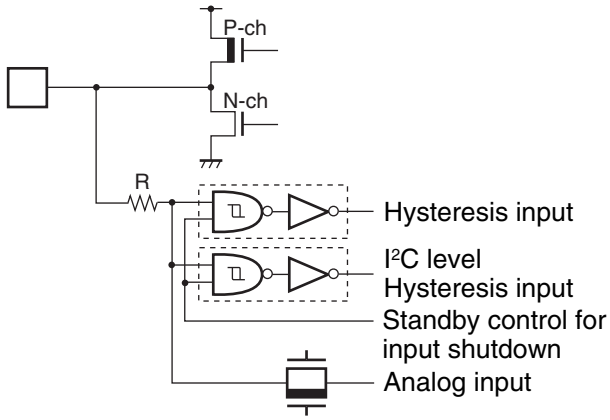
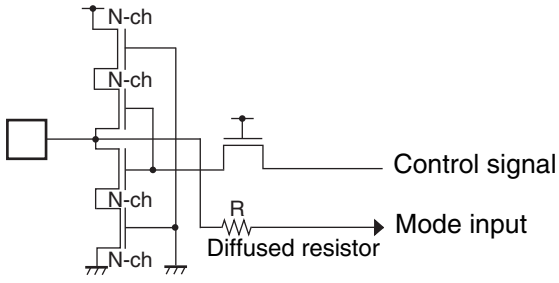
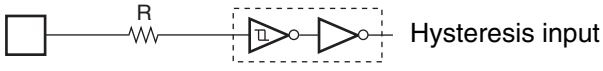
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistance X1, X0 : approx. 1 MΩ X1A, X0A : approx. 10 MΩ • Standby control provided
B		Hysteresis input with pull-up resistor
C		• Input pull-up resistor control provided • CMOS level output • Hysteresis input • CMOS input (in external bus mode)
D		• CMOS level output • Hysteresis input
E		• CMOS level output • Hysteresis input • I²C level hysteresis input

(Continued)

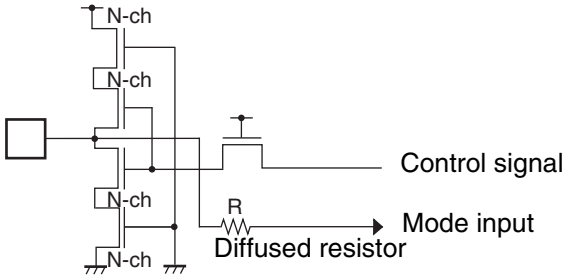
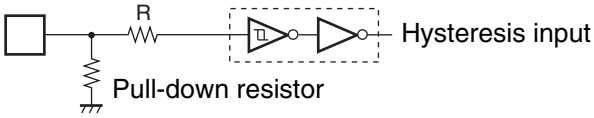
Type	Circuit	Remarks
F		• CMOS level output • Hysteresis input • CMOS input (in external bus mode)
G		• CMOS level output (Open-drain control provided) • 5 V tolerant • Hysteresis input • I²C level hysteresis input
H		• CMOS level output • Hysteresis input • Analog input
I		• CMOS level output (Open-drain control provided) • 5 V tolerant • Hysteresis input

(Continued)

Type	Circuit	Remarks
J		• CMOS/level output (high-current type) • Hysteresis input
K		• CMOS level output • Hysteresis input • Analog input • I²C level hysteresis input
L	Flash memory product 	Flash memory product • CMOS level input • High-voltage control for flash test provided
	MASK ROM product 	MASK ROM product Hysteresis input

(Continued)

(Continued)

Type	Circuit	Remarks
M	Flash memory product  	Flash memory product • CMOS level input • High-voltage control for flash test provided
	MASK ROM product, Evaluation product  	With pull-down resistor Hysteresis input

■ HANDLING DEVICES

1. Maximum rated voltages for the prevention of latch-up

Be cautious not to exceed the absolute maximum rating.

CMOS ICs may cause latch-up, when a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins other than medium-to-high resistant pins, or when a voltage exceeding the rating is applied between VCC and VSS pins.

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Take the utmost care not to let it occur.

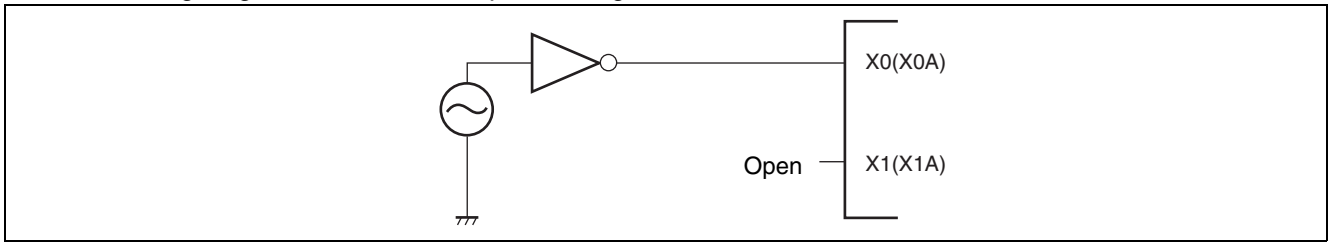
Likewise, care must be taken not to allow the analog power supply (AV_{CC}, AVRH) and analog input to exceed the digital power supply (V_{CC}) when turning on or off any analog system.

2. Handling unused pins

Leaving unused input pins open may cause a malfunction or latch-up which leads to fatal damage to the device. Therefore, they must be pulled up or down through at least 2 kΩ resistance. Also, any unused I/O pin should be left open in the output state, or set to the input state and handled in the same way as an unused input pin.

3. Notes on using external clock

Even when an external clock is being used, oscillation stabilization wait time is required for a power-on reset or release from sub clock mode or stop mode.
The following diagram shows an example of using an external clock.



4. Handling power supply pins (VCC/VSS)

When multiple VCC and VSS pins supply pins are used, all the power supply pins must be connected to external power and ground lines due to the device design, to reduce latch-up and unwanted radiation, prevent abnormal operation of strobe signals caused by the rise in the ground level and to conform to the total output current rating. Make sure to connect the VCC and VSS pins of this device via lowest impedance to power lines. It is recommended that a bypass capacitor of around 0.1 µF be placed between the VCC and VSS pins near the device.

5. Crystal oscillator circuit

Noises around X0/X1 or X0A/X1A pins may cause abnormal operations. It is strongly recommended to provide bypass capacitors via shortest distance from X0/X1, X0A/X1A pins, crystal oscillator (or ceramic oscillator) and ground lines and also not to allow the lines of the oscillation circuit to cross the lines of other circuits. This will ensure stable operations of the printed circuit boards. Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

6. Notes on PLL clock mode operation

If an oscillator comes off or clock input stops during PLL clock mode operation, this microcontroller may continue its operation using a free-running frequency from a self-excited oscillation circuit within PLL. This is not a guaranteed operation.

7. Power-on and power-off sequence of A/D converter and analog input

Turn on the A/D converters (AV_{CC}, AVRH) and analog inputs (AN0 to AN19) after turning on the digital power supply (V_{CC}) .

During power-off, turn off the digital power supply (V_{CC}) after turning off the A/D converters and analog inputs (AN0 to AN19) .

In this case, make sure that AVRH does not exceed AV_{CC} during the power-on/power-off procedure.

Also make sure that the input voltage does not exceed AV_{CC} when a pin which is also used as an analog input is used as an input port.

8. Handling power supply pins on A/D converter-mounted models

Make sure to achieve "AV_{CC} = AVRH = V_{CC}" and "AV_{SS} = V_{SS}" in connecting the circuits, even when not using the A/D converter function.

9. Note on power-up

To prevent the internal regulator from malfunctioning, maintain the voltage rise time at 50 µs (between 0.2V and 2.7V) or more during power-up.

10. Stabilization of power supply

Even when the V_{CC} power supply voltage is within the specified operating range, it may still cause the device to malfunction, if the power supply changes rapidly. For stabilization reference, it is recommended to control the supply voltage so that V_{CC} ripple variations (P-P values) at commercial frequencies (50/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

11. Note of MB90F883B(S), MB90F884B(S)

- Maximum operating frequency is 25 MHz.
- MB90F883B(S) and MB90F884B(S) do not contain the flash security function or protect function against erroneous write operation.

12. Note of MB90F883BH(S), MB90F884BH(S)

MB90F883BH(S) and MB90F884BH(S) do not contain the flash security function or protect function against erroneous write operation.

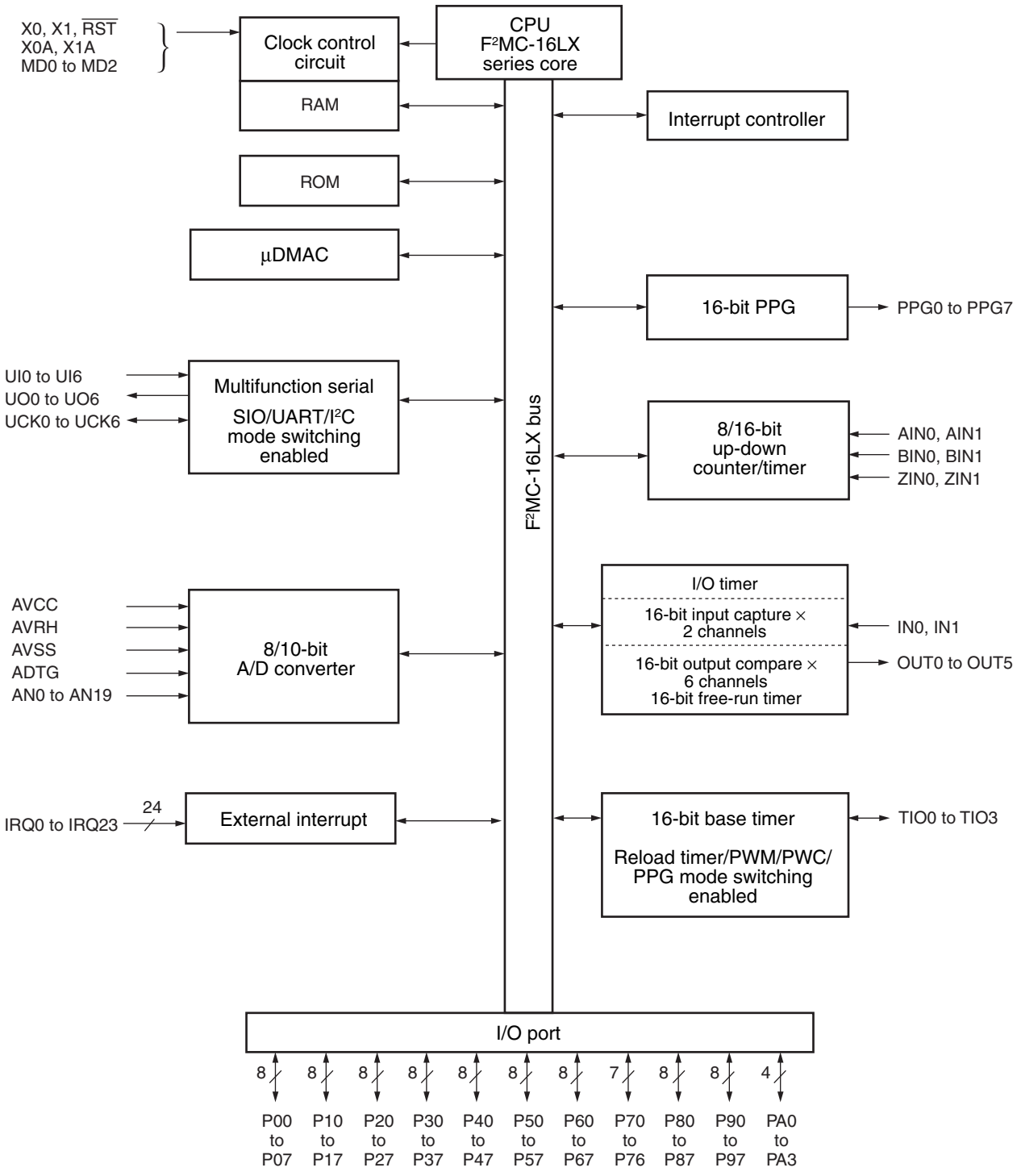
13. Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

14. When Using Dual Clock Products as Single Clock Products

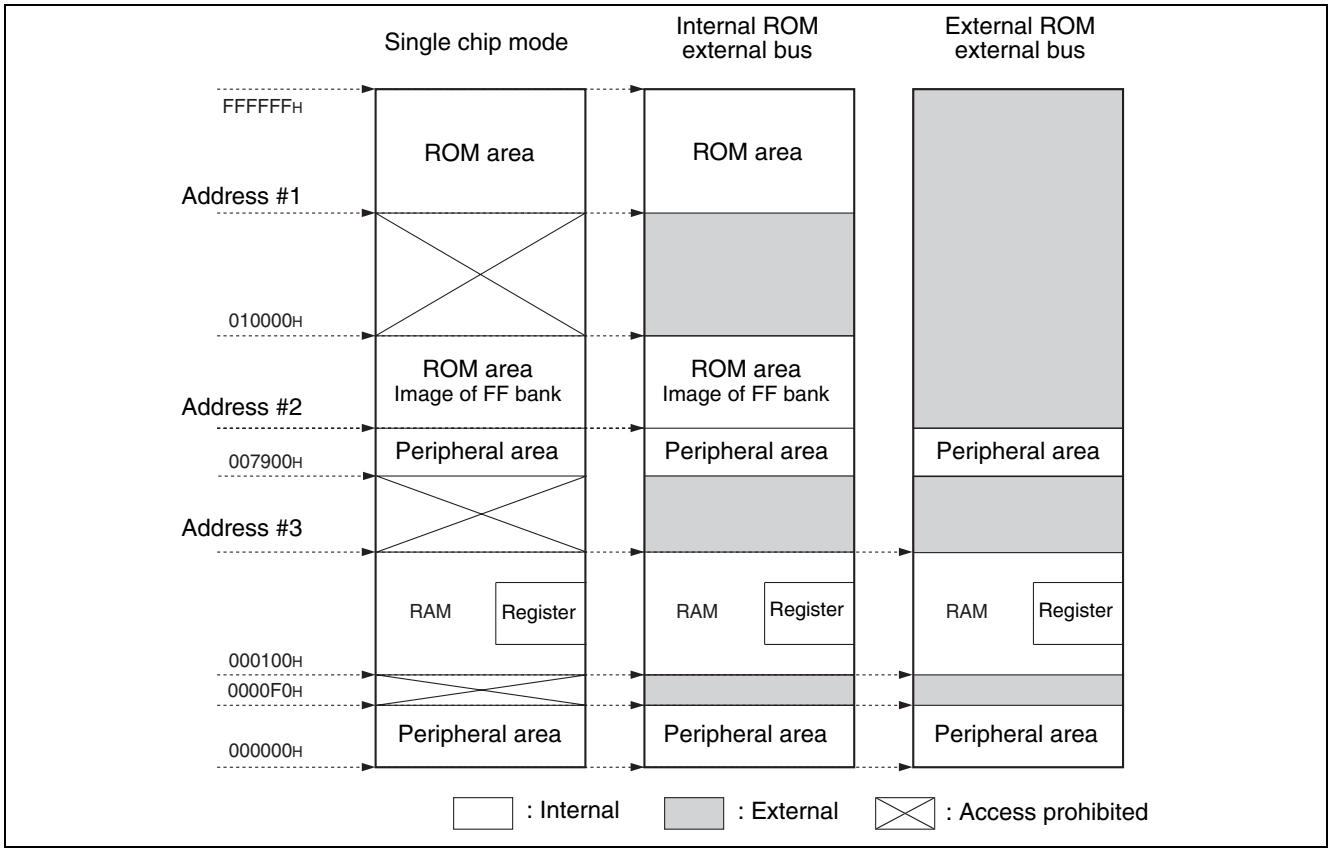
Use the X0A pin connected to Vss, and use the X1A pin as open.

■ BLOCK DIAGRAM



Note : The I/O ports shown in the diagram above are shared by other built-in function blocks. They cannot be used as I/O ports when used as pins for a built-in module.

■ MEMORY MAP

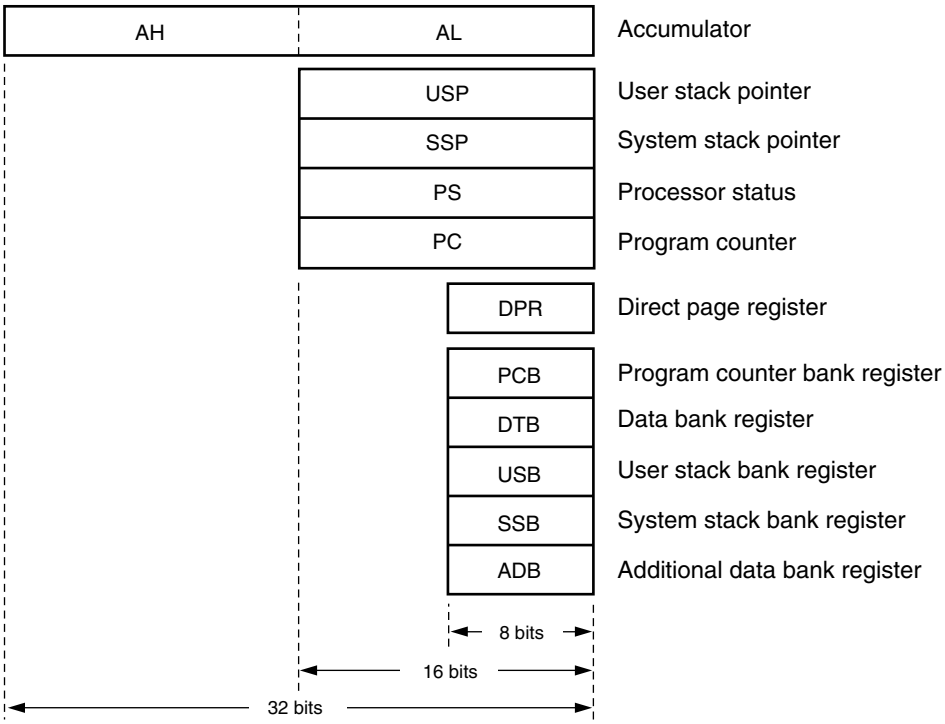


Parts No.	Address #1	Address #2	Address #3
MB90882 (S)	FC0000H	008000H fixed	004100H
MB90F882A (S)	FC0000H		004100H
MB90F883B (S) / MB90F883BH (S)/ MB90F883C(S)	FA0000H		006100H
MB90F884B (S) / MB90F884BH (S)/ MB90F884C(S)	F80000H		007900H
MB90V880A-101/102	(F80000H)		007900H

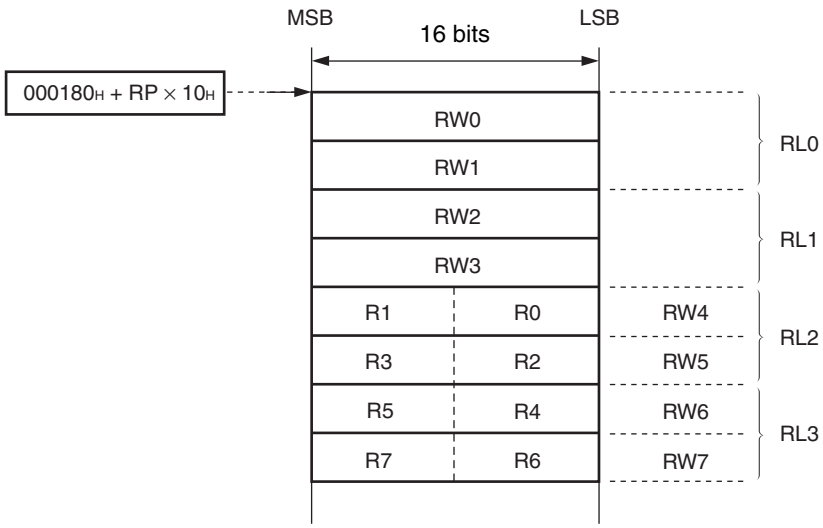
Note : The image of the ROM data in the FF bank appears at the top of the 00 bank in order to enable efficient use of the C compiler small memory model. The lower 16-bit address for the FF bank will be assigned to the same address as that for the 00 bank, so that tables in ROM can be referenced without declaring a "far" indication with the pointer.
For example, when accessing the address 00C000H, the actual access is to address FFC000H in ROM. Here the FF bank ROM area exceeds 32 Kbytes, it is not possible to show the entire area in the 00 bank image. Therefore, the ROM data in FF8000H to FFFFFFH can be seen in the 00 bank image, while the data in FF0000H to FF7FFFH can only be seen in the FF bank. For MB90F883B(S)/F883BH(S)/F883C(S), the areas of 006100H to 0078FFH and F80000H to F9FFFFH cannot be used as an external area.

■ F²MC-16LX CPU PROGRAMMING MODEL

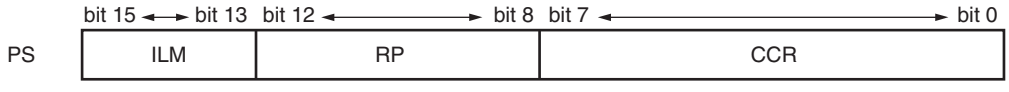
• Dedicated register



• General-purpose register



• Processor status



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Resource	Initial value
000000H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 data register	R/W	Port 7	XXXXXXXXB
000008H	PDR8	Port 8 data register	R/W	Port 8	XXXXXXXXB
000009H	PDR9	Port 9 data register	R/W	Port 9	XXXXXXXXB
00000AH	PDRA	Port A data register	R/W	Port A	XXXXXXXXB
00000BH	UDER	Up-down timer input enable register	R/W	Up-down timer input control	XX000000B
00000CH	ILSR0	Serial input level selection register 0	R/W	Multi-function serial control	00000000B
00000DH	ILSR1	Serial input level selection register 1	R/W		00000000B
00000EH	ILSR2	Serial input level selection register 2	R/W		---00000B
00000FH	Disabled				
000010H	DDR0	Port 0 direction register	R/W	Port 0	00000000B
000011H	DDR1	Port 1 direction register	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction register	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction register	R/W	Port 3	00000000B
000014H	DDR4	Port 4 direction register	R/W	Port 4	00000000B
000015H	DDR5	Port 5 direction register	R/W	Port 5	00000000B
000016H	DDR6	Port 6 direction register	R/W	Port 6	00000000B
000017H	DDR7	Port 7 direction register	R/W	Port 7	-0000000B
000018H	DDR8	Port 8 direction register	R/W	Port 8	00000000B
000019H	DDR9	Port 9 direction register	R/W	Port 9	00000000B
00001AH	DDRA	Port A direction register	R/W	Port A	----0000B
00001BH	ADER0	Analog input enable register 0	R/W	Port 6, A/D	11111111B
00001CH	ADER1	Analog input enable register 1	R/W	Port 9, A/D	11111111B
00001DH	ADER2	Analog input enable register 2	R/W	Port 7, A/D	----1111B
00001EH	RDR0	Port 0 input resistance register	R/W	Port 0 (pull-up resistance control)	00000000B
00001FH	RDR1	Port 1 input resistance register	R/W	Port 1 (pull-up resistance control)	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
000020H	SMR0	Serial bus mode register ch.0	R/W	Multi-function serial ch.0	$$$$$$$$B
000021H	SCR0/IBCR0	SCR0/IBCR0 serial bus control register/I²C bus control register ch.0	R/W		$$$$$$$$B
000022H	ESCR0/ IBSR0	Extended communication control register/I²C bus status register ch.0	R/W		$$$$$$$$B
000023H	SSR0	Serial status register ch.0	R/W		$$$$$$$$B
000024H	RDR00/ TDR00	Transmission/reception data register 0 ch.0	R,W		$$$$$$$$B
000025H	RDR10/ TDR10	Transmission/reception data register 1 ch.0	R,W		$$$$$$$$B
000026H	BGR00	Baud rate generator register 0 ch.0	R/W		$$$$$$$$B
000027H	BGR10	Baud rate generator register 1 ch.0	R/W		$$$$$$$$B
000028H	ISBA0	7-bit slave address register ch.0	R/W		00000000B
000029H	ISMK0	7-bit slave address mask register ch.0	R/W		01111111B
00002AH	SMR1	Serial bus mode register ch.1	R/W	Multi-function serial ch.1	$$$$$$$$B
00002BH	SCR1/IBCR1	Serial bus control register / I²C bus control register ch.1	R/W		$$$$$$$$B
00002CH	ESCR1/ IBSR1	Extended communication control register / I²C bus status register ch.1	R/W		$$$$$$$$B
00002DH	SSR1	Serial status register ch.1	R/W		$$$$$$$$B
00002EH	RDR01/ TDR01	Transmission/reception data register 0 ch.1	R,W		$$$$$$$$B
00002FH	RDR11/ TDR11	Transmission/reception data register 1 ch.1	R,W		$$$$$$$$B
000030H	BGR01	Baud rate generator register 0 ch.1	R/W		$$$$$$$$B
000031H	BGR11	Baud rate generator register 1 ch.1	R/W		$$$$$$$$B
000032H	ISBA1	7-bit slave address register ch.1	R/W		00000000B
000033H	ISMK1	7-bit slave address mask register ch.1	R/W		01111111B
000034H	ADCSL	Lower A/D control status register	R/W	A/D Converter	00011110B
000035H	ADCSH	Higher A/D control status register	R/W		00000000B
000036H	ADCRL	Lower A/D data register	R		XXXXXXXXB
000037H	ADCRH	Higher A/D data register	R		111111XXB
000038H	ADSRL	Lower A/D conversion channel setting register	R/W		00000000B
000039H	ADSRH	Higher A/D conversion channel setting register	R/W		00000000B
00003AH	Reserved				

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
00003B$_H$	PACSR1	Address detection control status register 1	R/W	Address match detection function	00000000$_B$
00003C$_H$	OLSR0	Output level selection register 0	R/W	Port 7 (N-ch open-drain control)	-000----$_B$
00003D$_H$	OLSR1	Output level selection register 1	R/W	Port 8 (N-ch open-drain control)	00000000$_B$
00003E$_H$	SMR2	Serial bus mode register ch.2	R/W	Multi-function serial ch.2	$$$$$$$$_B$
00003F$_H$	SCR2/IBCR2	Serial bus control register / I²C bus control register ch.2	R/W		$$$$$$$$_B$
000040$_H$	ESCR2/ IBSR2	Extended communication control register / I²C bus status register ch.2	R/W		$$$$$$$$_B$
000041$_H$	SSR2	Serial status register ch.2	R/W		$$$$$$$$_B$
000042$_H$	RDR02/ TDR02	Transmission/reception data register 0 ch.2	R,W		$$$$$$$$_B$
000043$_H$	RDR12/ TDR12	Transmission/reception data register 1 ch.2	R,W		$$$$$$$$_B$
000044$_H$	BGR02	Baud rate generator register 0 ch.2	R/W		$$$$$$$$_B$
000045$_H$	BGR12	Baud rate generator register 1 ch.2	R/W		$$$$$$$$_B$
000046$_H$	ISBA2	7-bit slave address register ch.2	R/W		00000000$_B$
000047$_H$	ISMK2	7-bit slave address mask register ch.2	R/W		01111111$_B$
000048$_H$	SMR3	Serial bus mode register ch.3	R/W	Multi-function serial ch.3	$$$$$$$$_B$
000049$_H$	SCR3/IBCR3	Serial bus control register / I²C bus control register ch.3	R/W		$$$$$$$$_B$
00004A$_H$	ESCR3/ IBSR3	Extended communication control register / I²C bus status register ch.3	R/W		$$$$$$$$_B$
00004B$_H$	SSR3	Serial status register ch.3	R/W		$$$$$$$$_B$
00004C$_H$	RDR03/ TDR03	Transmission/reception data register 0 ch.3	R,W		$$$$$$$$_B$
00004D$_H$	RDR13/ TDR13	Transmission/reception data register 1 ch.3	R,W		$$$$$$$$_B$
00004E$_H$	BGR03	Baud rate generator register 0 ch.3	R/W		$$$$$$$$_B$
00004F$_H$	BGR13	Baud rate generator register 1 ch.3	R/W		$$$$$$$$_B$
000050$_H$	ISBA3	7-bit slave address register ch.3	R/W		00000000$_B$
000051$_H$	ISMK3	7-bit slave address mask register ch.3	R/W		01111111$_B$
000052$_H$	SMR4	Serial bus mode register ch.4	R/W	Multi-function serial ch.4	$$$$$$$$_B$
000053$_H$	SCR4/IBCR4	Serial bus control register / I²C bus control register ch.4	R/W		$$$$$$$$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
000054H	ESCR4/ IBSR4	Extended communication control register / I²C bus status register ch.4	R/W	Multi-function serial ch.4	$$$$$$$$B
000055H	SSR4	Serial status register ch.4	R/W		$$$$$$$$B
000056H	RDR04/ TDR04	Transmission/reception data register 0 ch.4	R,W		$$$$$$$$B
000057H	RDR14/ TDR14	Transmission/reception data register 1 ch.4	R,W		$$$$$$$$B
000058H	BGR04	Baud rate generator register 0 ch.4	R/W		$$$$$$$$B
000059H	BGR14	Baud rate generator register 1 ch.4	R/W		$$$$$$$$B
00005AH	ISBA4	7-bit slave address register ch.4	R/W		00000000B
00005BH	ISMK4	7-bit slave address mask register ch.4	R/W		01111111B
00005CH	SMR5	Serial bus mode register ch.5	R/W	Multi-function serial ch.5	$$$$$$$$B
00005DH	SCR5/IBCR5	Serial bus control register / I²C bus control register ch.5	R/W		$$$$$$$$B
00005EH	ESCR5/ IBSR5	Extended communication control register / I²C bus status register ch.5	R/W		$$$$$$$$B
00005FH	SSR5	Serial status register ch.5	R/W		$$$$$$$$B
000060H	RDR05/ TDR05	Transmission/reception data register 0 ch.5	R,W		$$$$$$$$B
000061H	RDR15/ TDR15	Transmission/reception data register 1 ch.5	R,W		$$$$$$$$B
000062H	BGR05	Baud rate generator register 0 ch.5	R/W		$$$$$$$$B
000063H	BGR15	Baud rate generator register 1 ch.5	R/W		$$$$$$$$B
000064H	ISBA5	7-bit slave address register ch.5	R/W		00000000B
000065H	ISMK5	7-bit slave address mask register ch.5	R/W		01111111B
000066H	OCCP0	Lower output compare register (ch.0)	R/W	16-bit I/O timer output compare (ch.0 to ch.5)	00000000B
000067H		Higher output compare register (ch.0)			00000000B
000068H	OCCP1	Lower output compare register (ch.1)	R/W		00000000B
000069H		Higher output compare register (ch.1)			00000000B
00006AH	OCCP2	Lower output compare register (ch.2)	R/W		00000000B
00006BH		Higher output compare register (ch.2)			00000000B
00006CH	OCCP3	Lower output compare register (ch.3)	R/W		00000000B
00006DH		Higher output compare register (ch.3)			00000000B
00006EH	Reserved				
00006FH	ROMM	ROM mirror function selection register	R/W	ROM mirror function	-------1B

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
000070H	OCCP4	Lower output compare register (ch.4)	R/W	16-bit I/O timer output compare (ch.0 to ch.5)	00000000B
000071H		Higher output compare register (ch.4)			00000000B
000072H	OCCP5	Lower output compare register (ch.5)	R/W		00000000B
000073H		Higher output compare register (ch.5)			00000000B
000074H	OCS01	Lower output compare control register (ch.0, ch.1)	R/W		0000--00B
000075H		Higher output compare control register (ch.0, ch.1)	R/W		---00000B
000076H	OCS23	Lower output compare control register (ch.2, ch.3)	R/W		0000--00B
000077H		Higher output compare control register (ch.2, ch.3)	R/W		---00000B
000078H	OCS45	Lower output compare control register (ch.4, ch.5)	R/W		0000--00B
000079H		Higher output compare control register (ch.4, ch.5)	R/W		---00000B
00007AH	IPCP0	Lower input capture data register (ch.0)	R	16-bit I/O timer input capture (ch.0, ch.1)	XXXXXXXXB
00007BH		Higher input capture data register (ch.0)	R		XXXXXXXXB
00007CH	IPCP1	Lower input capture data register (ch.1)	R		XXXXXXXXB
00007DH		Higher input capture data register (ch.1)	R		XXXXXXXXB
00007EH	ICS01	Input capture control status register	R/W		00000000B
00007FH	ICE01	Input capture edge register	R		------XXB
000080H	TCDT	Lower timer counter data register	R/W	16-bit I/O timer free-run timer	00000000B
000081H	TCDT	Higher timer counter data register	R/W		00000000B
000082H	TCCS	Timer control status register	R/W		00000000B
000083H	TCCS	Timer control status register	R/W		XX-00000B
000084H	CPCLR	Lower compare clear register	R/W		XXXXXXXXB
000085H		Higher compare clear register			XXXXXXXXB
000086H to 00009AH	Reserved				
00009BH	DCSR	DMAC descriptor channel specification register	R/W	DMAC	00000000B
00009CH	DSRL	DMAC lower status register	R/W	DMAC	00000000B
00009DH	DSRH	DMAC higher status register	R/W	DMAC	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
00009E$_H$	PACSR0	Address detection control status register 0	R/W	Address match detection function	00000000$_B$
00009F$_H$	DIRR	Delayed interrupt source generation/ release register	R/W	Delayed interrupt generation module	-------0$_B$
0000A0$_H$	LPMCR	Low power consumption mode control register	W, R/W	Low power consumption	00011000$_B$
0000A1$_H$	CKSCR	Clock selection register	R, R/W		11111100$_B$
0000A2$_H$, 0000A3$_H$	Reserved				
0000A4$_H$	DSSR	DMAC stop status register	R/W	DMAC	00000000$_B$
0000A5$_H$	ARSR	Auto ready function selection register	W	External bus	0011--00$_B$
0000A6$_H$	HACR	External address output control register	W		********$_B$
0000A7$_H$	EPCR	Bus control signal selection register	W		1000*10-$_B$
0000A8$_H$	WDTC	Watchdog timer control register	R, W	Watchdog timer	XXXXX111$_B$
0000A9$_H$	TBTC	Time base timer control register	W, R/W	Time base timer	1XX00100$_B$
0000AA$_H$	WTC	Watch timer control register	R, R/W	Watch timer	10001000$_B$
0000AB$_H$	Reserved				
0000AC$_H$	DERL	DMAC lower enable register	R/W	DMAC	00000000$_B$
0000AD$_H$	DERH	DMAC higher enable register	R/W		00000000$_B$
0000AE$_H$	FMCS	Flash memory control status register	W, R/W	Flash memory I/F	000X0000$_B$
0000AF$_H$	Prohibited				
0000B0$_H$	ICR00	Interrupt control register 00	W, R/W	Interrupt control	00000111$_B$
0000B1$_H$	ICR01	Interrupt control register 01	W, R/W		00000111$_B$
0000B2$_H$	ICR02	Interrupt control register 02	W, R/W		00000111$_B$
0000B3$_H$	ICR03	Interrupt control register 03	W, R/W		00000111$_B$
0000B4$_H$	ICR04	Interrupt control register 04	W, R/W		00000111$_B$
0000B5$_H$	ICR05	Interrupt control register 05	W, R/W		00000111$_B$
0000B6$_H$	ICR06	Interrupt control register 06	W, R/W		00000111$_B$
0000B7$_H$	ICR07	Interrupt control register 07	W, R/W		00000111$_B$
0000B8$_H$	ICR08	Interrupt control register 08	W, R/W		00000111$_B$
0000B9$_H$	ICR09	Interrupt control register 09	W, R/W		00000111$_B$
0000BA$_H$	ICR10	Interrupt control register 10	W, R/W		00000111$_B$
0000BB$_H$	ICR11	Interrupt control register 11	W, R/W		00000111$_B$
0000BC$_H$	ICR12	Interrupt control register 12	W, R/W		00000111$_B$
0000BD$_H$	ICR13	Interrupt control register 13	W, R/W		00000111$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
0000BE$_H$	ICR14	Interrupt control register 14	W, R/W	Interrupt control	00000111$_B$
0000BF$_H$	ICR15	Interrupt control register 15	W, R/W		00000111$_B$
0000C0$_H$	CMR0	Chip select area MASK register 0	R/W	Bus interface	00001111$_B$
0000C1$_H$	CAR0	Chip select area register 0	R/W		11111111$_B$
0000C2$_H$	CMR1	Chip select area MASK register 1	R/W		00001111$_B$
0000C3$_H$	CAR1	Chip select area register 1	R/W		11111111$_B$
0000C4$_H$	CMR2	Chip select area MASK register 2	R/W		00001111$_B$
0000C5$_H$	CAR2	Chip select area register 2	R/W		11111111$_B$
0000C6$_H$	CMR3	Chip select area MASK register 3	R/W		00001111$_B$
0000C7$_H$	CAR3	Chip select area register 3	R/W		11111111$_B$
0000C8$_H$	CSCR	Chip select control register	R/W		----000*$_B$
0000C9$_H$	CALR	Chip select active level register	R/W		----0000$_B$
0000CA$_H$ to 0000CE$_H$	Reserved				
0000CF$_H$	PLLOS	PLL output selection register	W	PLL	------X0$_B$
0000D0$_H$	BAPL	DMA buffer address pointer (low)	R/W	DMAC	XXXXXXXX$_B$
0000D1$_H$	BAPM	DMA buffer address pointer (middle)	R/W		XXXXXXXX$_B$
0000D2$_H$	BAPH	DMA buffer address pointer (high)	R/W		XXXXXXXX$_B$
0000D3$_H$	DMACS	DMA control register	R/W		XXXXXXXX$_B$
0000D4$_H$	IOAL	DMAI/O register address pointer (low)	R/W		XXXXXXXX$_B$
0000D5$_H$	IOAH	DMAI/O register address pointer (high)	R/W		XXXXXXXX$_B$
0000D6$_H$	DCTL	DMA data counter (low)	R/W		XXXXXXXX$_B$
0000D7$_H$	DCTH	DMA data counter (high)	R/W		XXXXXXXX$_B$
0000D8$_H$ to 0000DF$_H$	Reserved				
0000E0$_H$	ENIR0	Interrupt/DTP enable register 0	R/W	DTP / external interrupt	00000000$_B$
0000E1$_H$	EIRR0	Interrupt/DTP source register 0	R/W		XXXXXXXX$_B$
0000E2$_H$	ELVR0	Request level setting register 0	R/W		00000000$_B$
0000E3$_H$		Request level setting register 0	R/W		00000000$_B$
0000E4$_H$	ENIR1	Interrupt/DTP enable register 1	R/W	DTP / external interrupt	00000000$_B$
0000E5$_H$	EIRR1	Interrupt/DTP source register 1	R/W		XXXXXXXX$_B$
0000E6$_H$	ELVR1	Request level setting register 1	R/W		00000000$_B$
0000E7$_H$		Request level setting register 1	R/W		00000000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
0000E8H	ENIR2	Interrupt/DTP enable register 2	R/W	DTP / external interrupt	XXXX0000B
0000E9H	EIRR2	Interrupt/DTP source register 2	R/W		XXXXXXXXB
0000EAH	ELVR2	Request level setting register 2	R/W		00000000B
0000EBH		Request level setting register 2	R/W		00000000B
0000ECH to 0000EFH	Reserved				
0000F0H to 0000FFH	External area				
000100H to 00017FH	RAM area/extended intelligent I/O service (EI²OS)				
000180H to #H*	RAM area				
007900H	PCNTL0	PPG0 lower control status register	R/W	16-bit PPG0	00000000B
007901H	PCNTH0	PPG0 higher control status register	R/W		00000001B
007902H	PCNTL1	PPG1 lower control status register	R/W	16-bit PPG1	00000000B
007903H	PCNTH1	PPG1 higher control status register	R/W		00000001B
007904H	PCNTL2	PPG2 lower control status register	R/W	16-bit PPG2	00000000B
007905H	PCNTH2	PPG2 higher control status register	R/W		00000001B
007906H	PCNTL3	PPG3 lower control status register	R/W	16-bit PPG3	00000000B
007907H	PCNTH3	PPG3 higher control status register	R/W		00000001B
007908H	PCNTL4	PPG4 lower control status register	R/W	16-bit PPG4	00000000B
007909H	PCNTH4	PPG4 higher control status register	R/W		00000001B
00790AH	PCNTL5	PPG5 lower control status register	R/W	16-bit PPG5	00000000B
00790BH	PCNTH5	PPG5 higher control status register	R/W		00000001B
00790CH	PCNTL6	PPG6 lower control status register	R/W	16-bit PPG6	00000000B
00790DH	PCNTH6	PPG6 higher control status register	R/W		00000001B
00790EH	PCNTL7	PPG7 lower control status register	R/W	16-bit PPG7	00000000B
00790FH	PCNTH7	PPG7 higher control status register	R/W		00000001B
007910H	PPGDIV	PPG0 output division setting register	R/W	16-bit PPG0	11111100B
007911H	Reserved				
007912H	PDCRL0	PPG0 down counter register	R	16-bit PPG0	11111111B
007913H	PDCRH0				11111111B
007914H	PCSRL0	PPG0 period setting register	W		11111111B
007915H	PCSRH0				11111111B

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
007916H	PUDUTL0	PPG0 duty setting register	W	16-bit PPG0	00000000B
007917H	PUDUTH0				00000000B
007918H	Disabled				
007919H	Disabled				
00791AH	PDCRL1	PPG1 down counter register	R	16-bit PPG1	11111111B
00791BH	PDCRH1				11111111B
00791CH	PCSRL1	PPG1 period setting register	W		11111111B
00791DH	PCSRH1				11111111B
00791EH	PUDUTL1	PPG1 duty setting register	W		00000000B
00791FH	PUDUTH1				00000000B
007920H	Disabled				
007921H	Disabled				
007922H	PDCRL2	PPG2 down counter register	R	16-bit PPG2	11111111B
007923H	PDCRH2				11111111B
007924H	PCSRL2	PPG2 period setting register	W		11111111B
007925H	PCSRH2				11111111B
007926H	PUDUTL2	PPG2 duty setting register	W		00000000B
007927H	PUDUTH2				00000000B
007928H	Disabled				
007929H	Disabled				
00792AH	PDCRL3	PPG3 down counter register	R	16-bit PPG3	11111111B
00792BH	PDCRH3				11111111B
00792CH	PCSRL3	PPG3 period setting register	W		11111111B
00792DH	PCSRH3				11111111B
00792EH	PUDUTL3	PPG3 duty setting register	W		00000000B
00792FH	PUDUTH3				00000000B
007930H	Disabled				
007931H	Disabled				
007932H	PDCRL4	PPG4 down counter register	R	16-bit PPG4	11111111B
007933H	PDCRH4				11111111B
007934H	PCSRL4	PPG4 period setting register	W		11111111B
007935H	PCSRH4				11111111B
007936H	PUDUTL4	PPG4 duty setting register	W		00000000B
007937H	PUDUTH4				00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
007938H	Disabled				
007939H	Disabled				
00793AH	PDCRL5	PPG5 down counter register	R	16-bit PPG5	11111111B
00793BH	PDCRH5				11111111B
00793CH	PCSRL5	PPG5 period setting register	W		11111111B
00793DH	PCSRH5				11111111B
00793EH	PUDUTL5	PPG5 duty setting register	W		00000000B
00793FH	PUDUTH5				00000000B
007940H	Disabled				
007941H	Disabled				
007942H	PDCRL6	PPG6 down counter register	R	16-bit PPG6	11111111B
007943H	PDCRH6				11111111B
007944H	PCSRL6	PPG6 period setting register	W		11111111B
007945H	PCSRH6				11111111B
007946H	PUDUTL6	PPG6 duty setting register	W		00000000B
007947H	PUDUTH6				00000000B
007948H	Disabled				
007949H	Disabled				
00794AH	PDCRL7	PPG7 down counter register	R	16-bit PPG7	11111111B
00794BH	PDCRH7				11111111B
00794CH	PCSRL7	PPG7 period setting register	W		11111111B
00794DH	PCSRH7				11111111B
00794EH	PUDUTL7	PPG7 duty setting register	W		00000000B
00794FH	PUDUTH7				00000000B
007950H	Disabled				
007951H	Disabled				
007952H	TMCR0	Timer control register ch.0	R/W	Base timer ch.0	00000000B
007953H					00000000B
007954H	STC0	Status control register ch.0	R/W		00000000B
007955H	Disabled				
007956H	TMR0	Timer register ch.0	R/W	Base timer ch.0	00000000B/ XXXXXXXXB
007957H					00000000B/ XXXXXXXXB

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
007958H	PCSR0/ PRLL0	Period/L-width setting register ch.0	R/W	Base timer ch.0	XXXXXXXXB
007959H					XXXXXXXXB
00795AH	PDUT0/ PRLH0/ DTBF0	Duty/H-width/data buffer register ch.0	R/W		XXXXXXXXB/ 00000000B
00795BH					XXXXXXXXB/ 00000000B
00795CH	TMCR1	Timer control register ch.1	R/W	Base timer ch.1	00000000B
00795DH					00000000B
00795EH	STC1	Status control register ch.1	R/W		00000000B
00795FH	Disabled				
007960H	TMR1	Timer register ch.1	R/W	Base timer ch.1	00000000B/ XXXXXXXXB
007961H					00000000B/ XXXXXXXXB
007962H	PCSR1/ PRLL1	Period/L-width setting register ch.1	R/W		XXXXXXXXB
007963H					XXXXXXXXB
007964H	PDUT1/ PRLH1/ DTBF1	Duty/H-width/data buffer register ch.1	R/W		XXXXXXXXB/ 00000000B
007965H					XXXXXXXXB/ 00000000B
007966H	TMCR2	Timer control register ch.2	R/W	Base timer ch.2	00000000B
007967H					00000000B
007968H	STC2	Status control register ch.2	R/W		00000000B
007969H	Disabled				
00796AH	TMR2	Timer register ch.2	R/W	Base timer ch.2	00000000B/ XXXXXXXXB
00796BH					00000000B/ XXXXXXXXB
00796CH	PCSR2/ PRLL2	Period/L-width setting register ch.2	R/W		XXXXXXXXB
00796DH					XXXXXXXXB
00796EH	PDUT2/ PRLH2/ DTBF2	Duty/H-width/data buffer register ch.2	R/W		XXXXXXXXB/ 00000000B
00796FH					XXXXXXXXB/ 00000000B
007970H	TMCR3	Timer control register ch.3	R/W	Base timer ch.3	00000000B
007971H					00000000B
007972H	STC3	Status control register ch.3	R/W		00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
007973H	Disabled				
007974H	TMR3	Timer register ch.3	R/W	Base timer ch.3	00000000B/ XXXXXXXXB
007975H					00000000B/ XXXXXXXXB
007976H	PCSR3/ PRLL3	Period/L-width setting register ch.3	R/W		XXXXXXXXB
007977H					XXXXXXXXB
007978H	PDUT3/ PRLH3/ DTBF3	Duty/H-width/data buffer register ch.3	R/W		XXXXXXXXB/ 00000000B
007979H					XXXXXXXXB/ 00000000B
00797AH	UDCR0	Up-down count register (ch.0)	R	8/16-bit up-down counter/timer	00000000B
00797BH	UDCR1	Up-down count register (ch.1)	R		00000000B
00797CH	RCR0	Reload/compare register (ch.0)	W		00000000B
00797DH	RCR1	Reload/compare register (ch.1)	W		00000000B
00797EH	CCRL0	Lower counter control register (ch.0)	W, R/W		XX00X000B
00797FH	CCRH0	Higher counter control register (ch.0)	R/W		00000000B
007980H	CCRL1	Lower counter control register (ch.1)	W, R/W		XX00X000B
007981H	CCRH1	Higher counter control register (ch.1)	R/W		-0000000B
007982H	CSR0	Counter status register (ch.0)	R, R/W		00000000B
007983H	Reserved				
007984H	CSR1	Counter status register (ch.1)	R, R/W	8/16-bit up-down counter/timer	00000000B
007985H to 00798FH	Reserved				
007990H	SMR6	Serial bus mode register ch.6	R/W	Multi-function serial ch.6	$$$$$$$$B
007991H	SCR6/IBCR6	Serial bus control register / I²C bus control register ch.6	R/W		$$$$$$$$B
007992H	ESCR6/ IBSR6	Extended communication control register / I²C bus status register ch.6	R/W		$$$$$$$$B
007993H	SSR6	Serial status register ch.6	R/W		$$$$$$$$B
007994H	RDR06/ TDR06	Transmission/reception data register 0 ch.6	R,W		$$$$$$$$B
007995H	RDR16/ TDR16	Transmission/reception data register 1 ch.6	R,W		$$$$$$$$B
007996H	BGR06	Baud rate generator register 0 ch.6	R/W		$$$$$$$$B
007997H	BGR16	Baud rate generator register 1 ch.6	R/W		$$$$$$$$B

(Continued)

Address	Register abbreviation	Register name	R/W	Resource	Initial value
007998H	ISBA6	7-bit slave address register ch.6	R/W	Multi-function serial ch.6	00000000B
007999H	ISMK6	7-bit slave address mask register ch.6	R/W		01111111B
00799AH	PAFSR	PPG pin assignment switching register	R/W	PPG pin switching control	----0000B
00799BH	PMSSR	PPG multi-channel start register	R/W	PPG multi-start control	00000000B
00799CH	Reserved				
00799DH	P9FSR	Serial pin switching register 1	R/W	Multi-function serial pin control	-----000B
00799CH to 0079A1H	Reserved				
0079A2H	P7FSR	Serial pin switching register 0	R/W	Multi-function serial pin control	----000XB
0079A3H	LSYNS	LIN SYNCH FIELD switching register	R/W	Input capture input control	10001000B
0079A4H, 0079A5H	Reserved				
0079A6H	FWR0	Flash memory write control register 0	R/W	Flash memory I/F	00000000B
0079A7H	FWR1	Flash memory write control register 1	R/W		00000000B
0079A8H to 0079DFH	Reserved				
0079E0H	PADR0	Detection address register 0 (low)	R/W	Address match detection function	XXXXXXXXB
0079E1H		Detection address register 0 (middle)			XXXXXXXXB
0079E2H		Detection address register 0 (high)			XXXXXXXXB
0079E3H	PADR1	Detection address register 1 (low)	R/W	Address match detection function	XXXXXXXXB
0079E4H		Detection address register 1 (middle)			XXXXXXXXB
0079E5H		Detection address register 1 (high)			XXXXXXXXB
0079E6H	PADR2	Detection address register 2 (low)	R/W	Address match detection function	XXXXXXXXB
0079E7H		Detection address register 2 (middle)			XXXXXXXXB
0079E8H		Detection address register 2 (high)			XXXXXXXXB
0079E9H to 0079EFH	Reserved				
0079F0H	PADR3	Detection address register 3 (low)	R/W	Address match detection function	XXXXXXXXB
0079F1H		Detection address register 3 (middle)			XXXXXXXXB
0079F2H		Detection address register 3 (high)			XXXXXXXXB

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Address	Register abbreviation	Register name	R/W	Resource	Initial value
0079F3H	PADR4	Detection address register 4 (low)	R/W	Address match detection function	XXXXXXXXB
0079F4H		Detection address register 4 (middle)			XXXXXXXXB
0079F5H		Detection address register 4 (high)			XXXXXXXXB
0079F6H	PADR5	Detection address register 5 (low)	R/W	Address match detection function	XXXXXXXXB
0079F7H		Detection address register 5 (middle)			XXXXXXXXB
0079F8H		Detection address register 5 (high)			XXXXXXXXB
0079F9H to 007FFFH	Reserved				

Explanation on R/W
R/W : Readable/Writable
R : Read only
W : Write only

Explanation on initial value
0 : The initial value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.
- : This bit is not used.
* : The initial value of this bit is “1” or “0”.
It varies depending on the mode pin (MD2, MD1 or MD0 pin) .
+ : The initial value of this bit is “1” or “0”.
$: The initial value of this bit varies depending on the operation mode of the resource.
#H* : Varies depending on the RAM area of the device.

■ INTERRUPT SOURCES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTERS

Interrupt source	Clearing of EI²OS	μDMAC channel no.	Interrupt vector		Interrupt control register	
			No.	Address	No.	Address
Reset	×	—	#08	FFFFDC$_H$	—	—
INT9 instruction	×	—	#09	FFFFD8$_H$	—	—
Exception	×	—	#10	FFFFD4$_H$	—	—
INT0 (IRQ0/1)	○	0	#11	FFFFD0$_H$	ICR00	0000B0$_H$
INT0 (IRQ2 to IRQ7)	○	—	#12	FFFFCC$_H$		
INT0 (IRQ8 to IRQ15)	○	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
INT0 (IRQ16 to IRQ23)	○	—	#14	FFFFC4$_H$		
Base timer ch.0 (source 0,1)	○	1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Base timer ch.1 (source 0,1)	○	2	#16	FFFFBC$_H$		
Base timer ch.2 (source 0,1)	○	3	#17	FFFFB8$_H$	ICR03	0000B3$_H$
Base timer ch.3 (source 0,1)	○	4	#18	FFFFB4$_H$		
PPG0/PPG4 counter borrow	○	5	#19	FFFFB0$_H$	ICR04	0000B4$_H$
PPG1/PPG5 counter borrow	○	6	#20	FFFFAC$_H$		
PPG2/PPG6 counter borrow	○	7	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG3/PPG7 counter borrow	×	8	#22	FFFFA4$_H$		
8/16-bit up-down counter/timer (ch.0/1) compare / underflow / overflow / up-down inversion	×	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
Input capture retrieval (ch.0/1)	○	—	#24	FFFF9C$_H$		
Output compare (ch.0/1/2) match	○	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
Output compare (ch.3/4/5) match	○	—	#26	FFFF94$_H$		
A/D converter	○	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
Overflow in 16-bit free-run timer / compare clear / multi-function serial ch.4/5/6 status	○	9	#28	FFFF8C$_H$		
Multi-function serial ch.4 reception	○	10	#29	FFFF88$_H$	ICR09	0000B9$_H$
Multi-function serial ch.4 transmission	○	11	#30	FFFF84$_H$		
Multi-function serial ch.5 reception	○	12	#31	FFFF80$_H$	ICR10	0000BA$_H$
Multi-function serial ch.5 transmission	○	13	#32	FFFF7C$_H$		
Multi-function serial ch.6 reception	○	14	#33	FFFF78$_H$	ICR11	0000BB$_H$
Multi-function serial ch.6 transmission	○	15	#34	FFFF74$_H$		
Multi-function serial ch.0/1 reception / status	◎	—	#35	FFFF70$_H$	ICR12	0000BC$_H$
Multi-function serial ch.0/1 transmission	○	—	#36	FFFF6C$_H$		
Multi-function serial ch.2 reception / status	◎	—	#37	FFFF68$_H$	ICR13	0000BD$_H$
Multi-function serial ch.2 transmission	○	—	#38	FFFF64$_H$		

(Continued)

(Continued)

Interrupt source	Clearing of EI²OS	µDMAC channel no.	Interrupt vector		Interrupt control register	
			No.	Address	No.	Address
Multi-function serial ch.3 reception / status	◎	—	#39	FFFF60H	ICR14	0000BEH
Multi-function serial ch.3 transmission	○	—	#40	FFFF5CH		
Flash writing/deletion, time base timer, watch timer*	×	—	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt generation module	×	—	#42	FFFF54H		

× : The interrupt request flag is not cleared by the interrupt clear signal.

○ : The interrupt request flag is cleared by the interrupt clear signal.

◎ : The interrupt request flag is cleared by the interrupt clear signal. Stop request function provided at receiving only.

* : Flash writing/deletion, the time base timer and watch timer cannot be used simultaneously.

Note : If a resource has two interrupt sources for the same interrupt number, both of the interrupt request flags are cleared by the EI²OS/µDMAC interrupt clear signal. Therefore, when either of the two sources for the EI²OS/µDMAC function is used, the other interrupt function can not be used. In this case, set the interrupt request enable bit to “0” in the appropriate resource and take measures by software polling.

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	DVcc = Vcc*2
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
	AVRH	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 7.0	V	*3, *8
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 7.0	V	*3, *8
Maximum clamp current	I_{CLAMP}	– 2.0	+2.0	mA	*7
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*7
“L” level maximum output current	I_{OL1}	—	10	mA	*4
	I_{OL2}	—	20	mA	PA0 to PA3*4
“L” level average output current	I_{OLAV1}	—	3	mA	*5
	I_{OLAV2}	—	10	mA	PA0 to PA3*5
“L” level maximum total output current	ΣI_{OL1}	—	60	mA	
	ΣI_{OL2}	—	80	mA	PA0 to PA3
“L” level average total output current	ΣI_{OLAV1}	—	30	mA	*6
	ΣI_{OLAV2}	—	40	mA	PA0 to PA3*6
“H” level maximum output current	I_{OH1}	—	–10	mA	*4
	I_{OH2}	—	–20	mA	PA0 to PA3*4
“H” level average output current	I_{OHAV1}	—	–3	mA	*5
	I_{OHAV2}	—	–10	mA	PA0 to PA3*5
“H” level maximum total output current	ΣI_{OH1}	—	–60	mA	
	ΣI_{OH2}	—	–80	mA	PA0 to PA3
“H” level average total output current	ΣI_{OHAV1}	—	–30	mA	*6
	ΣI_{OHAV2}	—	–40	mA	PA0 to PA3*6
Power consumption	P_D	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0.0$ V.

*2 : Set AV_{CC}, DV_{CC} and AVRH to the same voltage. AV_{CC} and DV_{CC} must not exceed V_{CC}. Also, AVRH must not exceed AV_{CC}.

*3 : V_I and V_O must not exceed 0.3V. When the maximum current to/from an input is limited by using an external component, the I_{CLAMP} rating supersedes the V_I rating.

*4 : The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

(Continued)

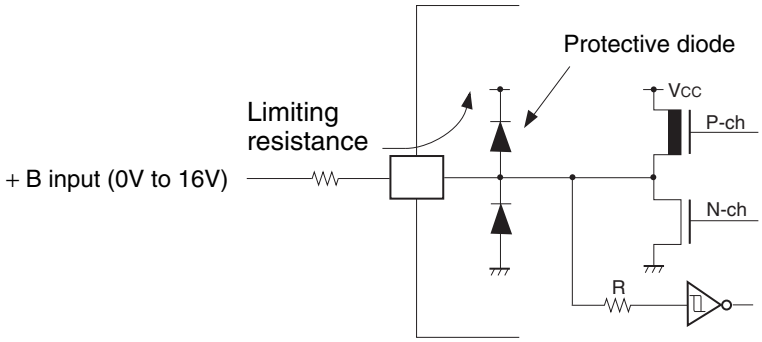
(Continued)

*5 : The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*6 : The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

*7 :
- Relevant pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P76, P80 to P87, P90 to P97, PA0 to PA3
- Use within recommended operating conditions.
- Use with DC voltage (current) .
- The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- Set the limiting resistor value, whether instantaneous or stationary, so that the current to be input to the microcontroller pin does not exceed the rating during the input of the + B signal.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuit :

• Input/Output equivalent circuit



*8 : P74 to P76 and P80 to P87 can be used as 5V I/F pins.

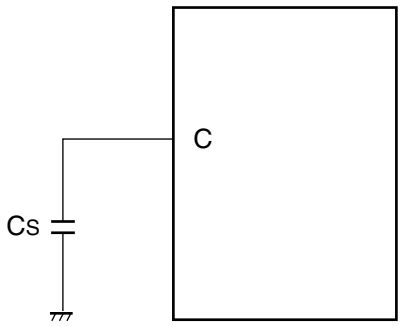
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed any of these ratings.

2. Recommended operating conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} DVcc	2.7	3.6	V	In normal operation
		1.8	3.6	V	Hold stop status
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	All pins other than V_{IH2}, V_{IHS}, V_{IHM} and V_{IHX}
	V_{IH2}	0.7 V_{CC}	V_{SS} + 5.8	V	P74 to P76, P80 to P87
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	Hysteresis input pins
	V_{IHS2}	0.7 V_{CC}	V_{CC} + 0.3	V	Hysteresis input pins (multi-function serial pins)
	V_{IHS3}	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS input pins (external bus mode input pins)
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
	V_{IHX}	0.8 V_{CC}	V_{CC} + 0.3	V	X0A and X1A pins
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	All pins other than V_{ILS}, V_{ILM} and V_{IHX}
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	Hysteresis input pins
	V_{ILS2}	V_{SS} – 0.3	0.3 V_{CC}	V	Hysteresis input pins (multi-function serial pins)
	V_{ILS3}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input pins (external bus mode pins)
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
	V_{ILX}	V_{SS} – 0.3	0.2 Vcc	V	X0A and X1A pins
Smoothing capacitor	C_S	0.1	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the VCC pin should be greater than this capacitor.
Operating temperature	T_A	–40	+85	°C	In ordinary operation.
		0	+70	°C	When external bus is in operation.

• C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC characteristics

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	All pins except P74 to P76, P80 to P87 and PA0 to PA3	V_{CC} = 3.0 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
		P74 to P76, P80 to P87	V_{CC} = 3.0 V, I_{OH} = –2.0 mA	V_{CC} – 0.5	—	—	V	
		PA0 to PA3	DV_{CC} = 3.0 V, I_{OH} = –10.0 mA	DV_{CC} – 0.6	—	—	V	
"L" level output voltage	V_{OL}	All pins except P74 to P76, P80 to P87 and PA0 to PA3	V_{CC} = 3.0 V, I_{OL} = 4.0 mA	—	—	0.4	V	
		P74 to P76, P80 to P87	V_{CC} = 3.0 V, I_{OH} = –2.0 mA	—	—	0.4	V	
		PA0 to PA3	DV_{CC} = 3.0 V, I_{OL} = 10.0 mA	—	—	0.5	V	
Input leak current	I_{IL}	All input pins	V_{CC} = 3.3 V, $V_{SS} < V_I < V_{CC}$	–10	—	+10	µA	
Pull-up resistance	R_{PULL}	—	—	25	50	100	kΩ	Evaluation product
				15	33	66	kΩ	Flash memory product / MASK ROM product
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Evaluation product
				40	100	200	kΩ	MASK ROM product
Open-drain output current	I_{leak}	P31, P32, P34, P35, P43, P44, P46, P47, P72 to P76, P80 to P87, P96, P97	—	—	0.1	10	µA	

(Continued)

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	—	V_{CC} = 3.3 V, Internal 25 MHz operation at normal operation	—	15	23	mA	MB90882(S)
				—	20	28	mA	MB90F882A(S)
				—	27	37	mA	MB90F883C(S), MB90F884C(S)
				—	30	40	mA	MB90F883B(S)/BH(S), MB90F884B(S)/BH(S)
			V_{CC} = 3.3 V, Internal 33 MHz operation at normal operation	—	22	30	mA	MB90882(S)
				—	28	38	mA	MB90F882A(S)
				—	35	45	mA	MB90F883C(S), MB90F884C(S)
				—	40	52	mA	MB90F883BH(S), MB90F884BH(S)
			V_{CC} = 3.3 V, Internal 25 MHz operation, flash write	—	30	40	mA	MB90F882A(S)
				—	37	47	mA	MB90F883C(S), MB90F884C(S)
				—	40	50	mA	MB90F883B(S)/BH(S), MB90F884B(S)/BH(S)
			V_{CC} = 3.3 V, Internal 33 MHz operation, flash write	—	40	52	mA	MB90F882A(S)
				—	45	57	mA	MB90F883C(S), MB90F884C(S)
				—	50	62	mA	MB90F883BH(S), MB90F884BH(S)

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Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS}	—	V_{CC} = 3.3 V, Internal 25 MHz operation, sleep mode	—	6	12	mA	
			V_{CC} = 3.3 V, Internal 33 MHz operation, sleep mode	—	10	20	mA	
	I_{CTS}	—	V_{CC} = 3.3 V, Internal 2 MHz, operation, Time-base timer	—	0.25	0.9	mA	
	I_{CCL}	—	V_{CC} = 3.3 V, External 32 kHz, internal 8 kHz operation, sub-operation (T_A = + 25 °C)	—	80	200	µA	
	I_{CCLS}	—	V_{CC} = 3.3 V, External 32 kHz, Internal 8 kHz operation, sub sleep mode (T_A = + 25 °C)	—	50	160	µA	
	I_{CCT}	—	V_{CC} = 3.3 V, External 32 kHz, internal 8 kHz operation, watch operation (T_A = + 25 °C)	—	20	110	µA	
	I_{CCH}	—	T_A = + 25 °C, Stop mode, V_{CC} = 3.3 V	—	15	100	µA	
Input capacitance	C_{IN}	All pins except AVCC, AVSS, VCC, DVCC, VSS, DVSS	AV_{CC}, AV_{SS}, V_{CC}, DV_{CC}, V_{SS}, DV_{SS}	—	5	15	pF	

Note : P74 to P76 and P80 to P87 are N-ch open-drain pins with controls and normally used at the CMOS level.

4. AC characteristics

(1) Clock timing ratings

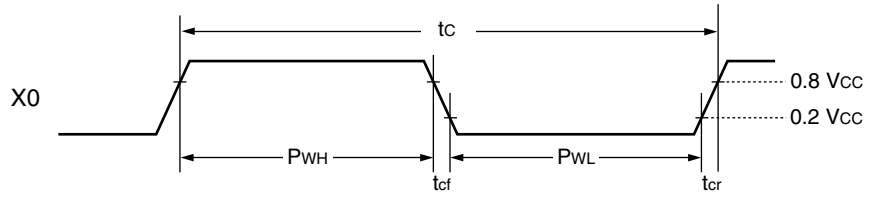
(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	3	—	25	MHz	External crystal oscillation
			—	3	—	50		External clock input
			—	4	—	25		PLL1 multiplication
			—	3	—	16.5		PLL2 multiplication
			—	3	—	11		PLL3 multiplication
			—	3	—	8.25		PLL4 multiplication
			—	3	—	5.5		PLL6 multiplication
			—	3	—	4.125		PLL8 multiplication
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t_C	X0, X1	—	20	—	333	ns	*1
	t_{CL}	X0A, X1A	—	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	—	5	—	—	ns	
	P_{WLH} P_{WLL}	X0A	—	—	15.2	—	µs	*2
Input clock rise/fall time	t_{cr} t_{cf}	X0	—	—	—	5	ns	External clock in use
Internal operating clock frequency	f_{CP}	—	—	1.5	—	33	MHz	*1
	f_{CPL}	—	—	—	8.192	—	kHz	
Internal operating clock cycle time	t_{CP}	—	—	30.3	—	666	ns	*1
	t_{CPL}	—	—	—	122.1	—	µs	

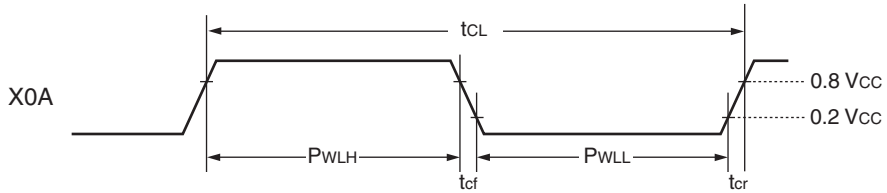
*1 : The maximum operating frequency is 25 MHz in MB90F883B (S), MB90F884B (S).
The maximum operating frequency is 25 MHz in all models when external bus is in operation.

*2 : Input it at a duty ratio of 50% ±3%.

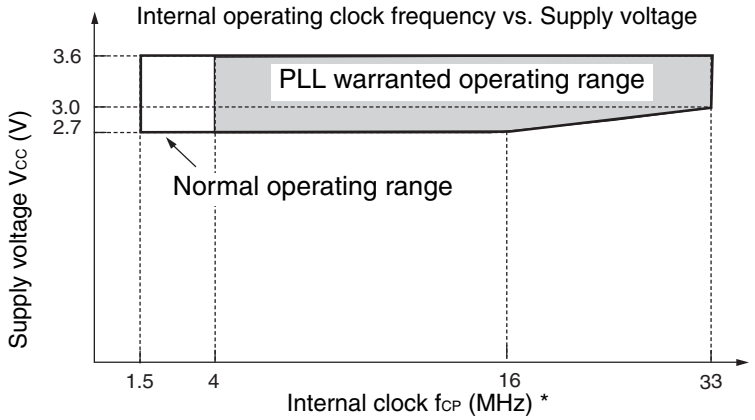
• X0, X1 clock timing



• X0A, X1A clock timing

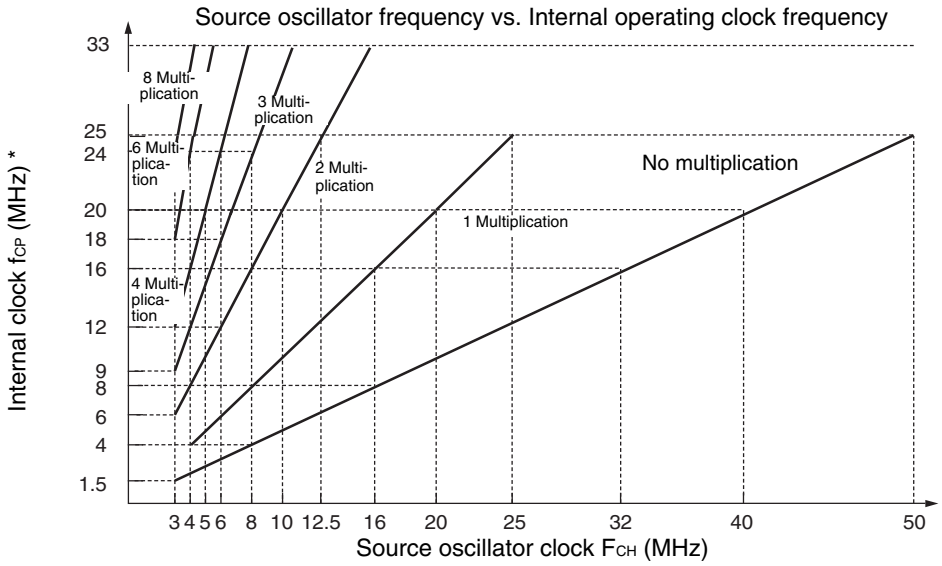


• PLL warranted operating range



* : The maximum operating frequency of MB90F883B(S),MB90F884B(S) is 25 MHz.

Notes: • Use the f_{CP} at 4 MHz or higher only for PLL1 multiplication.
• For A/D operating frequencies, refer to “5. A/D Converter electrical characteristics”.



* : The maximum operating frequency of MB90F883B(S),MB90F884B(S) is 25 MHz.

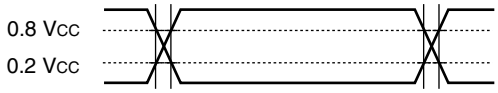
Setting correspondence for the registers PLLOS, CKSCR between the PLL multiple and the source oscillator clock/internal clock frequencies

PLL multiple	DIV2	PLL2	CS1	CS0	Source oscillator clock	Internal clock
1	0	0	0	0	4 MHz to 25 MHz	4 MHz to 25 MHz
1	1	1	0	0	8 MHz to 25 MHz	8 MHz to 25 MHz
2	0	0	0	1	3 MHz to 12.5 MHz	6 MHz to 25 MHz
2	0	1	0	0	4 MHz to 16.5 MHz	8 MHz to 33 MHz
2	1	0	1	1	6 MHz to 12.5 MHz	12 MHz to 25 MHz
2	1	1	0	1	6 MHz to 16.5 MHz	12 MHz to 33 MHz
3	0	0	1	0	3 MHz to 8.33 MHz	9 MHz to 25 MHz
3	1	1	1	0	6 MHz to 11 MHz	18 MHz to 33 MHz
4	0	0	1	1	3 MHz to 6.25 MHz	12 MHz to 25 MHz
4	0	1	0	1	3 MHz to 8.25 MHz	12 MHz to 33 MHz
4	1	1	1	1	6 MHz to 8.25 MHz	24 MHz to 33 MHz
6	0	1	1	0	3 MHz to 5.5 MHz	18 MHz to 33 MHz
8	0	1	1	1	3 MHz to 4.125 MHz	24 MHz to 33 MHz

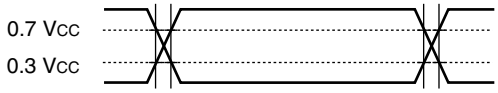
AC characteristics are determined using the following measurement reference voltage values.

- Input signal waveform

Hysteresis input pins

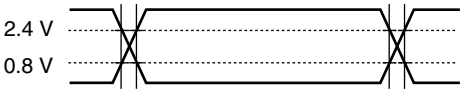


Pins other than hysteresis input/MD input pins



- Output signal waveform

Output pins

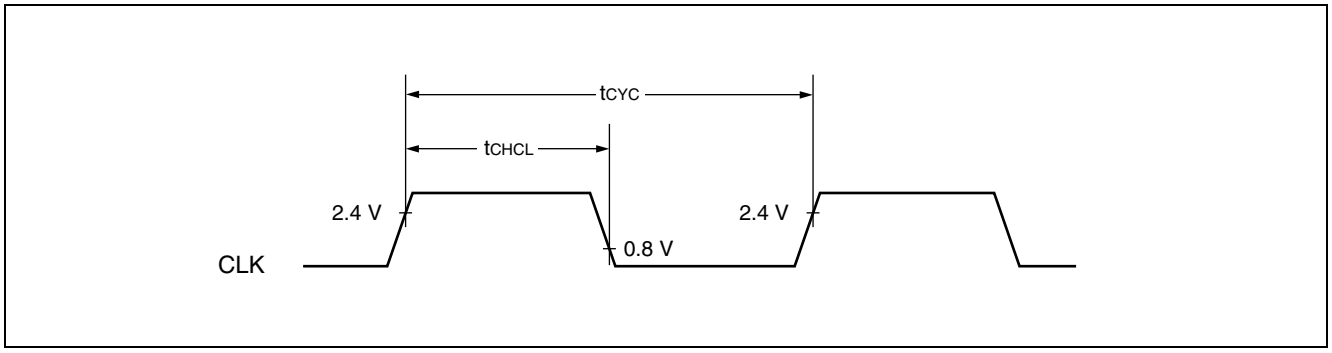


(2) Clock output timing

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}*	—	ns	
CLK↑ → CLK↓	t_{CHCL}	CLK	V_{CC} = 3.0 V to 3.6 V	t_{CP}* / 2 – 15	t_{CP}* / 2 + 15	ns	f_{CP} = 25 MHz
			V_{CC} = 2.7 V to 3.3 V	t_{CP}* / 2 – 20	t_{CP}* / 2 + 20	ns	f_{CP} = 16 MHz
			V_{CC} = 2.7 V to 3.3 V	t_{CP}* / 2 – 64	t_{CP}* / 2 + 64	ns	f_{CP} = 5 MHz

* : t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.



(3) Reset input ratings

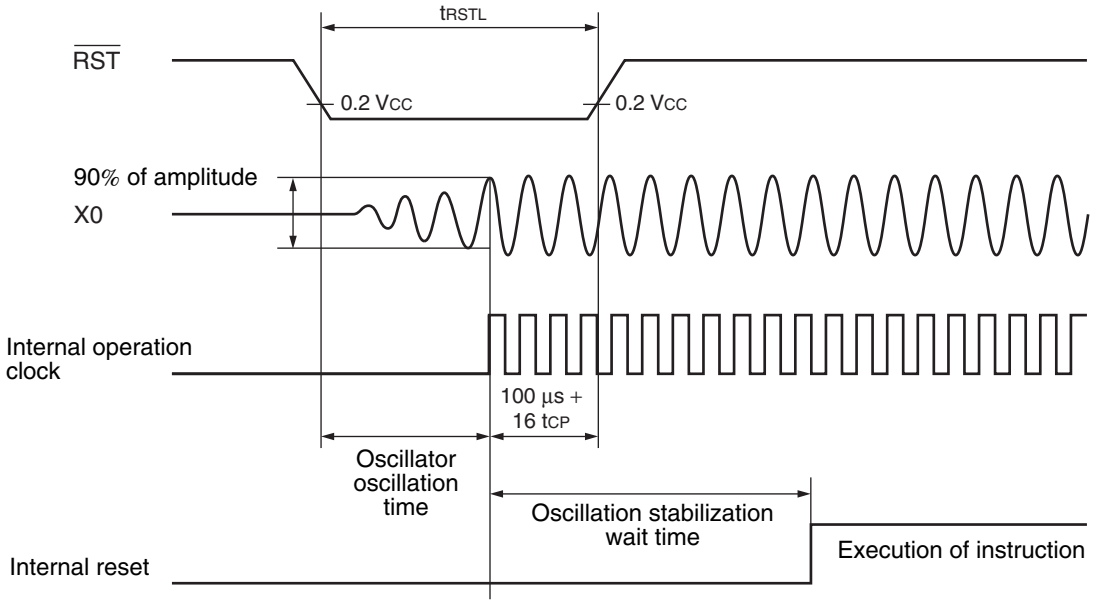
(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}*1	—	ns	In normal operation
				Oscillator oscillation time*2 + 100 µs + 16 t_{CP}*1	—	ms	In sub clock, sub-sleep, watch and stop modes
				100	—	µs	In time base timer mode

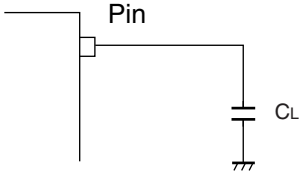
*1 : t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.

*2 : Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several tens of ms; for a ceramic oscillator, this is several hundred ms to a few ms, and for an external clock this is 0 ms.

- In sub clock, sub-sleep, watch and stop modes



- Measurement conditions for AC ratings



C_L : Load capacitance applied to pin during testing

CLK, ALE : C_L = 30 pF
AD15 to AD00 (Address, data bus) , $\overline{RD}$, $\overline{WR}$,
A23 to A00/D15 to D00 : C_L = 30 pF

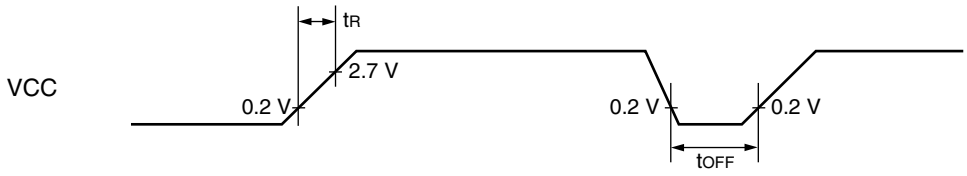
(4) Power-on ratings (Power-on reset)

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

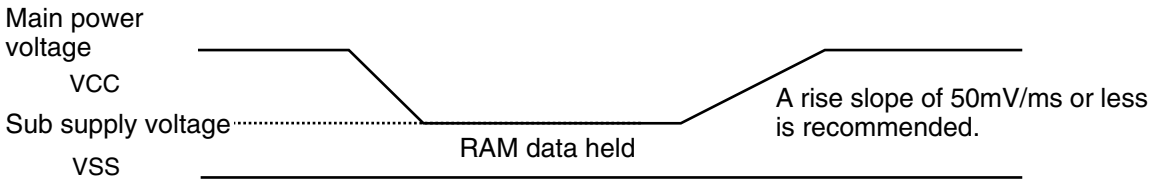
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power rise time	t_R	VCC	—	0.05	30	ms	*
Power cutoff time	t_{OFF}	VCC		1	—	ms	For continuous operation

* : During the power rise time, V_{CC} must be less than 0.2V.

Notes : • The above ratings are values used for power-on reset.
• A power-on reset should be applied by restarting the power supply inside the device.



A sudden change in the supply voltage may activate a power-on reset.
As shown in the following figure, it is recommended to apply a smooth voltage rise with suppressed fluctuation when changing the supply voltage during operation.

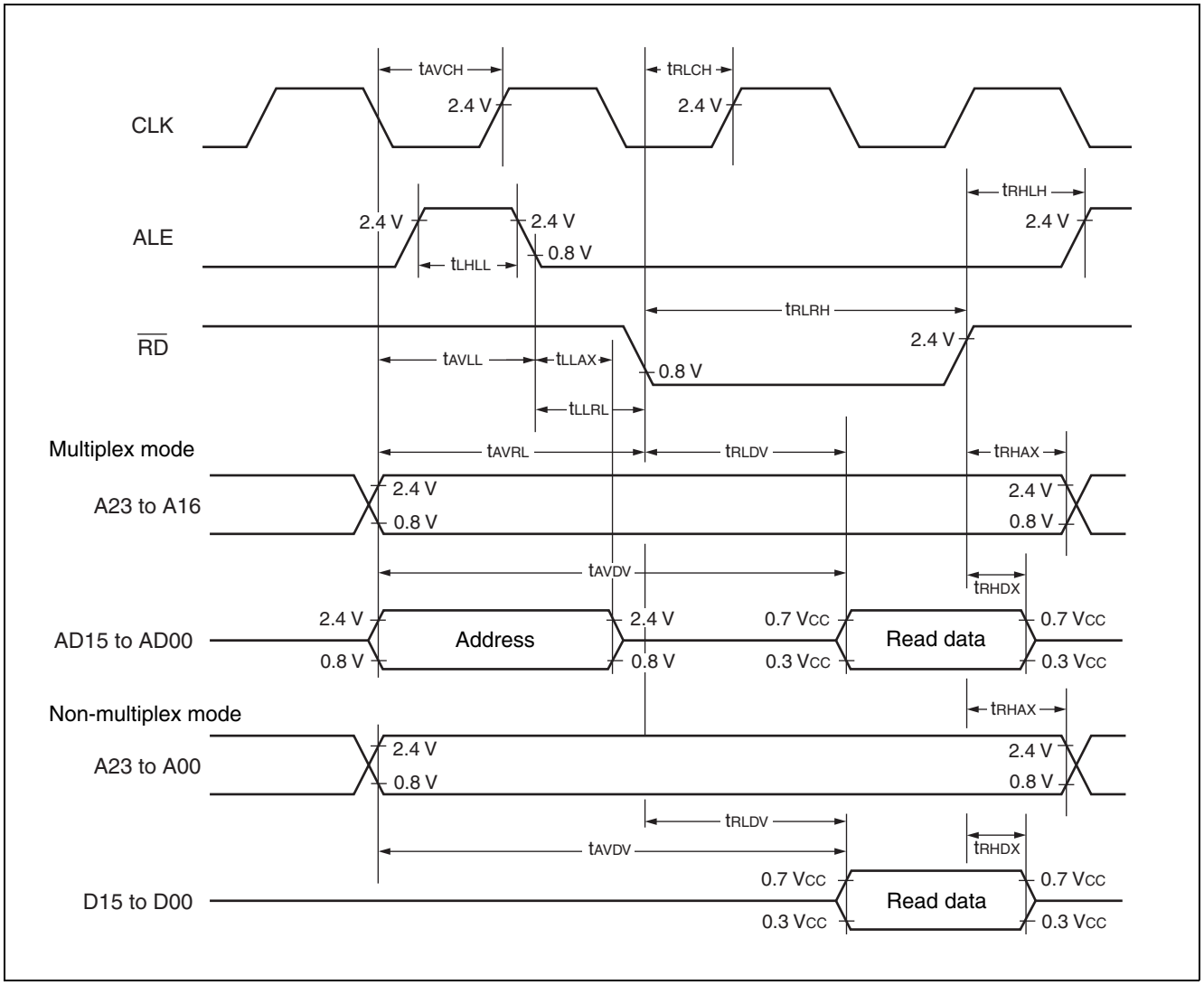


(5) Bus read timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C, fcp ≤ 25 MHz)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	t_{CP}* / 2 – 15	—	ns	16 MHz < f_{CP} ≤ 25 MHz
				t_{CP}* / 2 – 20	—	ns	8 MHz < f_{CP} ≤ 16 MHz
				t_{CP}* / 2 – 35	—	ns	f_{CP} ≤ 8 MHz
Valid address → ALE↓ time	t_{AVLL}	Address, ALE	—	t_{CP}* / 2 – 17	—	ns	
				t_{CP}* / 2 – 40	—	ns	f_{CP} ≤ 8 MHz
ALE ↓ → valid address time	t_{LLAX}	ALE, address	—	t_{CP}* / 2 – 15	—	ns	
valid address → $\overline{RD}$↓ Time	t_{AVRL}	$\overline{RD}$, address	—	t_{CP}* – 25	—	ns	
Valid address → valid data input	t_{AVDV}	Address / data	—	—	5 t_{CP}* / 2 – 55	ns	
				—	5 t_{CP}* / 2 – 80	ns	f_{CP} ≤ 8 MHz
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	3 t_{CP}* / 2 – 25	—	ns	16 MHz < f_{CP} ≤ 25 MHz
				3 t_{CP}* / 2 – 20	—	ns	8 MHz < f_{CP} ≤ 16 MHz
$\overline{RD}$↓ → valid data input	t_{RLDV}	$\overline{RD}$, data	—	—	3 t_{CP}* / 2 – 55	ns	
				—	3 t_{CP}* / 2 – 80	ns	f_{CP} ≤ 8 MHz
$\overline{RD}$↑→ data hold time	t_{RHDX}	$\overline{RD}$, data	—	0	—	ns	
$\overline{RD}$↑ → ALE↑ time	t_{RHLH}	$\overline{RD}$, ALE	—	t_{CP}* / 2 – 15	—	ns	
$\overline{RD}$↑ → valid address time	t_{RHAX}	Address, $\overline{RD}$	—	t_{CP}* / 2 – 10	—	ns	
Valid address → CLK↑ time	t_{AVCH}	Address, CLK	—	t_{CP}* / 2 – 17	—	ns	
$\overline{RD}$↓ → CLK↑ time	t_{RLCH}	$\overline{RD}$, CLK	—	t_{CP}* / 2 – 17	—	ns	
ALE↓ → $\overline{RD}$↓ time	t_{LLRL}	$\overline{RD}$, ALE	—	t_{CP}* / 2 – 15	—	ns	

* : t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.

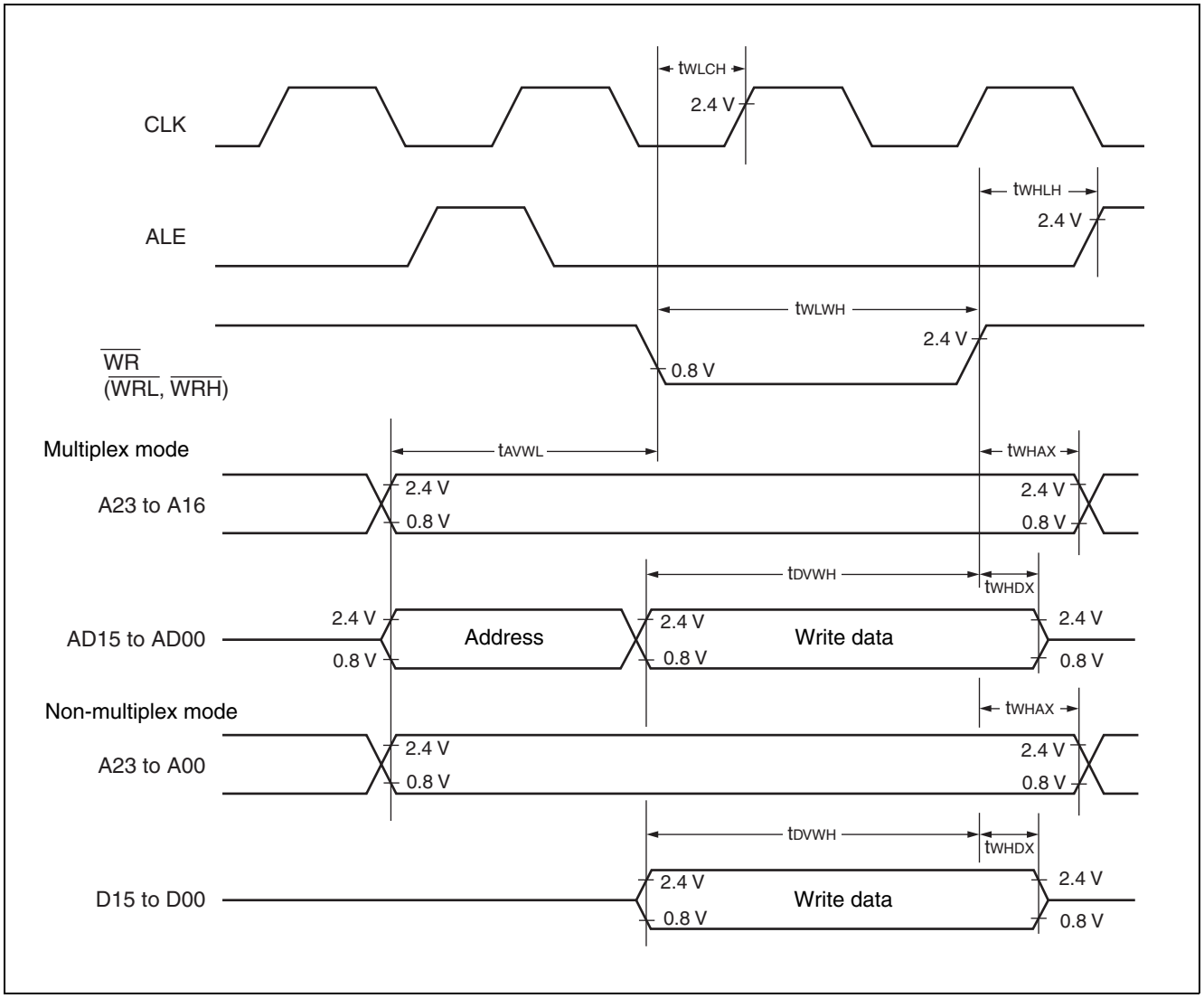


(6) Bus write timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C, fcp ≤ 25 MHz)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	Address, $\overline{WR}$	—	t_{CP}* – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$ ($\overline{WRL}$, $\overline{WRH}$)	—	3 t_{CP}* / 2 – 25	—	ns	16 MHz < f_{CP} ≤ 25 MHz
			—	3 t_{CP}* / 2 – 20	—	ns	8 MHz < f_{CP} ≤ 16 MHz
Valid data output → $\overline{WR}$↑ time	t_{DVWH}	Data, $\overline{WR}$	—	3 t_{CP}* / 2 – 15	—	ns	
$\overline{WR}$↑ → data hold time	t_{WHDX}	$\overline{WR}$, data	—	10	—	ns	16 MHz < f_{CP} ≤ 25 MHz
			—	20	—	ns	8 MHz < f_{CP} ≤ 16 MHz
			—	30	—	ns	f_{CP} ≤ 8 MHz
$\overline{WR}$↑ → valid address time	t_{WHAX}	$\overline{WR}$, address	—	t_{CP}* / 2 – 10	—	ns	
$\overline{WR}$↑ → ALE↑ time	t_{WHLH}	$\overline{WR}$, ALE	—	t_{CP}* / 2 – 15	—	ns	
$\overline{WR}$↓ → CLK↑ time	t_{WLCH}	$\overline{WR}$, CLK	—	t_{CP}* / 2 – 17	—	ns	

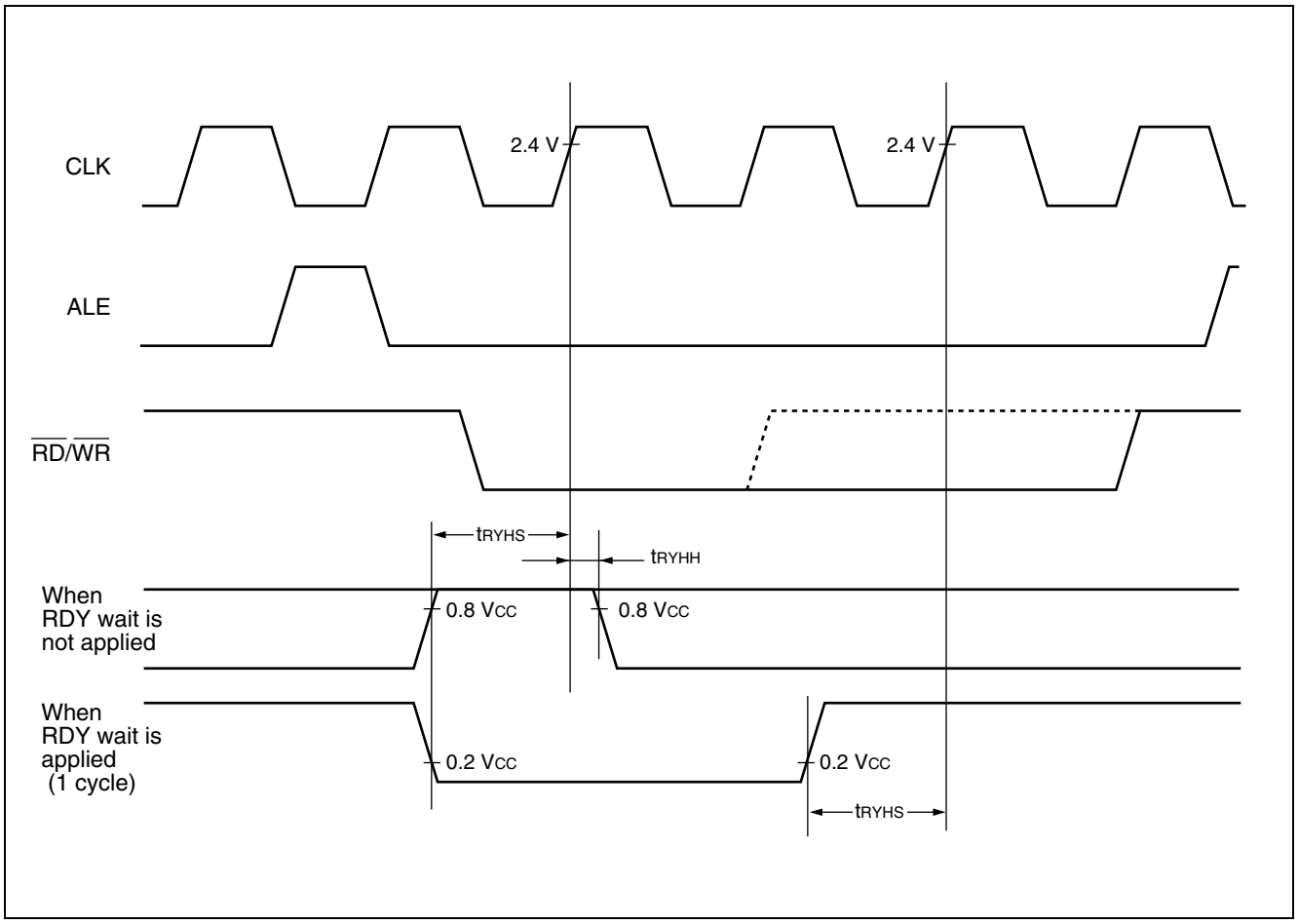
* : t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.



(7) Ready input timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C, fcp ≤ 25 MHz)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
			—	70	—	ns	f_{CP} = 8 MHz
RDY hold time	t_{RYHH}		—	0	—	ns	



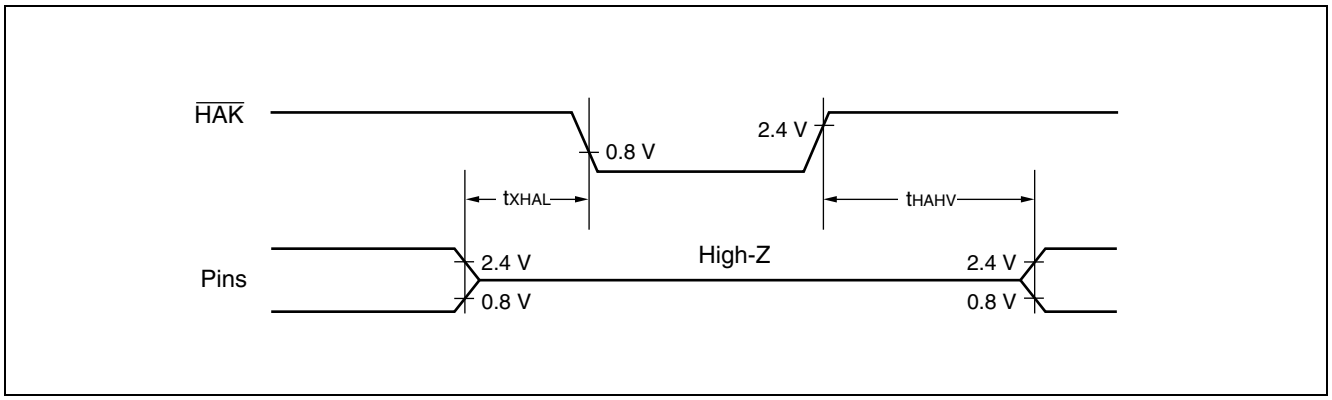
(8) Hold timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C, fcp ≤ 25 MHz)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Pin floating → $\overline{HAK}$↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}*	ns
$\overline{HAK}$↓ → valid pin time	t_{HAHV}	$\overline{HAK}$		t_{CP}*	2 t_{CP}*	ns

* : t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.

Note : It takes one or more cycles from when the HRQ pin is read to when $\overline{HAK}$ changes.



(9) Multi-function serial timing (UART, SIO)

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

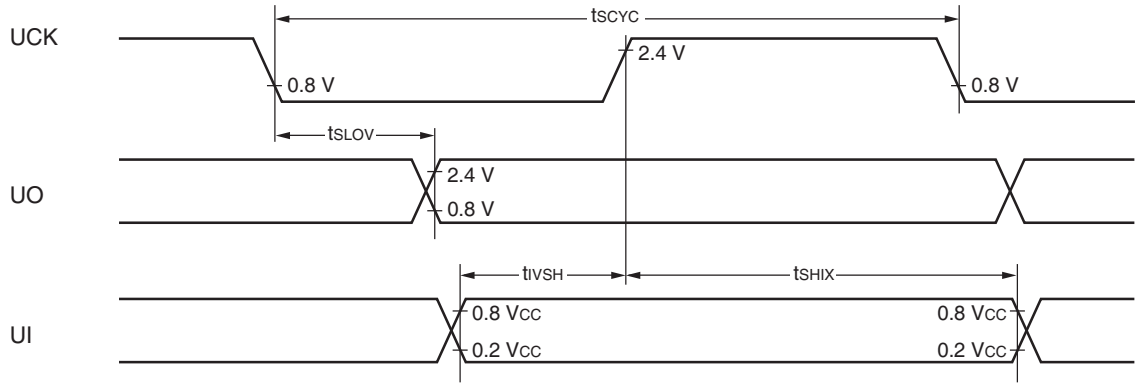
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pin : C_L*1 = 80 pF + 1 TTL	4 t_{CP}*2	—	ns
UCK↓ → UO delay time	t_{SLOV}	—		–50	+50	ns
Valid UI → UCK↑	t_{IVSH}	—		50	—	ns
UCK↑ → valid UI hold time	t_{SHIX}	—		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode output pin : C_L*1 = 80 pF + 1 TTL	2 t_{CP}*2	—	ns
Serial clock “L” pulse width	t_{SLSH}	—		2 t_{CP}*2	—	ns
UCK↓ → UO delay time	t_{SLOV}	—		—	50	ns
Valid UI → UCK↑	t_{IVSH}	—		50	—	ns
UCK↑ → valid UI hold time	t_{SHIX}	—		50	—	ns

*1 : C_L is the load capacitance applied to pins during testing.

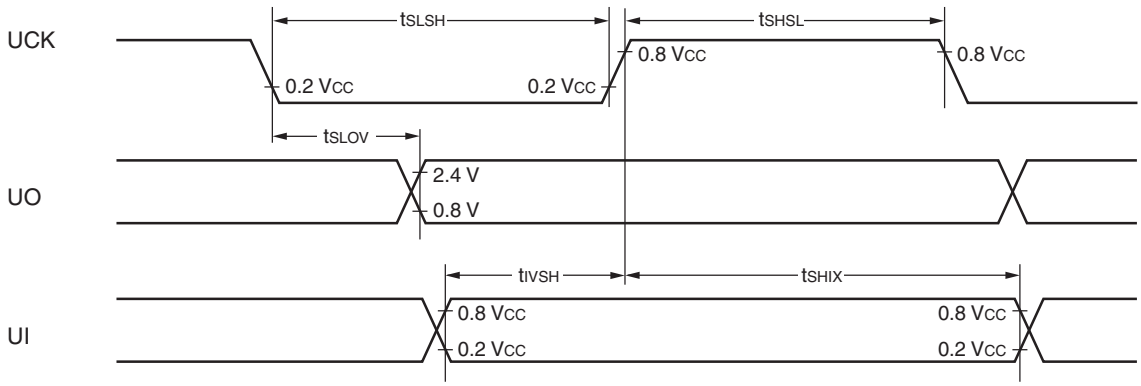
*2 : t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.

Note : The above AC characteristics are for CLK synchronous mode operation.

• Internal shift clock mode



• External shift clock mode



(10) Multi-function serial timing (I^2C)

a. Master mode operation

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condi-tions	Standard mode		High-speed mode*3		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R=1kΩ C=50pF*4	0	100	0	400	kHz
SCL clock “L” width	t_{LOW}		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}		4.0	—	0.6	—	µs
Bus-free time between “stop” condition and “start” condition	t_{BUS}		4.7	—	1.3	—	µs
Repeat “start” condition setup time SCL↑ → SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
(Repeat) “start” condition hold time SDA↓ → SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
“Stop” condition setup time SCL↑ → SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Data hold time SCL↓ → SDA↓↑	t_{HDDAT}		2tcp*1	—	2tcp*1	—	µs
Data setup time SDA↓↑ → SCL↑	t_{SUDAT}		250	—	100*2	—	ns

b. Slave mode operation

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condi-tions	Standard mode		High-speed mode *3		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R=1kΩ C=50pF*4	0	100	0	400	kHz
SCL clock “L” width	t_{LOW}		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}		4.0	—	0.6	—	µs
Bus-free time between “stop” condition and “start” condition	t_{BUS}		4.7	—	1.3	—	µs
Repeat “start” condition setup time SCL↑ → SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
(Repeat) “start” condition hold time SDA↓ → SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
“Stop” condition setup time SCL↑ → SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Data hold time SCL↓ → SDA↓↑	t_{HDDAT}		2tcp*1	—	2tcp*1	—	µs
Data setup time SDA↓↑ → SCL↑	t_{SUDAT}		250	—	100*2	—	ns

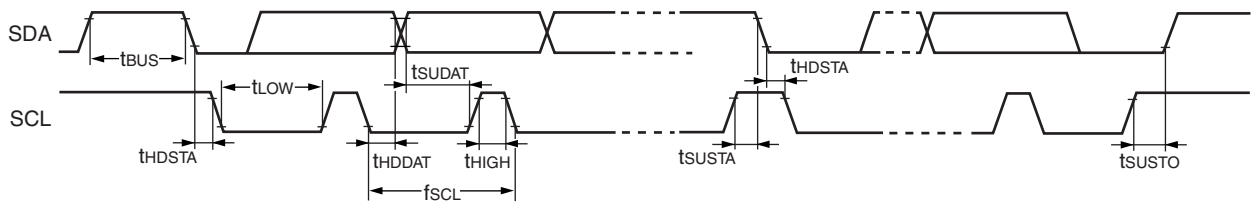
*1 : t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.

*2 : The high-speed mode I²C bus device can be used in a standard mode I²C bus system. However, the device must satisfy the required condition “$t_{SUDAT} \geq 250$ ns”. If the device does not extend the “L” period of the SCL signal, the succeeding data must be output to the SDA line before a period of 1250 ns (the maximum time of SDA/SCL rise + t_{SUDAT}) in which the SCL line is open.

*3 : Set the internal operation clock to 6MHz or higher when using this over 100kHz.

*4 : “R” and “C” are the pull-up resistance and load capacitance of the SCL/SDA lines.

- Timing definition

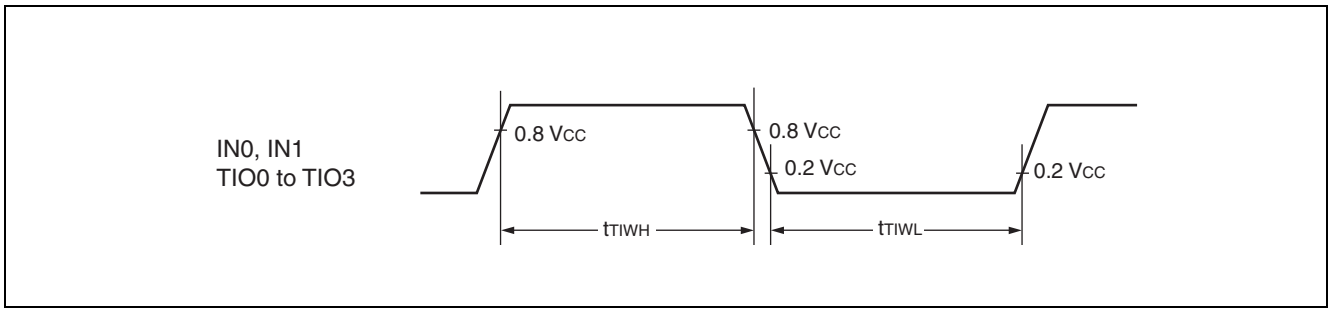


(11) Timer input timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	IN0, IN1, TIO0 to TIO3	—	4 t_{CP}*	—	ns

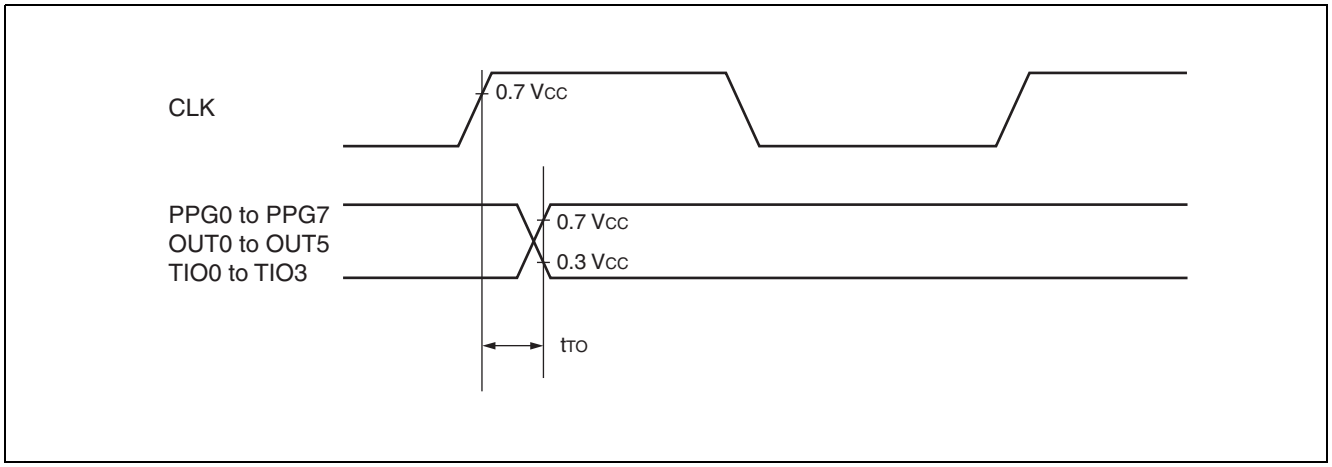
*: t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.



(12) Timer output timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
CLK↑ → change time PPG0 to PPG7 change time OUT0 to OUT5 change time	t_{TO}	PPG0 to PPG7, OUT0 to OUT5, TIO0 to TIO3	Load condition : 80 pF	30	—	ns

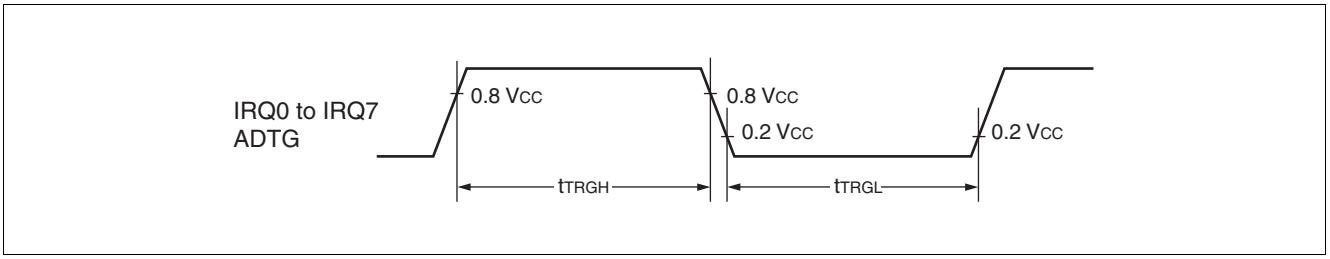


(13) Trigger input timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	ADTG, IRQ0 to IRQ7	—	5 t_{CP}*	—	ns	In normal operation
				1	—	µs	In stop mode

*: t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.

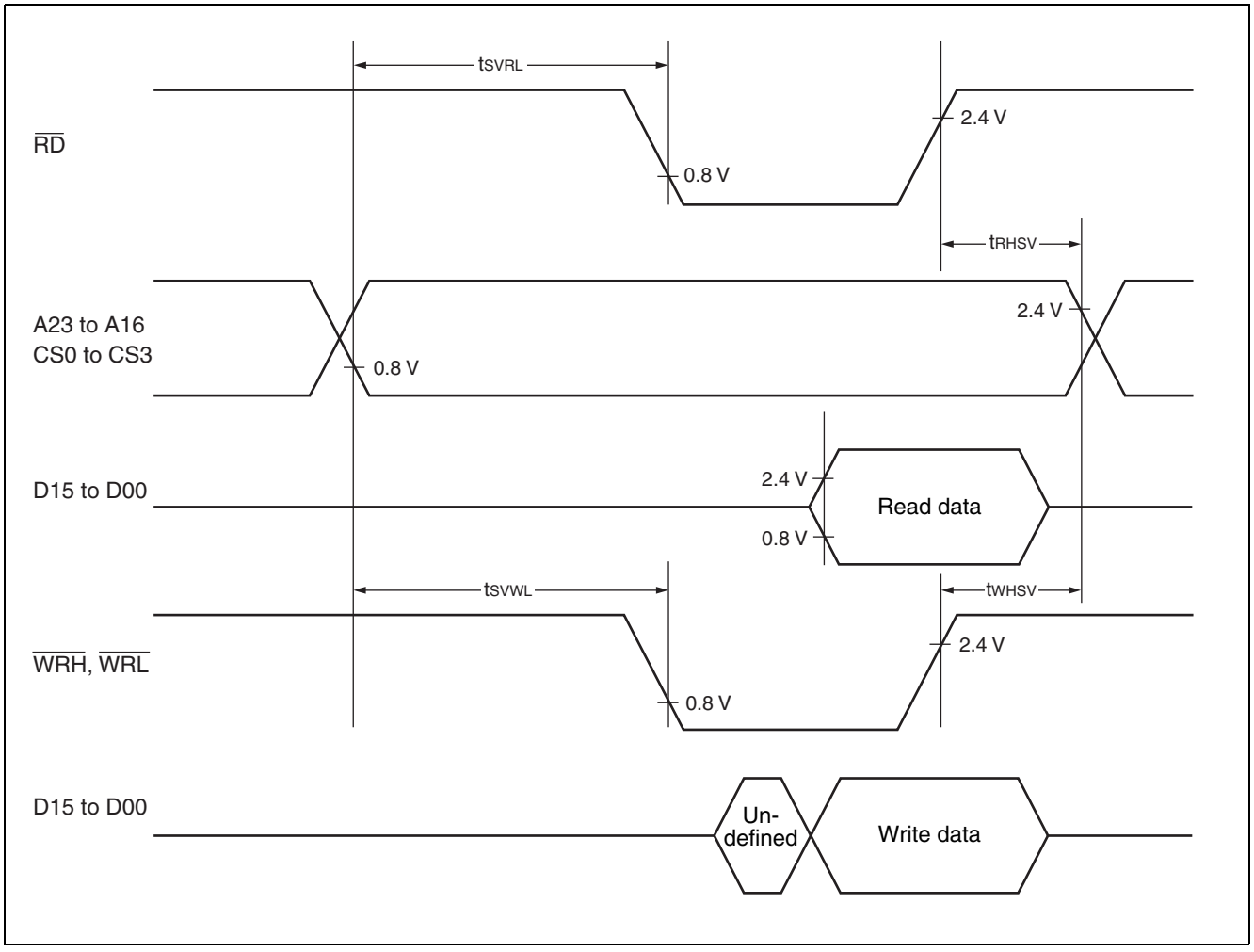


(14) Chip select output timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C, fcp ≤ 25 MHz)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Chip select output valid time → $\overline{RD}$↓	t_{SVRL}	CS0 to CS3, $\overline{RD}$	—	t_{CP}* / 2 – 7	—	ns
Chip select output valid time → $\overline{WR}$↓	t_{SVWL}	CS0 to CS3, $\overline{WRH}$, $\overline{WRL}$	—	t_{CP}* / 2 – 7	—	ns
$\overline{RD}$↑ → Chip select output valid time	t_{RHSV}	$\overline{RD}$, CS0 to CS3	—	t_{CP}* / 2 – 17	—	ns
$\overline{WR}$↑ → Chip select output valid time	t_{WHSV}	$\overline{WRH}$, $\overline{WRL}$, CS0 to CS3	—	t_{CP}* / 2 – 17	—	ns

*: t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.



Note : The chip select output signal changes simultaneously due to the internal bus configuration; therefore, this may generate a bus wait. AC cannot be warranted between the ALE output signal and the chip select output signal.

5. A/D converter electrical characteristics

(V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, 2.7 V ≤ AVRH, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Standard	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Linear error	—	—	—	—	±2.5	LSB	
Differential linear error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN19	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AN0 to AN19	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	1.2	—	—	µs	*1
Compare time	t_{CMP}	—	1.8	—	—	µs	*1
Conversion time	t_{CNV}	—	3.0	—	—	µs	*1
Analog port input current	I_{AIN}	AN0 to AN19	– 3.0	—	+ 3.0	µA	
Analog input voltage	V_{AIN}	AN0 to AN19	AV_{SS}	—	AVRH	V	
Reference voltage	—	AVRH	AV_{SS} + 2.2	—	AV_{CC}	V	
Supply current	I_A	AVCC	—	1.9	3.7	mA	
	I_{AH}	AVCC	—	—	5*2	µA	
Reference voltage supply current	I_R	AVRH	—	520	720	µA	
	I_{RH}	AVRH	—	—	5*2	µA	
Inter-channel variation	—	AN0 to AN19	—	—	4	LSB	

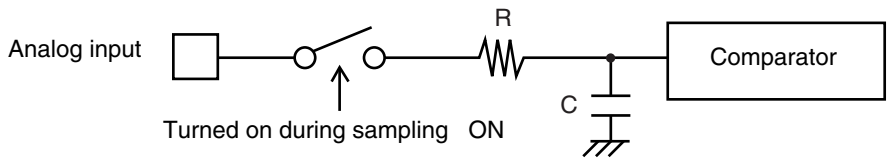
*1 : Time per channel

*2 : Current when the A/D converter is not in operation and the CPU is stopped (V_{CC} = AV_{CC} = AVRH = 3.0 V)

• **External impedance and sampling time for analog input**

This is an A/D converter with a sample hold function. If high external impedance is preventing it from securing sufficient sampling time, a sufficient analog voltage will not be charged in the internal sample hold capacitor, affecting the accuracy of the A/D conversion. In order to satisfy the A/D conversion accuracy specifications, adjust the register values and operating frequency or decrease the external impedance so that the sampling time becomes longer than the minimum value, based on the relationship between the external impedance and the minimum sampling time. If a sufficient sampling time cannot be secured, connect a capacitor with a capacitance of approximately 0.1 µF to the analog input pin.

Model diagram of analog input circuit



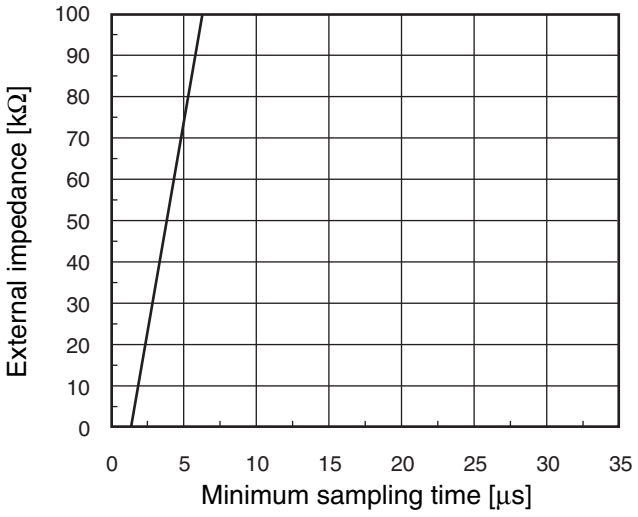
R	C
12.2 kΩ (Max)	8.5 pF (Max)

Note : These are reference values.

• Relation between external impedance and minimum sampling time

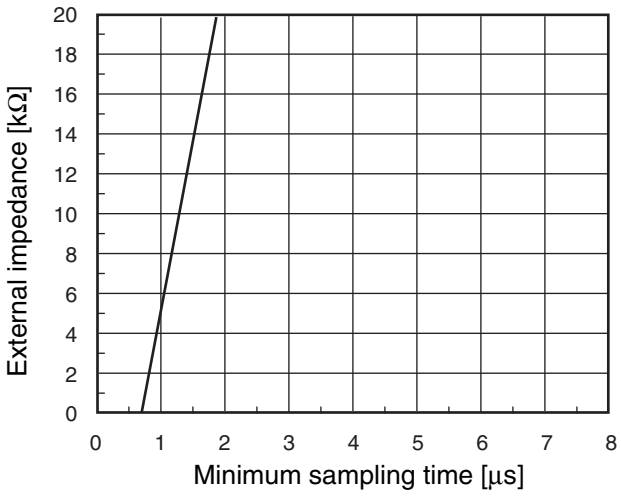
[External impedance = 0 kΩ to 100 kΩ]

Flash memory device
MASK ROM device



[External impedance = 0 kΩ to 20 kΩ]

Flash memory device
MASK ROM device



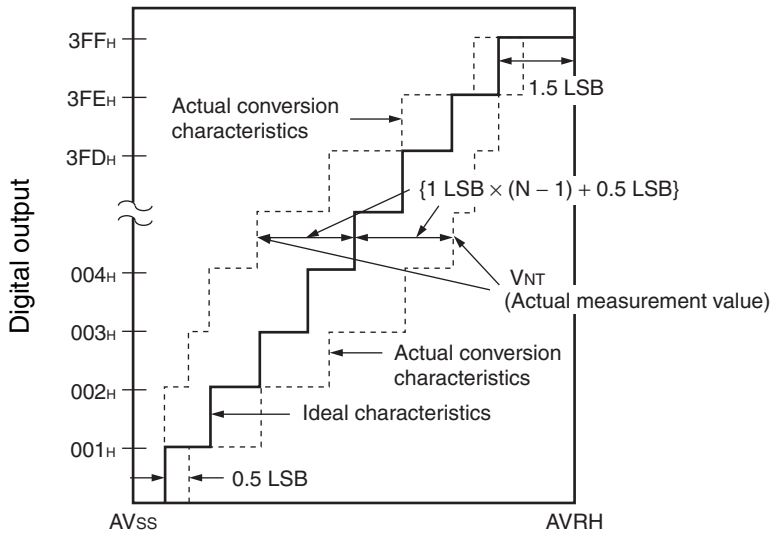
• **Errors :**

As | AVRH—AVss | decreases, the absolute error increases.

6. Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation between a line across zero-transition line (“00 0000 0000” ← → “00 0000 0001”) and full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) and actual conversion characteristics.
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between an actual value and a theoretical value. A total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{AVRH - AV_{SS}}{1024}\ [\text{V}]$$

V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transits from (N – 1) H, NH.

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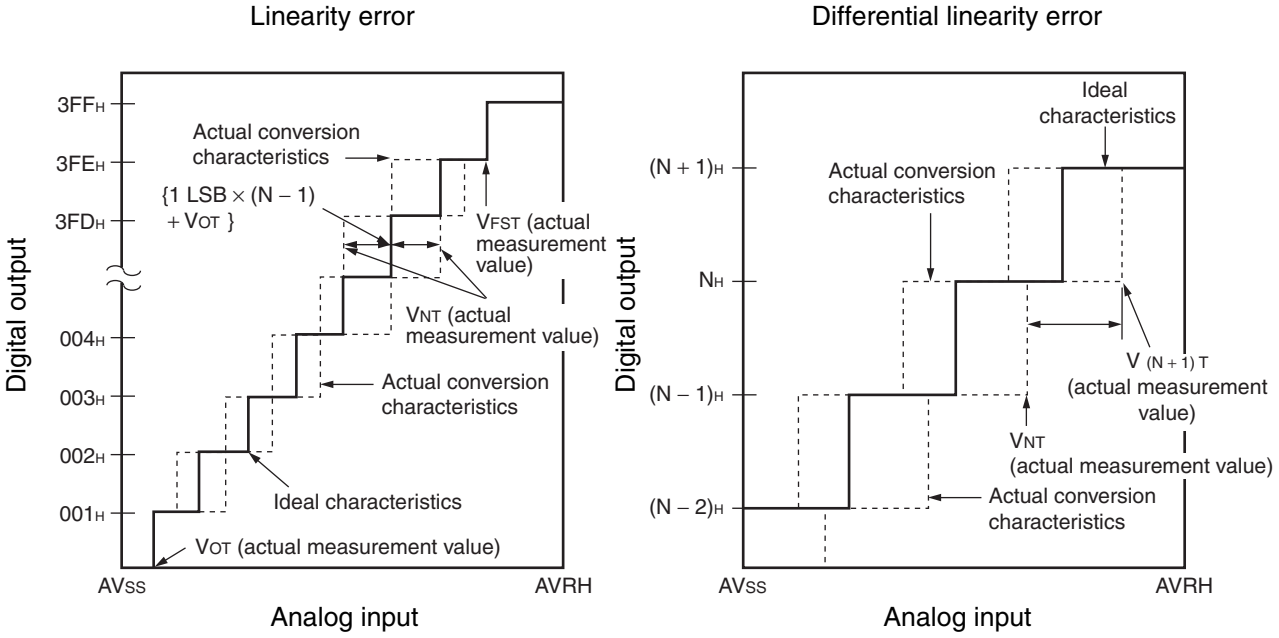


$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

• **Flash memory write/erase characteristics**

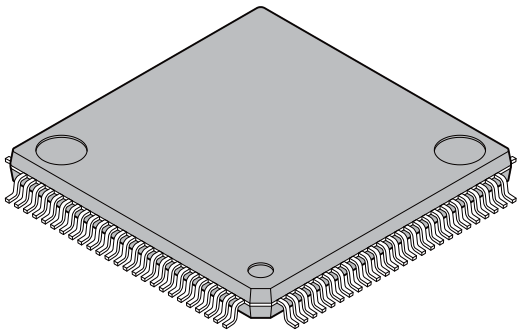
Parameter	Conditions	Value			Unit	Remarks
		Min	Standard	Max		
Sector erase time	T_A = +25 °C, V_{CC} = 3.0 V	—	0.9	3.6	s	Excludes internal write time before erase operation.
Chip erase time		—	6.2	—	s	Excludes internal write time before erase operation.
Word (16-bit width) write time		—	23	—	µs	Excludes overhead time at system level.
Number of write/erase cycles	—	10000	—	—	cycle	
Flash memory data hold time	Average T_A = +85 °C	100000	—	—	h	*

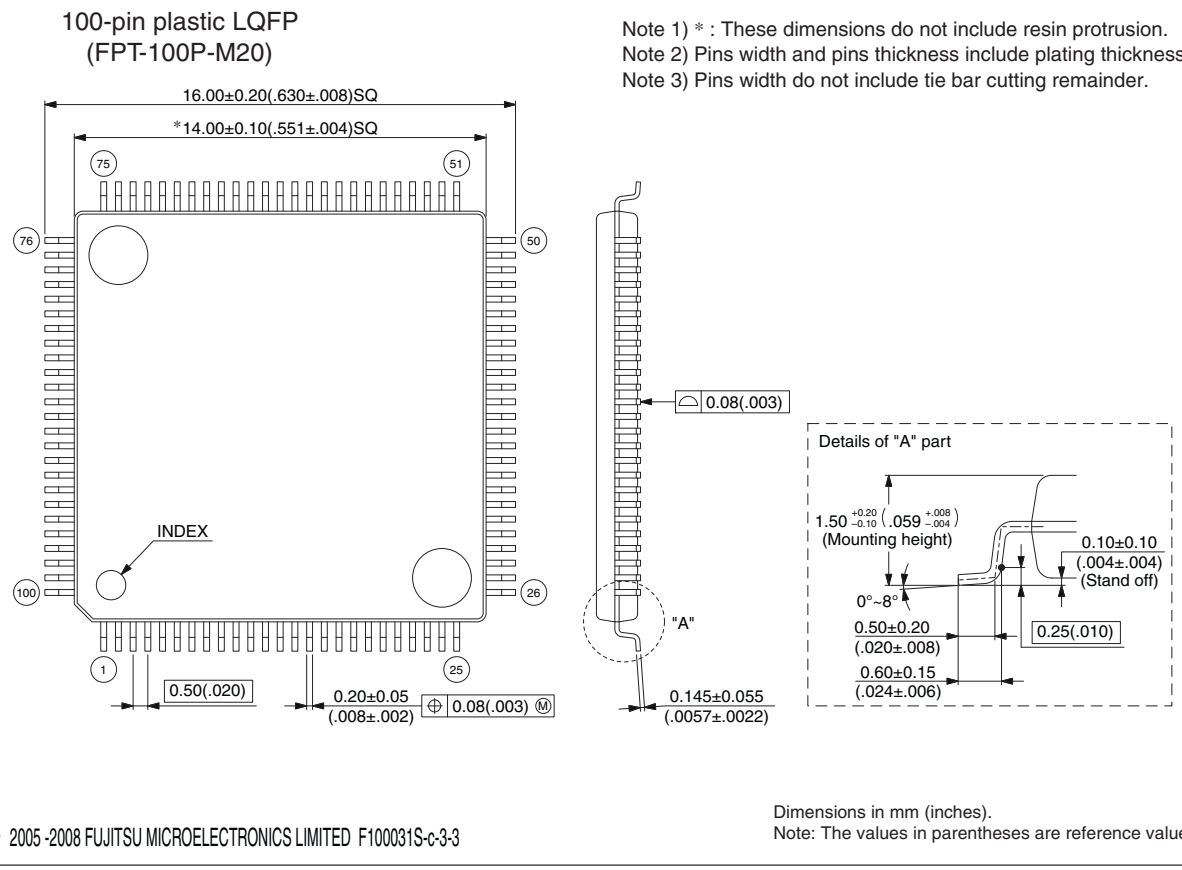
* : Value converted from the evaluation result of technology reliability (The Arrhenius equation is used to convert the high-temperature high-speed test result into the average temperature + 85 °C.)

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F882APF MB90F883BPF MB90F883BHPF MB90F883CPF MB90F884BPF MB90F884BHPF MB90F884CPF MB90882PF MB90F882ASPF MB90F883BSPF MB90F883BHSPF MB90F883CSPF MB90F884BSPF MB90F884BHSPF MB90F884CSPF MB90882SPF	100-pin plastic QFP (FPT-100P-M06)	Products with S-suffix: Single clock product (without sub clock) Products without S-suffix: Dual clock product (with sub clock)
MB90F882APMC MB90F883BPMC MB90F883BHPMC MB90F883CPMC MB90F884BPMC MB90F884BHPMC MB90F884CPMC MB90882PMC MB90F882SPMC MB90F882ASPMC MB90F883BSPMC MB90F883BHSPMC MB90F883CSPMC MB90F884BSPMC MB90F884BHSPMC MB90F884CSPMC MB90882SPMC	100-pin plastic LQFP (FPT-100P-M20)	Products with S-suffix: Single clock product (without sub clock) Products without S-suffix: Dual clock product (with sub clock)
MB90V880A-101CR-ES MB90V880A-102CR-ES	299-pin ceramic PGA (PGA-299C-A01)	Evaluation product 101 : Single clock product (without sub clock) 102 : Dual clock product (with sub clock)

■ PACKAGE DIMENSIONS

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50



Please check the latest Package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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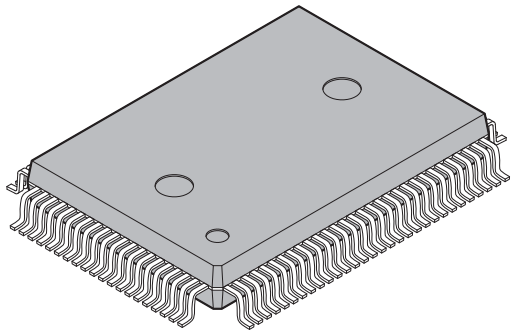
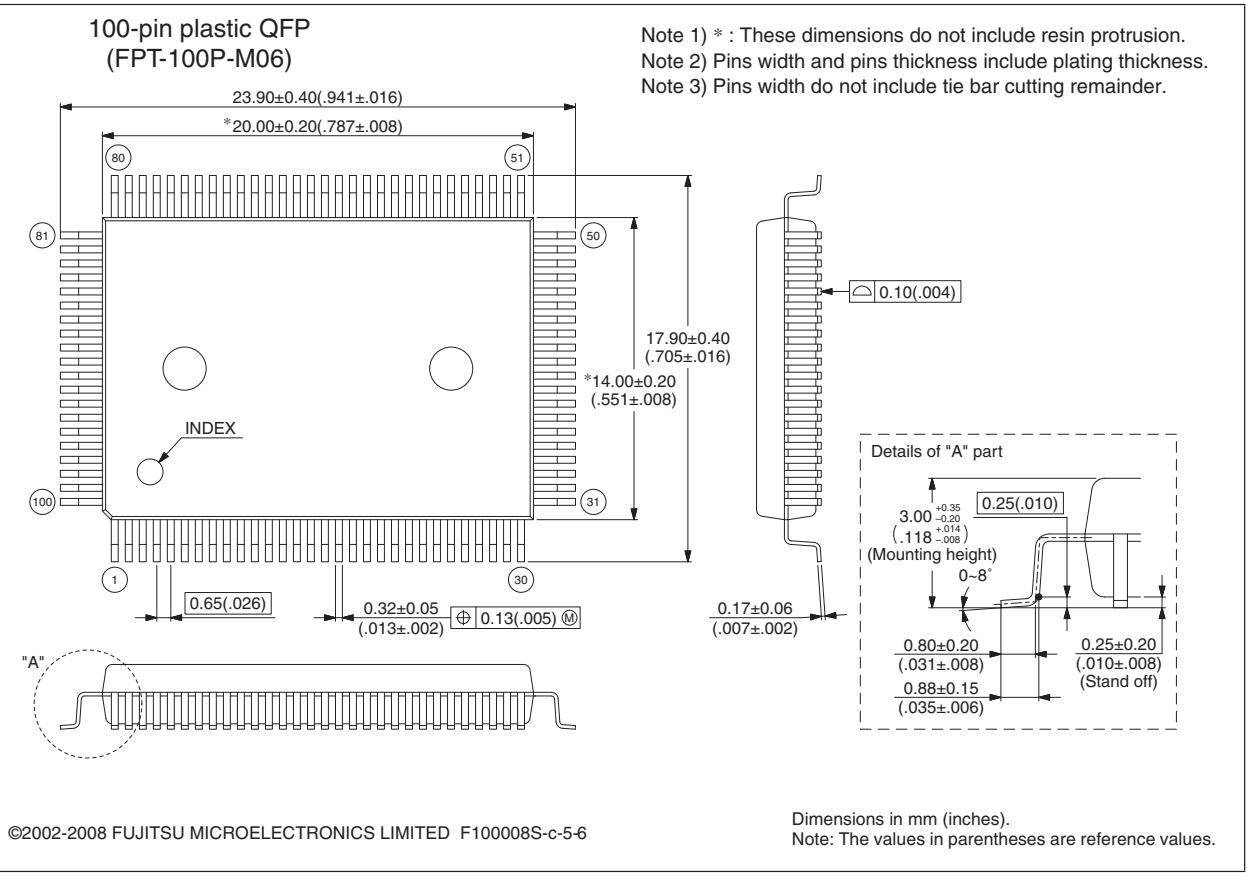
100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M06)		



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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
45	■ ELECTRICAL CHARACTERISTICS 2. Recommended operating conditions	Added “when external bus is in operation” in parameter “Operating temperature” to the table.
50	4. AC characteristics (1) Clock timing ratings	Changed the footnote *1. “Observe the operating voltage with care. The maximum operating frequency is 25 MHz in MB90F883B(S), MB90F884B (S).” → “The maximum operating frequency is 25 MHz in MB90F883B(S), MB90F884B (S). The maximum operating frequency is 25 MHz in all models when external bus is in operation.”
73	■ ORDERING INFORMATION	Deleted the part number: MB90F882SPF

The vertical lines marked in the left side of the page show the changes.

MEMO

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MB90880 Series

FUJITSU MICROELECTRONICS LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

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