

# 27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer

## ABSOLUTE MAXIMUM RATINGS

VCC_ to _GND	-0.5V to +4.0V
Any Ground to Any Ground	-0.5V to +0.5V
OUT+, OUT- to LVDS GND	-0.5V to +4.0V
OUT+, OUT- Short Circuit to LVDS GND or VCCLVDS	Continuous
OUT+, OUT- Short Through 0.125μF (or smaller), 25V Series Capacitor	-0.5V to +16V
RGB_IN[17:0], CNTL_IN[8:0], DE_IN, RNG0, RNG1, PCLK_IN, PWRDWN, CMF to GND	-0.5V to (VCCIN + 0.5V)
Continuous Power Dissipation (TA = +70°C)	
48-Lead LQFP (derate 21.7mW/°C above +70°C)	1739mW
48-Lead Thin QFN (derate 37mW/°C above +70°C)	2963mW

### ESD Protection

Machine Model (RD = 0Ω, CS = 200pF)	
All Pins to GND	±200V
Human Body Model (RD = 1.5kΩ, CS = 100pF)	
All Pins to GND	±2kV
ISO 10605 (RD = 2kΩ, CS = 330pF)	
Contact Discharge (OUT+, OUT-) to GND	±10kV
Air Discharge (OUT+, OUT-) to GND	±30kV
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(VCC\_ = +3.0V to +3.6V, RL = 100Ω ±1%, PWRDWN = high, TA = -40°C to +85°C, unless otherwise noted. Typical values are at VCC\_ = +3.3V, TA = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
SINGLE-ENDED INPUTS (RGB_IN[17:0], CNTL_IN[8:0], DE_IN, PCLK_IN, PWRDWN, RNG_)								
High-Level Input Voltage	V <sub>IH</sub>	V <sub>CCIN</sub> = 1.71V to <3V		0.65V <sub>CCIN</sub>	V <sub>CCIN</sub> + 0.3		V	
				2	V <sub>CCIN</sub> + 0.3			
Low-Level Input Voltage	V <sub>IL</sub>	V <sub>CCIN</sub> = 1.71V to <3V		-0.3	0.3V <sub>CCIN</sub>		V	
				-0.3	+0.8			
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = -0.3V to (V <sub>CCIN</sub> + 0.3V), V <sub>CCIN</sub> = 1.71V to 3.6V, PWRDWN = high or low		-70	+70		μA	
Input Clamp Voltage	V <sub>CL</sub>	I <sub>CL</sub> = -18mA					-1.5	V
LVDS OUTPUTS (OUT+, OUT-)								
Differential Output Voltage	V <sub>OD</sub>	Figure 1		250	335	450	mV	
Change in V <sub>OD</sub> Between Complementary Output States	ΔV <sub>OD</sub>	Figure 1		20			mV	
Common-Mode Voltage	V <sub>OS</sub>	Figure 1		1.125	1.29	1.375	V	
Change in V <sub>OS</sub> Between Complementary Output States	ΔV <sub>OS</sub>	Figure 1		20			mV	
Output Short-Circuit Current	I <sub>OS</sub>	V <sub>OUT+</sub> or V <sub>OUT-</sub> = 0 or 3.6V		-15	±8	+15	mA	
Magnitude of Differential Output Short-Circuit Current	I <sub>OSD</sub>	V <sub>OD</sub> = 0		5.5			15	mA
Output High-Impedance Current	I <sub>OZ</sub>	PWRDWN = low or V <sub>CC-</sub> = 0	V <sub>OUT+</sub> = 0, V <sub>OUT-</sub> = 3.6V	-1			+1	μA
			V <sub>OUT+</sub> = 3.6V, V <sub>OUT-</sub> = 0					

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## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC-} = +3.0V$  to  $+3.6V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $\overline{PWRDWN} = \text{high}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC-} = +3.3V$ ,  $T_A = +25^\circ\text{C}$ .) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Resistance	$R_O$		78	110	147	$\Omega$
Worst-Case Supply Current	$I_{CCW}$	$R_L = 100\Omega \pm 1\%$ , $C_L = 5pF$ , continuous 10 transition words, modulation off	3MHz	15	25	mA
			5MHz	18	25	
			10MHz	23	28	
			20MHz	33	39	
			35MHz	50	70	
Power-Down Supply Current	$I_{CCZ}$	(Note 3)			50	$\mu A$

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC-} = +3.0V$  to  $+3.6V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 5pF$ ,  $\overline{PWRDWN} = \text{high}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC-} = +3.3V$ ,  $T_A = +25^\circ\text{C}$ .) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>PCLK_IN TIMING REQUIREMENTS</b>						
Clock Period	$t_T$	Figure 2	28.57		333.00	ns
Clock Frequency	$f_{CLK}$		3		35	MHz
Clock Frequency Difference from Deserializer Reference Clock	$\Delta f_{CLK}$		-2		+2	%
Clock Duty Cycle	DC	$t_{HIGH}/t_T$ or $t_{LOW}/t_T$ , Figure 2	35	50	65	%
Clock Transition Time	$t_R, t_F$	Figure 2			2.5	ns
<b>SWITCHING CHARACTERISTICS</b>						
Output Rise Time	$t_{RISE}$	20% to 80%, $V_{OD} \geq 250mV$ , modulation off, Figure 3		215	350	ps
Output Fall Time	$t_{FALL}$	80% to 20%, $V_{OD} \geq 250mV$ , modulation off, Figure 3		206	350	ps
Input Setup Time	$t_{SET}$	Figure 4	3			ns
Input Hold Time	$t_{HOLD}$	Figure 4	3			ns
Serializer Delay	$t_{SD}$	Figure 5	$3.15 \times t_T$		$3.2 \times t_T$	ns
PLL Lock Time	$t_{LOCK}$	Figure 6			$16385 \times t_T$	ns
Power-Down Delay	$t_{PD}$	Figure 7			1	$\mu s$

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## AC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC-} = +3.0V$  to  $+3.6V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 5pF$ ,  $\overline{PWRDWN} = \text{high}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC-} = +3.3V$ ,  $T_A = +25^\circ\text{C}$ .) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak-to-Peak Output Offset Voltage	$V_{OSp-p}$	700Mbps data rate, CMF open, Figure 8		22	70	mV
		700Mbps data rate, CMF 0.1 $\mu$ F to ground, Figure 8		12	50	

**Note 1:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except  $V_{OD}$ ,  $\Delta V_{OD}$ , and  $\Delta V_{OS}$ .

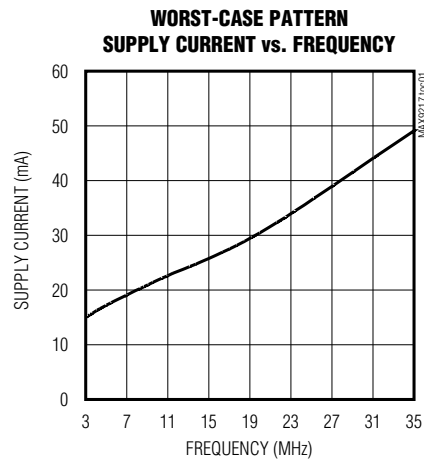
**Note 2:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at  $T_A = +25^\circ\text{C}$ .

**Note 3:** All LVTTTL/LVCMOS inputs, except  $\overline{PWRDWN}$  at  $\leq 0.3V$  or  $\geq V_{CCIN} - 0.3V$ .  $\overline{PWRDWN}$  is  $\leq 0.3V$ .

**Note 4:** AC parameters are guaranteed by design and characterization and are not production tested. Limits are set at  $\pm 6$  sigma.

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ ,  $V_{CC-} = +3.3V$ ,  $R_L = 100\Omega$ , modulation off, unless otherwise noted.)



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## Pin Description

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PIN	NAME	FUNCTION
1, 13, 37	GND	Input Buffer Supply and Digital Supply Ground
2	VCCIN	Input Buffer Supply Voltage. Bypass to GND with 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
3–10, 39–48	RGB_IN[17:0]	LVTTL/LVCMOS Red, Green, and Blue Digital Video Data Inputs. Eighteen data bits are loaded into the input latch on the rising edge of PCLK_IN when DE_IN is high. Internally pulled down to GND.
11, 12, 15–21	CNTL_IN[8:0]	LVTTL/LVCMOS Control Data Inputs. Control data are latched on the rising edge of PCLK_IN when DE_IN is low. Internally pulled down to GND.
14, 38	VCC	Digital Supply Voltage. Bypass to GND with 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
22	DE_IN	LVTTL/LVCMOS Data Enable Input. Logic-high selects RGB_IN[17:0] to be latched. Logic-low selects CNTL_IN[8:0] to be latched. DE_IN must be switching for proper operation. Internally pulled down to GND.
23	PCLK_IN	LVTTL/LVCMOS Parallel Clock Input. Latches data and control inputs and provides the PLL reference clock. Internally pulled down to GND.
24, 25	I.C.	Internally connected to GND. Connect to GND or leave unconnected.
26	PLL GND	PLL Supply Ground
27	VCCPLL	PLL Supply Voltage. Bypass to PLL GND with 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
28	PWRDWN	LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND.
29	CMF	Common-Mode Filter. Optionally connect a capacitor between CMF and ground to filter common-mode switching noise.
30, 31	LVDS GND	LVDS Supply Ground
32	OUT-	Inverting LVDS Serial Data Output
33	OUT+	Noninverting LVDS Serial Data Output
34	VCCLVDS	LVDS Supply Voltage. Bypass to LVDS GND with 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
35	RNG1	LVTTL/LVCMOS Frequency Range Select Input. Set to the frequency range that includes the PCLK_IN frequency as shown in Table 3. Internally pulled down to GND.
36	RNG0	LVTTL/LVCMOS Frequency Range Select Input. Set to the frequency range that includes the PCLK_IN frequency as shown in Table 3. Internally pulled down to GND.
—	EP	Exposed Pad (Thin QFN Package Only). Connect Thin QFN exposed pad to PCB GND.

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## Functional Diagram

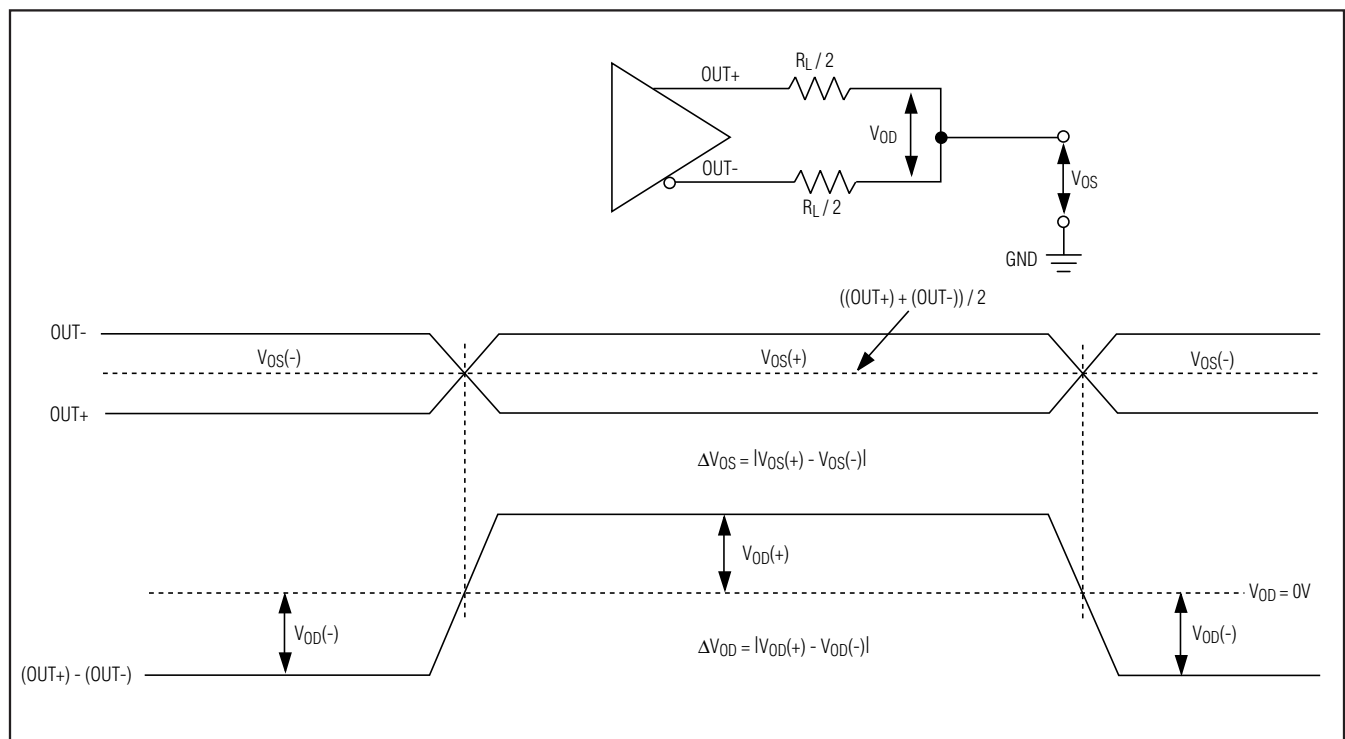
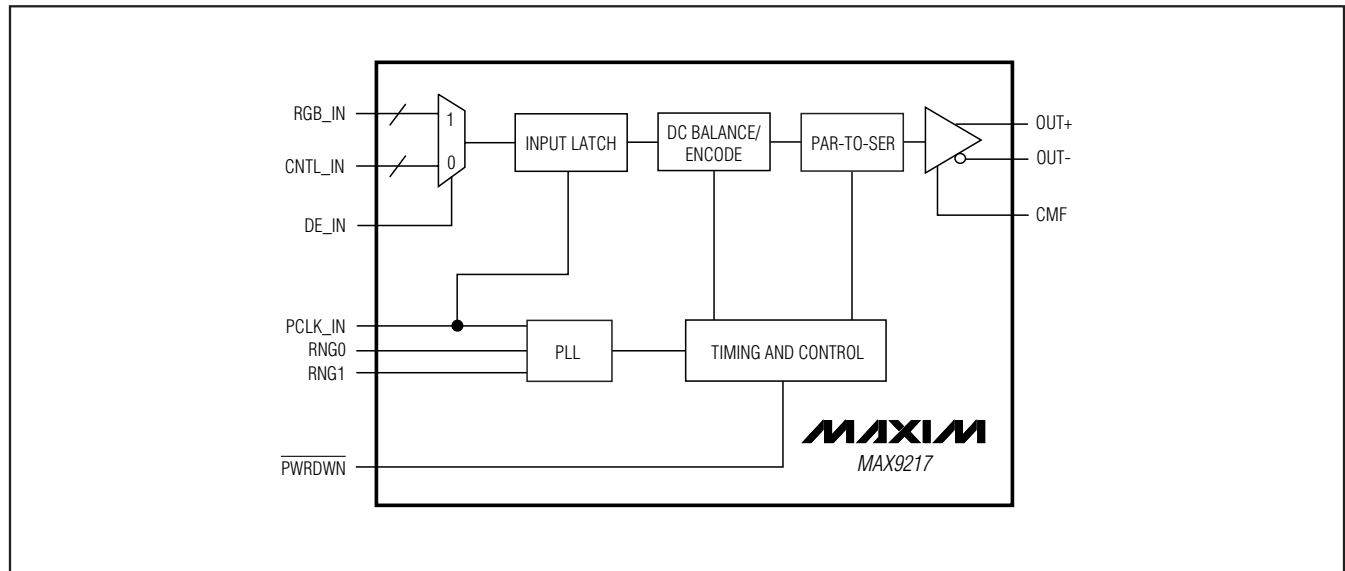


Figure 1. LVDS DC Output Load and Parameters

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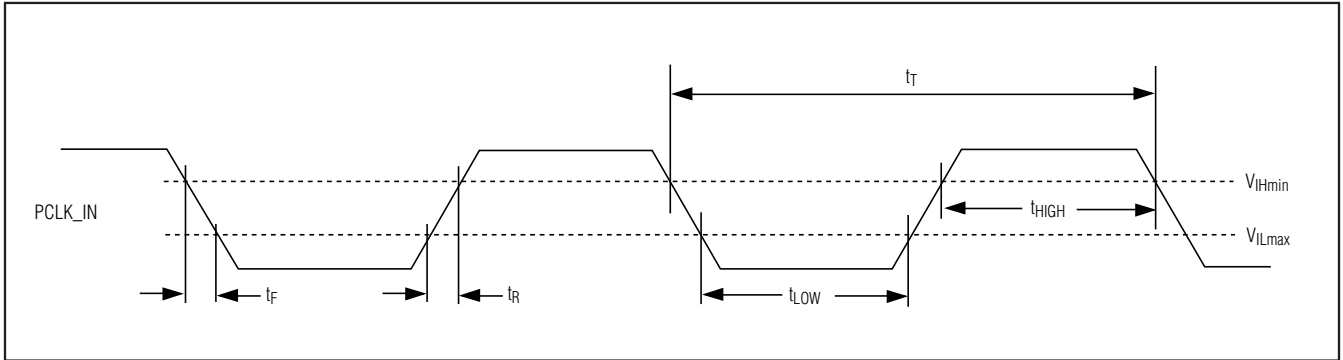


Figure 2. Parallel Clock Requirements

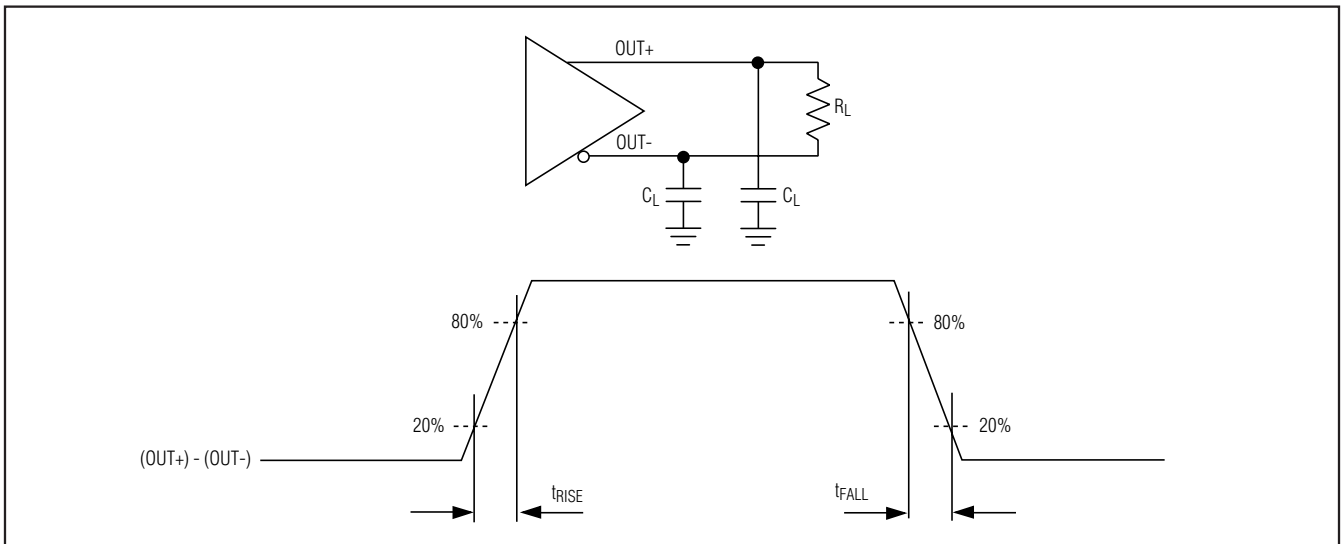


Figure 3. Output Rise and Fall Times

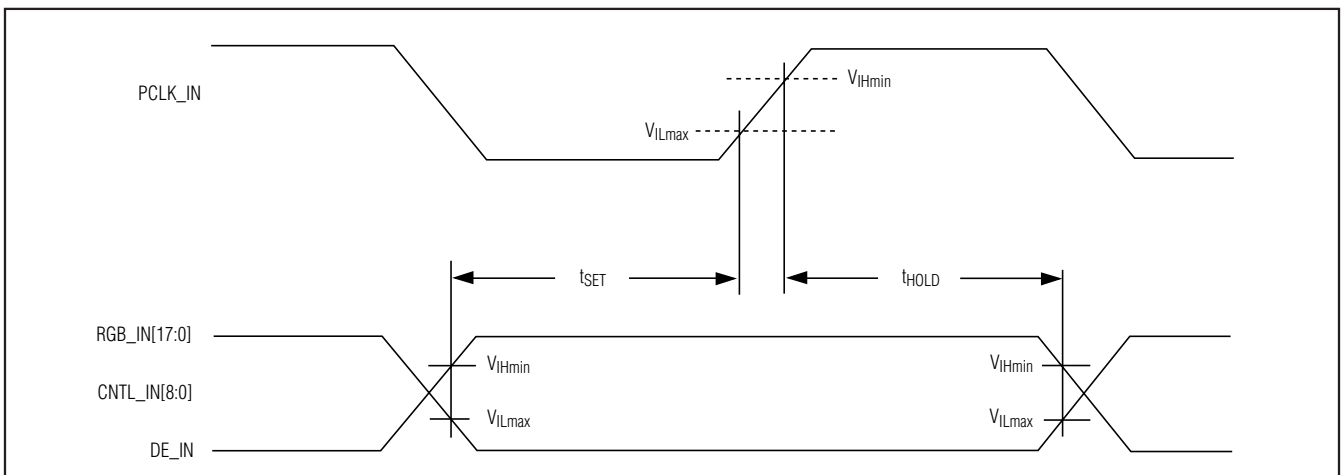


Figure 4. Synchronous Input Timing

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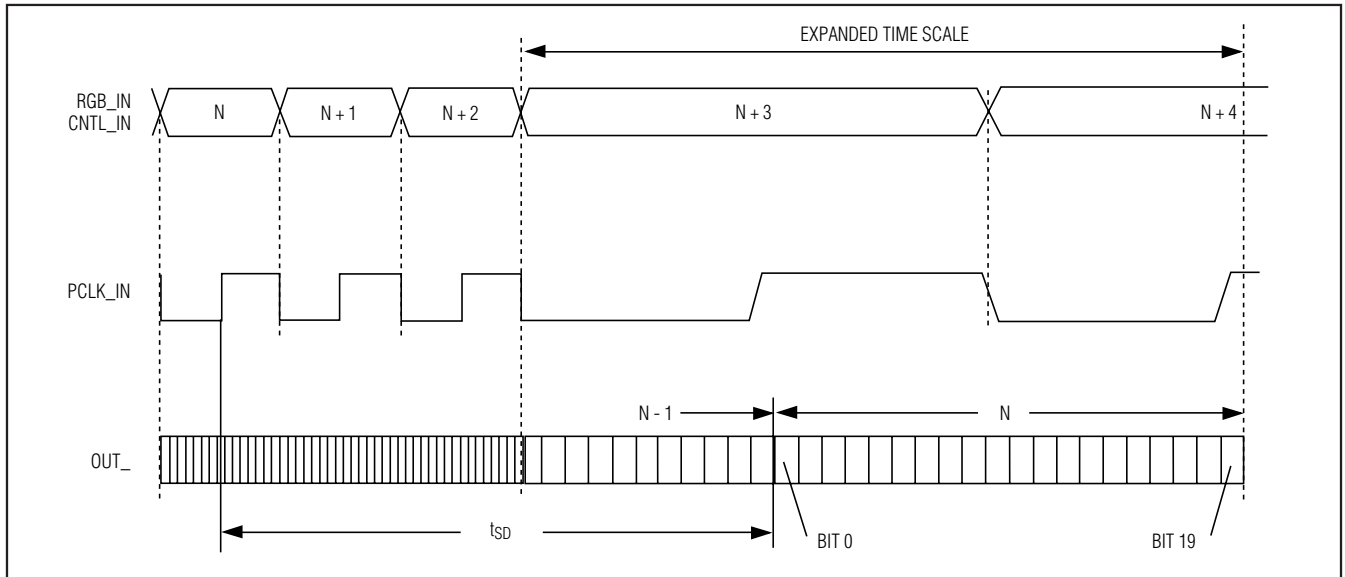


Figure 5. Serializer Delay

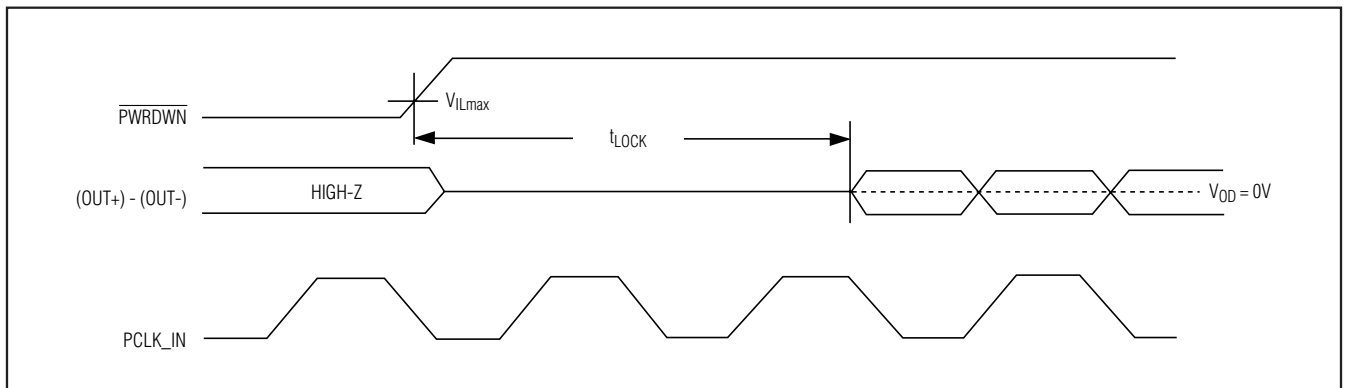


Figure 6. PLL Lock Time

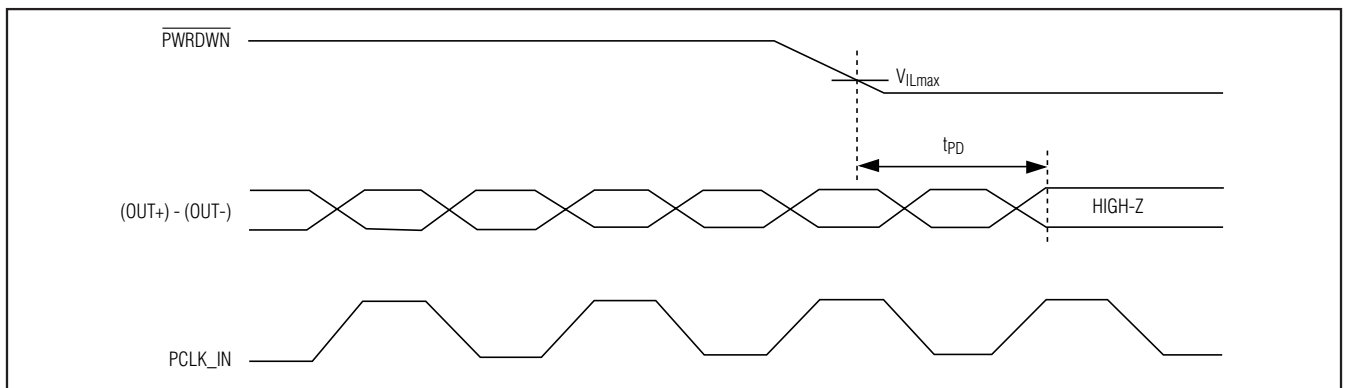


Figure 7. Power-Down Delay

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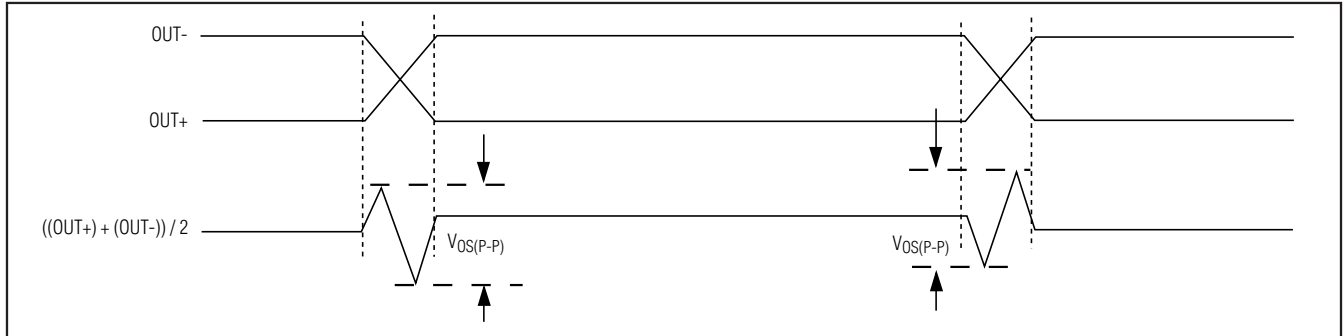


Figure 8. Peak-to-Peak Output Offset Voltage

## Detailed Description

The MAX9217 DC-balanced serializer operates at a parallel clock frequency of 3MHz to 35MHz, serializing 18 bits of parallel video data RGB\_IN[17:0] when the data enable input DE\_IN is high, or 9 bits of parallel control data CNTL\_IN[8:0] when DE\_IN is low. The RGB video input data are encoded using 2 overhead bits, EN0 and EN1, resulting in a serial word length of 20 bits (Table 1). Control inputs are mapped to 19 bits and encoded with 1 overhead bit, EN0, also resulting in a 20-bit serial word. Encoding reduces EMI and main-

tains DC balance across the serial cable. Two transition words, which contain a unique bit sequence, are inserted at the transition boundaries of video-to-control and control-to-video phases.

Control data inputs C0 to C4 are mapped to 3 bits each in the serial control word (Table 2). At the deserializer, 2 or 3 bits at the same state determine the state of the recovered bit, providing single bit-error tolerance for C0 to C4. Control data that may be visible if an error occurs, such as VSYNC and HSYNC, can be connected to these inputs. Control data inputs C5 to C8 are mapped to 1 bit each.

Table 1. Serial Video Phase Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	EN1	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17

Bit 0 is the LSB and is serialized first. EN[1:0] are encoding bits. S[17:0] are encoded symbols.

Table 2. Serial Control Phase Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	C0	C0	C0	C1	C1	C1	C2	C2	C2	C3	C3	C3	C4	C4	C4	C5	C6	C7	C8

Bit 0 is the LSB and is serialized first. C[8:0] are the control inputs.



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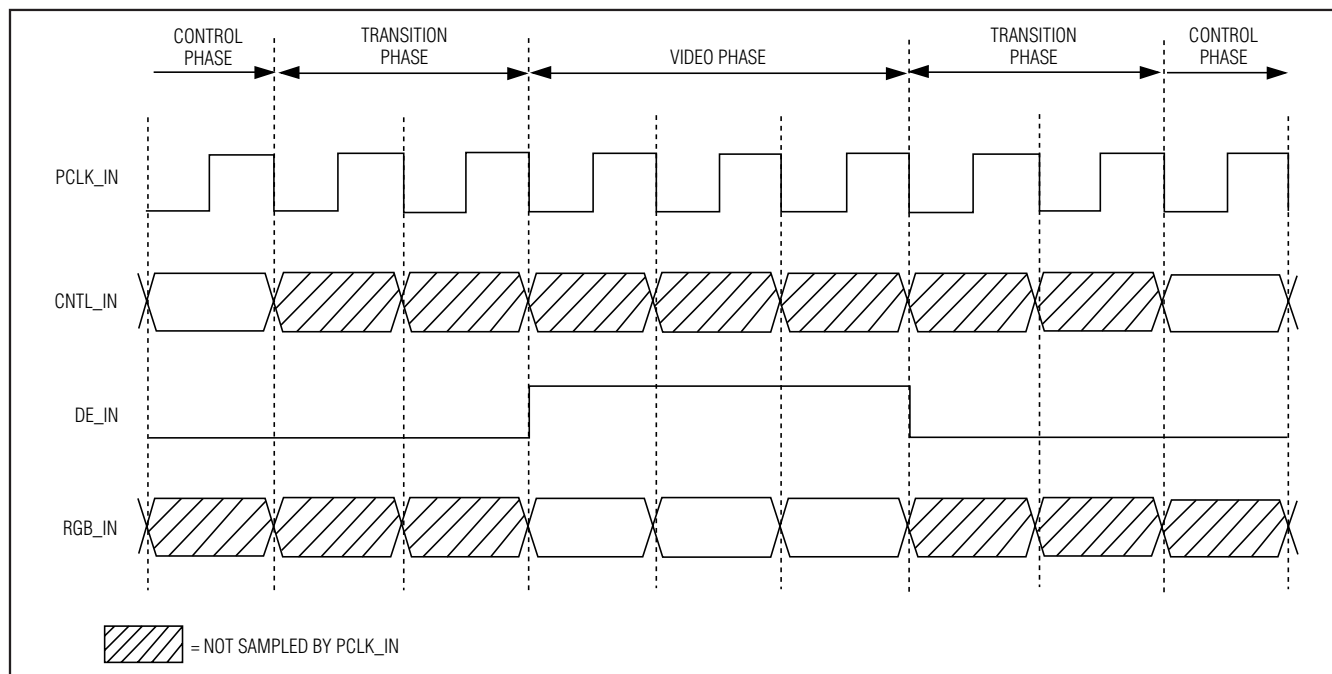


Figure 9. Transition Timing

### Transition Timing

The transition words require interconnect bandwidth and displace control data. Therefore, control data is not sampled (see Figure 9):

- Two clock cycles before DE\_IN goes high.
- During the video phase.
- Two clock cycles after DE\_IN goes low.

The last sampled control data are latched at the deserializer control data outputs during the transition and video phases. Video data are latched at the deserializer RGB data outputs during the transition and control phases.

### Applications Information

#### AC-Coupling Benefits

AC-coupling increases the common-mode voltage to the voltage rating of the capacitor. Two capacitors are sufficient for isolation, but four capacitors—two at the serializer output and two at the deserializer input—provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and common-mode noise. The MAX9217 serializer can also be DC-coupled to the MAX9218 deserializer.

Figure 10 shows an AC-coupled serializer and deserializer with two capacitors per link, and Figure 11 is the AC-coupled serializer and deserializer with four capacitors per link.

### Selection of AC-Coupling Capacitors

See Figure 12 for calculating the capacitor values for AC-coupling, depending on the parallel clock frequency. The plot shows capacitor values for two- and four-capacitor-per-link systems. For applications using less than 18MHz clock frequency, use 0.1μF capacitors.

### Frequency-Range Setting RNG[1:0]

The RNG[1:0] inputs select the operating frequency range of the MAX9217 serializer. An external clock within this range is required for operation. Table 3 shows the selectable frequency ranges and corresponding data rates for the MAX9217.

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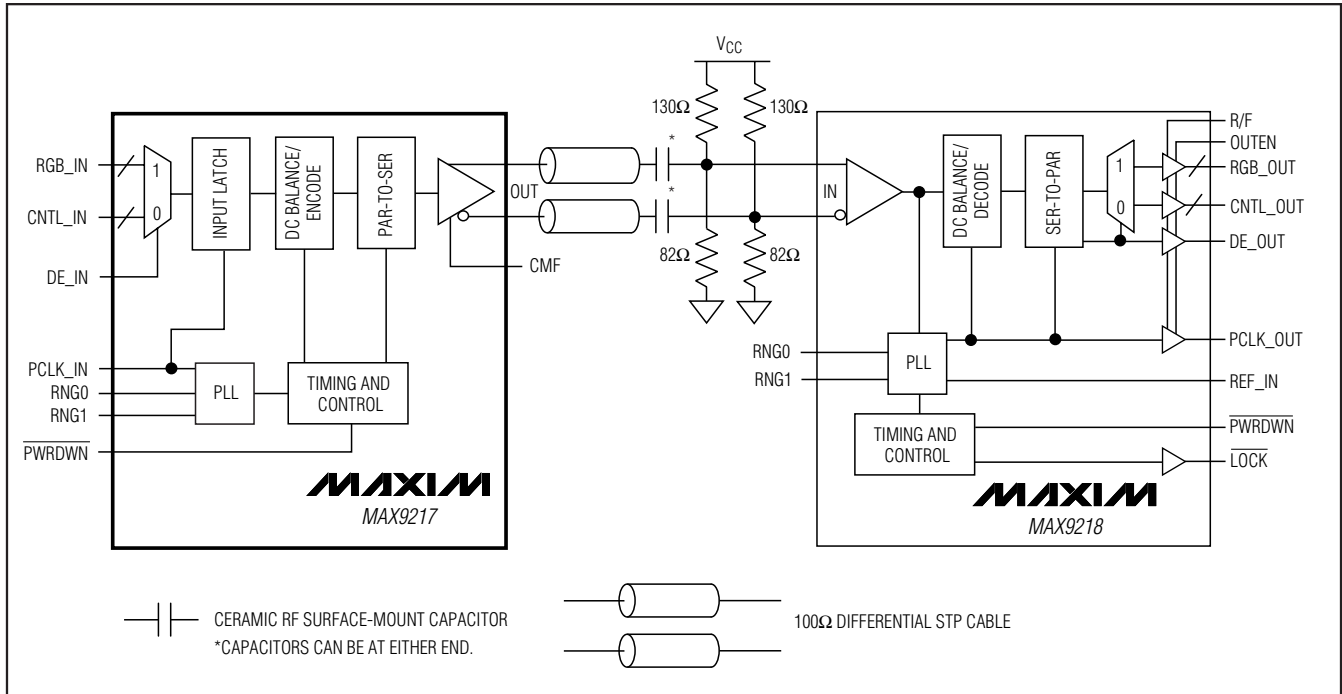


Figure 10. AC-Coupled Serializer and Deserializer with Two Capacitors per Link

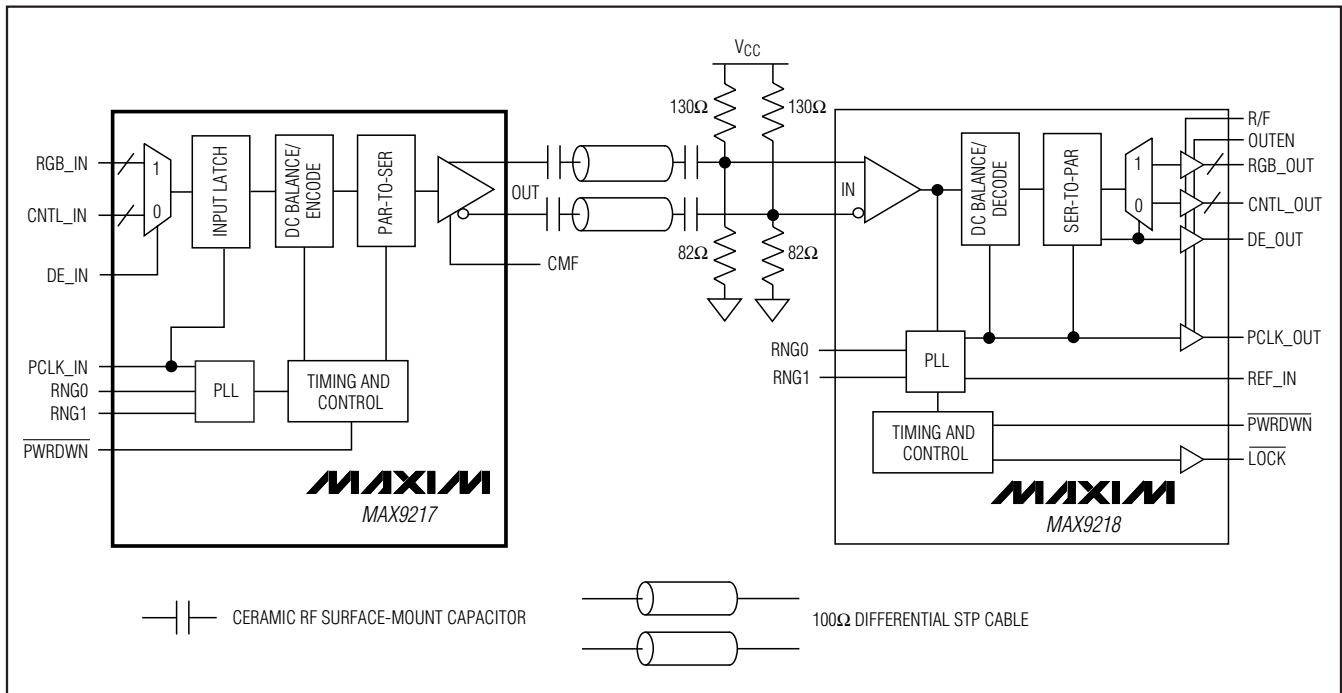


Figure 11. AC-Coupled Serializer and Deserializer with Four Capacitors per Link

# 27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer

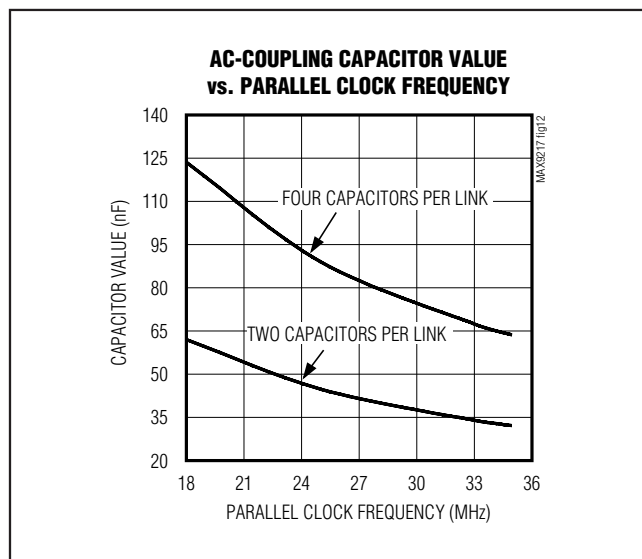


Figure 12. AC-Coupling Capacitor Values vs. Clock Frequency of 18MHz to 35MHz

## Termination

The MAX9217 has an integrated  $100\Omega$  output-termination resistor. This resistor damps reflections from induced noise and mismatches between the transmission line impedance and termination resistors at the deserializer input. With  $PWRDWN = \text{low}$  or with the supply off, the output termination is switched out and the LVDS output is high impedance.

## Common-Mode Filter

The integrated  $100\Omega$  output termination is made up of two  $50\Omega$  resistors in series. The junction of the resistors is connected to the CMF pin for connecting an optional common-mode filter capacitor. Connect the filter capacitor to ground close to the MAX9217 as shown in Figure 13. The capacitor shunts common-mode switching current to ground to reduce EMI.

Table 3. Parallel Clock Frequency Range Select

RNG1	RNG0	PARALLEL CLOCK (MHz)	SERIAL DATA RATE (Mbps)
0	0	3 to 5	60 to 100
0	1	5 to 10	100 to 200
1	0	10 to 20	200 to 400
1	1	20 to 35	400 to 700

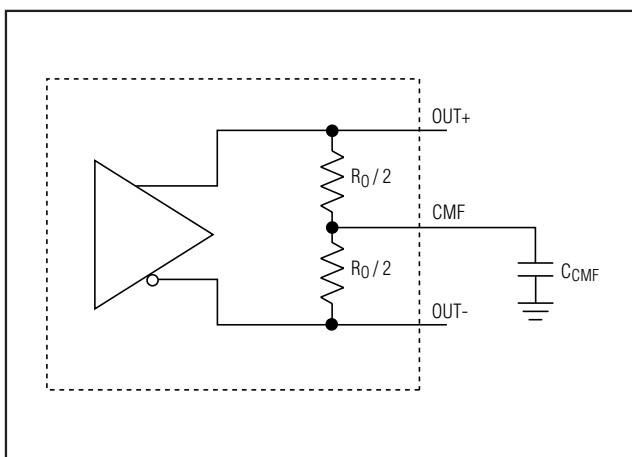


Figure 13. Common-Mode Filter Capacitor Connection

## 27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer

### Power-Down and Power-Off

Driving  $\overline{\text{PWRDWN}}$  low stops the PLL, switches out the integrated  $100\Omega$  output termination, and puts the output in high impedance to ground and differentially. With  $\overline{\text{PWRDWN}} \leq 0.3\text{V}$  and all LVTTTL/LVCMOS inputs  $\leq 0.3\text{V}$  or  $\geq V_{\text{CCIN}} - 0.3\text{V}$ , supply current is reduced to  $50\mu\text{A}$  or less.

Driving  $\overline{\text{PWRDWN}}$  high starts PLL lock to PCLK\_IN and switches in the  $100\Omega$  output termination resistor. The LVDS output is not driven until the PLL locks. The LVDS output is high impedance to ground and  $100\Omega$  differential. The  $100\Omega$  integrated termination pulls OUT+ and OUT- together while the PLL is locking so that  $V_{\text{OD}} = 0\text{V}$ .

If  $V_{\text{CC}} = 0$ , the output resistor is switched out and the LVDS outputs are high impedance to ground and differentially.

### PLL Lock Time

The PLL lock time is set by an internal counter. The lock time is 16,385 PCLK\_IN cycles. Power and clock should be stable to meet the lock-time specification.

### Input Buffer Supply

The single-ended inputs (RGB\_IN[17:0], CNTL\_IN[8:0], DE\_IN, RNG0, RNG1, PCLK\_IN, and  $\overline{\text{PWRDWN}}$ ) are powered from  $V_{\text{CCIN}}$ .  $V_{\text{CCIN}}$  can be connected to a 1.71V to 3.6V supply, allowing logic inputs with a nominal swing of  $V_{\text{CCIN}}$ . If no power is applied to  $V_{\text{CCIN}}$  when power is applied to  $V_{\text{CC}}$ , the inputs are disabled and  $\overline{\text{PWRDWN}}$  is internally driven low, putting the device in the power-down state.

### Power-Supply Circuits and Bypassing

The MAX9217 has isolated on-chip power domains. The digital core supply ( $V_{\text{CC}}$ ) and single-ended input supply ( $V_{\text{CCIN}}$ ) are isolated but have a common ground (GND). The PLL has separate power and ground ( $V_{\text{CCPLL}}$  and  $V_{\text{CCPLL GND}}$ ) and the LVDS input also has separate power and ground ( $V_{\text{CCLVDS}}$  and  $V_{\text{CCLVDS GND}}$ ). The grounds are isolated by diode connections. Bypass each  $V_{\text{CC}}$ ,  $V_{\text{CCIN}}$ ,  $V_{\text{CCPLL}}$ , and  $V_{\text{CCLVDS}}$  pin with high-frequency, surface-mount ceramic  $0.1\mu\text{F}$  and  $0.001\mu\text{F}$  capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

### LVDS Output

The LVDS output is a current source. The voltage swing is proportional to the termination resistance. The output is rated for a differential load of  $100\Omega \pm 1\%$ .

### Cables and Connectors

Interconnect for LVDS typically has a differential impedance of  $100\Omega$ . Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

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## Board Layout

Separate the LVTTTL/LVCMOS inputs and LVDS output to prevent crosstalk. A four-layer PCB with separate layers for power, ground, and signals is recommended.

## ESD Protection

The MAX9217 ESD tolerance is rated for Human Body Model, Machine Model, and ISO 10605. ISO 10605

specifies ESD tolerance for electronic systems. The Human Body Model, Machine Model, discharge components are  $C_S = 100\text{pF}$  and  $R_D = 1.5\text{k}\Omega$  (Figure 14). The ISO 10605 discharge components are  $C_S = 330\text{pF}$  and  $R_D = 2\text{k}\Omega$  (Figure 15). The Machine Model discharge components are  $C_S = 200\text{pF}$  and  $R_D = 0\Omega$  (Figure 16).

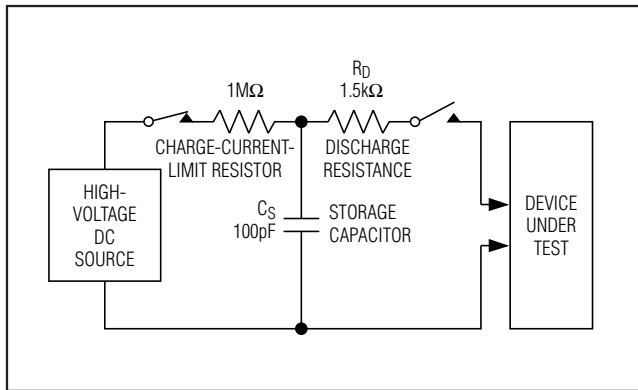


Figure 14. Human Body ESD Test Circuit

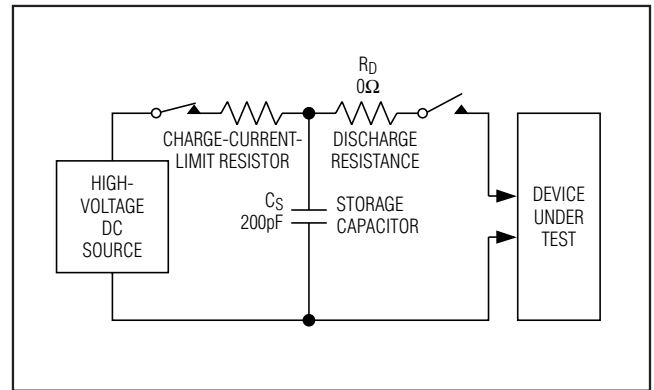


Figure 16. Machine Model ESD Test Circuit

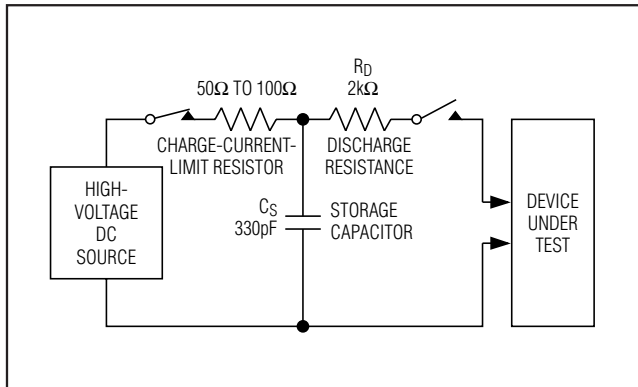


Figure 15. ISO 10605 Contact-Discharge ESD Test Circuit

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 LQFP	C48+5	<a href="#">21-0054</a>
48 TQFN	T4866+1	<a href="#">21-0141</a>

# 27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	5/08	Corrected LQFP package, removed MOD function pins, added Machine Model ESD, and corrected diagrams	1, 2, 5, 6, 10–15
4	8/09	Added automotive qualified part to <i>Ordering Information</i>	1

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