

# +5V Microprocessor Supervisory Circuits

## ABSOLUTE MAXIMUM RATINGS

Input Voltage	
V <sub>CC</sub> , BATT .....	-0.3V to +6.0V
All Other Pins (Note 1) .....	-0.3V to (V <sub>CC</sub> + 0.3V)
Input Current	
V <sub>CC</sub> Peak .....	1A
V <sub>CC</sub> Continuous .....	250mA
BATT Peak .....	250mA
BATT Continuous .....	50mA
GND .....	25mA
Output Current	
OUT .....	250mA
All Other Outputs .....	25mA
OUT Short-Circuit Duration .....	10sec

Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
Plastic DIP (derate 9.09mW/°C above +70°C) .....	727mW
SO (derate 5.88mW/°C above +70°C) .....	471mW
μMAX (derate 4.10mW/°C above +70°C) .....	330mW
Operating Temperature Ranges	
MAX81__C_A .....	0°C to +70°C
MAX81__E_A .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +160°C
Lead Temperature (soldering, 10sec) .....	+300°C

**Note 1:** The input voltage limits on PFI and WDI may be exceeded (up to 12V V<sub>IN</sub>) if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +4.75V to +5.5V for MAX81\_L, V<sub>CC</sub> = +4.5V to +5.5V for MAX81\_M, V<sub>BATT</sub> = 2.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V <sub>CC</sub> , V <sub>BATT</sub> (Note 2)			0		5.5	V
Supply Current (excluding I <sub>OUT</sub> )	I <sub>SUPPLY</sub>	As applicable; $\overline{CE}$ IN = 0V, WDI and $\overline{MR}$ unconnected	MAX81__C	11	45	μA
			MAX81__E	11	60	
Supply Current in Battery-Backup Mode (excluding I <sub>OUT</sub> )		V <sub>CC</sub> = 0V	T <sub>A</sub> = +25°C	0.05	1.0	μA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		5.0	
BATT Standby Current (Note 3)		5.5V > V <sub>CC</sub> > (V <sub>BATT</sub> + 0.2V)	T <sub>A</sub> = +25°C	-0.10	0.02	μA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	-1.00	0.02	
BATT Leakage Current, Freshness Seal Enabled		V <sub>CC</sub> = 0V, V <sub>OUT</sub> = 0V			1	μA
V <sub>OUT</sub> Output		I <sub>OUT</sub> = 5mA	V <sub>CC</sub> - 0.05	V <sub>CC</sub> - 0.025		V
		I <sub>OUT</sub> = 50mA	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.25		
V <sub>CC</sub> to OUT On-Resistance				5	10	Ω
BATT to OUT On-Resistance				100		Ω
V <sub>OUT</sub> in Battery-Backup Mode		I <sub>OUT</sub> = 250μA, V <sub>CC</sub> < (V <sub>BATT</sub> - 0.2V)	V <sub>BATT</sub> - 0.1	V <sub>BATT</sub> - 0.02		V
Battery Switch Threshold (V <sub>CC</sub> - V <sub>BATT</sub> )		V <sub>CC</sub> < V <sub>RST</sub>	Power-up	20		mV
			Power-down	-20		
Battery Switchover Hysteresis				40		mV

# +5V Microprocessor Supervisory Circuits

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = +4.75V to +5.5V for MAX81\_L, V<sub>CC</sub> = +4.5V to +5.5V for MAX81\_M, V<sub>BATT</sub> = 2.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
RESET AND WATCHDOG TIMER							
Reset Threshold	VRST	MAX81_L	4.50	4.65	4.75	V	
		MAX81_M	4.25	4.40	4.50		
Reset Threshold Hysteresis			25			mV	
Reset Timeout Period	trp		140	200	280	ms	
RESET Output Voltage	VOH	VCC > VRST(MAX), ISOURCE = 800μA	VCC - 1.5			V	
	VOL	VCC < VRST(MIN), ISINK = 3.2mA	0.4				
		MAX81__C, VCC = 1V, VCC falling, VBATT = 0V, ISINK = 50μA	0.3				
		MAX81__E, VCC = 1.2V, VCC falling, VBATT = 0V, ISINK = 100μA	0.3				
VCC to RESET Delay		From VRST, VCC falling at 10V/ms	100			μs	
Watchdog Timeout Period	tWD		1.00	1.60	2.25	sec	
WDI Pulse Width	tWDI	VIL = 0.4V, VIH = 0.8VCC	50				ns
WDI Input Threshold (Note 4)	VIL	VCC = 5V	0.8			V	
	VIH		3.5				
WDI Input Current (Note 5)		WDI = VCC, time average	120		160	μA	
		WDI = GND, time average	-20	-15			
POWER-FAIL COMPARATOR (MAX817/MAX819 only)							
PFI Input Threshold	VPFT		1.20	1.25	1.30	V	
PFI Input Hysteresis			4			mV	
PFI Input Current	IPFI		-25	0.01	25	nA	
PFO Output Voltage	VOL	VPFI < 1.20V, ISINK = 3.2mA, VCC > 4.50V	0.4			V	
	VOH	VPFI > 1.30V, ISOURCE = 40μA, VCC > 4.5V	VCC - 1.5				
PFO Short-Circuit Current		VPFO = 0V	250		500	μA	
MANUAL RESET INPUT (MAX819 only)							
MR Input Threshold	VIL		0.8			V	
	VIH		2.0				
MR Pulse Width			1			μs	
MR Pulse that Would Not Cause a Reset			100			ns	
MR to Reset Delay			120			ns	
MR Pull-Up Resistance			45	63	85	kΩ	

MAX817L/M, MAX818L/M, MAX819L/M

# +5V Microprocessor Supervisory Circuits

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$  = +4.75V to +5.5V for MAX81\_L,  $V_{CC}$  = +4.5V to +5.5V for MAX81\_M,  $V_{BATT}$  = 2.8V,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A$  = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHIP-ENABLE GATING (MAX818 only)						
$\overline{CE}$ IN Leakage Current		Disable mode		±0.005	±1	μA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance (Note 6)		Enable mode		40	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)		Disable mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN to $\overline{CE}$ OUT Propagation Delay (Note 7)		50Ω source impedance driver, C <sub>LOAD</sub> = 50pF		3	8	ns
$\overline{CE}$ OUT Output	V <sub>OH</sub>	I <sub>OUT</sub> = -100μA, V <sub>CC</sub> = 0V	V <sub>CC</sub> - 1V			V
		I <sub>OUT</sub> = -1μA, V <sub>CC</sub> = 0V, V <sub>BATT</sub> = 2.8V	2.7			
$\overline{CE}$ OUT Input Threshold	V <sub>IH</sub>	V <sub>CC</sub> = 5V	0.8			V
	V <sub>IL</sub>		3.5			
$\overline{RESET}$ to $\overline{CE}$ OUT Delay		Power-down		15		μs

**Note 2:** Either  $V_{CC}$  or  $V_{BATT}$  can go to 0V if the other is greater than 2.0V.

**Note 3:** “-” = battery-charging current, “+” = battery-discharging current.

**Note 4:** WDI is internally serviced within the watchdog timeout period if WDI is left unconnected.

**Note 5:** WDI input is designed to be driven by a three-stated output device. To float WDI, the “high-impedance mode” of the output device must have a maximum leakage current of 10μA and a maximum output capacitance of 200pF. The output device must also be able to source and sink at least 200μA when active.

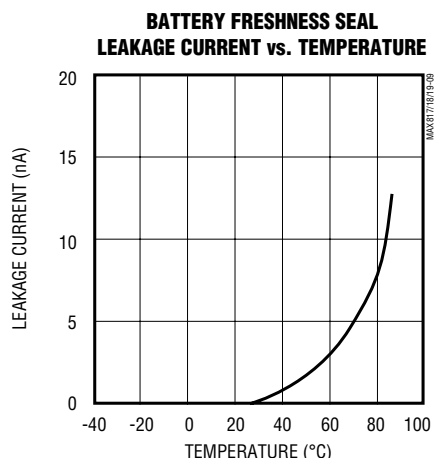
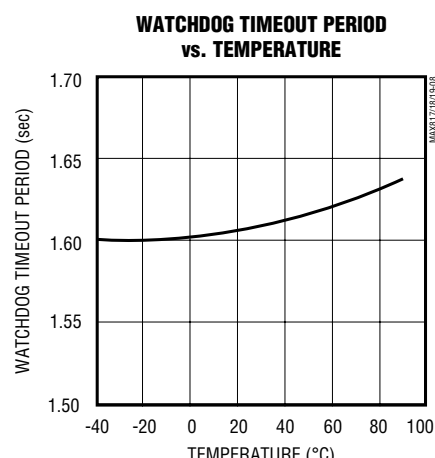
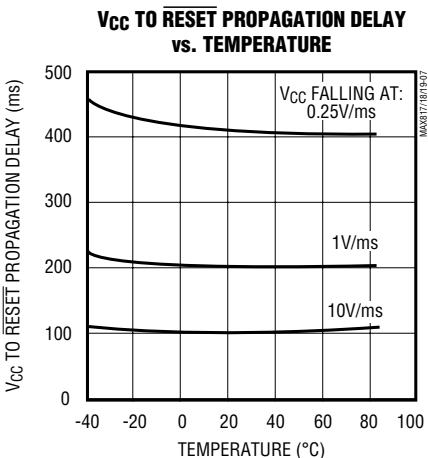
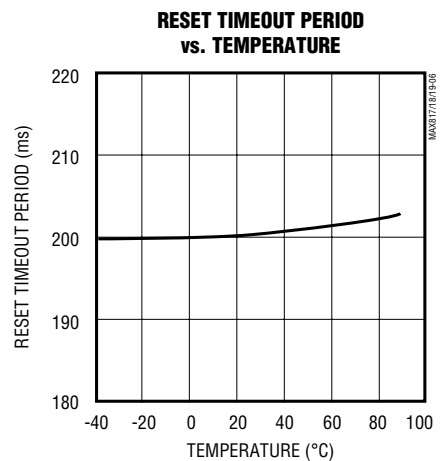
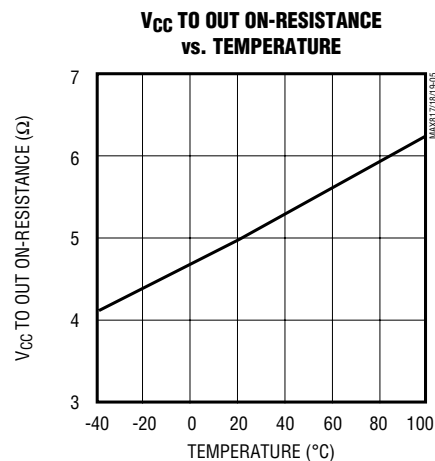
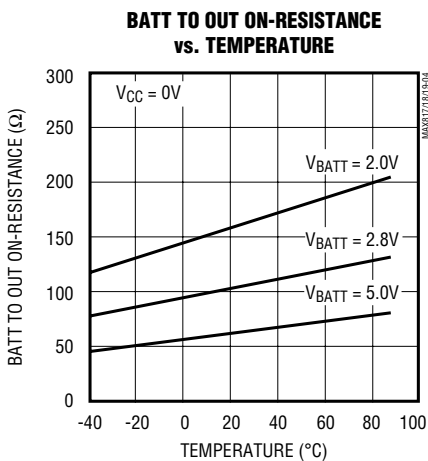
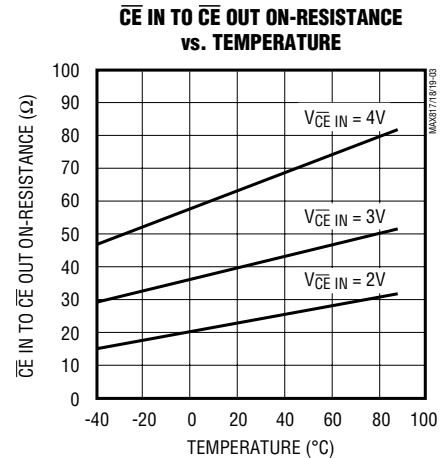
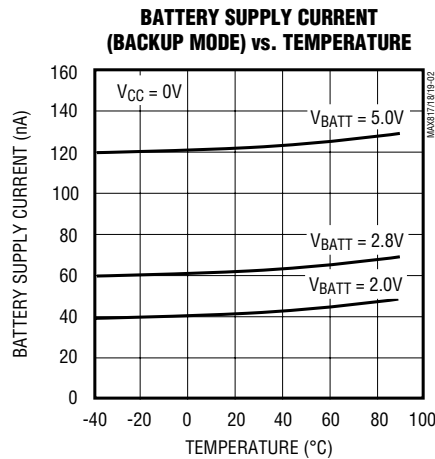
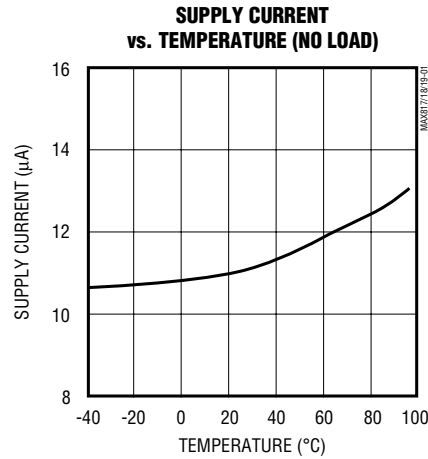
**Note 6:** The chip-enable resistance is tested with  $V_{CC}$  = +4.75V for the MAX818L and  $V_{CC}$  = +4.5V for the MAX818M.  $V_{\overline{CE} IN} = V_{\overline{CE} OUT} = V_{CC}/2$ .

**Note 7:** The chip-enable propagation delay is measured from the 50% point at  $\overline{CE}$  IN to the 50% point at  $\overline{CE}$  OUT.

# +5V Microprocessor Supervisory Circuits

## Typical Operating Characteristics

( $V_{CC} = +5V$ ,  $V_{BATT} = 3.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

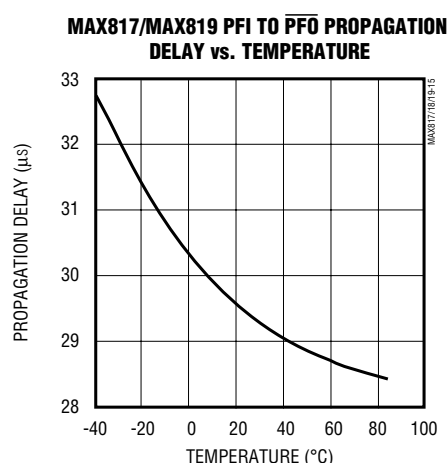
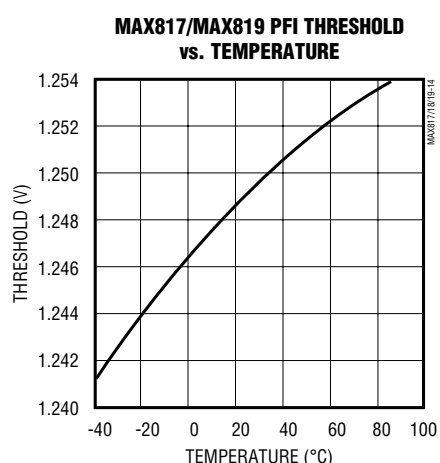
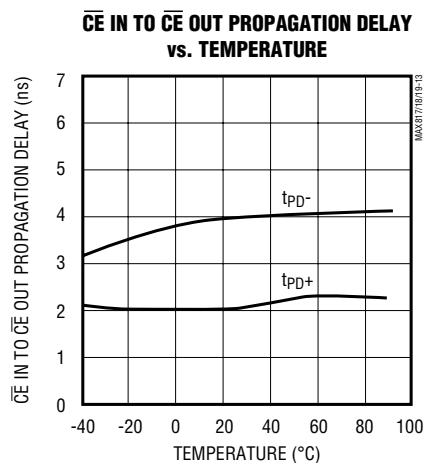
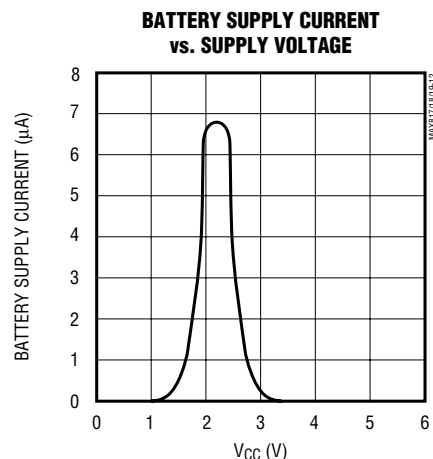
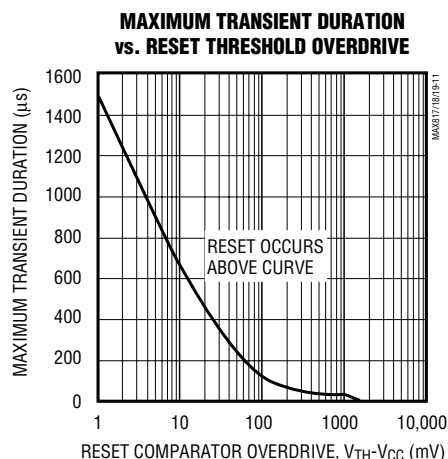
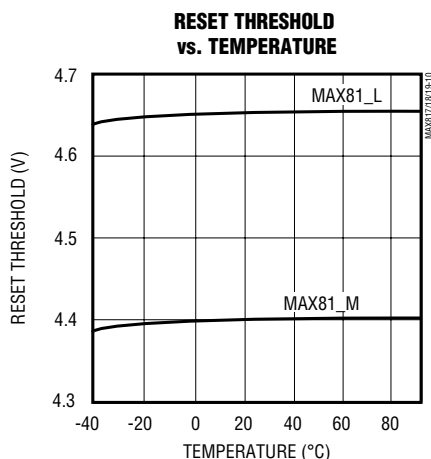


MAX817L/M, MAX818L/M, MAX819L/M

# +5V Microprocessor Supervisory Circuits

## Typical Operating Characteristics (continued)

( $V_{CC} = +5V$ ,  $V_{BATT} = 3.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# +5V Microprocessor Supervisory Circuits

## Pin Description

MAX817L/M, MAX818L/M, MAX819L/M

PIN			NAME	FUNCTION
MAX817	MAX818	MAX819		
1	1	1	OUT	Supply Output for CMOS RAM. When $V_{CC}$ rises above the reset threshold or above $V_{BATT}$ , OUT is connected to $V_{CC}$ through an internal P-channel MOSFET switch. When $V_{CC}$ falls below $V_{BATT}$ , BATT connects to OUT.
2	2	2	$V_{CC}$	Input Supply Voltage, +5V input.
3	3	3	GND	Ground. 0V reference for all signals.
4	—	4	PFI	Power-Fail Comparator Input. When $V_{PFI}$ is below $V_{PFT}$ or when $V_{CC}$ is below $V_{BATT}$ , $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high (see <i>Power-Fail Comparator</i> section). Connect to ground if unused.
—	4	—	$\overline{CE}$ IN	Chip-Enable Input. The input to the chip-enable gating circuit. Connect to ground if unused.
5	—	5	$\overline{PFO}$	Power-Fail Comparator Output. When PFI is less than $V_{PFT}$ or when $V_{CC}$ is below $V_{BATT}$ , $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. $\overline{PFO}$ is also used to enable the battery freshness seal (see <i>Battery Freshness Seal</i> and <i>Power-Fail Comparator</i> sections).
—	5	—	$\overline{CE}$ OUT	Chip-Enable Output. $\overline{CE}$ OUT goes low only if $\overline{CE}$ IN is low while reset is not asserted. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will remain low for 15 $\mu$ s or until $\overline{CE}$ IN goes high, whichever occurs first. $\overline{CE}$ OUT is pulled up to OUT in battery-backup mode. $\overline{CE}$ OUT is also used to enable the battery freshness seal (see <i>Battery Freshness Seal</i> section).
6	6	—	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a reset is triggered. If WDI is left unconnected or is connected to a high-impedance three-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge. The WDI input is designed to be driven by a three-stated-output device with a maximum high-impedance leakage current of 10 $\mu$ A and a maximum output capacitance of 200pF. The output device must also be capable of sinking and sourcing 200 $\mu$ A when active.
—	—	6	$\overline{MR}$	Manual Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted for as long as $\overline{MR}$ is held low and for 200ms after $\overline{MR}$ returns high. The active-low input has an internal 63k $\Omega$ pull-up resistor. It can be driven from a TTL- or CMOS-logic line or shorted to ground with a switch. Leave open, or connect to $V_{CC}$ if unused.
7	7	7	$\overline{RESET}$	Active-Low Reset Output. Pulses low for 200ms when triggered and remains low whenever $V_{CC}$ is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for 200ms after $V_{CC}$ rises above the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes low to high.
8	8	8	BATT	Backup-Battery Input. When $V_{CC}$ falls below $V_{BATT}$ , OUT switches from $V_{CC}$ to BATT. When $V_{CC}$ rises above $V_{BATT}$ , OUT reconnects to $V_{CC}$ .

# +5V Microprocessor Supervisory Circuits

**MAX817L/M, MAX818L/M, MAX819L/M**

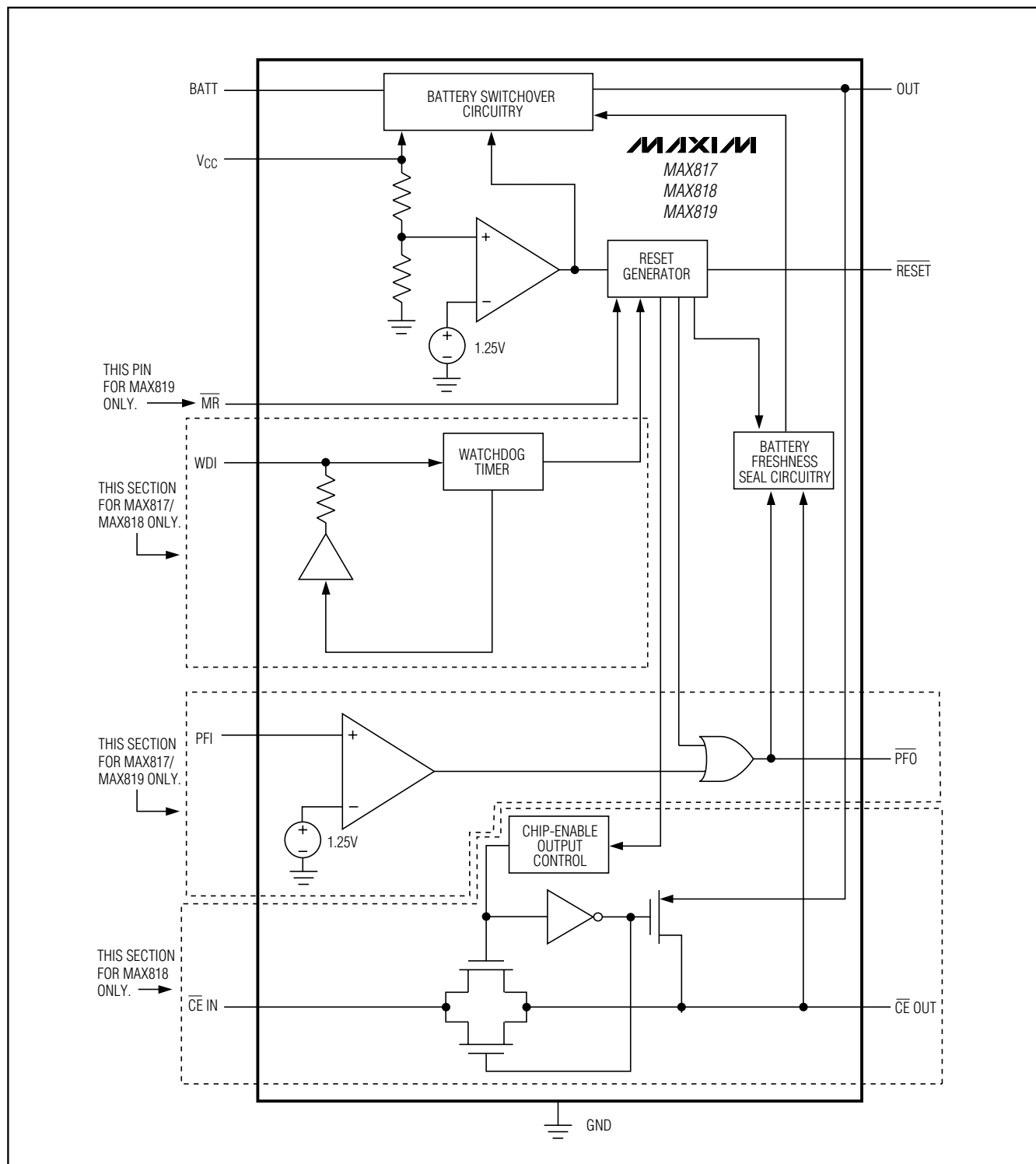


Figure 1. Functional Diagram

# +5V Microprocessor Supervisory Circuits

## Detailed Description

### General Timing Characteristics

Designed for 5V systems, the MAX817/MAX818/MAX819 provide a number of microprocessor ( $\mu$ P) supervisory functions (see the *Selector Guide* on the first page). Figure 2 shows the typical timing relationships of the various outputs during power-up and power-down with typical  $V_{CC}$  rise and fall times.

### RESET Output

A  $\mu$ P's reset input starts the  $\mu$ P in a known state. The MAX817/MAX818/MAX819  $\mu$ P supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions.  $\overline{\text{RESET}}$  is guaranteed to be a logic low for  $0V < V_{CC} < V_{RST}$  if  $V_{BATT}$  is greater than 1V. Without a backup battery ( $V_{BATT} = \text{GND}$ )  $\overline{\text{RESET}}$  is guaranteed valid for  $V_{CC} \geq 1V$ . Once  $V_{CC}$  exceeds the reset threshold an internal timer keeps  $\overline{\text{RESET}}$  low for the reset timeout period,  $t_{RP}$ . After this interval  $\overline{\text{RESET}}$  returns high (Figure 2).

If a brownout condition occurs ( $V_{CC}$  drops below the reset threshold),  $\overline{\text{RESET}}$  goes low. Each time  $\overline{\text{RESET}}$  is asserted it stays low for at least the reset timeout period. Any time  $V_{CC}$  goes below the reset threshold the internal timer clears. The reset timer starts when  $V_{CC}$  returns above the reset threshold.  $\overline{\text{RESET}}$  both sources and sinks current.

### Manual Reset Input (MAX819)

Many  $\mu$ P-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX819, a logic low on  $\overline{\text{MR}}$  asserts reset. Reset remains asserted while  $\overline{\text{MR}}$  is low, and for  $t_{RP}$  (200ms) after it returns high.

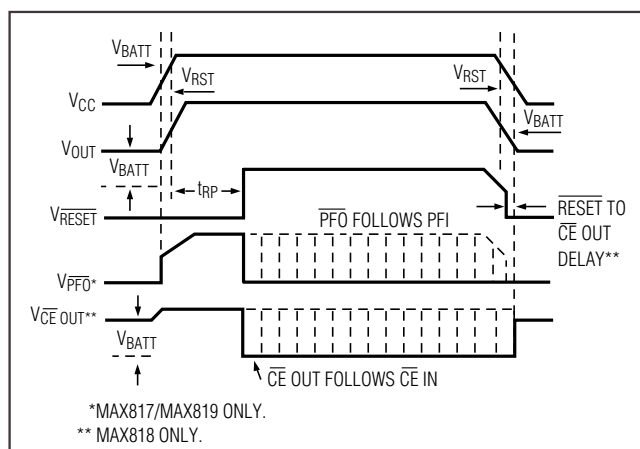


Figure 2. Power-Up and Power-Down Timing

During the reset timeout period ( $t_{RP}$ ),  $\overline{\text{MR}}$ 's state is ignored if the battery freshness seal is enabled.  $\overline{\text{MR}}$  has an internal 63k $\Omega$  pull-up resistor, so it can be left open if not used. This input can be driven with TTL/CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{\text{MR}}$  to GND to create a manual reset function; external debounce circuitry is not required. If  $\overline{\text{MR}}$  is driven from long cables or the device is used in a noisy environment, connect a 0.1 $\mu$ F capacitor from  $\overline{\text{MR}}$  to GND to provide additional noise immunity.

Note that  $\overline{\text{MR}}$  must be high or open to enable the battery freshness seal. Once the battery freshness seal is enabled its operation is unaffected by  $\overline{\text{MR}}$ .

### Battery Freshness Seal

The MAX817/MAX818/MAX819 battery freshness seal disconnects the backup battery from internal circuitry and OUT until it is needed. This allows an OEM to ensure that the backup battery connected to BATT will be fresh when the final product is put to use. To enable the freshness seal on the MAX817 and MAX819:

- 1) Connect a battery to BATT.
- 2) Ground  $\overline{\text{PFO}}$ .
- 3) Bring  $V_{CC}$  above the reset threshold and hold it there until reset is deasserted following the reset timeout period.
- 4) Bring  $V_{CC}$  down again (Figure 3).

Use the same procedure for the MAX818, but ground  $\overline{\text{CE OUT}}$  instead of  $\overline{\text{PFO}}$ . Once the battery freshness seal is enabled (disconnecting the backup battery from internal circuitry and anything connected to OUT), it remains enabled until  $V_{CC}$  is brought above  $V_{RST}$ .

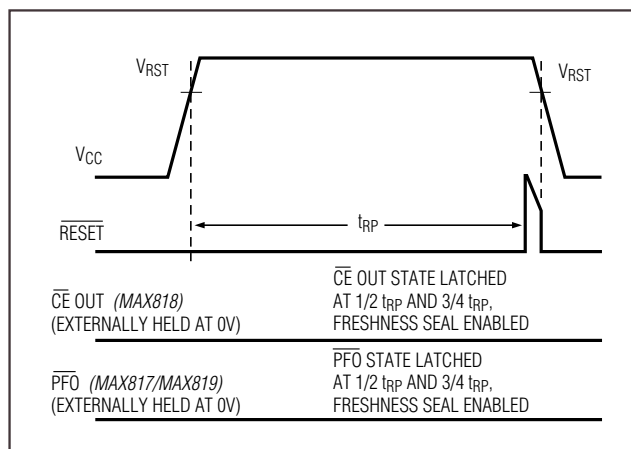


Figure 3. Battery Freshness Seal Timing



## +5V Microprocessor Supervisory Circuits

On the MAX819,  $\overline{MR}$  must be high or open to enable the battery freshness seal. Once the battery freshness seal is enabled its operation is unaffected by  $\overline{MR}$ .

### Watchdog Input (MAX817/MAX818)

In the MAX817/MAX818, the watchdog circuit monitors the  $\mu P$ 's activity. If the  $\mu P$  does not toggle the watchdog input (WDI) within  $t_{WD}$  (1.6sec), reset asserts. The internal 1.6sec timer is cleared by either a reset pulse or by toggling WDI, which can detect pulses as short as 50ns. The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting (Figure 4).

To disable the watchdog function, leave WDI unconnected or three-state the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period, then momentarily pulses high, resetting the watchdog counter. When WDI is left open-circuited, this internal driver clears the 1.6sec timer every 1.4sec. When WDI is three-stated or left unconnected, the maximum allowable leakage current is 10 $\mu A$  and the maximum allowable load capacitance is 200pF.

### Chip-Enable Gating (MAX818)

Internal gating of the chip-enable (CE) signal prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX818 uses a series transmission gate from  $\overline{CE\ IN}$  to  $\overline{CE\ OUT}$  (Figure 5). During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from  $\overline{CE\ IN}$  to  $\overline{CE\ OUT}$  enables the MAX818 to be used with most  $\mu P$ s. If  $\overline{CE\ IN}$  is low when reset asserts,  $\overline{CE\ OUT}$  remains low for typically 15 $\mu s$  to permit the current write cycle to complete.

### Chip-Enable Input (MAX818)

The CE transmission gate is disabled and  $\overline{CE\ IN}$  is high impedance (disabled mode) while reset is asserted. During a power-down sequence when  $V_{CC}$  passes the reset threshold, the CE transmission gate disables and  $\overline{CE\ IN}$  immediately becomes high impedance if the voltage at  $\overline{CE\ IN}$  is high. If  $\overline{CE\ IN}$  is low when reset asserts, the CE transmission gate will disable 15 $\mu s$  after reset asserts (Figure 6). This permits the current write cycle to complete during power-down.

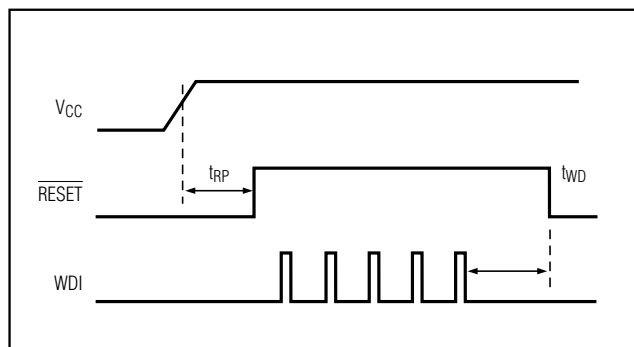


Figure 4. Watchdog Timing

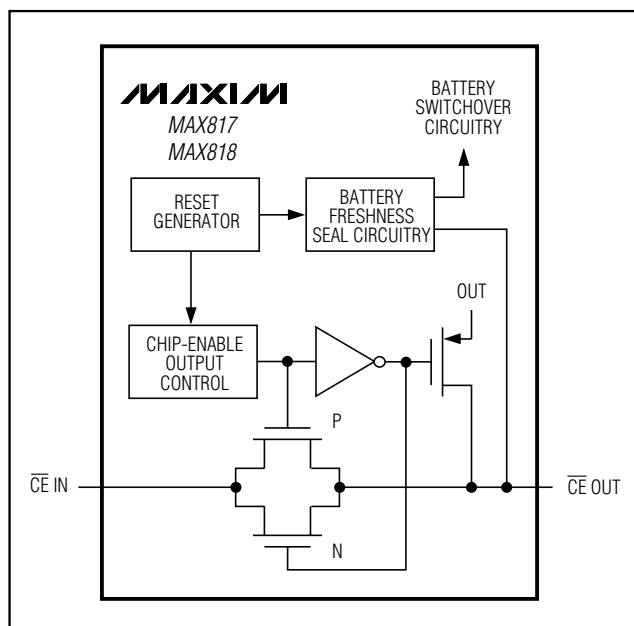


Figure 5. Chip-Enable Transmission Gate

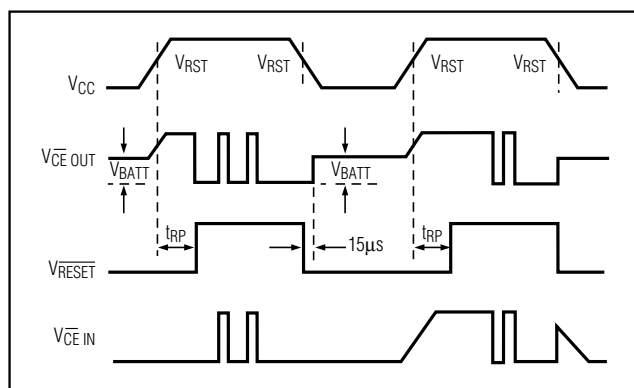


Figure 6. Chip-Enable Timing

## +5V Microprocessor Supervisory Circuits

Any time a reset is generated, the CE transmission gate remains disabled and  $\overline{\text{CE}}$  IN remains high impedance (regardless of  $\overline{\text{CE}}$  IN activity) for the reset timeout period. When the CE transmission gate is enabled, the impedance of  $\overline{\text{CE}}$  IN appears as a  $40\Omega$  resistor in series with the load at  $\overline{\text{CE}}$  OUT. The propagation delay through the CE transmission gate depends on  $V_{\text{CC}}$ , the source impedance of the drive connected to  $\overline{\text{CE}}$  IN, and the loading on  $\overline{\text{CE}}$  OUT (see *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on  $\overline{\text{CE}}$  IN to the 50% point on  $\overline{\text{CE}}$  OUT using a  $50\Omega$  driver and a  $50\text{pF}$  load capacitance (Figure 7). For minimum propagation delay, minimize the capacitive load at  $\overline{\text{CE}}$  OUT and use a low-output-impedance driver.

### Chip-Enable Output (MAX818)

When the CE transmission gate is enabled, the impedance of  $\overline{\text{CE}}$  OUT is equivalent to a  $40\Omega$  resistor in series with the source driving  $\overline{\text{CE}}$  IN. In the disabled mode, the transmission gate is off and an active pull-up connects  $\overline{\text{CE}}$  OUT to OUT (Figure 5). This pull-up turns off when the transmission gate is enabled.

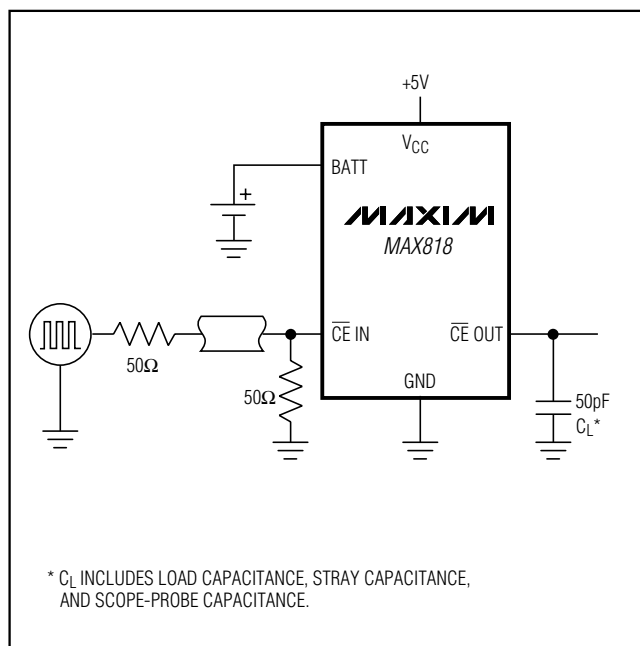


Figure 7. CE Propagation Delay Test Circuit

### Power-Fail Comparator (MAX817/MAX819)

The MAX817/MAX819 PFI input is compared to an internal reference. If PFI is less than the power-fail threshold ( $V_{\text{PFT}}$ ),  $\overline{\text{PFO}}$  goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply (Figure 8). However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

The power-fail comparator turns off and  $\overline{\text{PFO}}$  goes low when  $V_{\text{CC}}$  falls below  $V_{\text{BATT}}$ . During the reset timeout period ( $t_{\text{RP}}$ ),  $\overline{\text{PFO}}$  is forced high, regardless of the state of  $V_{\text{PFI}}$  (see *Battery Freshness Seal* section). If the comparator is unused, connect PFI to ground and leave  $\overline{\text{PFO}}$  unconnected.  $\overline{\text{PFO}}$  can be connected to  $\overline{\text{MR}}$  on the MAX819 so that a low voltage on PFI will generate a reset (Figure 9). In this configuration, when the monitored voltage causes PFI to fall below  $V_{\text{PFT}}$ ,  $\overline{\text{PFO}}$  pulls  $\overline{\text{MR}}$  low, causing a reset to be asserted. Reset remains asserted as long as  $\overline{\text{PFO}}$  holds  $\overline{\text{MR}}$  low, and for  $t_{\text{RP}}$  (200ms) after  $\overline{\text{PFO}}$  pulls  $\overline{\text{MR}}$  high when the monitored supply is above the programmed threshold. When PFO is connected to  $\overline{\text{MR}}$ , it is not possible to enable the battery freshness seal. Enabling the battery freshness seal requires  $\overline{\text{MR}}$  to be high or open. Once the battery freshness seal is enabled, it is no longer affected by  $\overline{\text{PFO}}$ 's connection to  $\overline{\text{MR}}$ .

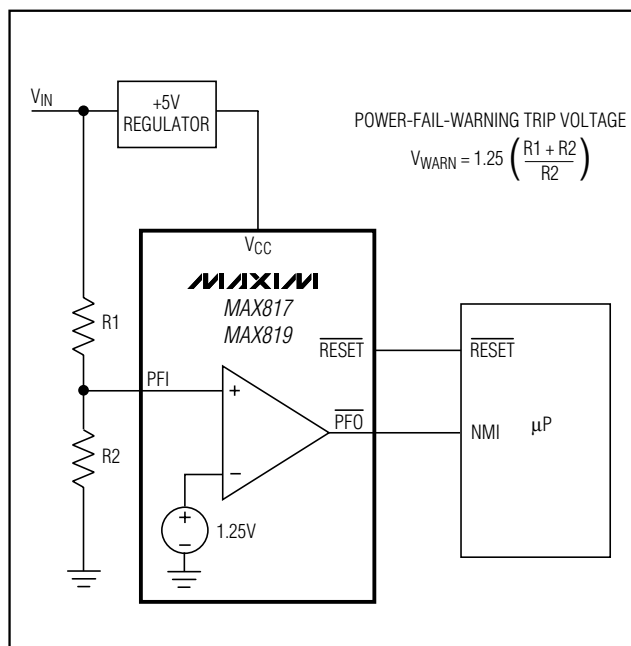


Figure 8. Using the Power-Fail Comparator to Generate a Power-Fail Warning

# +5V Microprocessor Supervisory Circuits

## Backup-Battery Switchover

In a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at BATT, the MAX817/MAX818/MAX819 automatically switch RAM to backup power when VCC falls. These devices require two conditions before switching to battery-backup mode: 1) VCC must be below the reset threshold, and 2) VCC must be below VBATT. Table 1 lists the status of the inputs and outputs in battery-backup mode.

As long as VCC exceeds the reset threshold, OUT connects to VCC through a 5Ω PMOS power switch. Once VCC falls below the reset threshold, VCC or VBATT (whichever is higher) switches to OUT. When VCC falls below V<sub>RST</sub> and VBATT, BATT switches to OUT through an 80Ω switch.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
VCC	Disconnected from V <sub>OUT</sub> .
V <sub>OUT</sub>	Connected to VBATT through an internal 80Ω PMOS switch.
VBATT	Connected to V <sub>OUT</sub> . Current drawn from the battery is less than 1μA, as long as VCC < VBATT - 0.2V.
V <sub>RESET</sub>	Logic low
V <sub>WDI</sub>	Watchdog timer is disabled.
V <sub>CEOUT</sub>	Logic high. The open-circuit voltage is equal to V <sub>OUT</sub> .
V <sub>CEIN</sub>	High impedance

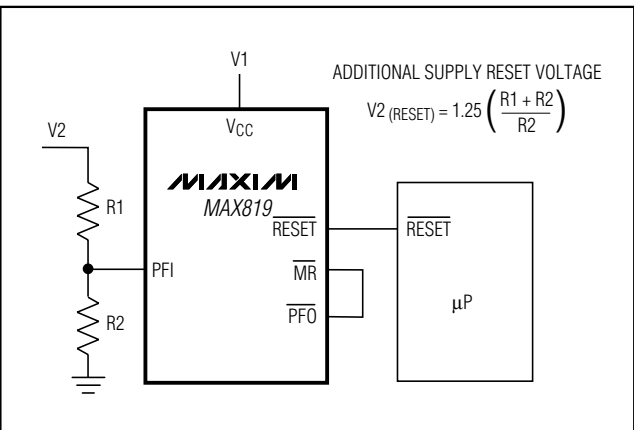


Figure 9. Monitoring an Additional Supply by Connecting PFO to MR.

When VCC exceeds the reset threshold, it is connected to the substrate, regardless of the voltage applied to BATT (Figure 10). During this time, the diode (D1) between BATT and the substrate will conduct current from BATT to VCC if VBATT is 0.6V greater than VCC. When BATT connects to OUT, backup mode is activated and the internal circuitry is powered from the battery (Table 1). When VCC is just below VBATT, the current draw from BATT is typically 6μA. When VCC drops to more than 1V below VBATT, the internal switchover comparator shuts off and the supply current falls to less than 1μA.

## Applications Information

The MAX817/MAX818/MAX819 are protected for typical short-circuit conditions of 10sec or less. Shorting OUT to ground for longer than 10sec destroys the device. Decouple VCC, OUT, and BATT to ground by placing 0.1μF capacitors as close to the device as possible.

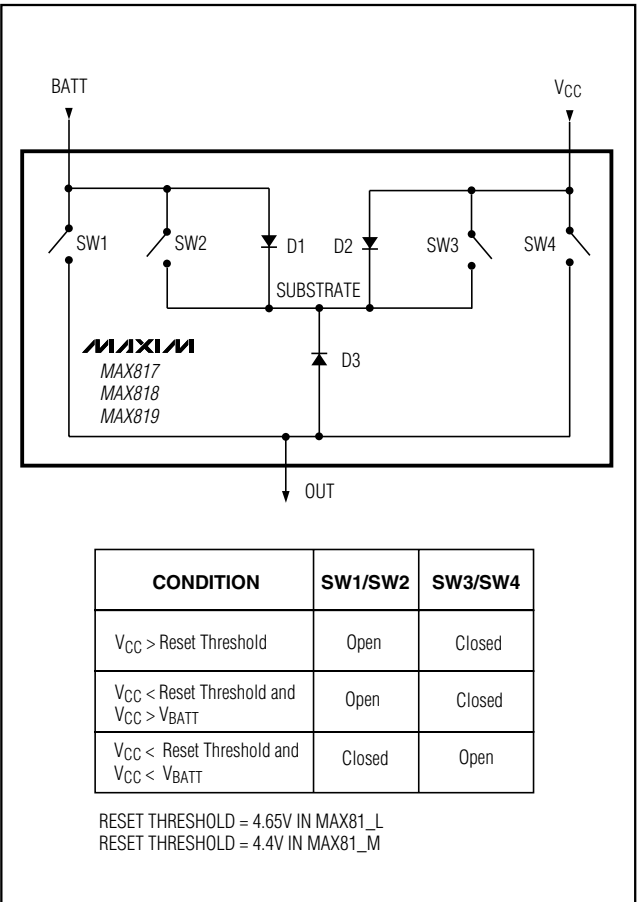


Figure 10. Backup-Battery-Switchover Block Diagram

## +5V Microprocessor Supervisory Circuits

### Watchdog Input Current

The MAX817/MAX818 WDI inputs are internally driven through a buffer and series resistor from the watchdog counter (Figure 1). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within  $\frac{7}{8}$  of the watchdog timeout period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the timeout period, up to 150 $\mu$ A can flow into WDI.

### Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values (on the order of 0.47F) for their size. Since BATT has the same operating voltage range as VCC, and the battery switchover threshold voltages are typically  $\pm 30$ mV centered at VBATT, a SuperCap and simple charging circuit can be used as a backup power source. Figure 11 shows a SuperCap used as a backup source.

If VCC is above the reset threshold and VBATT is 0.5V above VCC, current flows to OUT and VCC from BATT until the voltage at BATT is less than 0.5V above VCC. For example, if a SuperCap is connected to BATT through a diode to VCC, and VCC quickly changes from 5.4V to 4.9V, the capacitor discharges through OUT and VCC until VBATT reaches 5.1V typical. Leakage current through the SuperCap charging diode and the internal power diode eventually discharges the SuperCap to VCC. Also, if VCC and VBATT start from 0.1V above the reset threshold and power is lost at

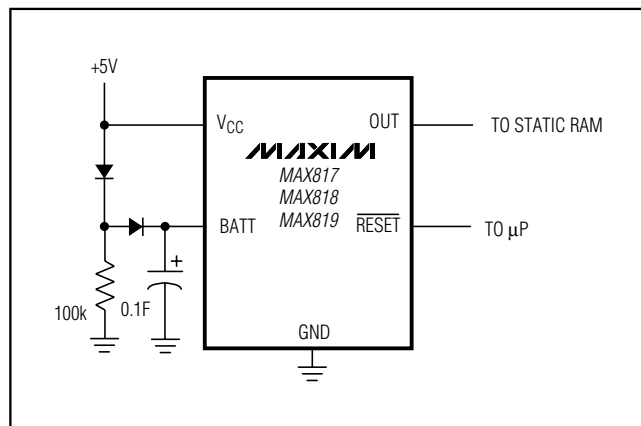


Figure 11. Using a SuperCap™ as a Backup Power Source with a +5V  $\pm 10\%$  Supply

SuperCap is a trademark of Baknor Industries.

VCC, the SuperCap on BATT discharges through VCC until VBATT reaches the reset threshold. Battery-backup mode is then initiated and the current through VCC goes to zero.

### Operation Without a Backup Power Source

The MAX817/MAX818/MAX819 were designed for battery-backed applications. If a backup battery is not used, connect VCC to OUT, and connect BATT to ground.

### Replacing the Backup Battery

The backup power source can be removed while VCC remains valid, without danger of triggering a reset pulse, if BATT is decoupled with a 0.1 $\mu$ F capacitor to ground. As long as VCC stays above the reset threshold, battery-backup mode cannot be entered.

### Adding Hysteresis to the Power-Fail Comparator (MAX817/MAX819)

The power-fail comparator has a typical input hysteresis of 4mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see *Monitoring an Additional Supply*).

For additional noise margin, connect a resistor between PFO and PFI, as shown in Figure 12. Select the ratio of R1 and R2 such that PFI sees VPFT when VIN falls to the

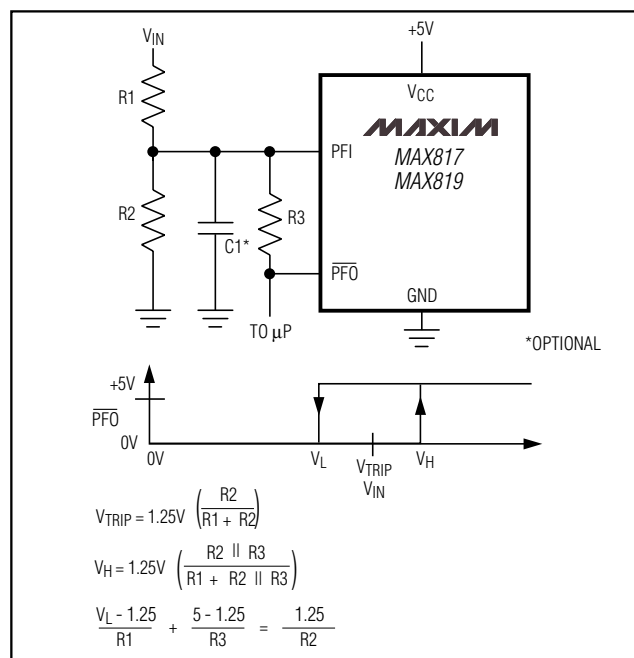


Figure 12. Adding Hysteresis to the Power-Fail Comparator

## +5V Microprocessor Supervisory Circuits

desired trip point ( $V_{TRIP}$ ). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1 $\mu$ A to ensure that the 25nA (max) PFI input leakage current does not shift the trip point. R3 should be larger than 200k $\Omega$  to prevent it from loading down the  $\overline{PFO}$  pin. Capacitor C1 adds additional noise rejection.

### Monitoring an Additional Supply (MAX817/MAX819)

The MAX817/MAX819  $\mu$ P supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI.  $\overline{PFO}$  can be used to generate an interrupt to the  $\mu$ P or to trigger a reset (Figures 9 and 13).

### Interfacing to $\mu$ Ps with Bidirectional Reset Pins

$\mu$ Ps with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX817/MAX818/MAX819  $\overline{RESET}$  output. If, for example, the  $\overline{RESET}$  output is driven high and the  $\mu$ P wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7k $\Omega$  resistor between the  $\overline{RESET}$  output and the  $\mu$ P reset I/O, as in Figure 14. Buffer the  $\overline{RESET}$  output to other system components.

### Negative-Going $V_{CC}$ Transients

These supervisors are relatively immune to short-duration, negative-going  $V_{CC}$  transients (glitches) while issuing a reset to the  $\mu$ P during power-up, power-down, and brownout conditions. Therefore, resetting the  $\mu$ P when  $V_{CC}$  experiences only small glitches is usually not desirable.

The *Typical Operating Characteristics* show a graph of Maximum Transient Duration vs. Reset Threshold Overdrive for which reset pulses are **not** generated. The graph was produced using negative-going  $V_{CC}$  pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going  $V_{CC}$  transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a  $V_{CC}$  transient that goes 100mV below the reset threshold and lasts for 135 $\mu$ s will not trigger a reset pulse.

A 0.1 $\mu$ F bypass capacitor mounted close to the  $V_{CC}$  pin provides additional transient immunity.

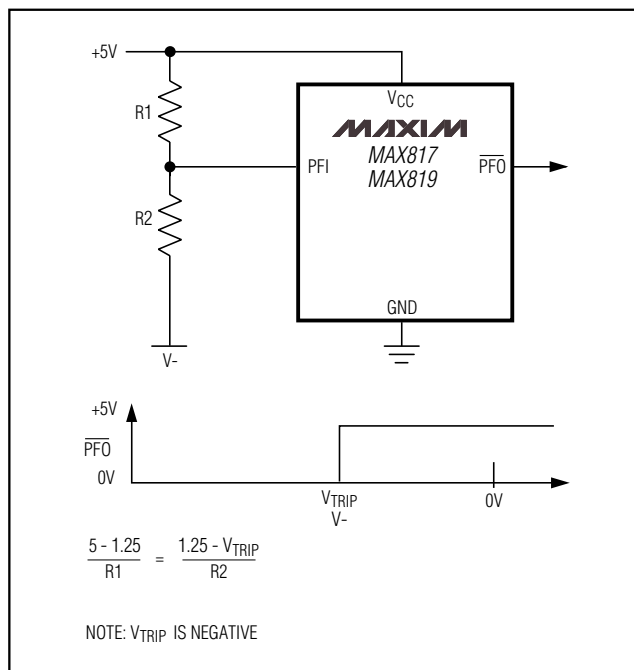


Figure 13. Monitoring a Negative Voltage

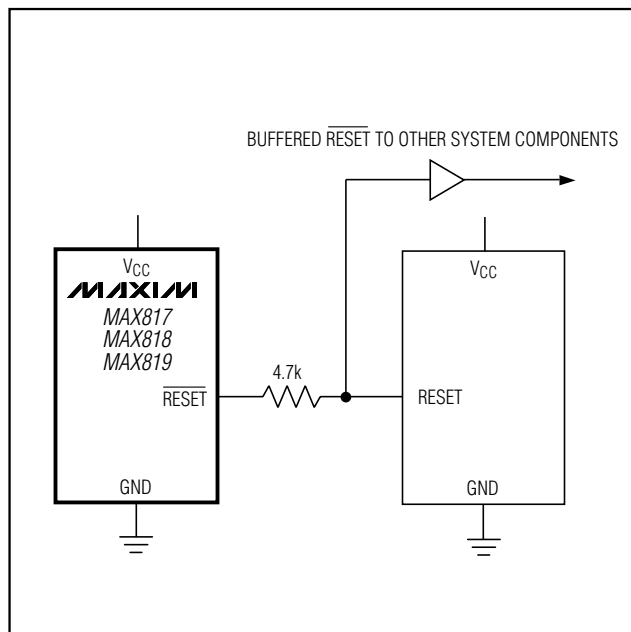


Figure 14. Interfacing to  $\mu$ Ps with Bidirectional Reset I/O

# +5V Microprocessor Supervisory Circuits

## Watchdog Software Considerations (MAX817/MAX818)

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than “pulsing” the watchdog input high-low-high or low-high-low. This technique avoids a “stuck” loop, in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out. Figure 15 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should “hang” in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, triggering a reset or an interrupt. As described in the *Watchdog Input Current* section, this scheme results in higher average WDI input current than does the method of leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

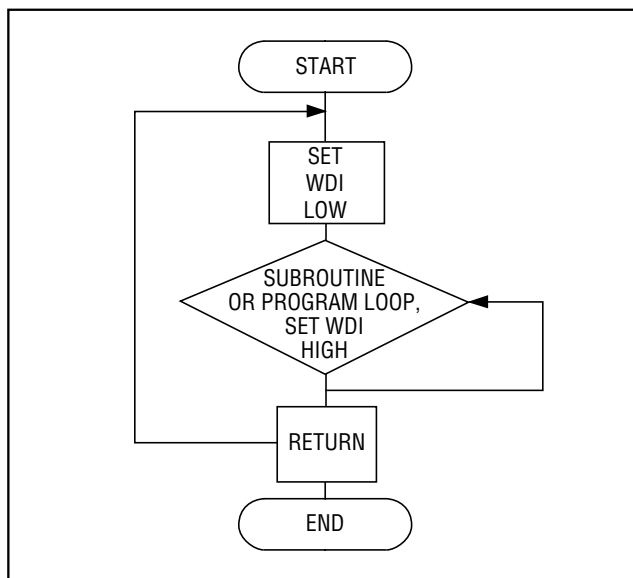
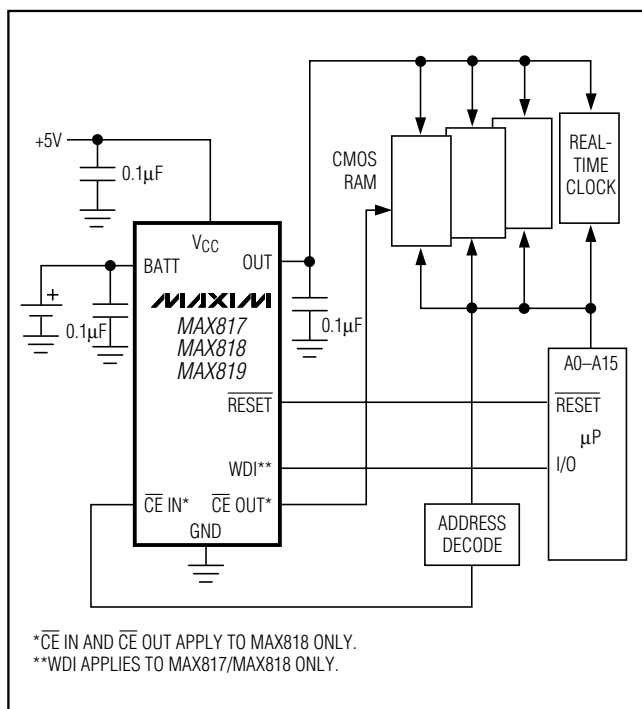
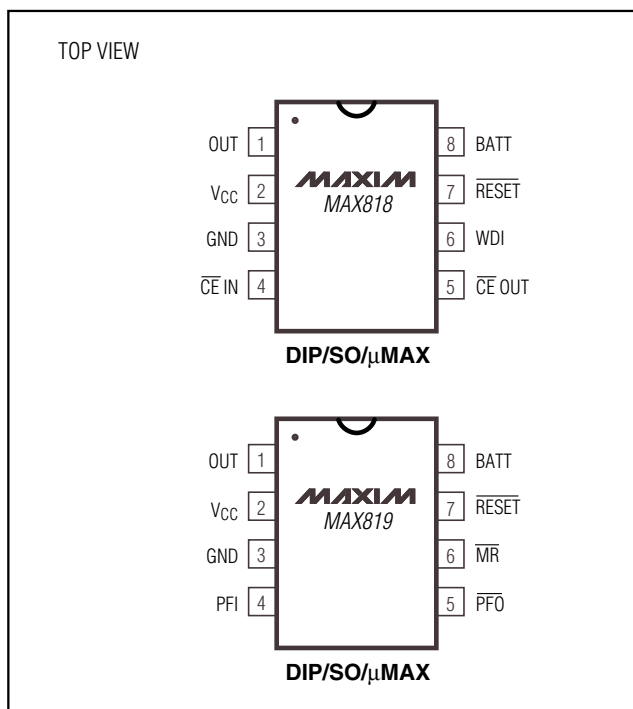


Figure 15. Watchdog Flow Diagram

## Typical Operating Circuit



## Pin Configurations (continued)



# +5V Microprocessor Supervisory Circuits

## Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE
MAX817_EPA	-40°C to +85°C	8 Plastic DIP
MAX817_ESA	-40°C to +85°C	8 SO
<b>MAX818_CPA</b>	0°C to +70°C	8 Plastic DIP
MAX818_CSA	0°C to +70°C	8 SO
MAX818_CUA	0°C to +70°C	8 $\mu$ MAX
MAX818_EPA	-40°C to +85°C	8 Plastic DIP
MAX818_ESA	-40°C to +85°C	8 SO
<b>MAX819_CPA</b>	0°C to +70°C	8 Plastic DIP
MAX819_CSA	0°C to +70°C	8 SO
MAX819_CUA	0°C to +70°C	8 $\mu$ MAX
MAX819_EPA	-40°C to +85°C	8 Plastic DIP
MAX819_ESA	-40°C to +85°C	8 SO

†These parts offer a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.

Devices are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering.

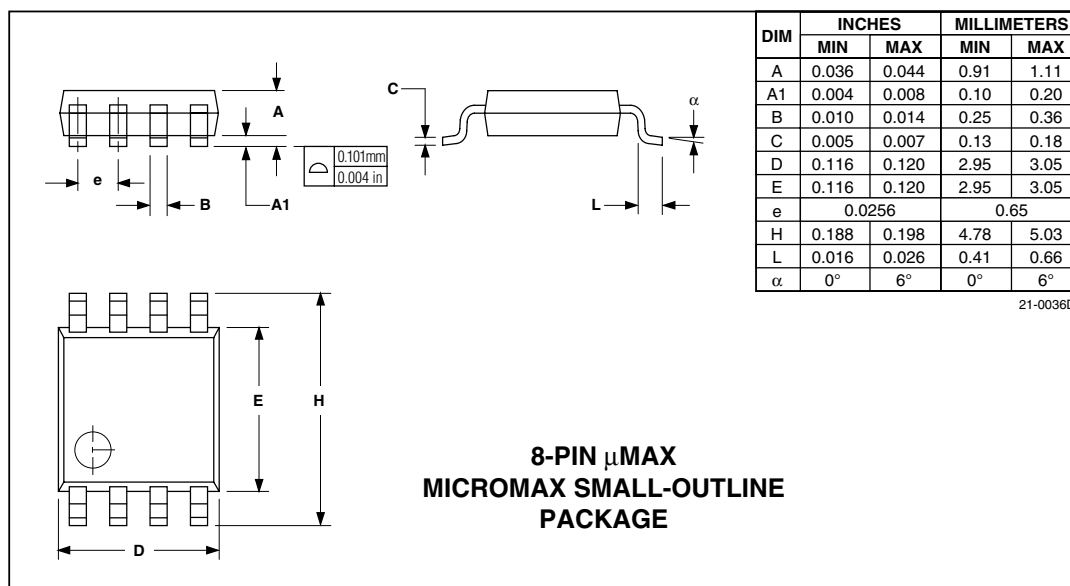
SUFFIX	RESET THRESHOLD (V)
L	4.65
M	4.40

## Chip Information

TRANSISTOR COUNT: 719

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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