

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V+	-0.3V to +4V
COL2/PORT2–COL7/PORT7	-0.3V to +4V
SDA, SCL, AD0, ALERT, INT	-0.3V to +6V
All Other Pins	-0.3V to (V+ + 0.3V)
DC Current on COL2/PORT2–COL7/PORT7	25mA
DC Current on SOUNDER	±25mA
GND Current	80mA

Continuous Power Dissipation (T_A = +70°C)

16-Pin QSOP (derate 8.3mW/°C above +70°C)	666mW
16-Pin TQFN (derate 16.9mW/°C above +70°C)	1349.1mW
20-Pin QSOP (derate 9.1mW/°C above +70°C)	727mW
24-Pin QSOP (derate 9.5mW/°C above +70°C)	761mW
24-Pin TQFN (derate 20.8mW/°C above +70°C)	1666.7mW
Operating Temperature Range (T _{MIN} to T _{MAX})	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 2.4V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		2.4		3.6	V
Operating Supply Current	I+	All key switches open		75	100	μA
Shutdown Supply Current	I _{SH}			6.44	10	μA
SOUNDER Output High Voltage	VOHBUZ	I _{SOURCE} = 10mA	V+ - 0.45			V
SOUNDER Output Low Voltage	VOLBUZ	I _{SINK} = 10mA			0.15	V
SOUNDER Frequency Accuracy		T _A = +25°C, V+ = 3.3V		1.2		%
Key-Switch Source Current	I _{KEY}			28	40	μA
Key-Switch Source Voltage	V _{KEY}			0.35	0.65	V
Key-Switch Resistance	R _{KEY}	(Note 3)			1	kΩ
Startup Time from Shutdown	t _{START}			57	200	μs
Output Low Voltage COL2/PORT2 to COL7/PORT7, INT Output	VOLPORT	I _{SINK} = 10mA			0.15	V
Input Leakage Current Alert		Input voltage ≤ V+	-1		+1	μA
		Input voltage > V+	-5		+5	
Input High Voltage ALERT	V _{IH}		2.2			V
Input Low Voltage ALERT	V _{IL}				0.8	V
SERIAL-INTERFACE SPECIFICATIONS						
Serial Bus Timeout	t _{OUT}	With bus timeout enabled	20		68	ms
Input High Voltage SDA, SCL, AD0	V _{IH}		2.2			V
Input Low Voltage SDA, SCL, AD0	V _{IL}				0.6	V
Input Leakage Current SDA, SCL, AD0		Input voltage ≤ V+	-1		+1	μA
		Input voltage > V+	-5		+5	

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

MAX7347/MAX7348/MAX7349

I²C TIMING CHARACTERISTICS

(V₊ = 2.4V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V₊ = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance (SCL, SDA, AD0)	C _{IN}	(Notes 3, 4)			10	pF
SCL Serial Clock Frequency	f _{SCL}	With bus timeout enabled	0.05		400	kHz
		With bus timeout disabled	0		400	
Bus Free Time Between a STOP and a START Condition	t _{BUF}		1.3			μs
Hold Time (Repeated) START Condition	t _{HD, STA}		0.6			μs
Repeated START Condition Setup Time	t _{SU, STA}		0.6			μs
STOP Condition Setup Time	t _{SU, STO}		0.6			μs
Data Hold Time	t _{HD, DAT}	(Note 5)			0.9	μs
Data Setup Time	t _{SU, DAT}		100			ns
SCL Clock Low Period	t _{LOW}		1.3			μs
SCL Clock High Period	t _{HIGH}		0.7			μs
Rise Time of Both SDA and SCL Signals, Receiving	t _R	(Notes 3, 4)		20 + 0.1C _b	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t _F	(Notes 3, 4)		20 + 0.1C _b	300	ns
Fall Time of SDA Transmitting	t _{F, TX}	(Notes 3, 6)		20 + 0.1C _b	250	ns
Pulse Width of Spike Suppressed	t _{SP}	(Notes 3, 7)			50	ns
Capacitive Load for Each Bus Line	C _b	(Note 3)			400	pF

Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: All digital inputs at V₊ or GND.

Note 3: Guaranteed by design.

Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.

Note 5: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

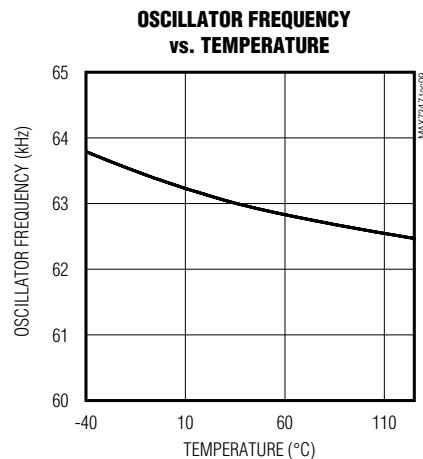
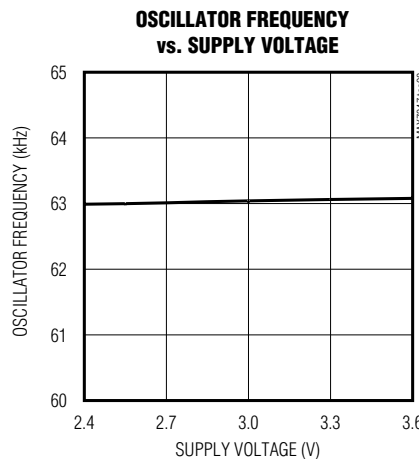
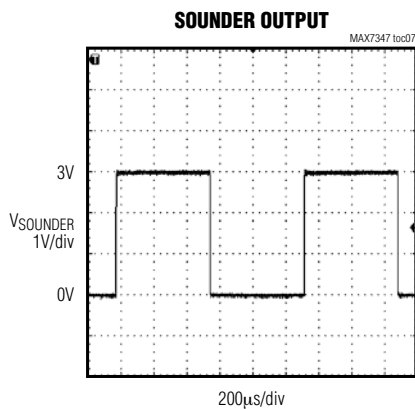
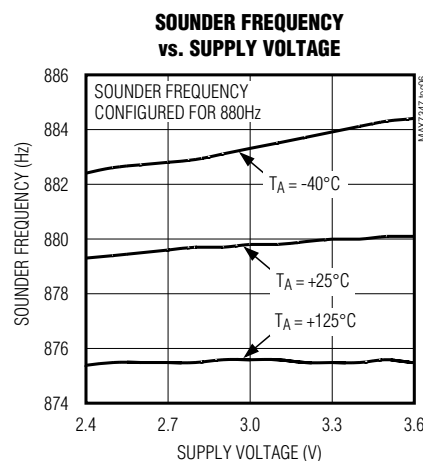
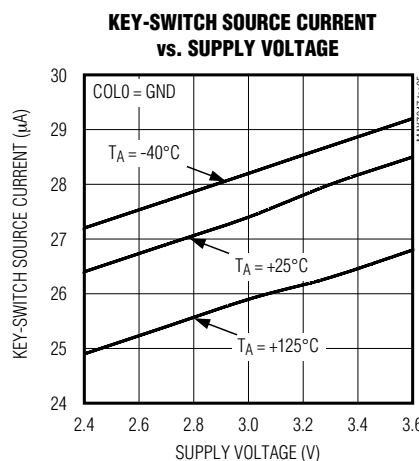
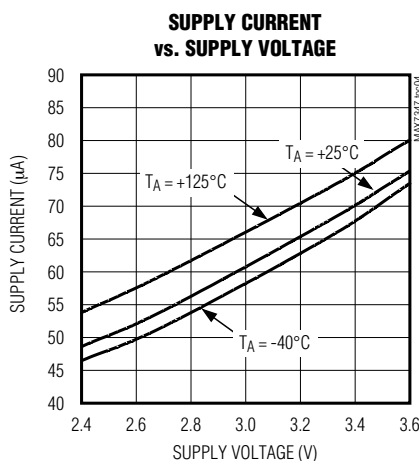
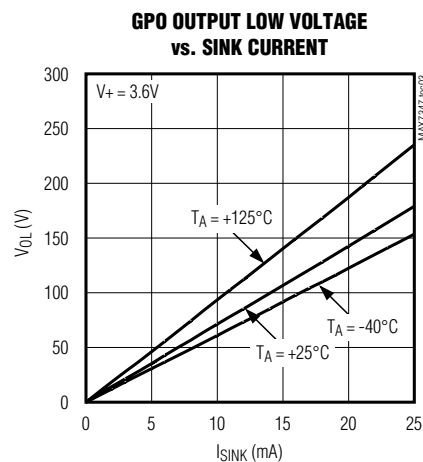
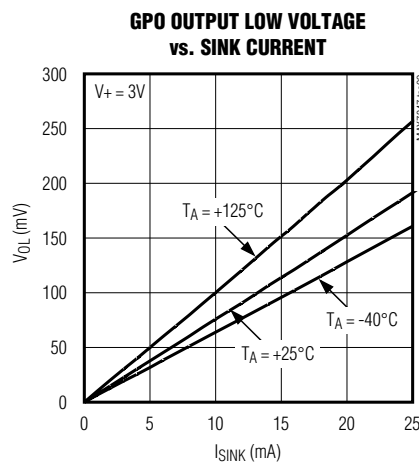
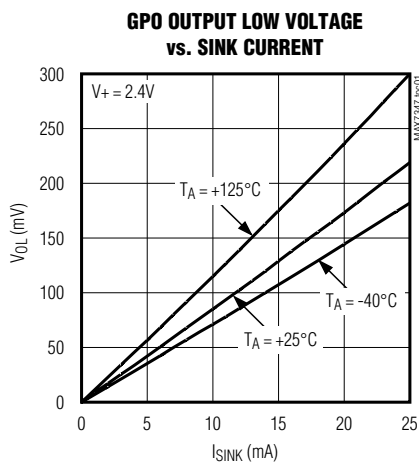
Note 6: I_{SINK} ≤ 6mA. C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.

Note 7: Input filters on the SDA, SCL, and AD0 inputs suppress noise spikes less than 50ns.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Typical Operating Characteristics

($V_+ = 3.3\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. Supply range for V_+ is 2.4V to 3.6V. Temperature range is -40°C to $+125^\circ\text{C}$.)



2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Pin Description

PIN					NAME	FUNCTION
MAX7347 (QSOP)	MAX7347 (TQFN)	MAX7348	MAX7349 (QSOP)	MAX7349 (TQFN)		
1	15	1	2	23	ROW0	Row Input from Key Matrix. Leave open circuit if unused.
2	16	2	3	24	ROW1	Row Input from Key Matrix. Leave open circuit if unused.
3	1	3	4	1	ROW2	Row Input from Key Matrix. Leave open circuit if unused.
4	2	4	5	2	ROW3	Row Input from Key Matrix. Leave open circuit if unused.
5	3	7	8	5	ROW4	Row Input from Key Matrix. Leave open circuit if unused.
6	4	8	9	6	ROW5	Row Input from Key Matrix. Leave open circuit if unused.
7	5	9	10	7	ROW6	Row Input from Key Matrix. Leave open circuit if unused.
8	6	10	11	8	ROW7	Row Input from Key Matrix. Leave open circuit if unused.
9	7	11	14	11	COL2/PORT2	Column Output to Key Matrix or GPO
10	8	12	15	12	COL1	Column Output to Key Matrix
11	9	13	16	13	COL0	Column Output to Key Matrix
12	10	15	18	15	GND	Ground
13	11	17	20	17	SDA	I ² C-Compatible Serial Data I/O
14	12	18	21	18	SCL	I ² C-Compatible Serial Clock Input
15	13	19	22	19	INT	Active-Low Interrupt Output. Output is open drain.
16	14	20	23	20	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.047μF or higher ceramic capacitor.
—	—	5	6	3	COL3/PORT3	Column Output to Key Matrix or GPO
—	—	6	7	4	COL4/PORT4	Column Output to Key Matrix or GPO
—	—	14	17	14	SOUNDER	Sounder Driver Output. Typically connect a piezo-ceramic sounder or other transducer from this output to ground. Output is push-pull.
—	—	16	19	16	AD0	Address Input 0. Sets device slave address. Connect to GND, V+, SDA, or SCL to give four logic combinations. See Table 3.
—	—	—	1	22	COL7/PORT7	Column Output to Key Matrix or GPO
—	—	—	12	9	COL6/PORT6	Column Output to Key Matrix or GPO
—	—	—	13	10	COL5/PORT5	Column Output to Key Matrix or GPO
—	—	—	24	21	ALERT	Alert Input. Connect to GND or V+ if unused.
—	EP	—	—	EP	EP	Exposed Paddle. Internally connected to GND. Connect to a large ground plane to maximize thermal performance.

Detailed Description

The MAX7347/MAX7348/MAX7349 are microprocessor peripherals that combine a low-noise key-switch interface with a piezo sounder controller. Up to 64 key switches can be monitored and debounced with optional autorepeat, and the key events are presented in an eight-deep FIFO. Key-switch functionality can be traded to provide up to one (MAX7347), three (MAX7348), or six (MAX7349) open-drain logic outputs. (Table 1).

The piezo sounder controller generates a variety of audio tones. Tones are programmable for frequency and duration, and may be intermittent, two tone, or continuous. The piezo sounder controller can be configured to deliver an automatic, customizable sound on every key press to provide a audible key-click feedback.

Interrupt requests can be configured to be issued on every key-press event, or can be limited to a maximum rate to prevent overloading the microprocessor with

MAX7347/MAX7348/MAX7349

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 1. Product Features Table

PART	PACKAGE-PINS	MAXIMUM KEY SWITCHES	INT OUTPUT	KEY-SCAN SLAVE IDs	SOUNDER SLAVE IDs	SOUNDER OUTPUT	GPOs	ALERT INPUT
MAX7349	24	64	Yes	4	4	Yes	6 + 1 ($\overline{\text{INT}}$)	Yes
MAX7348	20	40	Yes	4	4	Yes	3 + 1 ($\overline{\text{INT}}$)	—
MAX7347	16	24	Yes	1 fixed	—	—	1 + 1 ($\overline{\text{INT}}$)	—

too many interrupts. The key-switch status can be checked at any time by reading the key-switch FIFO. A 1-byte read access returns both the first key-press event in the FIFO (if there is one) and the FIFO status, so it is easy to operate the MAX7347/MAX7348/MAX7349 by polling. If the $\overline{\text{INT}}$ pin is not required, it can be configured as an open-drain general-purpose output (GPO) capable of driving an LED.

The MAX7349 monitors up to 64 keys. The MAX7348 monitors up to 40 keys. The MAX7347 monitors up to 24 keys (Table 1).

If the application requires fewer keys to be scanned, up to six of the key-switch outputs can be configured as open-drain GPOs capable of driving LEDs. For each key-switch output used as a GPO, the number of key switches that can be scanned is reduced by eight.

An alert logic input (MAX7349 only) can be configured to deliver an automatic, customizable sound and/or an interrupt on every falling edge of the logic input. The logic state of the alert input can be read at any time.

Tone Generator

The piezo sounder controller generates a square wave with the frequency of a musical tone under processor control. The selection of tones covers the 5th musical octave (523.25Hz to 987.77Hz), plus seven other notes up to 2637Hz. The sounder output is also programmable to be either high or low for the entire sound duration to operate an electronic sounder, relay, or lamp instead of a piezo transducer. The sound duration is programmable from 15.625ms in seven binary steps up to a maximum of 1s.

The piezo sounder controller interface uses a single 1-byte access to its own separate slave address. Commands are double-buffered to allow two commands (2 bytes) to be stored and executed in succession. The sounder controller performs the transition between queued sound commands without click artifacts. The controller can also autoloop between the two most recent commands. Autolooping allows a wide range of intermittent and two-tone sounds to be initiated, and then run automatically without further intervention.

Key-Scan Controller

Key inputs are scanned statically, not dynamically, to ensure low-EMI operation. As inputs only toggle in response to switch changes, the key matrix can be routed closer to sensitive circuit nodes.

The key controller debounces and maintains a FIFO of key-press events (including autorepeated key presses, if autorepeat is enabled). Figure 1 shows keys order.

Serial Interface

Figure 2 shows the 2-wire serial interface timing details.

Serial Addressing

The MAX7347/MAX7348/MAX7349 operate as slaves that send and receive data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX7347/MAX7348/MAX7349 and generates the SCL clock that synchronizes the data transfer.

The MAX7347/MAX7348/MAX7349s' SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7k Ω , is required on SDA. The MAX7347/MAX7348/MAX7349s' SCL line operates only as an input. A pullup resistor, typically 4.7k Ω , is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 3) sent by a master, followed by the MAX7347/MAX7348/MAX7349 7-bit slave address plus R/W bit, a register address byte, 1 or more data bytes, and finally a STOP condition.

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

MAX7347/MAX7348/MAX7349

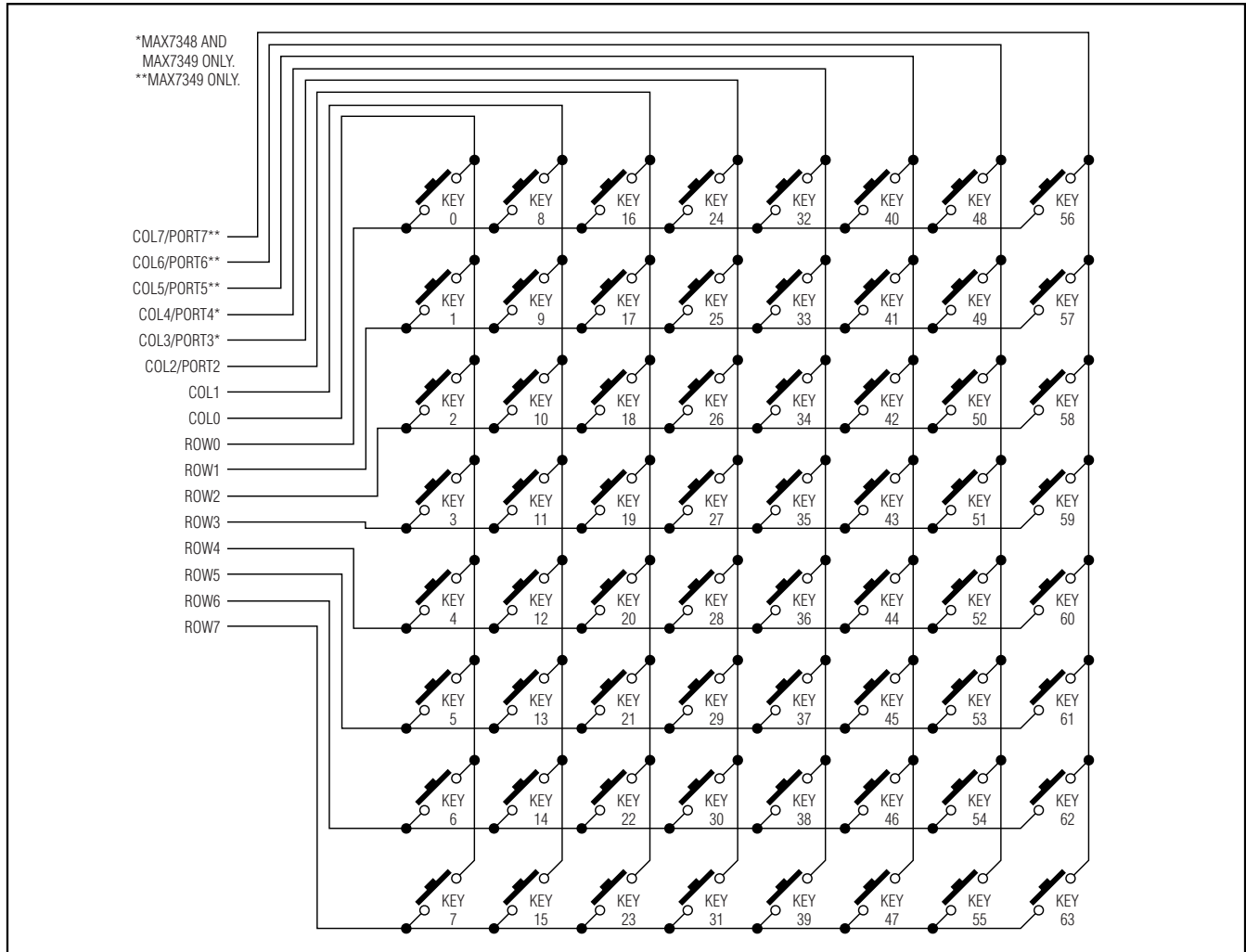


Figure 1. Keys Order

STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 4). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 5), which the recipient uses to handshake receipt of each

byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7347/MAX7348/MAX7349, the MAX7347/MAX7348/MAX7349 generate the acknowledge bit because the MAX7347/MAX7348/MAX7349 are the recipients. When the MAX7347/MAX7348/MAX7349 are transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

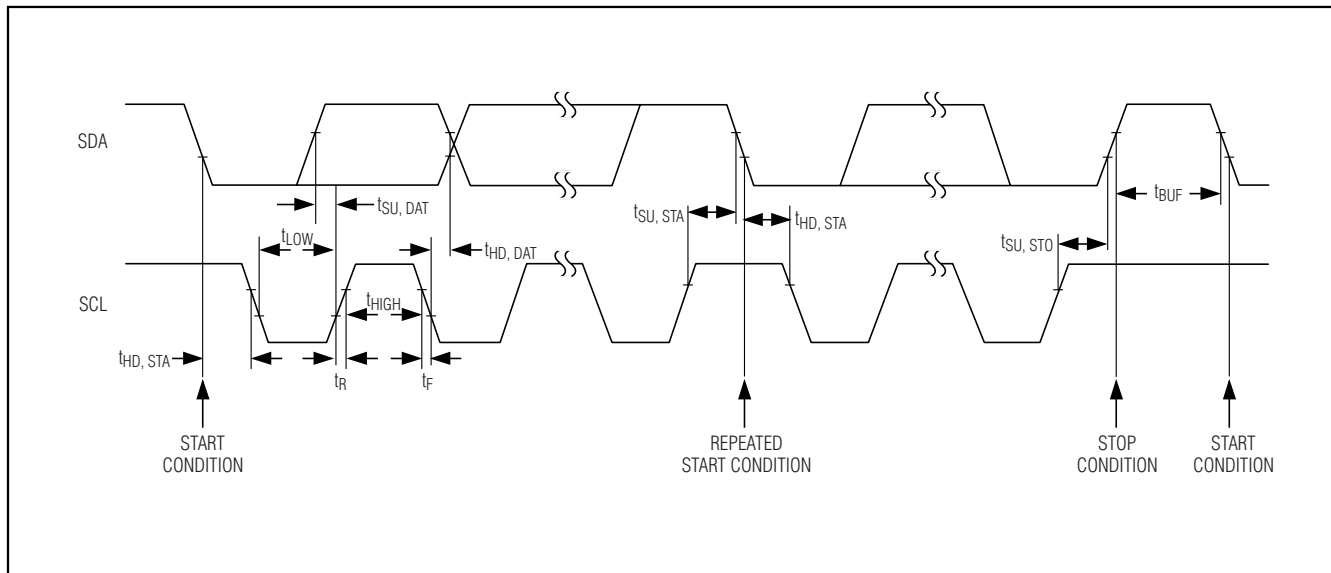


Figure 2. 2-Wire Serial Interface Timing Details

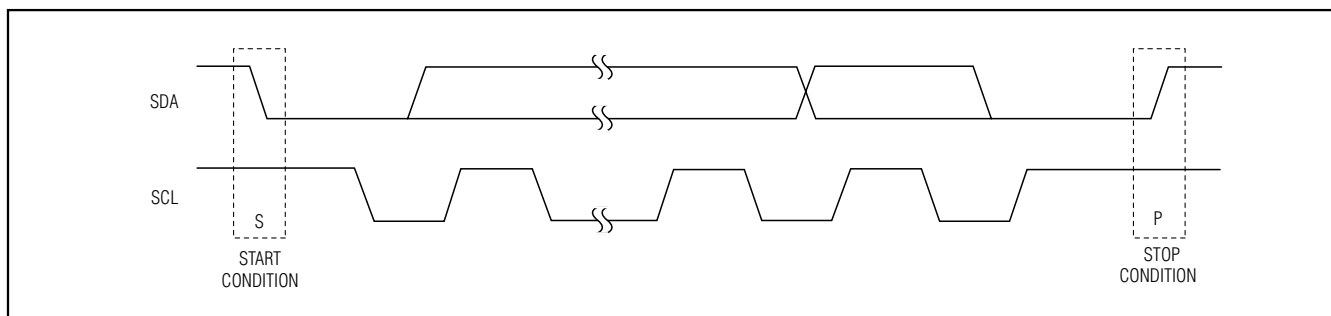


Figure 3. Start and Stop Conditions

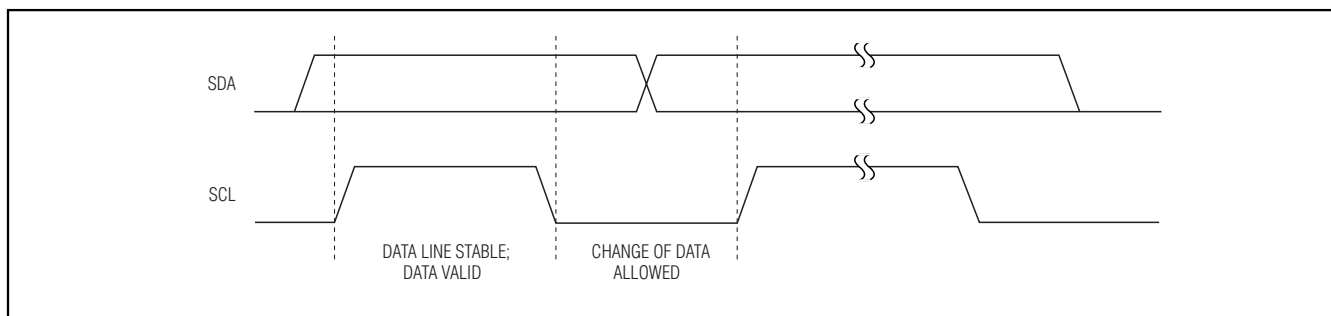


Figure 4. Bit Transfer

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 2. Key-Switch Mapping

PIN	COL0	COL1	COL2/PORT2	COL3/PORT3	COL4/PORT4	COL5/PORT5	COL6/PORT6	COL7/PORT7
ROW0	KEY 0	KEY 8	KEY 16	KEY 24	KEY 32	KEY 40	KEY 48	KEY 56
ROW1	KEY 1	KEY 9	KEY 17	KEY 25	KEY 33	KEY 41	KEY 49	KEY 57
ROW2	KEY 2	KEY 10	KEY 18	KEY 26	KEY 34	KEY 42	KEY 50	KEY 58
ROW3	KEY 3	KEY 11	KEY 19	KEY 27	KEY 35	KEY 43	KEY 51	KEY 59
ROW4	KEY 4	KEY 12	KEY 20	KEY 28	KEY 36	KEY 44	KEY 52	KEY 60
ROW5	KEY 5	KEY 13	KEY 21	KEY 29	KEY 37	KEY 45	KEY 53	KEY 61
ROW6	KEY 6	KEY 14	KEY 22	KEY 30	KEY 38	KEY 46	KEY 54	KEY 62
ROW7	KEY 7	KEY 15	KEY 23	KEY 31	KEY 39	KEY 47	KEY 55	KEY 63

Table 3. 2-Wire Interface Address Map

PIN AD0	DEVICE ADDRESS								FUNCTION
	A7	A6	A5	A4	A3	A2	A1	A0 R/W	
GND	0	1	1	1	0	0	0	0	Key-scan controller write
								1	Key-scan controller read
							1	0	Sounder controller write
								1	Sounder controller read
V+	0	1	1	1	0	1	0	0	Key-scan controller write
								1	Key-scan controller read
							1	0	Sounder controller write
								1	Sounder controller read
SDA	0	1	1	1	1	0	0	0	Key-scan controller write
								1	Key-scan controller read
							1	0	Sounder controller write
								1	Sounder controller read
SCL	0	1	1	1	1	1	0	0	Key-scan controller write
								1	Key-scan controller read
							1	0	Sounder controller write
								1	Sounder controller read

Slave Addresses

The MAX7347/MAX7348/MAX7349 have two 7-bit long slave addresses (Figure 6). The bit following a 7-bit slave address is the R/W bit, which is low for a write command and high for a read command.

The first 4 bits (MSBs) of the MAX7347/MAX7348/MAX7349 slave addresses are always 0111. Slave address bits A3, A2, and A1 correspond, by the matrix in Table 3, to the states of the device address input AD0, and A0 corresponds to the R/W bit. MAX7347/MAX7348/MAX7349 use two slave addresses, one for the main key-scan controller, and one for the sounder

controller. The AD0 input can be connected to any of four signals: GND, V+, SDA, or SCL, giving four possible slave address pairs, allowing up to four MAX7348/MAX7349 devices to share the bus. Only one MAX7347 can share the bus. The MAX7347 AD0 input is internally connected to GND.

The MAX7347/MAX7348/MAX7349 monitor the bus continuously, waiting for a START condition followed by its slave address. When MAX7347/MAX7348/MAX7349 recognize their slave address, they acknowledge and are then ready for continued communication.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

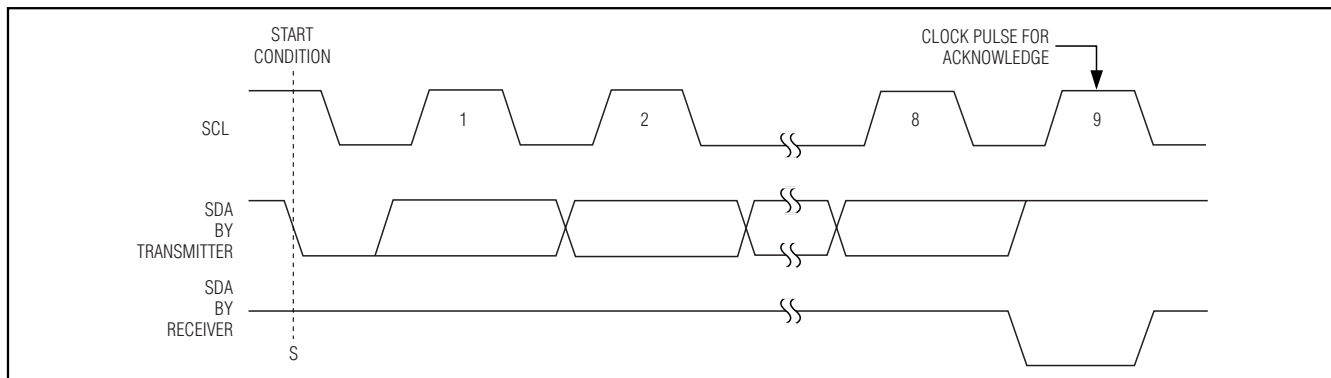


Figure 5. Acknowledge

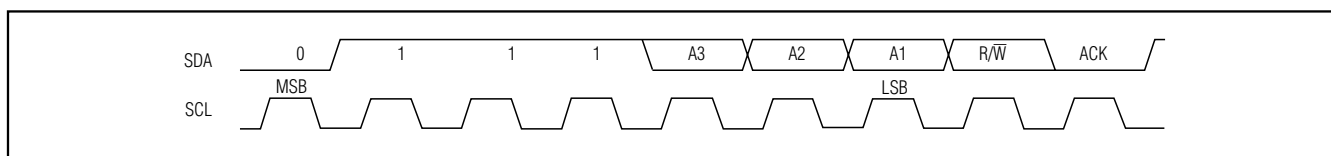


Figure 6. Slave Address

Bus Timeout

The MAX7347/MAX7348/MAX7349 feature a 20ms minimum bus timeout on the 2-wire serial interface, largely to prevent the MAX7347/MAX7348/MAX7349 from holding the SDA I/O low during a read transaction if the SCL hangs for any reason before a serial transaction has been completed. Bus timeout operates by causing the MAX7347/MAX7348/MAX7349 to internally terminate a serial transaction, either read or write, if the time between adjacent edges on SCL exceeds 20ms. After a bus timeout, the MAX7347/MAX7348/MAX7349 wait for a valid START condition before responding to a consecutive transmission. The bus timeout feature requires the serial interface to operate above 50Hz bus speed. This feature can be enabled or disabled under user control by writing to the configuration register (Table 12).

Message Format for Writing the Key-Scan Controller

A write to the MAX7347/MAX7348/MAX7349s' key-scan controller comprises the transmission of the MAX7347/MAX7348/MAX7349s' key-scan slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX7347/MAX7348/MAX7349 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, then the MAX7347/MAX7348/MAX7349 take no further action (Figure 7) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX7347/MAX7348/MAX7349 selected by the command byte (Figure 8).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX7347/MAX7348/MAX7349 internal registers (Table 7) because the command byte address generally autoincrements (Table 4).

Message Format for Reading the Key-Scan Controller

The MAX7347/MAX7348/MAX7349 are read using the MAX7347/MAX7348/MAX7349s' internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 4). Thus, a read is initiated by first configuring the MAX7347/MAX7348/MAX7349s' command byte by performing a write (Figure 7). The master can now read n consecutive bytes from the MAX7347/MAX7348/MAX7349, with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address is generally autoincremented after the write (Figure 9, Table 4).

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

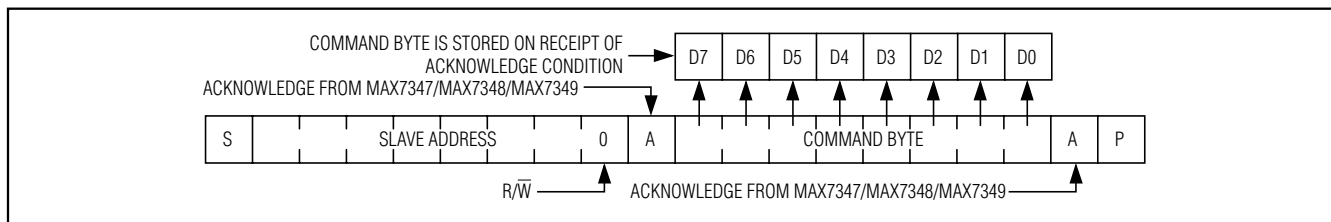


Figure 7. Command Byte Received

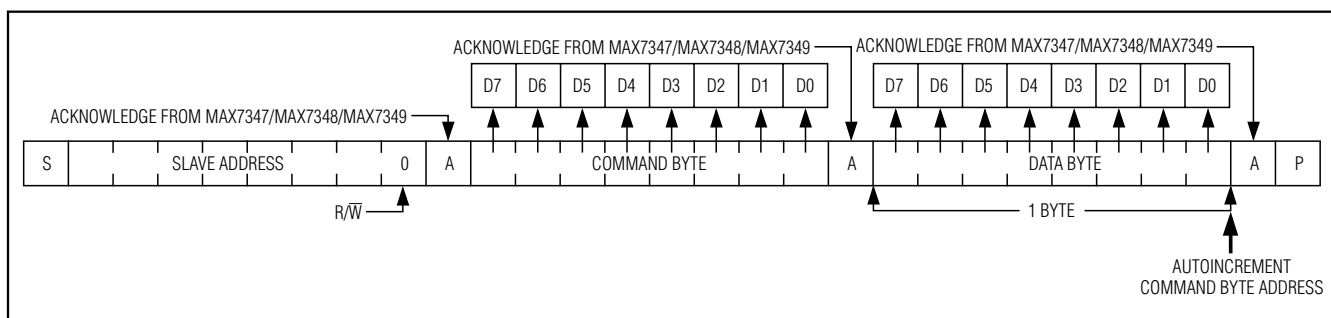


Figure 8. Command and Single Data Byte Received

Message Format for Writing the Sounder Controller

A write to the MAX7347/MAX7348/MAX7349s' sounder controller comprises the transmission of the MAX7347/MAX7348/MAX7349s' sounder slave address with the R/W bit set to zero, followed by at least 1 command byte of information. The sounder controller analyzes each incoming data byte, and depending on the state of the sounder controller's 2-deep FIFO and the contents of the command byte, the command byte is added to the FIFO or it overwrites the last FIFO data item (Table 16).

Message Format for Reading the Sounder Controller

A read from the MAX7347/MAX7348/MAX7349s' sounder controller comprises the transmission of the MAX7347/MAX7348/MAX7349s' sounder slave address with the R/W bit set to 1. The master can now read n consecutive bytes from the MAX7347/MAX7348/MAX7349, each byte being a snapshot of the FIFO status of the sounder controller (Table 16). If the master wishes to poll the sounder controller until there is room for another command to be sent, the master can read bytes continuously from the sounder controller until the information is satisfactory and then issue a STOP condition.

Table 4. Key-Scan Command Address Autoincrement Rules

REGISTER FUNCTION	ADDRESS CODE (hex)	AUTOINCREMENT ADDRESS (hex)
Keys FIFO	0x00	0x00
Debounce	0x01	0x02
Autorepeat	0x02	0x03
Interrupt	0x03	0x04
Configuration	0x04	0x05
Port	0x05	0x06
Key Sound	0x06	0x07
Alert Sound	0x07	0x00

Operation with Multiple Masters

If the MAX7347/MAX7348/MAX7349 are operated on a 2-wire interface with multiple masters, a master reading the MAX7347/MAX7348/MAX7349 should use a repeated start between the write that sets the MAX7347/MAX7348/MAX7349s' address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX7347/MAX7348/MAX7349s' address pointer but before master 1 has read the data. If master 2 subsequently resets the MAX7347/MAX7348/MAX7349s' address pointer, then master 1's read may be from an unexpected location.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 5. Key-Scan Power-Up Configuration

REGISTER FUNCTION	POWER-UP CONDITION	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Keys FIFO	Empty	0x00	0	0	0	0	0	0	0	0
Debounce	Ports 2–7 are enabled; debounce time is 39ms	0x01	1	1	1	1	1	1	1	1
Autorepeat	Autorepeat is disabled	0x02	0	0	0	0	0	0	0	0
Interrupt	$\overline{\text{INT}}$ is a port, not an interrupt output	0x03	0	0	0	0	0	0	0	0
Configuration	Shutdown mode: key sound is disabled; alert sound is disabled; alert $\overline{\text{INT}}$ is disabled; timeout enabled; no sound output	0x04	0	0	0	0	0	0	0	1
Ports	Ports 2–7 and $\overline{\text{INT}}$ are logic-high (high impedance)	0x05	1	1	1	1	1	1	1	X
Key Sound	Key-sound default is 31.25ms of 987.77Hz	0x06	0	1	0	1	0	0	0	1
Alert Sound	Key-sound default is 250ms of 2093Hz	0x07	1	0	1	1	1	0	1	1

X = Don't care.

Table 6. Sounder Power-Up Configuration

POWER-UP CONDITION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Sounder output is a general-purpose output, logic 0; queue is empty	0	0	0	0	0	0	0	0

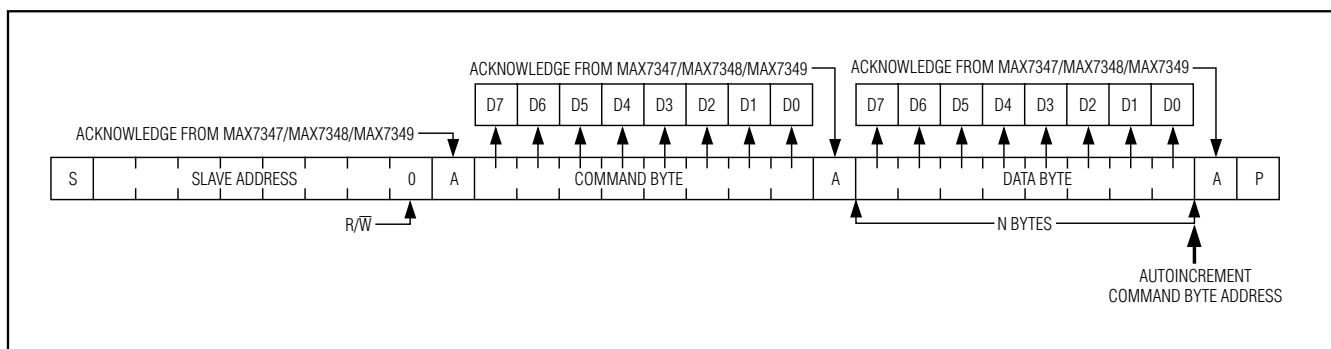


Figure 9. N Data Bytes Received

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 7. Key-Scan Register Address Map

REGISTER FUNCTION	COMMAND ADDRESS								ADDRESS CODE (hex)
	D15	D14	D13	D12	D11	D10	D9	D8	
Keys FIFO	0	0	0	0	0	0	0	0	0x00
Debounce	0	0	0	0	0	0	0	1	0x01
Autorepeat	0	0	0	0	0	0	1	0	0x02
Interrupt	0	0	0	0	0	0	1	1	0x03
Configuration	0	0	0	0	0	1	0	0	0x04
Ports	0	0	0	0	0	1	0	1	0x05
Key Sound	0	0	0	0	0	1	1	0	0x06
Alert Sound	0	0	0	0	0	1	1	1	0x07

Table 8. Keys FIFO Register Format

REGISTER	ADDRESS CODE (hex)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
KEYS FIFO REGISTER*	0x00	OVERFLOW FLAG	MORE FLAG	KEY SWITCH THAT HAS BEEN DEBOUNCED					
FIFO has not overflowed	0x00	0	X	X	X	X	X	X	X
FIFO overflowed; FIFO contains the first eight key events	0x00	1	X	X	X	X	X	X	X
This key is the last FIFO item (key-switch data not zero)	0x00	X	0	X	X	X	X	X	X
Key 0 was EITHER the last FIFO item OR the FIFO is empty and no key has been pressed	0x00	0	0	0	0	0	0	0	0
This key is not the last FIFO item	0x00	X	1	X	X	X	X	X	X
Power-up default setting	0x00	0	0	0	0	0	0	0	0

*Reading the key-scan FIFO clears the $\overline{INT}$. $\overline{INT}$ is only reasserted by a key event after the FIFO has been emptied by read(s).

Command Address Autoincrementing

Address autoincrementing allows the MAX7347/MAX7348/MAX7349 to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the MAX7347/MAX7348/MAX7349 generally increments after each data byte is written or read (Table 4). Autoincrementing applies only to the key-scan command addresses and not to the sounder command addresses.

Registers Description

Initial Power-Up

On power-up, all control registers are reset and the MAX7347/MAX7348/MAX7349 enter shutdown mode (Tables 5, 6). Table 7 shows the register address map for the key-scan section.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 9. Debounce Register Format

REGISTER	ADDRESS CODE (hex)	REGISTER DATA							
DEBOUNCE REGISTER	0x01	D7	D6	D5	D4	D3	D2	D1	D0
		PORTS ENABLE			DEBOUNCE TIME				
Debounce time is 9ms	0x01	X	X	X	0	0	0	0	0
Debounce time is 10ms	0x01	X	X	X	0	0	0	0	1
Debounce time is 11ms	0x01	X	X	X	0	0	0	1	0
Debounce time is 12ms	0x01	X	X	X	0	0	0	1	1
All the way through to	0x01	X	X	X	—	—	—	—	—
Debounce time is 37ms	0x01	X	X	X	1	1	1	0	0
Debounce time is 38ms	0x01	X	X	X	1	1	1	0	1
Debounce time is 39ms	0x01	X	X	X	1	1	1	1	0
Debounce time is 40ms	0x01	X	X	X	1	1	1	1	1
GPO ports disabled (full key-scan functionality)	0x01	0	0	0	X	X	X	X	X
GPO port 7 enabled	0x01	0	0	1	X	X	X	X	X
GPO ports 7 and 6 enabled	0x01	0	1	0	X	X	X	X	X
GPO ports 7, 6, and 5 enabled	0x01	0	1	1	X	X	X	X	X
GPO ports 7, 6, 5, and 4 enabled	0x01	1	0	0	X	X	X	X	X
GPO ports 7, 6, 5, 4, and 3 enabled	0x01	1	0	1	X	X	X	X	X
GPO ports 7, 6, 5, 4, 3, and 2 enabled	0x01	1	1	X	X	X	X	X	X
Power-up default setting	0x01	1	1	1	1	1	1	1	1

Key-Scan Registers

Eight key-scan registers are described in the following sections.

Keys FIFO Register

The keys FIFO register contains the information pertaining to the status of the keys FIFO, as well as the key-press events that have been debounced (Table 8). Bits D0 to D5 denote which of the 64 keys have been debounced and the keys are numbered as in Table 2 and Figure 1. D6 indicates whether the present debounced key is the last one in the FIFO, with 1 denoting that there are more keys after the present one, and 0 denoting that the present debounced key is the last one stored in the FIFO. D7 is the overflow flag, which denotes whether the keys FIFO has overflowed.

Reading the key-scan FIFO clears the interrupt $\overline{\text{INT}}$. $\overline{\text{INT}}$ is only reasserted after the FIFO has been emptied by performing enough read operations.

Debounce Register

The debounce register sets the time for each debounce cycle, as well as setting whether the GPO ports are enabled or disabled. Bits D0 through D4 set the debounce time in increments of 1ms starting at 9ms and ending at 40ms (Table 9). Bits D5 through D7 set which one of the GPO ports is to be enabled. Note that not any port can be enabled at a particular time. The GPO ports can be enabled only in the combinations shown in Table 9, from all disabled to all enabled.

Autorepeat Register

The autorepeat register sets the autorepeat frequency (repeat rate) and its delay. The autorepeat function allows a key to be consecutively asserted when the key itself is pressed down without being released. The autorepeat delay specifies the delay between the first press and the beginning of the autorepeating, provided that the key has not been released. The autorepeat frequency specifies how fast the continuously pressed-down key to be asserted once autorepeating has started is. Bits D0 through D3 specify the autorepeat delay in terms of debounce cycles

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

ranging from 8 debounce cycles to 128 debounce cycles (Table 10). Bits D4 through D6 specify the autorepeat rate or frequency ranging from 4 to 32 debounce cycles. Bit D7 specifies whether the auto-repeat function is enabled with 0 denoting autorepeat disabled and 1 denoting autorepeat enabled.

Interrupt Register

The interrupt register contains information related to the settings of the interrupt request function, as well as the status of the $\overline{\text{INT}}$ output, which can also be configured as a GPO. Bits D0 through D4 set the key-scan interrupt frequency. By setting bits D0 through D4 to an appropriate value, the interrupt can be asserted at the end of the selected number of debounce cycles (Table 11). This number ranges from 1 to 31 debounce cycles. If bits D0 through D4 are set to 00000, the $\overline{\text{INT}}$ output is configured as a GPO that is controlled by bit D6 in the ports register and the $\overline{\text{INT}}$ output is not asserted. However, the $\overline{\text{INT}}$ status bits D5, D6, and D7 are still set and cleared in the normal way at the end of each debounce cycle as if bits D0 through D4 were set to 00001.

Bits D5 and D6 denote whether an interrupt was set due to a key-scan event (bit D5) or to an alert event (bit D6). Bit D7 represents whether an interrupt request has been asserted with 0 denoting no $\overline{\text{INT}}$ asserted and 1 denoting that $\overline{\text{INT}}$ has been asserted.

The interrupt register is a read-only register and writes to it are ignored. Reading the interrupt register does clear an alert event $\overline{\text{INT}}$, but does not clear a key-scan event $\overline{\text{INT}}$. An interrupt request caused by a key-scan event(s) is cleared when the FIFO is emptied.

Configuration Register

The configuration register reflects the sounder status, controls the I²C bus timeout feature, enables the alert input interrupt feature, enables the sounder to respond to both alert input and key debounce events, and controls the shutdown of the device (Table 12).

Ports Register

The ports register sets the values of ports 2 through 7 and the $\overline{\text{INT}}$ port when configured as GPOs. The settings in this register are ignored for ports not configured as GPOs, and a read from this register returns the values stored in the register and not the actual port conditions (Table 13). The ports register also serves to read the alert input and this is done through bit D0 with a 0 denoting a low on the alert input and a 1 denoting a high.

Key-Sound Register

The key-sound register specifies the duration and frequency of the sound to be executed by the sounder controller when a key or a set of keys are debounced if the

sounder output has been enabled to be set by a key debounce event in the configuration register. When this happens, the information of bits D7 through D1 is passed on to the sounder register and the appropriate sound is executed (Tables 14, 16). Least significant bit D0 is ignored and always set to 1 when transferred to the sounder register. See Table 16 for the format of setting the frequency and duration of the sound to be executed. If a key-sound register command is sent as 000xxxx (continuous), then the command is stored as 111xxxx (1000ms) in the sounder register.

Alert Sound Register

The alert sound register specifies the duration and frequency of the sound to be executed by the sounder controller at the falling edge of the alert input if the sounder output has been enabled to be set by the alert input in the configuration register. If this is the case, the information of bits D7 through D1 is passed on to the sounder register and the appropriate sound is executed (Tables 15, 16). Least significant bit D0 is always set to 1 and this value is ignored when transferred to the sounder register. See Table 16 for the proper format of setting the frequency and duration of the sound to be executed. Note that if an alert sound register command is sent as 000xxxx (continuous), then the command is actually stored as 111xxxx (1000ms) in the sounder register.

Sounder Register

The sounder register stores the frequencies and duration of the sounds to be executed by the sounder, as well as the state of its two-deep FIFO (Table 16). D0 denotes whether another command is lined in the queue at any given moment. A 0 in D0 denotes that the queue is empty while a 1 denotes that there is another command. By writing 0 to D0, the present command is executed and the queue is cleared. When sending a command that has a D0 set to 1, the queue is checked and, if empty, the sent command is added to it while, if full, the sent command replaces the queued command.

Bits D0 and D1, when taken in conjunction, set the level of the sounder output when configured as a GPO and also control the autoloop function provided that the rest of the bits (D7 through D2) are set to 0. When the sounder is configured as a GPO, the levels of the output are set by D1, a 0 denoting a low and a 1 denoting a high. When D0 is set to 1 and the rest of the bits are set to 0, D1 controls the autoloop function as defined in Table 16.

Bits D7 through D1 control the frequency and duration of the sounds to be executed by the sounder. These sounds include the musical notes of the 5th octave plus some notes from the 6th and 7th octaves as well. See Table 16.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 10. Autorepeat Register Format

REGISTER	ADDRESS CODE (hex)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
AUTOREPEAT REGISTER	0x02	ENABLE	AUTOREPEAT RATE			AUTOREPEAT DELAY			
Autorepeat is disabled	0x02	0	X	X	X	X	X	X	X
Autorepeat is enabled	0x02	1	AUTOREPEAT RATE			AUTOREPEAT DELAY			
Key-switch autorepeat delay is 8 debounce cycles	0x02	1	X	X	X	0	0	0	0
Key-switch autorepeat delay is 16 debounce cycles	0x02	1	X	X	X	0	0	0	1
Key-switch autorepeat delay is 24 debounce cycles	0x02	1	X	X	X	0	0	1	0
Key-switch autorepeat delay is 32 debounce cycles	0x02	1	X	X	X	0	0	1	1
Key-switch autorepeat delay is 40 debounce cycles	0x02	1	X	X	X	0	1	0	0
Key-switch autorepeat delay is 48 debounce cycles	0x02	1	X	X	X	0	1	0	1
Key-switch autorepeat delay is 56 debounce cycles	0x02	1	X	X	X	0	1	1	0
Key-switch autorepeat delay is 64 debounce cycles	0x02	1	X	X	X	0	1	1	1
Key-switch autorepeat delay is 72 debounce cycles	0x02	1	X	X	X	1	0	0	0
Key-switch autorepeat delay is 80 debounce cycles	0x02	1	X	X	X	1	0	0	1
Key-switch autorepeat delay is 88 debounce cycles	0x02	1	X	X	X	1	0	1	0
Key-switch autorepeat delay is 96 debounce cycles	0x02	1	X	X	X	1	0	1	1
Key-switch autorepeat delay is 104 debounce cycles	0x02	1	X	X	X	1	1	0	0
Key-switch autorepeat delay is 112 debounce cycles	0x02	1	X	X	X	1	1	0	1
Key-switch autorepeat delay is 120 debounce cycles	0x02	1	X	X	X	1	1	1	0
Key-switch autorepeat delay is 128 debounce cycles	0x02	1	X	X	X	1	1	1	1
Key-switch autorepeat frequency is 4 debounce cycles	0x02	1	0	0	0	X	X	X	X
Key-switch autorepeat frequency is 8 debounce cycles	0x02	1	0	0	1	X	X	X	X
Key-switch autorepeat frequency is 12 debounce cycles	0x02	1	0	1	0	X	X	X	X
Key-switch autorepeat frequency is 16 debounce cycles	0x02	1	0	1	1	X	X	X	X
Key-switch autorepeat frequency is 20 debounce cycles	0x02	1	1	0	0	X	X	X	X
Key-switch autorepeat frequency is 24 debounce cycles	0x02	1	1	0	1	X	X	X	X
Key-switch autorepeat frequency is 28 debounce cycles	0x02	1	1	1	0	X	X	X	X
Key switch autorepeat frequency is 32 debounce cycles	0x02	1	1	1	1	X	X	X	X
Power-up default setting	0x02	0	0	0	0	0	0	0	0

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

MAX7347/MAX7348/MAX7349

Table 11. Interrupt Register Format

REGISTER	ADDRESS CODE (hex)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
INTERRUPT REGISTER	0x03	$\overline{\text{INT}}$ STATUS*	ALERT EVENT*	KEY-SCAN EVENT*	KEY-SCAN INTERRUPT FREQUENCY				
Current $\overline{\text{INT}}$ is due to key-scan event(s)	0x03	1	0	1	X	X	X	X	X
Current $\overline{\text{INT}}$ is due to alert event	0x03	1	1	0	X	X	X	X	X
Current $\overline{\text{INT}}$ is due to both key-scan event(s) and alert event	0x03	1	1	1	X	X	X	X	X
$\overline{\text{INT}}$ has not been asserted	0x03	0	0	0	X	X	X	X	X
$\overline{\text{INT}}$ has been asserted	0x03	1	ALERT EVENT	KEY-SCAN EVENT	X	X	X	X	X
$\overline{\text{INT}}$ output pin is NOT asserted; $\overline{\text{INT}}$ output pin is used as a general-purpose output called $\overline{\text{INT}}$ port under control of bit D6 in ports register; $\overline{\text{INT}}$ status bits D5, D6, D7 are still set and cleared in the normal way at the end of every debounce cycle as if bits D4–D0 were set to 00001	0x03	X	X	X	0	0	0	0	0
Key-scan $\overline{\text{INT}}$ is asserted at the end of every debounce cycle, if new key(s) is debounced	0x03	X	X	X	0	0	0	0	1
Key-scan $\overline{\text{INT}}$ is asserted at the end of every 2 debounce cycles, if new key(s) is debounced	0x03	X	X	X	0	0	0	1	0
—	—	—	—	—	—	—	—	—	—
Key-scan $\overline{\text{INT}}$ is asserted at the end of every 29 debounce cycles, if new key(s) is debounced	0x03	X	X	X	1	1	1	0	1
Key-scan $\overline{\text{INT}}$ is asserted at the end of every 30 debounce cycles, if new key(s) is debounced	0x03	X	X	X	1	1	1	1	0
Key-scan $\overline{\text{INT}}$ is asserted at the end of every 31 debounce cycles, if new key(s) is debounced	0x03	X	X	X	1	1	1	1	1
Power-up default setting	0x03	0	0	0	0	0	0	0	0

*Read-only register bits; write data is ignored. Reading the interrupt register does clear an alert event $\overline{\text{INT}}$, but does not clear a key-scan event $\overline{\text{INT}}$. $\overline{\text{INT}}$ caused by key-scan event(s) is cleared when FIFO is emptied.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 12. Configuration Register Format

REGISTER	ADDRESS CODE (hex)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
CONFIGURATION REGISTER	0x04	SHUTDOWN	KEY SOUND ENABLE	ALERT SOUND ENABLE	ALERT INT ENABLE	ALERT INT EVENT	SOUNDER STATUS		TIMEOUT ENABLE
Serial interface bus timeout enabled	0x04	X	X	X	X	X	X	X	0
Serial interface bus timeout disabled	0x04	X	X	X	X	X	X	X	1
No active sounder output	0x04	X	X	X	X	X	0	0	X
Active sounder output set by serial interface	0x04	X	X	X	X	X	0	1	X
Active sounder output set by key debounce event	0x04	X	X	X	X	X	1	0	X
Active sounder output set by an alert event	0x04	X	X	X	X	X	1	1	X
Alert input interrupt (if enabled) is asserted according to key-scan interrupt rules	0x04	X	X	X	X	0	X	X	X
Alert input interrupt (if enabled) is asserted immediately	0x04	X	X	X	X	1	X	X	X
Alert input does not cause an interrupt	0x04	X	X	X	0	X	X	X	X
Falling edge of alert input causes interrupt	0x04	X	X	X	1	X	X	X	X
Alert input does not cause an automatic sound	0x04	X	X	0	X	X	X	X	X
Falling edge of alert input causes the 8-bit contents of the alert sound register 0x07 to be sent to the sounder	0x04	X	X	1	X	X	X	X	X
Debounce key(s) do not cause an automatic sound	0x04	X	0	X	X	X	X	X	X
Debounced key(s), including autorepeated keys, cause the 8-bit contents of the key-sound register 0x06 to be sent to the sounder	0x04	X	1	X	X	X	X	X	X

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 12. Configuration Register Format (continued)

REGISTER	ADDRESS CODE (hex)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
CONFIGURATION REGISTER	0x04	SHUTDOWN	KEY SOUND ENABLE	ALERT SOUND ENABLE	ALERT INT ENABLE	ALERT INT EVENT	SOUNDER STATUS		TIMEOUT ENABLE
Shutdown mode; key-scan and sounder timing are disabled, interrupts disabled, but alert input can be read and port outputs (as selected) can be changed	0x04	0	X	X	X	X	X	X	X
Operating mode; key scan is started, and commands in sounder queue are actioned	0x04	1	X	X	X	X	X	X	X
Power-up default setting	0x04	0	0	0	0	0	0	0	1

Table 13. Ports Register Format

REGISTER	ADDRESS CODE (hex)	READ WRITE	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
PORTS REGISTER	0x05	READ	PORT 7	PORT 6	PORT 5	PORT 4	PORT 3	PORT 2	$\overline{\text{INT}}$ PORT	ALERT INPUT
		WRITE	PORT 7	PORT 6	PORT 5	PORT 4	PORT 3	PORT 2	$\overline{\text{INT}}$ PORT	X
Clear port 2 low	0x05	Write	X	X	X	X	X	0	X	X
Set port 2 high (high impedance)	0x05	Write	X	X	X	X	X	1	X	X
Clear port 3 low	0x05	Write	X	X	X	X	0	X	X	X
Set port 3 high (high impedance)	0x05	Write	X	X	X	X	1	X	X	X
Clear port 4 low	0x05	Write	X	X	X	0	X	X	X	X
Set port 4 high (high impedance)	0x05	Write	X	X	X	1	X	X	X	X
Clear port 5 low	0x05	Write	X	X	0	X	X	X	X	X
Set port 5 high (high impedance)	0x05	Write	X	X	1	X	X	X	X	X
Clear port 6 low	0x05	Write	X	0	X	X	X	X	X	X
Set port 6 high (high impedance)	0x05	Write	X	1	X	X	X	X	X	X

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 13. Ports Register Format (continued)

REGISTER	ADDRESS CODE (hex)	READ WRITE	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
PORTS REGISTER	0x05	READ	PORT 7	PORT 6	PORT 5	PORT 4	PORT 3	PORT 2	$\overline{\text{INT}}$ PORT	ALERT INPUT
		WRITE	PORT 7	PORT 6	PORT 5	PORT 4	PORT 3	PORT 2	$\overline{\text{INT}}$ PORT	X
Clear port 7 low	0x05	Write	0	X	X	X	X	X	X	X
Set port 7 high (high impedance)	0x05	Write	1	X	X	X	X	X	X	X
Clear $\overline{\text{INT}}$ port low; this setting is ignored unless the key-scan $\overline{\text{INT}}$ functionality is disabled by setting interrupt register bits D4 to D0 to 00000	0x05	Write	X	X	X	X	X	X	0	X
Set $\overline{\text{INT}}$ port high (high impedance); this setting is ignored unless the key-scan $\overline{\text{INT}}$ functionality is disabled by setting interrupt register bits D4 to D0 to 00000	0x05	Write	X	X	X	X	X	X	1	X
Alert input level is low	0x05	Read	X	X	X	X	X	X	X	0
Alert input level is high	0x05	Read	X	X	X	X	X	X	X	1
Power-up default setting	0x05	—	1	1	1	1	1	1	1	X

Table 14. Key-Sound Register Format

REGISTER	ADDRESS CODE (hex)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
This-8 bit value is passed to sounder controller when key(s) debounced, if enabled in the configuration register; these 7 bits define duration and frequency only; sounder command bit D0 is ignored and fixed internally at 1; if a key sound is sent as 000xxxxx (continuous), then the command is stored as 111xxxxx (1000 ms)	0x06	7-bit value (see Table 16 for functionality)							1
Power-up default setting	0x06	0	1	0	1	0	0	0	1

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

MAX7347/MAX7348/MAX7349

Table 15. Alert Sound Register Format

REGISTER	ADDRESS CODE (hex)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
This 8-bit value is passed to sounder controller on the falling edge of the alert input; these 7 bits define duration and frequency only; sounder command bit D0 is ignored and fixed internally at 1; if an alert sound is sent as 000xxxxx (continuous), then the command is stored as 111xxxxx (1000 ms)	0x07	7-bit value (see Table 16 for functionality)							1
Power-up default setting	0x07	1	0	1	1	1	0	1	1

Table 16. Sounder Register Format

REGISTER	READ WRITE	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
SOUNDER REGISTER		DURATION			FREQUENCY			LEVEL	BUFFER
No commands are active; OR output is GPO logic 0	Read	0	0	0	0	0	0	0	0
This current command is active, none are queued (so another command may be sent)	Read	DURATION			FREQUENCY			LEVEL	0
This current command is active, and another command is in the queue	Read	DURATION			FREQUENCY			LEVEL	1
Perform this command, terminating and clearing any previous active command, command queue, and autoloop; new command is now active, and queue is now empty	Write	X	X	X	X	X	X	X	0
Add command to queue if not full; command replaces queued command if queue is full	Write	X	X	X	X	X	X	X	1
Configure sounder output as general-purpose output, logic 0 (clear queue; sounder output active low with continuous duration, ie, until a buffer = 0 command)	Write	0	0	0	0	0	0	0	0
Configure sounder output as general-purpose output, logic 1 (clear queue; sounder output active high with continuous duration, ie, until a buffer = 0 command)	Write	0	0	0	0	0	0	1	0
Autoloop using the current two commands; the active command is command 1, and the inactive command is command 2; if no command is active, the oldest command is reactivated as command 1, and the other command is re-activated as command 2	Write	0	0	0	0	0	0	0	1
Autoloop is halted at the end of command 2, and output idles as defined by command 2	Write	0	0	0	0	0	0	1	1

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Table 16. Sounder Register Format (continued)

REGISTER	READ WRITE	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
SOUNDER REGISTER		DURATION			FREQUENCY			LEVEL	BUFFER
Sounder output active low for sound duration; queue cleared	—	Write	DURATION	0	0	0	0	0	
Sounder output active high for sound duration; queue cleared	—	Write		0	0	0	1	0	
Sound frequency is 523.25Hz, idles low	Note C5	Write		0	0	1	0	BUFFER	
Sound frequency is 587.33Hz, idles low	Note D5	Write		0	0	1	1		
Sound frequency is 659.26, idles low	Note E5	Write		0	1	0	0		
Sound frequency is 698.46Hz, idles low	Note F5	Write		0	1	0	1		
Sound frequency is 783.99Hz, idles low	Note G5	Write		0	1	1	0		
Sound frequency is 880Hz, idles low	Note A5	Write		0	1	1	1		
Sound frequency is 987.77Hz, idles low	Note B5	Write		1	0	0	0		
Sound frequency is 1046.5Hz, idles low	Note C6	Write		1	0	0	1		
Sound frequency is 1318.5Hz, idles low	Note E6	Write		1	0	1	0		
Sound frequency is 1568Hz, idles low	Note G6	Write		1	0	1	1		
Sound frequency is 1760Hz, idles low	Note A6	Write		1	1	0	0		
Sound frequency is 2093Hz, idles low	Note C7	Write		1	1	0	1		
Sound frequency is 2349.3Hz, idles low	Note D7	Write		1	1	1	0		
Sound frequency is 2637Hz, idles low	Note E7	Write		1	1	1	1		
Sound duration is continuous; if an alert sound or a key sound is programmed as 000xxxxx (continuous), then the command is treated as 111xxxxx (1000 ms)	Write	0	0	0	FREQUENCY			LEVEL	BUFFER
Sound duration is 15625ms*	Write	0	0	1					
Sound duration is 3125ms*	Write	0	1	0					
Sound duration is 625ms*	Write	0	1	1					
Sound duration is 125ms*	Write	1	0	0					
Sound duration is 250ms*	Write	1	0	1					
Sound duration is 500ms*	Write	1	1	0					
Sound duration is 1000ms*	Write	1	1	1					
Power-up default setting	—	0	0	0	0	0	0	0	0

*Sound duration will be slightly longer than these times because each sound always completes a full cycle before stopping.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Sounder Operation

When an alert sound or key sound is happening, the user cannot write to the sounder. The MAX7347/MAX7348/MAX7349 do not acknowledge a write to the sounder I²C address. However, a read from the sounder will work correctly. An alert sound or key sound event terminates a current user-programmed event and clears the queue. If an alert sound or key sound event is currently being processed, then a new alert sound or key sound event will be put into the queue, replacing an existing queued alert sound or key sound event, if one exists. User access to the sounder is restored when the last alert sound or key sound event is completed. Note this means that the buffer bit (D0) for an alert sound or key sound command is effectively ignored.

Shutdown

The MAX7347/MAX7348/MAX7349 are put into shutdown mode by clearing bit D7 in the configuration register (Table 12). In shutdown, the key-scan controller and sounder controller are both disabled, and the MAX7347/MAX7348/MAX7349 draw minimal current. No additional supply current is drawn if any keys are pressed. All switch matrix current sources are turned off, and row outputs ROW0 to ROW7 and column outputs COL0 to COL7 become high impedance.

The alert input status may still be read in shutdown, and an alert event can still cause an interrupt request if this feature is enabled (Table 12). This means that alert can be used for μ C wakeup while the system sleeps drawing minimum current.

Outputs configured as GPOs (COL2/PORT2 to COL2/PORT7 and INT) may still be controlled in shutdown and their output states can be changed under software control at any time.

The sounder output may not be changed in shutdown, even if it is effectively being used as a logic output. Writes to the sounder during shutdown are ignored, and the sounder FIFO is cleared on entering shutdown. However, the sounder retains its output logic state for the duration of shutdown, and so can be set low or high as desired by writing 0x00 or 0x02, respectively, to the sounder register (Table 12) before entering shutdown.

The MAX7347/MAX7348/MAX7349 may be taken out of shutdown mode and put into operating mode by setting bit D7 in the configuration register (Table 12). The key-scan and sounder controller FIFOs are cleared, and key monitoring starts. Note that rewriting the configuration register with bit D7 high when bit D7 was already high does not clear the FIFOs; the FIFOs are only cleared when the MAX7347/MAX7348/MAX7349 are actually coming out of shutdown.

Applications Information

Ghost-Key Elimination

Ghost keys are a phenomenon inherent with key-switch matrices. When three switches located at the corners of a matrix rectangle are pressed simultaneously, the switch that is located at the last corner of the rectangle (the ghost key) also appears to be pressed. This occurs because the potentials at the two sides of the ghost-key switch are identical due to the other three connections—the switch is electrically shorted by the combination of the other three switches (Figure 10). Because the key appears to be pressed electrically, it is impossible for software to detect which of the four keys is the ghost key.

The MAX7347/MAX7348/MAX7349 employ a proprietary scheme that detects any three-key combination that generates a fourth ghost key, and does not report any of these four keys as being pressed. This means that although ghost keys are never reported, many combinations of three keys are effectively ignored when pressed at the same time. Applications requiring three key combinations (such as <Ctrl><Alt>) must ensure that the 3 keys are not wired in positions that define the vertices of a rectangle (Figure 11).

Low-EMI Operation

The MAX7347/MAX7348/MAX7349 use two techniques to minimize EMI radiating from the key-switch wiring. First, the voltage across the switch matrix never exceeds 0.65V, irrespective of supply voltage V+. This reduces the voltage swing at any node when a switch is pressed to 0.65V maximum. Second, the keys are not dynamically scanned, which would cause the key-switch wiring to continuously radiate interference. Instead, the keys are monitored for current draw (only occurs when pressed), and debounce circuitry only operates when one or more keys are actually pressed.

Power-Supply Considerations

The MAX7347/MAX7348/MAX7349 operate with a 2.4V to 3.6V power-supply voltage. Bypass the power supply to GND with a 0.047 μ F or higher ceramic capacitor as close to the device as possible.

Switch On-Resistance

The MAX7347/MAX7348/MAX7349 are designed to be insensitive to resistance either in the key switches or the switch routing to and from the appropriate COLx and ROWx up to 1k Ω . These controllers are therefore compatible with low-cost membrane and conductive carbon switches.

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

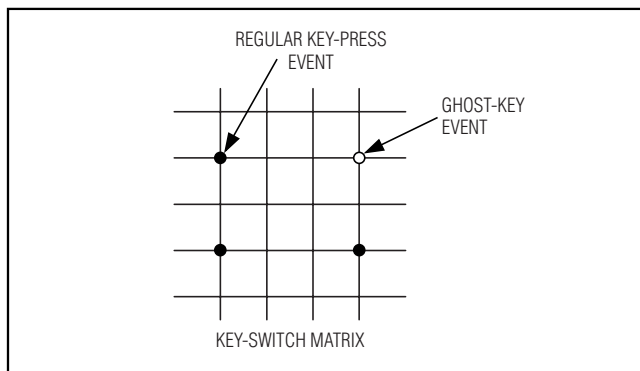


Figure 10. Ghost-Key Phenomenon

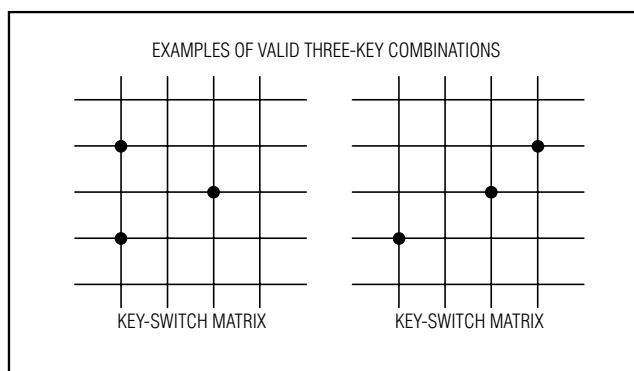


Figure 11. Valid Three-Key Combinations

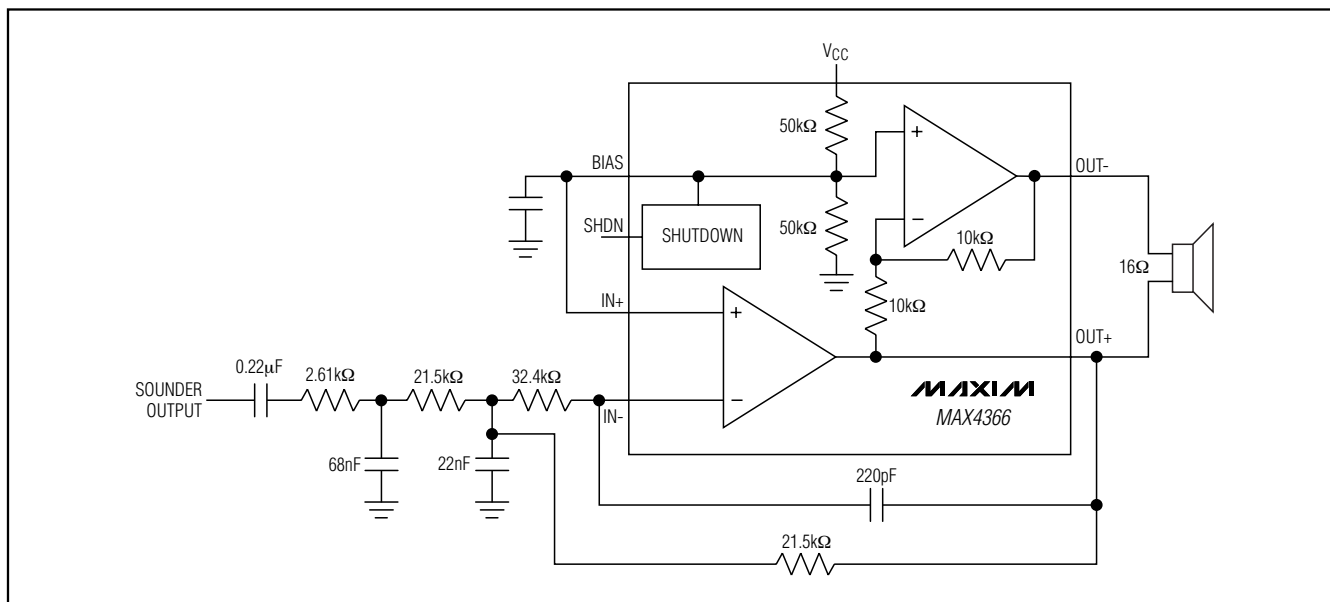


Figure 12. Third-Order Chebyshev Lowpass Filter and Output Stage

Audio Transducers

The sounder output is designed to drive a standard, low-cost piezo transducer directly without further buffering. Piezo transducers appear as a capacitive load of typically 10nF. If a resistive or inductive sounder is used, such as a small loudspeaker, fit a coupling capacitor between the sounder output and the transducer. For example, if a 32Ω speaker is used, connect the positive side of a 22µF electrolytic capacitor to the sounder output, the negative side of the capacitor to one end of the speaker, and the other end of the speaker to GND.

The sounder output can also drive a power amplifier for higher sound levels. In this case, it is usually desirable to include a lowpass filter before the speaker to convert the square-wave tones to something closer to a sinusoid. The recommended cutoff frequency of this filter is around 3kHz. An example circuit is shown in Figure 12, which uses the uncommitted op amp of the MAX4366 bridge power amplifier to implement a third-order Chebyshev lowpass filter.

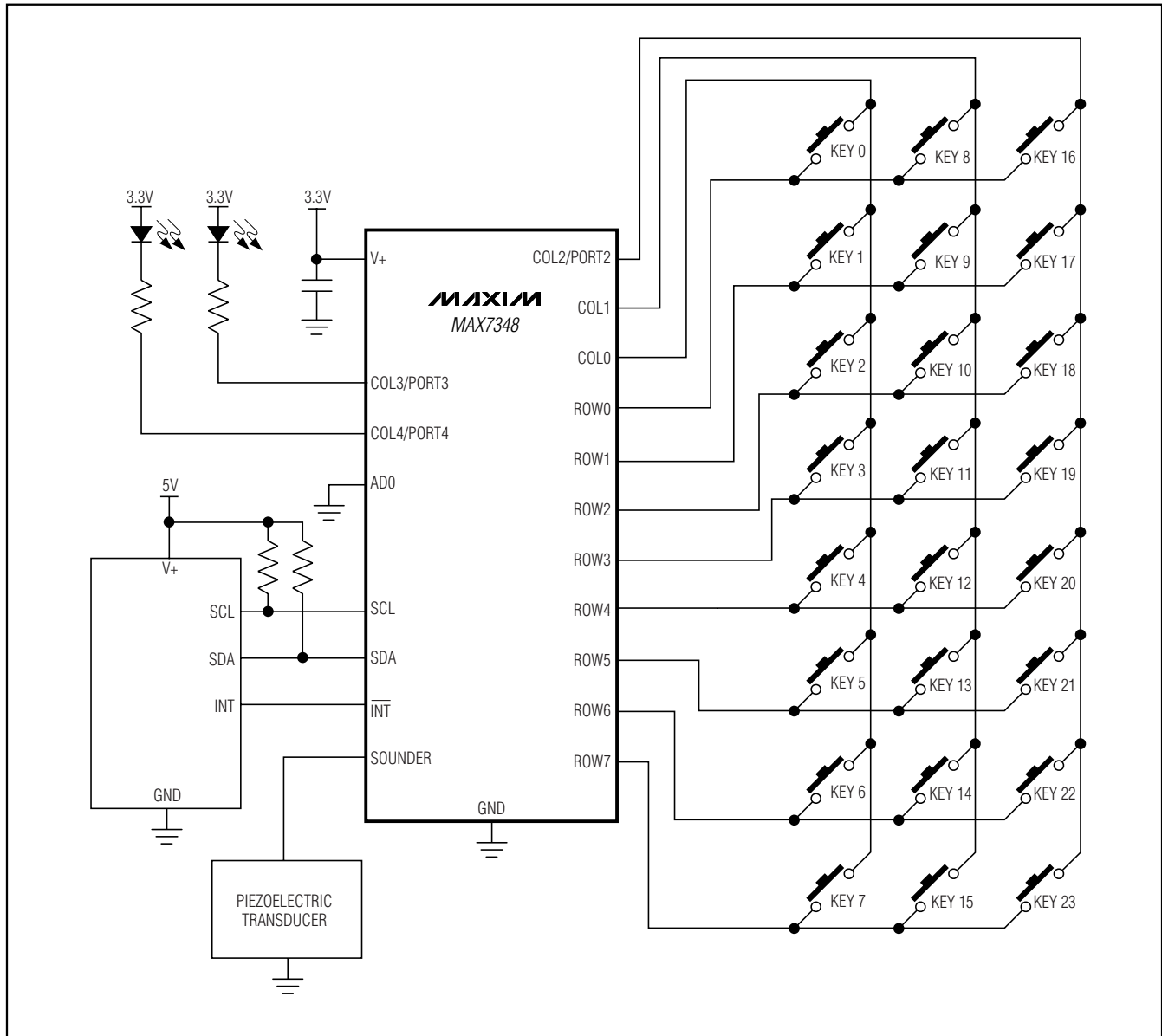
Chip Information

PROCESS: BiCMOS

2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Typical Application Circuit

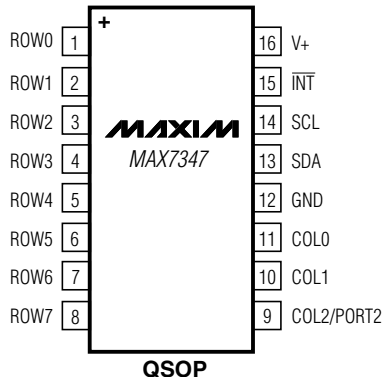
MAX7347/MAX7348/MAX7349



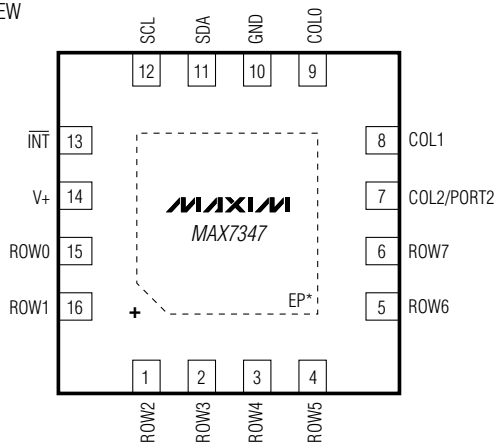
2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Pin Configurations

TOP VIEW

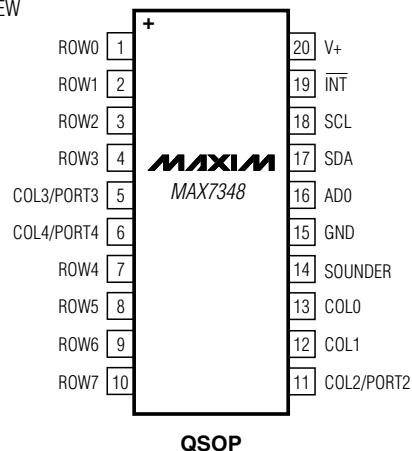


TOP VIEW

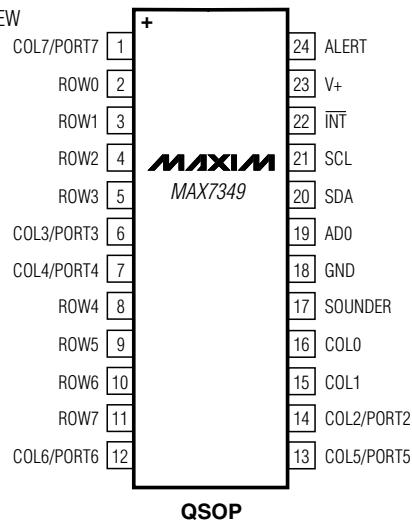


*EP = EXPOSED PADDLE

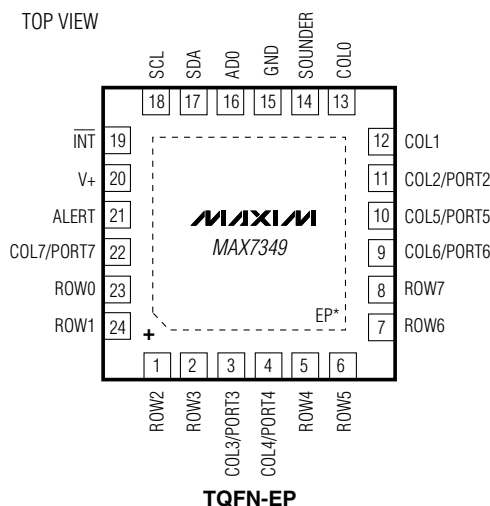
TOP VIEW



TOP VIEW



TOP VIEW



*EP = EXPOSED PADDLE

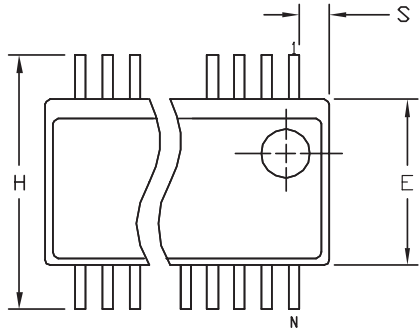
2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Package Information

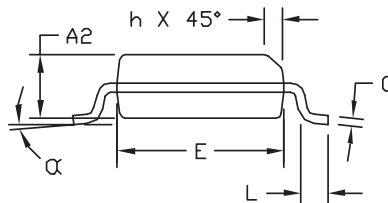
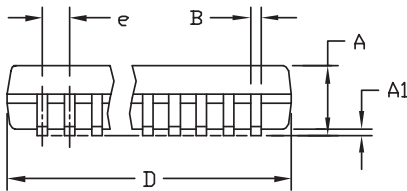
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX7347/MAX7348/MAX7349

QSOP-LEPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS		N
	MIN.	MAX.	MIN.	MAX.	
D	.189	.196	4.80	4.98	16 AB
S	.0020	.0070	0.05	0.18	
D	.337	.344	8.56	8.74	20 AD
S	.0500	.0550	1.270	1.397	
D	.337	.344	8.56	8.74	24 AE
S	.0250	.0300	0.635	0.762	
D	.386	.393	9.80	9.98	28 AF
S	.0250	.0300	0.635	0.762	

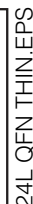
NOTES:

- 1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
- 2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
- 3). CONTROLLING DIMENSIONS: INCHES.
- 4). MEETS JEDEC MO137.

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE			
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH			
APPROVAL	DOCUMENT CONTROL NO. 21-0055	REV. F	1/ 1

MAX7347/MAX7348/MAX7349

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



2-Wire Interfaced Low-EMI Key Switch and Sounder Controllers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
JeDEC Var.	VGG8			VGGC			WGGD-1			WGGD-2			VGGE		

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.

△ THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

△ DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.

△ ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

△ COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9. DRAWING CONFORMS TO JEDEC M0220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.

△ MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

11. COPLANARITY SHALL NOT EXCEED 0.08mm

12. WARPAGE SHALL NOT EXCEED 0.10mm

△ LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

EXPOSED PAD VARIATIONS								
PKG CODES	D2			E2			DOWN BONDS ALLOWED	
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES	
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES	
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES	
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO	
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES	
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES	
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO	
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO	

	
TITLE PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm	
APPROVAL	DOCUMENT CONTROL NO. 21-0139
REV. E	2/2

Revision History

Pages changed at Rev 5: 1, 2, 23, 29

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MAX7347/MAX7348/MAX7349