

-48V Hot-Swap Controllers with External RSENSE

ABSOLUTE MAXIMUM RATINGS

(All voltages are referenced to V_{EE} , unless otherwise noted.)

Supply Voltage ($V_{DD} - V_{EE}$)	-0.3V to +100V
PWRGD, $\overline{PWRGD}$	-0.3V to +100V
DRAIN (Note 1)	-2V to +100V
PWRGD to DRAIN	-0.3V to +95V
PWRGD to V_{DD}	-95V to +85V
SENSE (Internally Clamped)	-0.3V to +1.0V
GATE (Internally Clamped)	-0.3V to +18V
UV and OV	-0.3V to +60V

Current Through SENSE	±40mA
Current into GATE	±300mA
Current into DRAIN	-100mA to +20mA
Current into Any Other Pin	±20mA
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
8-Pin SO (derate 5.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	471mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Note 1: Test condition per Figure 1. DRAIN current must be limited to the specified 100mA maximum.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{EE} = 0\text{V}$, $V_{DD} = 48\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Notes 2, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Input Voltage Range	V_{DD}		20		80	V
Supply Current	I_{DD}	(Note 3)		0.7	2	mA
GATE DRIVE AND CLAMPING CIRCUITS						
GATE Pin Pullup Current	I_{PU}	Gate drive on, $V_{GATE} = V_{EE}$	-30	-45	-60	μA
GATE Pin Pulldown Current	I_{PD}	Gate drive off, $V_{GATE} = 2\text{V}$, $T_A = +25^\circ\text{C}$	24	50	70	mA
External Gate Drive	ΔV_{GATE}	$V_{GATE} - V_{EE}$, $20\text{V} \leq V_{DD} \leq 80\text{V}$	10	13.5	18	V
GATE to V_{EE} Clamp Voltage	V_{GSCLMP}	$V_{GATE} - V_{EE}$, $I_{GS} = 30\text{mA}$	15	16.4	18	V
CIRCUIT BREAKER						
Current-Limit Trip Voltage	V_{CL}	$V_{CL} = V_{SENSE} - V_{EE}$	40	50	60	mV
SENSE Input Bias Current	I_{SENSE}	$V_{SENSE} = 50\text{mV}$	0	-0.2	-2	μA
UNDERVOLTAGE LOCKOUT						
Internal Undervoltage-Lockout Voltage High	V_{UVLOH}	V_{DD} increasing	13.8	15.4	17.0	V
Internal Undervoltage-Lockout Voltage Low	V_{UVLOL}	V_{DD} decreasing	11.8	13.4	15.0	V
UV PIN						
UV High Threshold	V_{UVH}	UV voltage increasing	1.240	1.255	1.270	V
UV Low Threshold	V_{UVL}	UV voltage decreasing	1.105	1.125	1.145	V
UV Hysteresis	V_{UVHY}			130		mV
UV Input Bias Current	I_{INUV}	$V_{UV} = V_{EE}$		0	-0.5	μA
OV PIN						
OV High Threshold	V_{OVH}	OV voltage increasing	1.235	1.255	1.275	V
OV Low Threshold	V_{OVL}	OV voltage decreasing	1.210	1.235	1.255	V
OV Hysteresis	V_{OVHY}			20		mV
OV Input Bias Current	I_{INOV}	$V_{OV} = V_{EE}$		0	-0.5	μA

-48V Hot-Swap Controllers with External RSENSE

MAX5949A/MAX5949B

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = 0V, V_{DD} = 48V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 2, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWRGD OUTPUT SIGNAL REFERENCED TO DRAIN						
DRAIN Input Bias Current	I _{DRAIN}	V _{DRAIN} = 48V	10	80	250	μA
DRAIN Threshold for Power-Good	V _{DL}	V _{DRAIN} - V _{EE} threshold for power-good condition, DRAIN decreasing	1.1	1.4	2.0	V
GATE High Threshold	V _{GH}	ΔV _{GATE} - V _{GATE} threshold for power-good condition, ΔV _{GATE} - V _{GATE} decreasing	1.0	1.4	2.0	V
PWRGD, $\overline{\text{PWRGD}}$ Output Leakage	I _{OH}	$\overline{\text{PWRGD}}$ (MAX5949A) = 80V, V _{DRAIN} = 48V, PWRGD (MAX5949B) = 80V, V _{DRAIN} = 0V			10	μA
$\overline{\text{PWRGD}}$ Output Low Voltage	V _{OL}	V $\overline{\text{PWRGD}}$ - V _{EE} ; V _{DRAIN} - V _{EE} < V _{DL} , I _{SINK} = 5mA (MAX5949A)		0.11	0.4	V
PWRGD Output Low Voltage	V _{OL}	V _{PWRGD} - V _{DRAIN} ; V _{DRAIN} = 5V, I _{SINK} = 1mA (MAX5949B)		0.11	0.4	V
AC PARAMETERS						
OV High to GATE Low	t _{PHLOV}	Figures 2a, 3		0.5		μs
UV Low to GATE Low	t _{PHLUV}	Figures 2a, 4		0.4		μs
OV Low to GATE High	t _{PLHOV}	Figures 2a, 3		4		μs
UV High to GATE High	t _{PLHVL}	Figures 2a, 4		5.5		μs
SENSE High to GATE Low	t _{PHLSENSE}	Figures 2a, 5a		1	3	μs
Current Limit to GATE Low	t _{PHLCB}	Figures 2b, 5b	350	500	650	μs
DRAIN Low to $\overline{\text{PWRGD}}$ Low DRAIN Low to (PWRGD - DRAIN) High	t _{PHLDL}	MAX5949A, Figures 2a, 6a		1.8		μs
		MAX5949B, Figures 2a, 6a		3.4		
GATE High to $\overline{\text{PWRGD}}$ Low GATE High to (PWRGD - DRAIN) High	t _{PHLGH}	MAX5949A, Figures 2a, 6b		1.6		μs
		MAX5949B, Figures 2a, 6b		2.5		
TURN-OFF						
Latch-Off Period	t _{OFF}	(Note 4)	51	64	78	ms

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE}, unless otherwise specified.

Note 3: Current into V_{DD} with UV = 3V, OV = DRAIN = PWRGD = SENSE = V_{EE}, GATE = open.

Note 4: Minimum duration of GATE pulldown following a circuit-breaker fault. The circuit breaker can be reset during this time by toggling UV low, but the GATE pulldown does not release until t_{OFF} has elapsed.

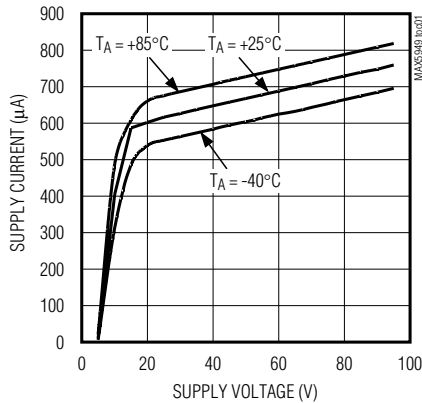
Note 5: Limits are 100% tested at T_A = +25°C and +85°C. Limits at -40°C are guaranteed by design.

-48V Hot-Swap Controllers with External RSENSE

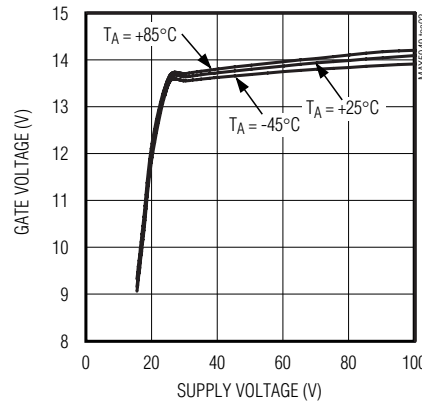
Typical Operating Characteristics

($V_{DD} = 48V$, $V_{EE} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

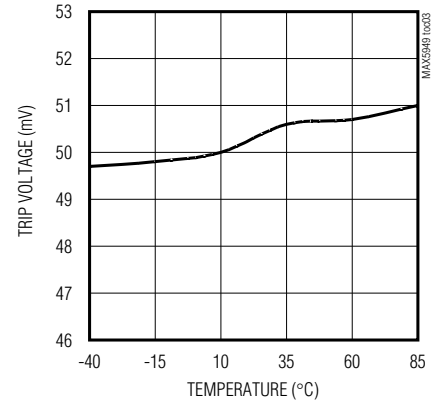
SUPPLY CURRENT vs. SUPPLY VOLTAGE



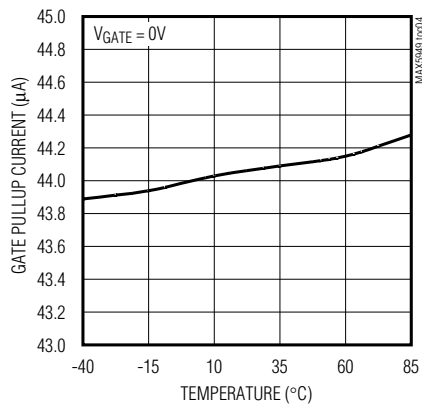
GATE VOLTAGE vs. SUPPLY VOLTAGE



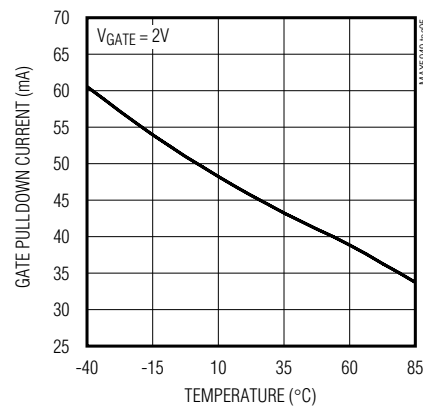
CURRENT-LIMIT TRIP VOLTAGE vs. TEMPERATURE



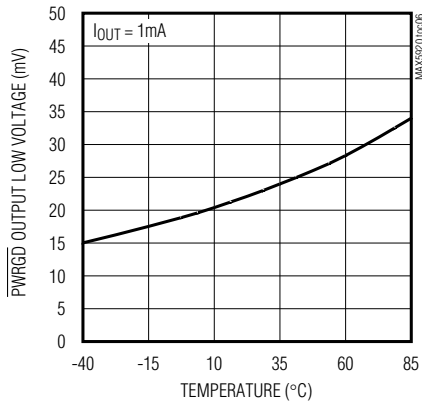
GATE PULLUP CURRENT vs. TEMPERATURE



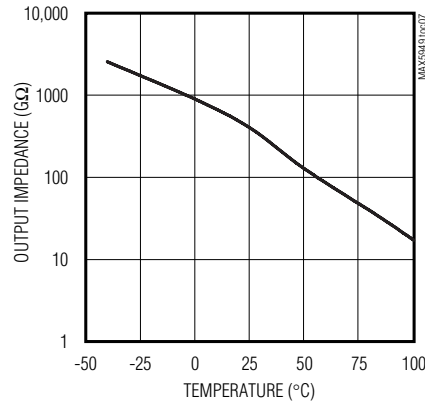
GATE PULLDOWN CURRENT vs. TEMPERATURE



PWRGD OUTPUT LOW VOLTAGE vs. TEMPERATURE (MAX5949A)



PWRGD OUTPUT IMPEDANCE vs. TEMPERATURE (MAX5949B)



-48V Hot-Swap Controllers with External RSENSE

Test Circuits

MAX5949A/MAX5949B

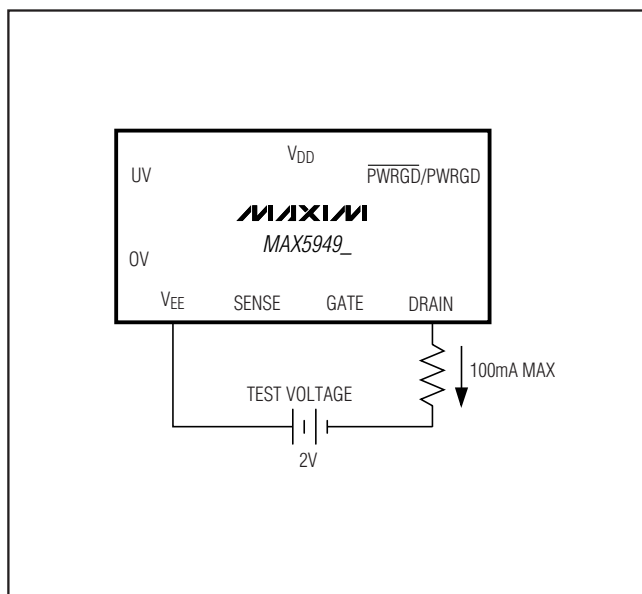


Figure 1. -2V DRAIN Voltage Test Circuit

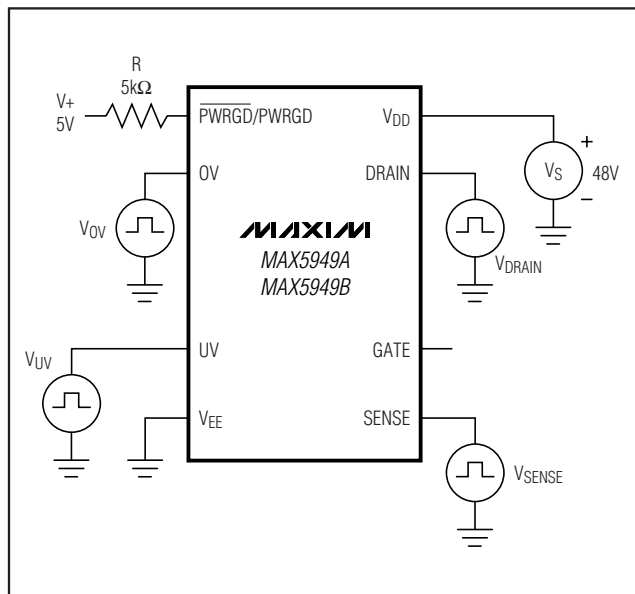


Figure 2a. Test Circuit 1

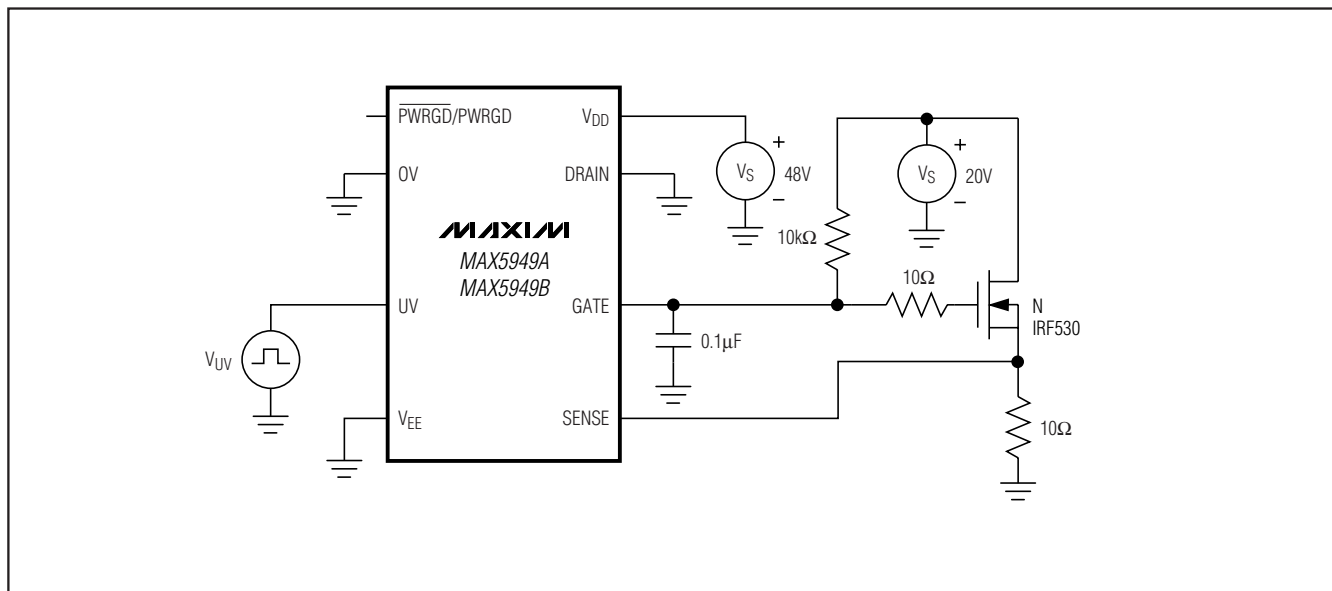


Figure 2b. Test Circuit 2

-48V Hot-Swap Controllers with External RSENSE

Timing Diagrams

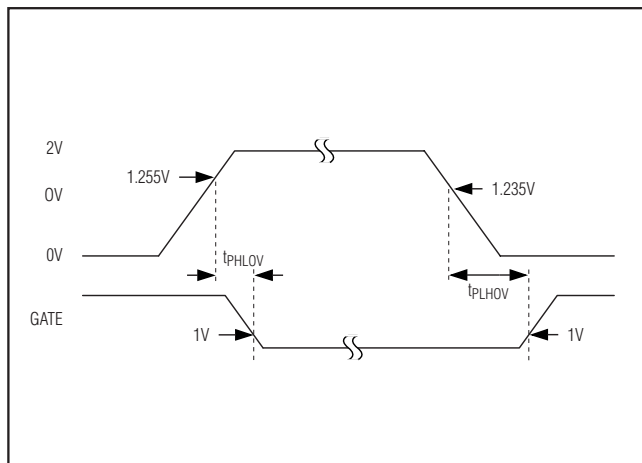


Figure 3. OV to GATE Timing

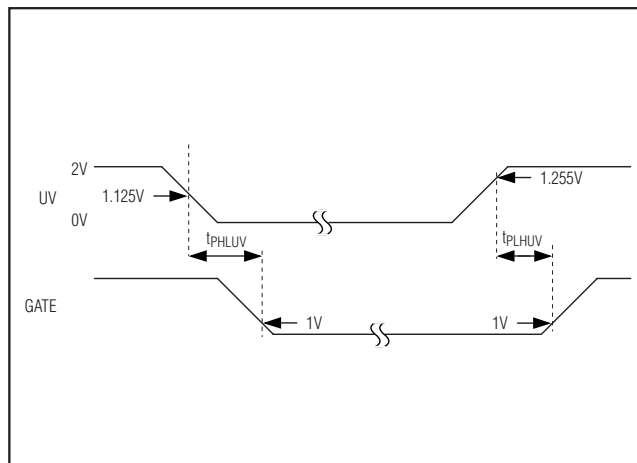


Figure 4. UV to GATE Timing

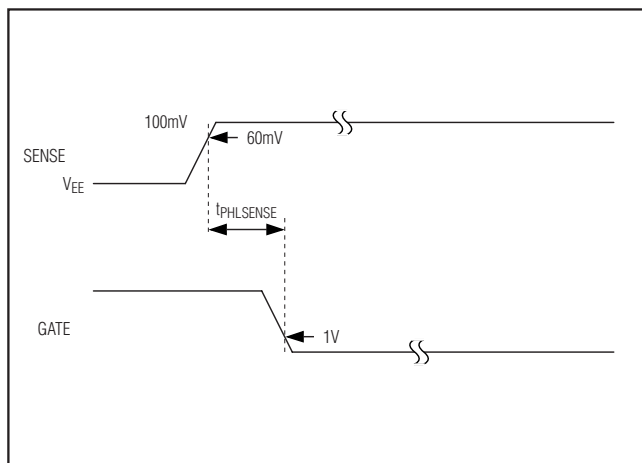


Figure 5a. SENSE to GATE Timing

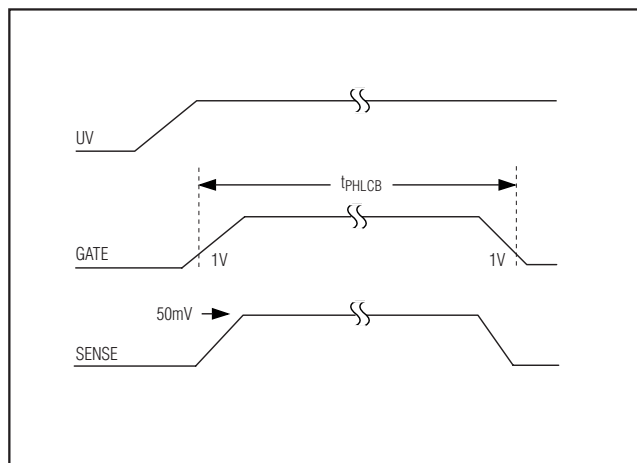


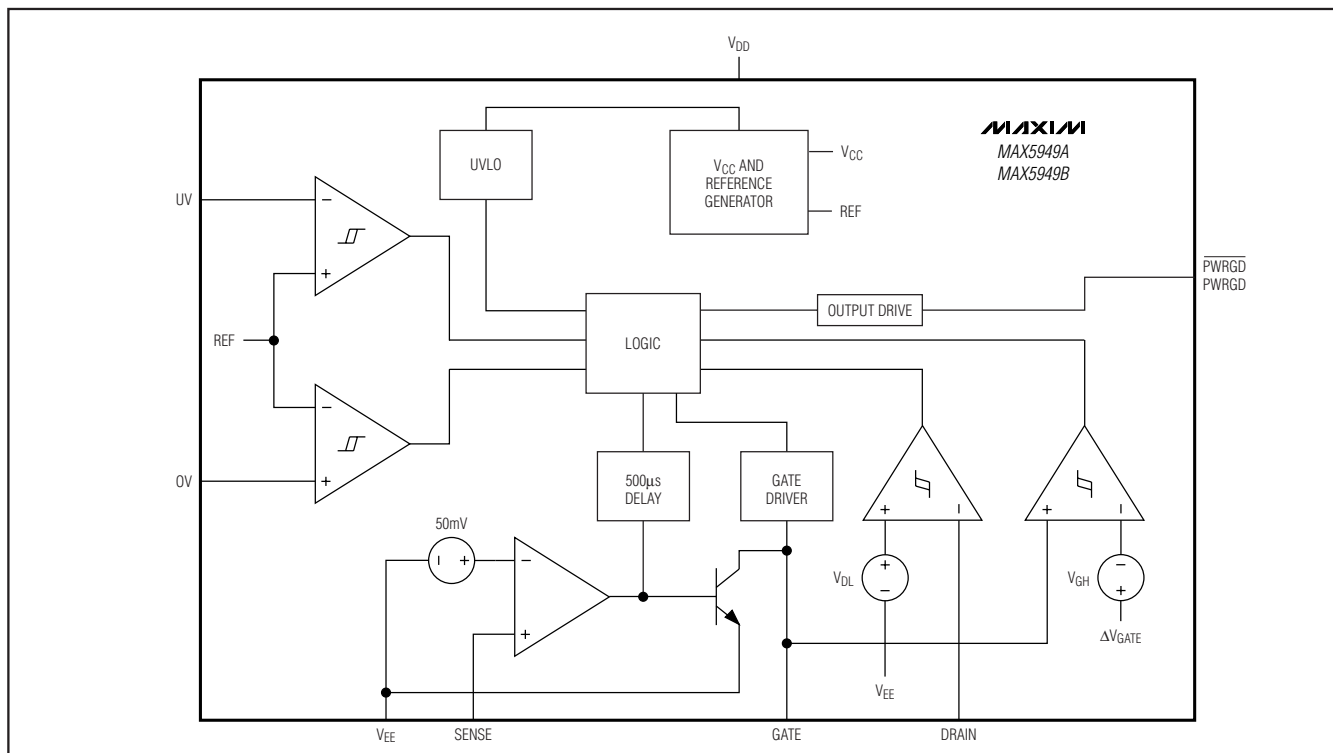
Figure 5b. Active Current-Limit Threshold

MAX5949A/MAX5949B

The diagram shows two timing scenarios for the PWRGD and DRAIN signals. In the top scenario, the DRAIN signal transitions from 1.4V to VEE while PWRGD is high. The time from the start of the DRAIN transition to the PWRGD falling edge is labeled t_{PHLDL} . In the bottom scenario, the DRAIN signal transitions from 1.4V to VEE while PWRGD is low. The time from the start of the DRAIN transition to the PWRGD rising edge is labeled t_{PHLDL} . Both scenarios show a 1V signal level for the PWRGD signal during the transition.

Timing diagram for PWRGD signal during a GATE signal transition. The diagram shows two scenarios: one where PWRGD goes low (top) and one where it goes high (bottom). In both, GATE transitions from low to high with a 1.4V overshoot. t_{PHLGH} is the time from GATE rising to PWRGD changing state. V_{EE} and V_{DD} are indicated as reference levels.

Block Diagram



-48V Hot-Swap Controllers with External RSENSE

Pin Description

PIN		NAME	FUNCTION
MAX5949A	MAX5949B		
1	—	$\overline{\text{PWRGD}}$	Power-Good Signal Output. $\overline{\text{PWRGD}}$ is an active-low open-drain status output referenced to V_{EE} . $\overline{\text{PWRGD}}$ is latched low when $V_{\text{DRAIN}} - V_{EE} \leq V_{\text{DL}}$ and $V_{\text{GATE}} > (\Delta V_{\text{GATE}} - V_{\text{GH}})$, indicating a power-good condition. $\overline{\text{PWRGD}}$ is open drain otherwise.
—	1	PWRGD	Power-Good Signal Output. PWRGD is an active-high open-drain status output referenced to DRAIN. PWRGD latches in a high-impedance state when $V_{\text{DRAIN}} - V_{EE} \leq V_{\text{DL}}$ and $V_{\text{GATE}} > (\Delta V_{\text{GATE}} - V_{\text{GH}})$, indicating a power-good condition. PWRGD is pulled low to DRAIN otherwise.
2	2	OV	Input Pin for Overvoltage Detection. OV is referenced to V_{EE} . When OV is pulled above the V_{OVH} voltage, the GATE pin is immediately pulled low. The GATE pin remains low until the OV pin voltage reduces to V_{OVL} .
3	3	UV	Input Pin for Undervoltage Detection. UV is referenced to V_{EE} . When UV is pulled above the V_{UVH} voltage, the GATE is enabled. When UV is pulled below V_{OVL} , GATE is pulled low. UV is also used to reset the circuit breaker after a fault condition. To reset the circuit breaker, pull UV below V_{OVL} . The reset command can be issued immediately after a fault condition; however, the device does not restart until a t_{OFF} delay time has elapsed after the fault.
4	4	V_{EE}	Device Negative Power-Supply Input. Connect to the negative power-supply rail.
5	5	SENSE	Current-Sense Voltage Input. Connect to an external sense resistor and the external MOSFET source. The voltage drop across the external sense resistor is monitored to detect overcurrent or short-circuit fault conditions. Connect SENSE to V_{EE} to disable the current-limiting feature.
6	6	GATE	Gate-Drive Output. Connect to the gate of the external n-channel MOSFET.
7	7	DRAIN	Output-Voltage Sense Input. Connect to the output-voltage node (drain of the external n-channel MOSFET).
8	8	V_{DD}	Positive Power-Supply Rail Input. This is the power ground in the negative-supply voltage system. Connect to the higher potential of the power-supply inputs.

Detailed Description

The MAX5949A/MAX5949B are integrated hot-swap controllers for -48V power systems. They allow circuit boards to be safely hot plugged into a live backplane without causing a glitch on the power-supply rail. When circuit boards are inserted into a live backplane without hot-swap control, the bypass capacitors at the input of the board's power module or switching power supply can draw large inrush currents as they charge. The inrush currents can cause glitches on the system power-supply rail and damage components on the board.

The MAX5949A/MAX5949B provide a controlled turn-on to circuit cards, preventing glitches on the power-supply rail and damage to board connectors and components. Both the MAX5949A and MAX5949B provide undervoltage, overvoltage, and overcurrent protection. The MAX5949A/MAX5949B ensure the input voltage is stable and within tolerance before applying power to the load. The devices also provide protection against input voltage steps. During an input voltage step, the MAX5949A/MAX5949B limit the current drawn by the load to a safe level without turning off power to the load.

MAX5949A/MAX5949B

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-48V Hot-Swap Controllers with External RSENSE

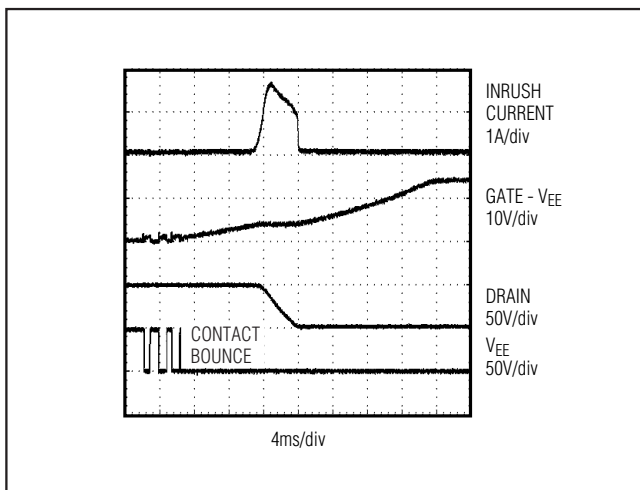


Figure 7b. Input Inrush Current

In either case, when the MOSFET is turned off, the output capacitor continues to discharge by the IC supply current, I_{DD} . The I_{DD} flows into the IC at the V_{DD} terminal, out at the V_{EE} terminal, and back to the capacitor through the external MOSFET's substrate diode. There is also a parallel current path between the V_{EE} and DRAIN terminals through multiple internal ESD-protection diodes. Protection circuits built into the IC allow the DRAIN terminal voltage to drop below that of the V_{EE} terminal so long as the allowed absolute-maximum DRAIN terminal current ($\sim 100\text{mA}$) is not exceeded. As I_{DD} is only 2mA maximum, this limiting current will not even be approached.

Current Limit and Electronic Circuit Breaker

The MAX5949_ provides current-limiting and circuit-breaker features that protect against excessive load current and short-circuit conditions. The load current is monitored by sensing the voltage across an external sense resistor connected between V_{EE} and SENSE.

If the voltage between V_{EE} and SENSE reaches the current-limit trip voltage (V_{CL}), the MAX5949_ pulls down the GATE pin and regulates the current through the external MOSFET so $V_{SENSE} - V_{EE} \leq V_{CL}$. If the current drawn by the load drops below V_{CL} / R_{SENSE} limit, the GATE pin voltage rises again. However, if the load current is at the regulation limit of V_{CL} / R_{SENSE} for a period of t_{PHLCB} , the electronic circuit breaker trips, causing the MAX5949A/MAX5949B to turn off the external MOSFET.

After an overcurrent fault condition, the circuit breaker is reset by pulling the UV pin low and then pulling UV high or by cycling power to the MAX5949A/MAX5949B. Unless power is cycled to the MAX5949A/MAX5949B,

the device waits until t_{OFF} has elapsed before turning on the gate of the external FET.

Overcurrent Fault Integrator

The MAX5949_ features an overcurrent fault integrator. When an overcurrent condition exists, an internal digital counter increments its count. When the counter reaches 500 μs (the maximum current-limit duration) for the MAX5949_, an overcurrent fault is generated. If the overcurrent fault does not last 500 μs , then the counter begins decrementing at a rate 128 (maximum current-limit duty cycle) times slower than the counter was incrementing. Repeated overcurrent conditions will generate a fault if duty cycle of the overcurrent condition is greater than 1/128.

Load-Current Regulation

The MAX5949_ accomplishes load-current regulation by pulling current from the GATE pin whenever $V_{SENSE} - V_{EE} > V_{CL}$ (see the *Typical Operating Characteristics*). This decreases the gate-to-source voltage of the external MOSFET, thereby reducing the load current. When $V_{SENSE} - V_{EE} < V_{CL}$, the MAX5949A/MAX5949B pull the GATE pin high by a 45 μA (I_{PU}) current.

Driving into a Shorted Load

In the event of a permanent short-circuit condition, the MAX5949_ limits the current drawn by the load to V_{CL} / R_{SENSE} for a period of t_{PHLCB} , after which the circuit breaker trips. Once the circuit breaker trips, the GATE of the external FET is pulled low by 50mA (I_{PD}) turning off power to the load.

Immunity to Input Voltage Steps

The MAX5949_ guards against input voltage steps on the input supply. A rapid increase in the input supply voltage ($V_{DD} - V_{EE}$ increasing) causes a current step equal to $I = C_L \times \Delta V_{IN} / \Delta T$. If the load current exceeds V_{CL} / R_{SENSE} during an input voltage step, the MAX5949A/MAX5949B current limit activates, pulling down the gate voltage and limiting the load current to V_{CL} / R_{SENSE} . The DRAIN voltage (V_{DRAIN}) then slews at a slower rate than the input voltage. As the drain voltage starts to slew down, the drain-to-gate feedback capacitor C_2 pushes back on the gate, reducing the gate-to-source voltage (V_{GS}) and the current through the external MOSFET. Once the input supply reaches its final value, the DRAIN slew rate (and therefore the inrush current) is limited by the capacitor C_2 just as it is limited in the startup condition. To ensure correct operation, R_{SENSE} must be chosen to provide a current limit larger than the sum of the load current and the dynamic current into the load capacitance in the slewing mode.

If the load current plus the capacitive charging current is

-48V Hot-Swap Controllers with External RSENSE

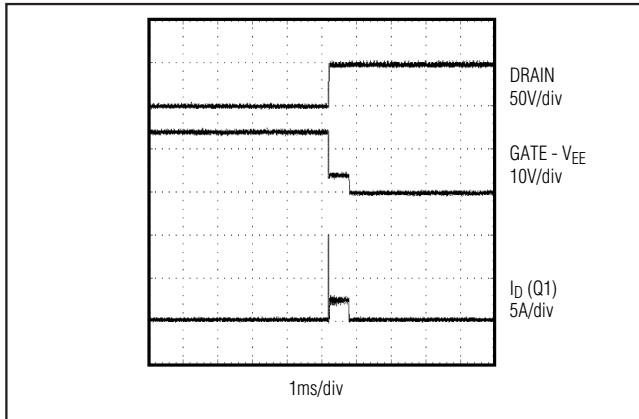


Figure 8. Short-Circuit Protection Waveform

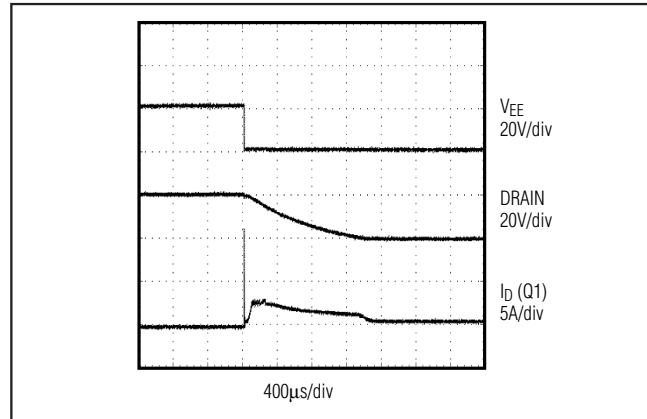


Figure 9. Voltage Step on Input Supply

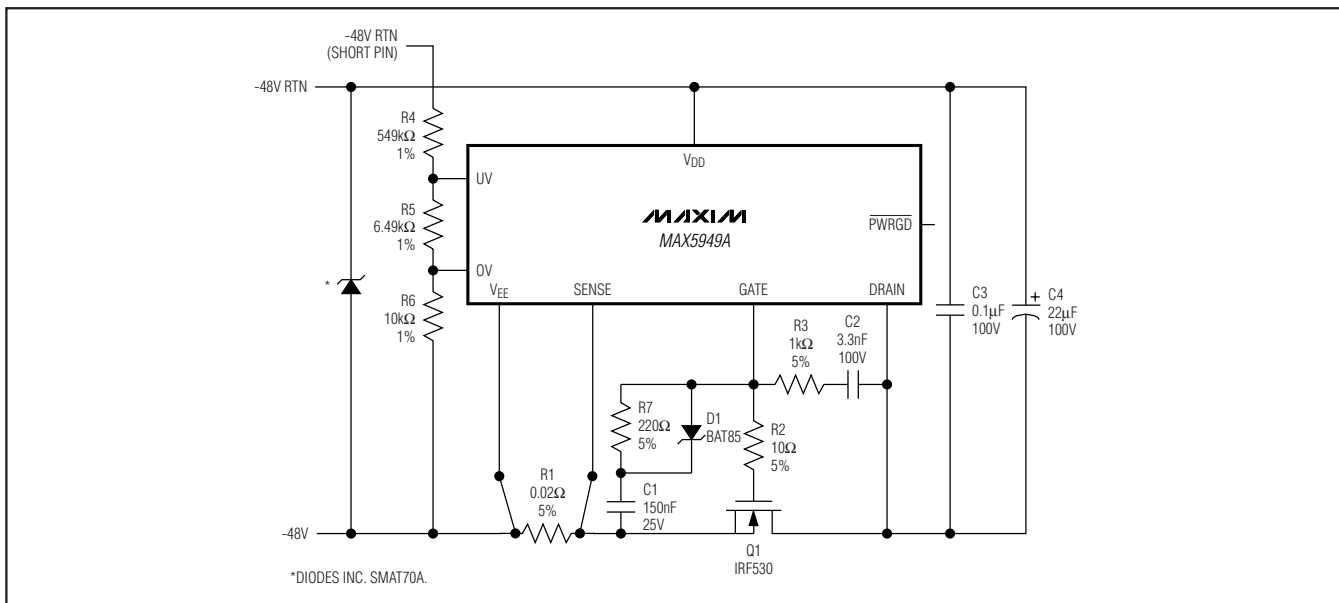


Figure 10. Circuit for Input Steps with Small C1

below the current limit, the circuit breaker does not trip.

For C2 values less than 10nF, a positive voltage step on the input supply can result in Q1 turning off momentarily, which can shut down the output. By adding an additional resistor and diode, Q1 remains on during the voltage step. This is shown as D1 and R7 in Figure 10. The purpose of D1 is to shunt current around R7 when the power pins first make contact and allow C1 to hold the GATE low. The value of R7 should be sized to generate an $R7 \times C1$ time constant of 33μs.

Undervoltage and Overvoltage Protection

The UV and OV pins can be used to detect undervoltage and overvoltage conditions. The UV and OV pins are internally connected to analog comparators with 130mV (UV) and 20mV (OV) of hysteresis. When the UV voltage falls below its threshold or the OV voltage rises above its threshold, the GATE pin is immediately pulled low. The GATE pin is held low until UV goes high and OV is low, indicating that the input supply voltage is within specification. The MAX5949_ includes an internal lockout (UVLO) that keeps the external MOSFET off until the input supply voltage exceeds 15.4V, regardless of the UV input.

-48V Hot-Swap Controllers with External RSENSE

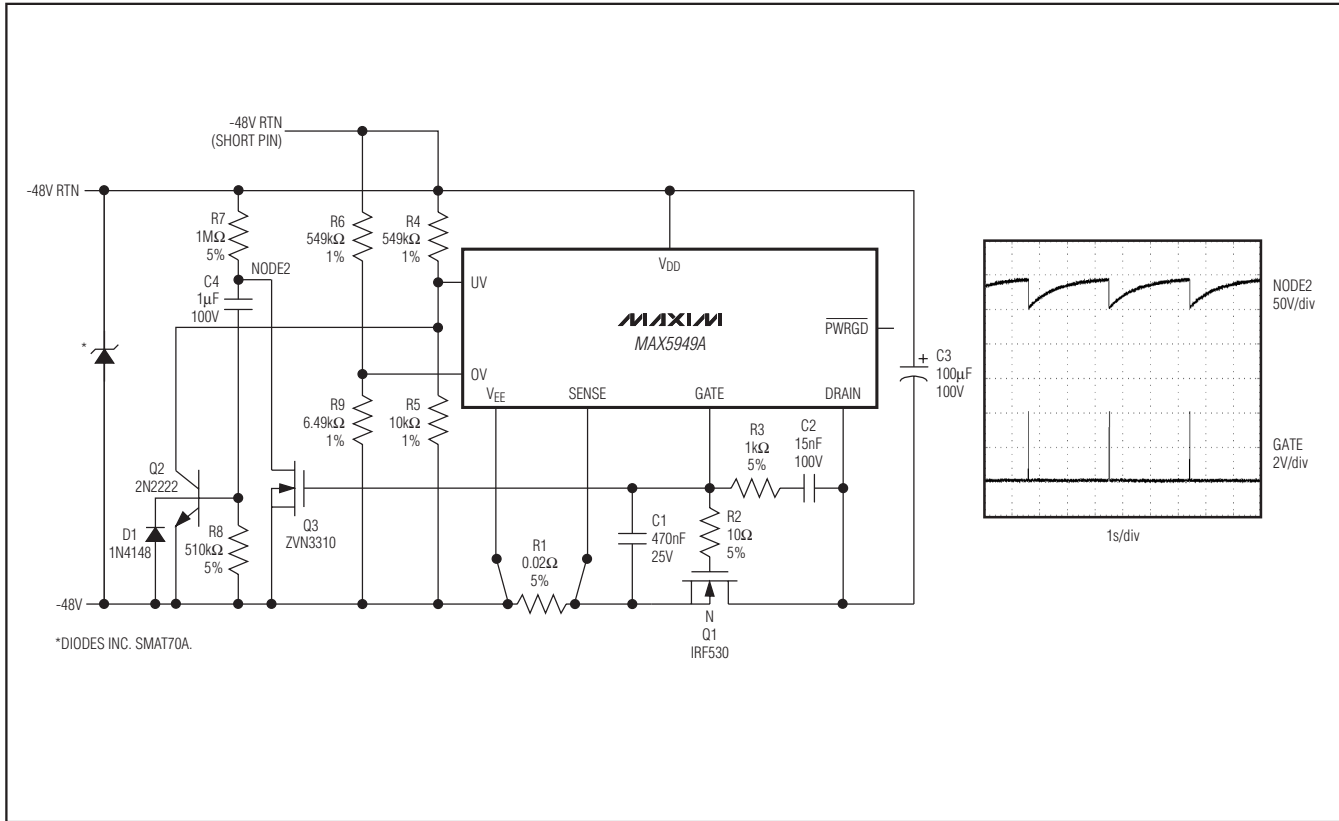


Figure 11. Automatic Restart After Current Fault

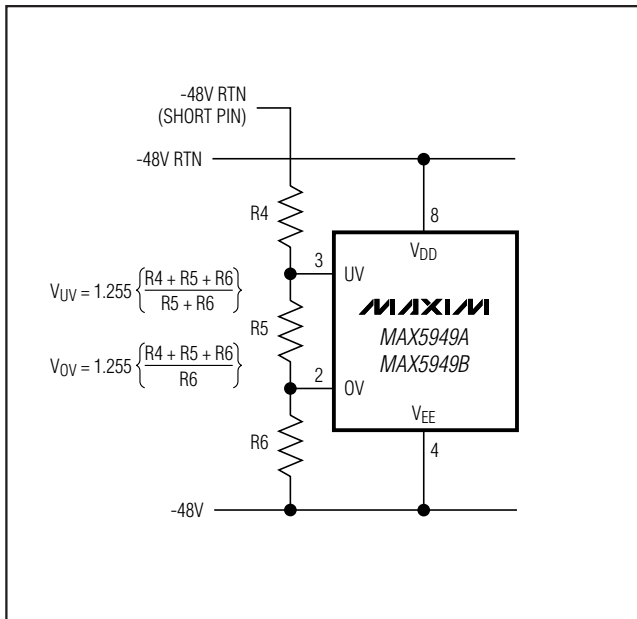


Figure 12. Undervoltage and Overvoltage Sensing

The UV pin is also used to reset the circuit breaker after a fault condition has occurred. The UV pin can be pulled below V_{UVL} to reset the circuit breaker.

Figure 12 shows how to program the undervoltage and overvoltage trip thresholds using three resistors. With $R4 = 549k\Omega$, $R5 = 6.49k\Omega$, and $R6 = 10k\Omega$, the undervoltage threshold is set to 38.5V (with a 43V release from undervoltage), and the overvoltage is set to 71V. The resistor-divider also increases the hysteresis of the overvoltage and overvoltage lockout, to 4.5V and 1.1V at the input supply, respectively.

PWRGD/PWRGD Output

The $\overline{PWRGD}$ (PWRGD) output can be used directly to enable a power module after hot insertion. The MAX5949A (PWRGD) can be used to enable modules with an active-low enable input (Figure 14), while the MAX5949B (PWRGD) is used to enable modules with an active-high enable input (Figure 13).

The PWRGD signal is referenced to the DRAIN terminal, which is the negative supply of the power module. The $\overline{PWRGD}$ signal is referenced to VEE.

-48V Hot-Swap Controllers with External RSENSE

MAX5949A/MAX5949B

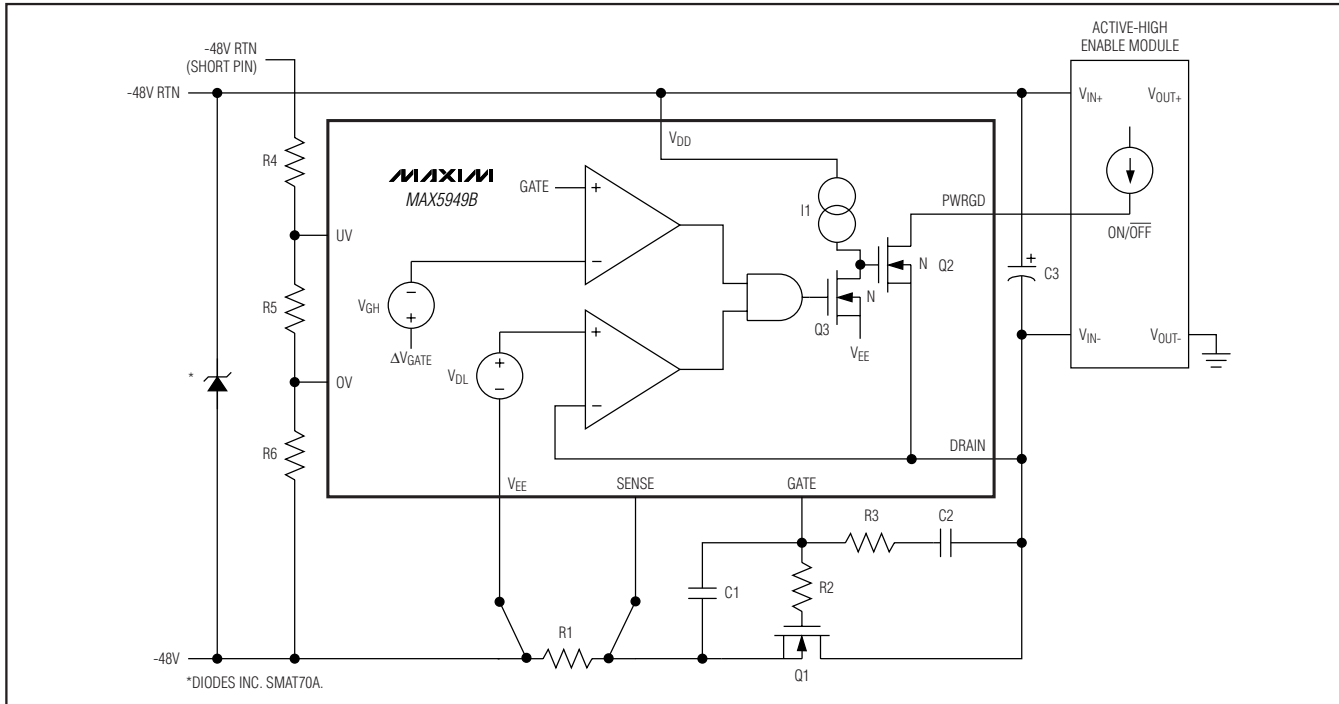


Figure 13. Active-High Enable Module

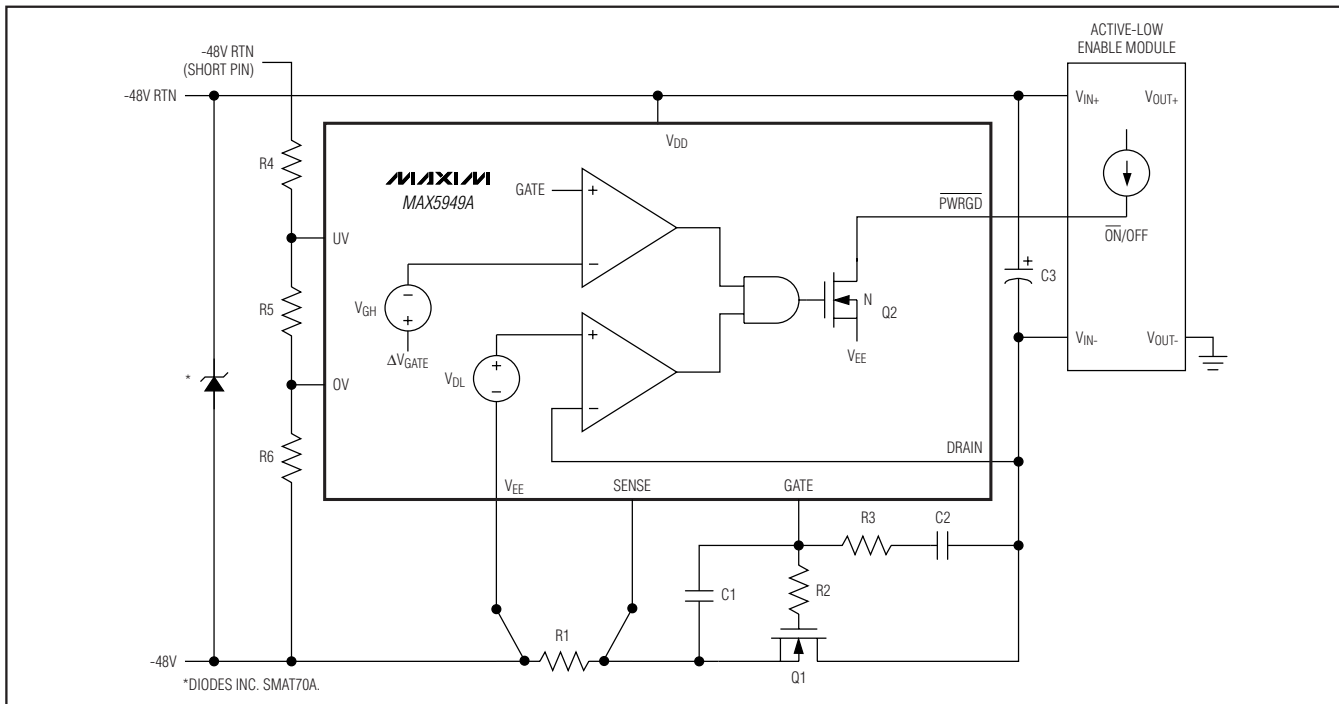


Figure 14. Active-Low Enable Module

-48V Hot-Swap Controllers with External RSENSE

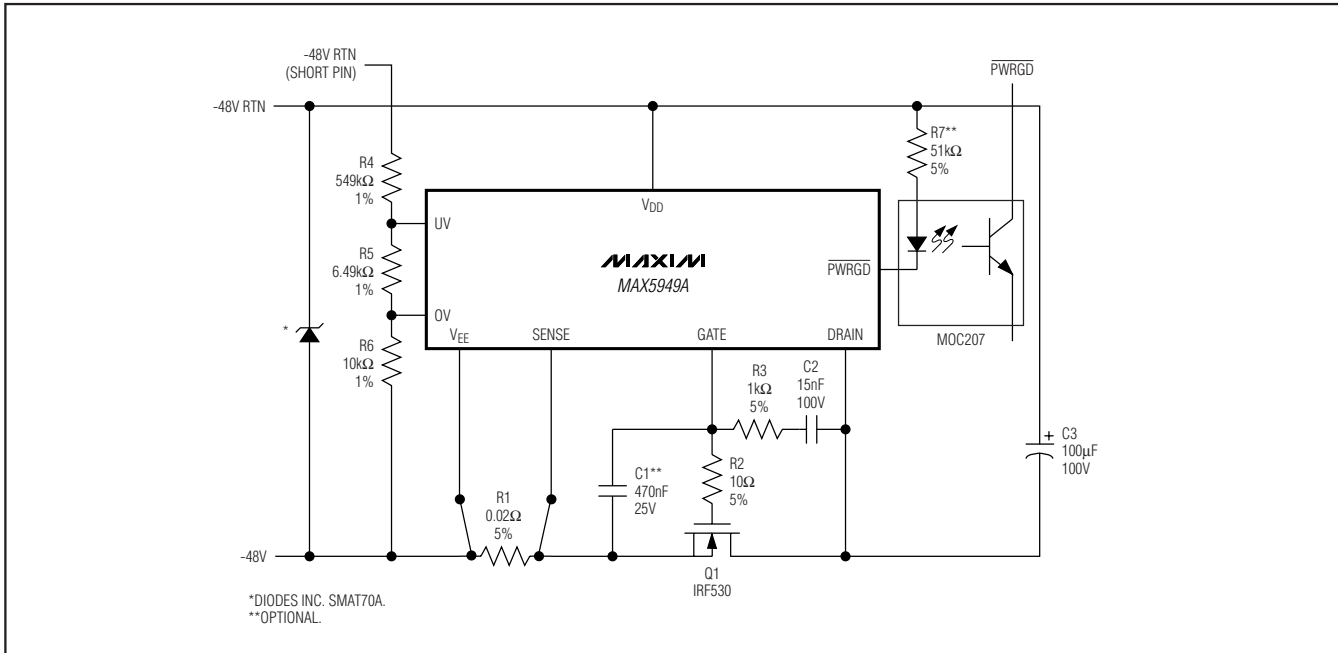


Figure 15. Using $\overline{\text{PWRGD}}$ to Drive an Optoisolator

When the DRAIN voltage of the MAX5949A is high with respect to V_{EE} or the GATE voltage is low, the internal pulldown MOSFET Q2 is off and the $\overline{\text{PWRGD}}$ pin is in a high-impedance state (Figure 14). The $\overline{\text{PWRGD}}$ pin is pulled high by the module's internal pullup current source, turning the module off. When the DRAIN voltage drops below V_{DL} and the GATE voltage is greater than $\Delta V_{\text{GATE}} - V_{GH}$, Q2 turns on and the $\overline{\text{PWRGD}}$ pin pulls low, enabling the module.

The $\overline{\text{PWRGD}}$ signal can also be used to turn on an LED or optoisolator to indicate that the power is good (Figure 15) (see the *Component Selection Procedure* section).

When the DRAIN voltage of the MAX5949B is high with respect to V_{EE} (Figure 13) or the GATE voltage is low, the internal MOSFET Q3 is turned off so that I1 and the internal MOSFET Q2 clamp the $\overline{\text{PWRGD}}$ pin to the DRAIN pin. MOSFET Q2 sinks the module's pullup current, and the module turns off.

When the DRAIN voltage drops below V_{DL} and the GATE voltage is greater than $\Delta V_{\text{GATE}} - V_{GH}$, MOSFET Q3 turns on, shorting I1 to V_{EE} and turning Q2 off. The pullup current in the module pulls the $\overline{\text{PWRGD}}$ pin high, enabling the module.

GATE Pin Voltage Regulation

The GATE pin goes high when the following startup conditions are met: the UV pin is high, the OV pin is low, the supply voltage is above V_{UVLOH} , and $(V_{\text{SENSE}} - V_{EE})$ is less than 50mV. The gate is pulled up with a 45μA current source and is regulated at 13.5V above V_{EE} . The MAX5949A/MAX5949B include an internal clamp that ensures the GATE voltage of the external MOSFET never exceeds 18V. During a fast-rising V_{DD} , the clamp also keeps the GATE and SENSE potentials as close as possible to prevent the FET from accidentally turning on. When a fault condition is detected, the GATE pin is pulled low with a 50mA current.

Applications Information

Sense Resistor

The circuit-breaker current-limit threshold is set to 50mV (typically). Select a sense resistor that causes a drop equal to or above the current-limit threshold at a current level above the maximum normal operating current. Typically, set the overload current to 1.5 to 2.0 times the nominal load current plus the load-capacitance charging current during startup. Choose the sense-resistor power rating to be greater than $(V_{CL})^2 / R_{\text{SENSE}}$.

-48V Hot-Swap Controllers with External RSENSE

Component Selection Procedure

- Determine load capacitance:
 $C_L = C_2 + C_3 + \text{module input capacitance}$
- Determine load current, I_{LOAD} .
- Select circuit-breaker current; for example:

$$I_{CB} = 2 \times I_{LOAD}$$

- Calculate RSENSE:

$$R_{SENSE} = \frac{50\text{mV}}{I_{CB}}$$

Realize that I_{CB} varies $\pm 20\%$ due to trip-voltage tolerance.

- Set allowable inrush current:

$$I_{INRUSH} \leq 0.8 \times \frac{40\text{mV}}{R_{SENSE}} - I_{LOAD} \text{ or}$$

$$I_{INRUSH} + I_{LOAD} \leq 0.8 \times I_{CB(MIN)}$$

- Determine value of C2:

$$C_2 = \frac{45\mu\text{A} \times C_L}{I_{INRUSH}}$$

- Calculate value of C1:

$$C_1 = (C_2 + C_{gd}) \times \left(\frac{V_{IN(MAX)} - V_{GS(TH)}}{V_{GS(TH)}} \right)$$

- Determine value of R3:

$$R_3 \leq \frac{150\mu\text{s}}{C_2} \text{ (typically } 1\text{k}\Omega\text{)}$$

- Set $R_2 = 10\Omega$.
- If an optocoupler is utilized as in Figure 15, determine the LED series resistor:

$$R_7 = \frac{V_{IN(NOMINAL)} - 2\text{V}}{3\text{mA} \leq I_{LED} \leq 5\text{mA}}$$

Although the suggested optocoupler is not specified for operation below 5mA, its performance is adequate for 36V temporary low-line voltage where LED current would then be $\approx 2.2\text{mA}$ to 3.7mA . If R_7 is set as high as $51\text{k}\Omega$, optocoupler operation should be verified over

the expected temperature and input voltage range to ensure suitable operation when LED current $\approx 0.9\text{mA}$ for 48V input and $\approx 0.7\text{mA}$ for 36V input.

If input transients are expected to momentarily raise the input voltage to $>100\text{V}$, select an input transient-voltage-suppression diode (TVS) to limit maximum voltage on the MAX5949 to less than 100V. A suitable device is the Diodes Inc. SMAT70A telecom-specific TVS.

Select Q1 to meet supply voltage, load current, efficiency, and Q1 package power-dissipation requirements:

$$BV_{DSS} \geq 100\text{V}$$

$$I_{D(ON)} \geq 3 \times I_{LOAD}$$

$$\text{DPAK, D}^2\text{PAK, or TO-220AB}$$

The lowest practical $R_{DS(ON)}$, within budget constraints and with values from $14\text{m}\Omega$ to $540\text{m}\Omega$, are available at 100V breakdown.

Ensure that the temperature rise of Q1 junction is not excessive at normal load current for the package selected. Ensure that I_{CB} current during voltage transients does not exceed allowable transient-safe operating-area limitations. This is determined from the SOA and transient-thermal-resistance curves in the Q1 manufacturer's data sheet.

Example 1:

$I_{LOAD} = 2.5\text{A}$, efficiency = 98%, then $V_{DS} = 0.96\text{V}$ is acceptable, or $R_{DS(ON)} \leq 384\text{m}\Omega$ at operating temperature is acceptable. An IRL520NS 100V NMOS with $R_{DS(ON)} \leq 180\text{m}\Omega$ and $I_{D(ON)} = 10\text{A}$ is available in D²PAK. (A Vishay Siliconix SUD40N10-25 100V NMOS with $R_{DS(ON)} \leq 25\text{m}\Omega$ and $I_{D(ON)} = 40\text{A}$ is available in DPAK, but may be more costly because of a larger die size.)

Using the IRL520NS, $V_{DS} \leq 0.625\text{V}$ even at $+80^\circ\text{C}$ so efficiency $\geq 98.6\%$ at 80°C . $P_D \leq 1.56\text{W}$ and junction temperature rise above case temperature would be 5°C due to the package $\theta_{JC} = 3.1^\circ\text{C/W}$ thermal resistance. Of course, using the SUD40N10-25 would yield an efficiency greater than 99.8% to compensate for the increased cost.

-48V Hot-Swap Controllers with External RSENSE

If I_{CB} is set to twice I_{LOAD}, or 5A, V_{DS} momentarily doubles to ≤1.25V. If C_{OUT} = 4000μF, transient-line input voltage is Δ36V, and the 5A charging-current pulse is:

$$t = \frac{4000\mu\text{F} \times 1.25\text{V}}{5\text{A}} = 1\text{ms}$$

Entering the data sheet transient-thermal-resistance curves at 1ms provides a θ_{JC} = 0.9°C/W. P_D = 6.25W, so Δt_{JC} = 5.6°C. Clearly, this is not a problem.

Example 2:

I_{LOAD} = 10A, efficiency = 98%, allowing V_{DS} = 0.96V but R_{DS(ON)} ≤ 96mΩ. An IRF530 in a D²PAK exhibits R_{DS(ON)} ≤ 90mΩ at +25°C and ≤ 135mΩ at +80°C. Power dissipation is 9.6W at +25°C or 14.4W at +80°C. Junction-to-case thermal resistance is 1.9W/°C, so the junction-temperature rise would be approximately 5°C above the +25°C case temperature. For higher efficiency, consider IRL540NS with R_{DS(ON)} ≤ 44mΩ. This allows η = 99%, P_D ≤ 4.4W, and T_{JC} = +4°C (θ_{JC} = 1.1°C/W) at +25°C.

Thermal calculations for the transient condition yield I_{CB} = 20A, V_{DS} = 1.8V, t = 0.5ms, transient θ_{JC} = 0.12°C/W, P_D = 36W and Δt_{JC} = 4.3°C.

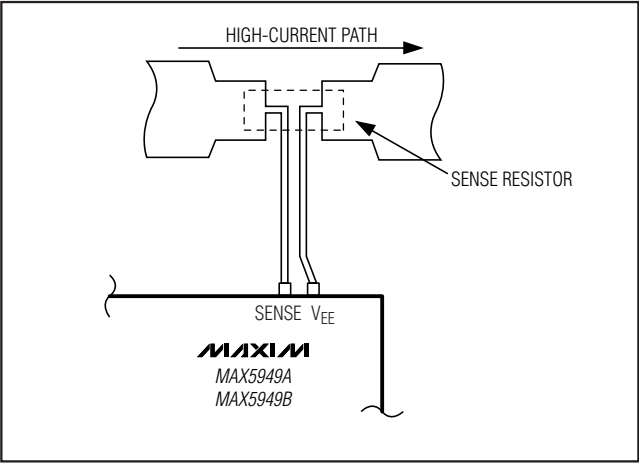


Figure 16. Recommended Layout for Kelvin-Sensing Current Through Sense Resistor

Selector Guide

PART	PWRGD POLARITY	FAULT MANAGEMENT
MAX5949AESA	Active low ($\overline{\text{PWRGD}}$)	Latched
MAX5949BESA	Active high (PWRGD)	Latched

MAX5949A/MAX5949B

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO
8 SO	S8+5	21-0041	90-0096

-48V Hot-Swap Controllers with External RSENSE

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/04	Initial release	—
1	8/11	Updated the <i>Electrical Characteristics</i> and Figure 11.	3, 12

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