50Ω, Dual SPST Analog Switches in UCSP

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V+ .....-0.3V to +12V
IN_, COM_, NO_, NC_ (Note 1).....-0.3V to (V+ + 0.3V)
Continuous Current (any pin) .....±10mA
Peak Current (any pin, pulsed at 1ms, 10% duty cycle)...±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.5mW/°C above +70°C).....362mW
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
9-Bump UCSP (derate 4.7mW/°C above +70°C).....379mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Bump Temperature (soldering, Note 2)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C

Note 1: Signals on IN_, NO_, NC_, or COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +2.7V, $I_{COM\_}$ = 5mA; $V_{NO\_}$ or $V_{NC\_}$ = +1.5V	+25°C		19	50	Ω
			T_{MIN} to T_{MAX}			60	
On-Resistance Matching Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = +2.7V, $I_{COM\_}$ = 5mA; $V_{NO\_}$ or $V_{NC\_}$ = +1.5V	+25°C		0.8	3.5	Ω
			T_{MIN} to T_{MAX}			4.5	
On-Resistance Flatness (Note 7)	$R_{FLAT(ON)}$	V+ = +2.7V, $I_{COM\_}$ = 5mA; $V_{NO\_}$ or $V_{NC\_}$ = +1V, +1.5V, +2V	+25°C		2.3	9	Ω
			T_{MIN} to T_{MAX}			11	
NO_ or NC_ Off-Leakage Current (Note 8)	$I_{NO\_(OFF)}$ $I_{NC\_(OFF)}$	V+ = +3.6V, $V_{COM\_}$ = +0.3V, +3V; $V_{NO\_}$ or $V_{NC\_}$ = +3V, +0.3V	+25°C	-0.1		+0.1	nA
			T_{MIN} to T_{MAX}	-2		+2	
COM_ Off-Leakage Current (Note 8)	$I_{COM\_(OFF)}$	V+ = +3.6V, $V_{COM\_}$ = +0.3V, +3V; $V_{NO\_}$ or $V_{NC\_}$ = +3V, +0.3V	+25°C	-0.1		+0.1	nA
			T_{MIN} to T_{MAX}	-2		+2	
COM_ On-Leakage Current (Note 8)	$I_{COM\_(ON)}$	V+ = +3.6V, $V_{COM\_}$ = +0.3V, +3.0V; $V_{NO\_}$ or $V_{NC\_}$ = +0.3V, +3V, or floating	+25°C	-0.2		+0.2	nA
			T_{MIN} to T_{MAX}	-4		+4	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		70	150	ns
			T_{MIN} to T_{MAX}			170	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		30	60	ns
			T_{MIN} to T_{MAX}			70	
Break-Before-Make (MAX4733 Only, Note 8)	t_{BBM}	$V_{NO\_}$ or $V_{NC\_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 3	+25°C		40		ns
			T_{MIN} to T_{MAX}	1			
Charge Injection	Q	V_{GEN} = 0V, R_{GEN} = 0, C_L = 1.0nF, Figure 4	+25°C		7.5		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out	+25°C		300		MHz
Off-Isolation (Note 9)	V_{ISO}	f = 1MHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		-72		dB
Crosstalk (Note 10)	V_{CT}	f = 1MHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF, Figure 6	+25°C		-108		dB
NO_ or NC_ Off-Capacitance	C_{OFF}	f = 1MHz, Figure 7	+25°C		20		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	f = 1MHz, Figure 7	+25°C		20		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, Figure 7	+25°C		40		pF
LOGIC INPUT							
Input Logic High	V_{IH}			1.4			V
Input Logic Low	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	$V_{IN\_}$ = 0V or V+		-1	+0.005	+1	µA
SUPPLY							
Power-Supply Range	V+			2.0		11	V
Positive Supply Current	I+	V+ = +5.5V, $V_{IN\_}$ = 0V or V+, all switches on or off			0.0001	1	µA

50Ω, Dual SPST Analog Switches in UCSP

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +4.5V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +3.5V	+25°C		8.5	25	Ω
			T_{MIN} to T_{MAX}			30	
On-Resistance Matching Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = +4.5V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +3.5V	+25°C		0.2	3	Ω
			T_{MIN} to T_{MAX}			4	
On-Resistance Flatness (Note 7)	$R_{FLAT(ON)}$	V+ = +4.5V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +1V, +2V, +3V	+25°C		2	5	Ω
			T_{MIN} to T_{MAX}			7	
NO_ or NC_ Off-Leakage Current (Note 8)	$I_{NO\_(OFF)}$ $I_{NC\_(OFF)}$	V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V; $V_{NO\_}$ or $V_{NC\_}$ = +4.5V, +1V	+25°C	-0.1		+0.1	nA
			T_{MIN} to T_{MAX}	-2		+2	
COM_ Off-Leakage Current (Note 8)	$I_{COM\_(OFF)}$	V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V; $V_{NO\_}$ or $V_{NC\_}$ = +4.5V, +1V	+25°C	-0.1		+0.1	nA
			T_{MIN} to T_{MAX}	-2		+2	
COM_ On-Leakage Current (Note 8)	$I_{COM\_(ON)}$	V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V; $V_{NO\_}$ or $V_{NC\_}$ = +1V, +4.5V, or floating	+25°C	-0.2		+0.2	nA
			T_{MIN} to T_{MAX}	-4		+4	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = +3.0V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		47	85	ns
			T_{MIN} to T_{MAX}			95	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = +3.0V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		23	45	ns
			T_{MIN} to T_{MAX}			55	
Break-Before-Make (MAX4733 Only, Note 8)	t_{BBM}	$V_{NO\_}$ or $V_{NC\_}$ = +3.0V, R_L = 300Ω, C_L = 35pF, Figure 3	+25°C		25		ns
			T_{MIN} to T_{MAX}	1			
Charge Injection	Q	V_{GEN} = 0V, R_{GEN} = 0, C_L = 1.0nF, Figure 4	+25°C		7.5		pC
On-Channel Bandwidth	BW	Signal = 0dBm, 50Ω in and out	+25°C		300		MHz
Off-Isolation (Note 9)	V_{ISO}	f = 1MHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		-72		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Crosstalk (Note 10)	V_{CT}	f = 1MHz, $V_{COM\_}$ = 1V_{RMS}, R_L = 50Ω, C_L = 5pF, Figure 6	+25°C		-108		dB
NO_ or NC_ Off-Capacitance	C_{OFF}	f = 1MHz, Figure 7	+25°C		20		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	f = 1MHz, Figure 7	+25°C		20		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, Figure 7	+25°C		40		pF
LOGIC INPUT							
Input Logic High	V_{IH}			2.0			V
Input Logic Low	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	$V_{IN\_}$ = 0V or V+		-1	+0.005	+1	µA
SUPPLY							
Power-Supply Range	V+			2.0		11	V
Positive Supply Current	I+	V+ = +5.5V, $V_{IN\_}$ = 0V or V+, all switches on or off			0.0001	1	µA

Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 4: UCSP and TDFN parts are 100% tested at +25°C only, and guaranteed by design over temperature. µMAX parts are 100% tested at +85°C and +25°C and guaranteed by design over temperature.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: UCSP on-resistance matching between channels and on-resistance flatness guaranteed by design.

Note 7: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 8: Guaranteed by design.

Note 9: Off-Isolation = 20 $\log_{10}$ ($V_{NO\_}/V_{COM\_}$), $V_{NO\_}$ = output, $V_{COM\_}$ = input to off switch.

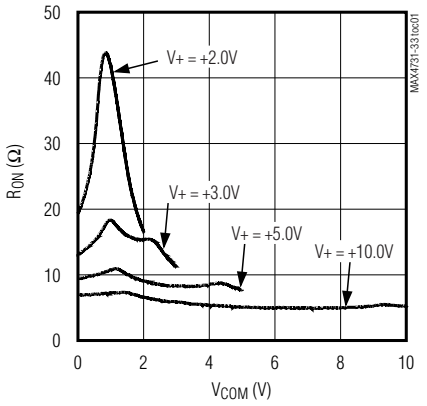
Note 10: Between any two switches.

50Ω, Dual SPST Analog Switches in UCSP

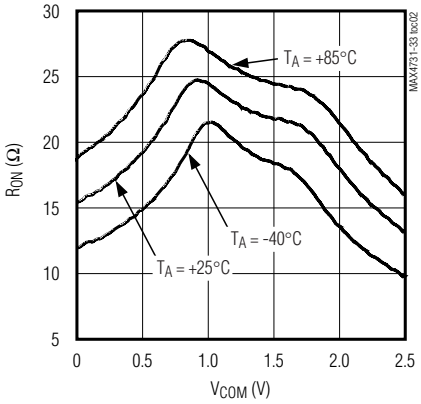
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

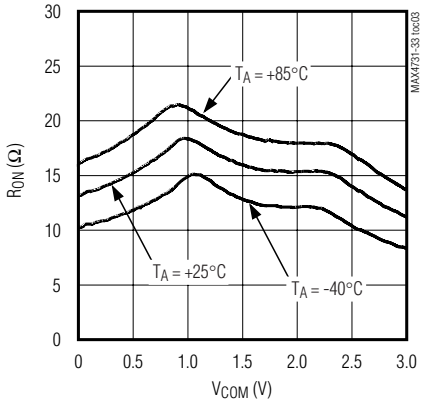
ON-RESISTANCE vs. V_{COM}



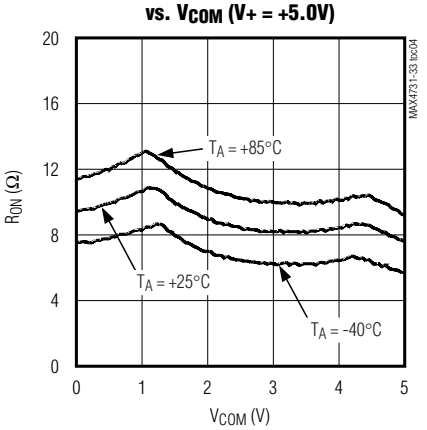
ON-RESISTANCE vs. V_{COM} (V+ = +2.5V)



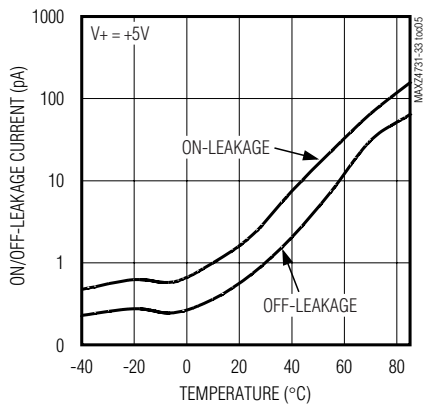
ON-RESISTANCE vs. V_{COM} (V+ = +3.0V)



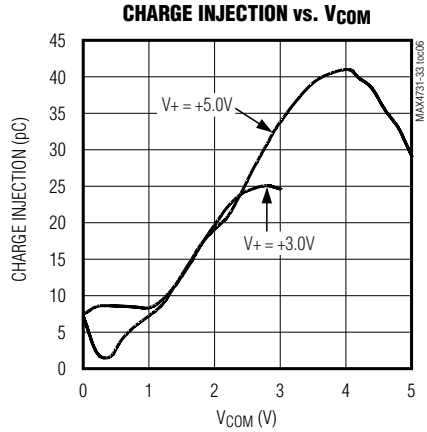
ON-RESISTANCE vs. V_{COM} (V+ = +5.0V)



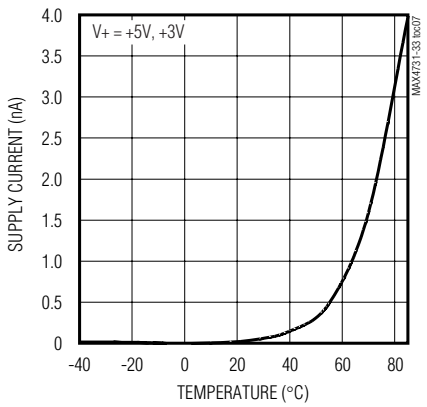
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



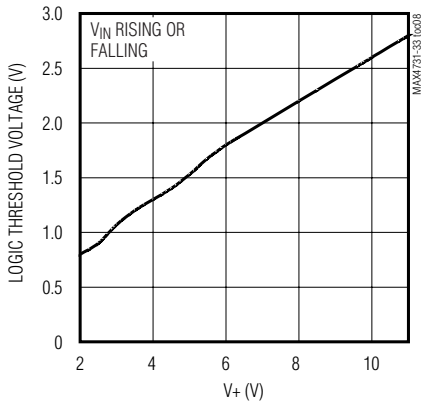
CHARGE INJECTION vs. V_{COM}



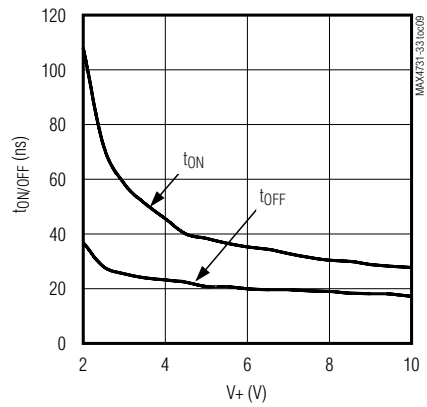
SUPPLY CURRENT vs. TEMPERATURE



LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



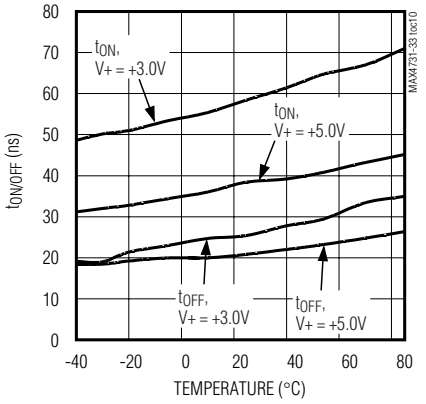
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



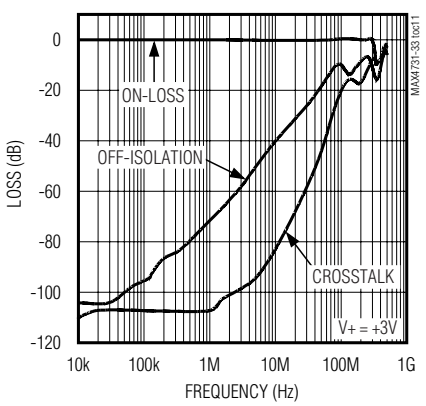
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

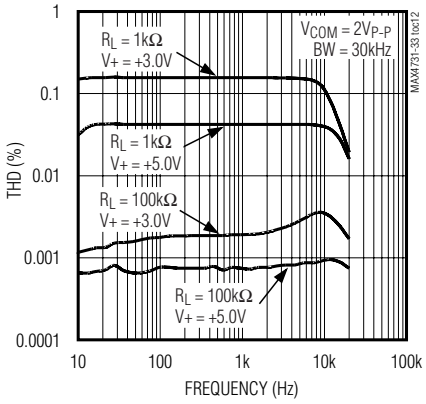
TURN-ON/OFF TIME vs. TEMPERATURE



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN						NAME	FUNCTION
MAX4731		MAX4732		MAX4733			
UCSP	µMAX/ TDFN	UCSP	µMAX/ TDFN	UCSP	µMAX/ TDFN		
A1	1	—	—	A1	1	NO1	Analog-Switch Normally Open Terminal
A2	2	A2	2	A2	2	COM1	Analog-Switch Common Terminal
A3	4	A3	4	A3	4	GND	Ground. Connect to digital ground.
B1	7	B1	7	B1	7	IN1	Logic-Control Digital Input
B3	3	B3	3	B3	3	IN2	Logic-Control Digital Input
C1	8	C1	8	C1	8	V+	Positive Supply Voltage Input
C2	6	C2	6	C2	6	COM2	Analog-Switch Common Terminal
C3	5	—	—	—	—	NO2	Analog-Switch Normally Open Terminal
—	—	A1	1	—	—	NC1	Analog-Switch Normally Closed Terminal
—	—	C3	5	C3	5	NC2	Analog-Switch Normally Closed Terminal
—	EP (TDFN only)	—	EP (TDFN only)	—	EP (TDFN only)	EP	Exposed Pad. Connect to V+.

Applications Information

Operating Considerations for High-Voltage Supply

The MAX4731/MAX4732/MAX4733 operate to +11V with some precautions. The absolute maximum rating for V+ is +12V (referenced to GND). When operating near this region, bypass V+ with a minimum 0.1µF capacitor to ground as close to the IC as possible.

Logic Levels

The MAX4731/MAX4732/MAX4733 are TTL compatible when powered from a single +5V supply. When powered from other supply voltages, the logic inputs should be driven rail-to-rail. For example, with a +11V supply, IN1 and IN2 should be driven low to 0V and high to 11V. With a +3.3V supply, IN1 and IN2 should be driven low to 0V and high to 3.3V. Driving IN1 and IN2 rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (GND to V+) pass with very little change in R_{ON} (see *Typical Operating Characteristics*). The bidirectional switches allow NO_, NC_, and COM_ connections to be used as either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

CAUTION: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings can cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to < 20mA, add a small-signal diode, D1, as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +11V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. The most significant shift occurs when using low supply voltages (+5V or less). With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

Protection diodes D1 and D2 also protect against some overvoltage situations. Using the circuit in Figure 1, no damage results if the supply voltage is below the absolute maximum rating (+12V) and if a fault voltage up to the absolute maximum rating (V+ + 0.3V) is applied to an analog signal terminal.

UCSP Applications Information

For the latest application details on USCP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile as well as the latest information on reliability testing results, go to the Maxim web site at www.maxim-ic.com/ucsp to find the Application Note: *UCSP—A Wafer-Level Chip-Scale Package*.

Test Circuits/Timing Diagrams

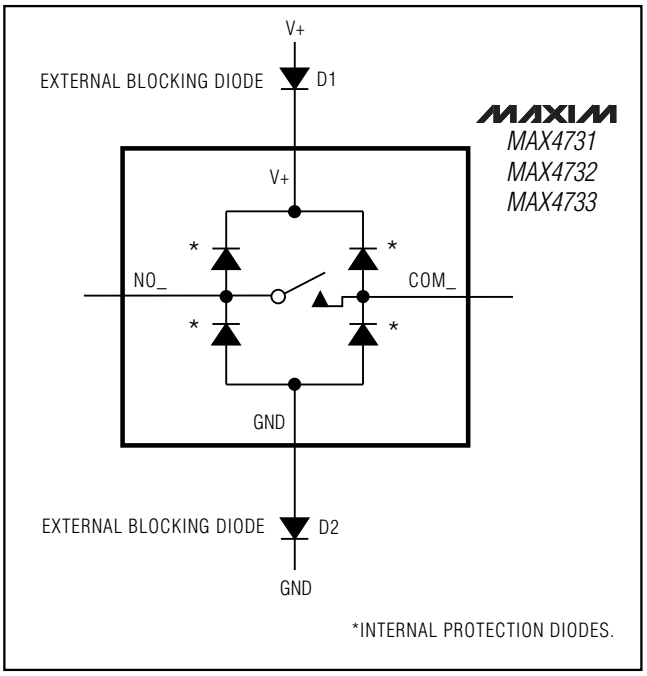


Figure 1. Overvoltage Protection Using External Blocking Diodes

Test Circuits/Timing Diagrams (continued)

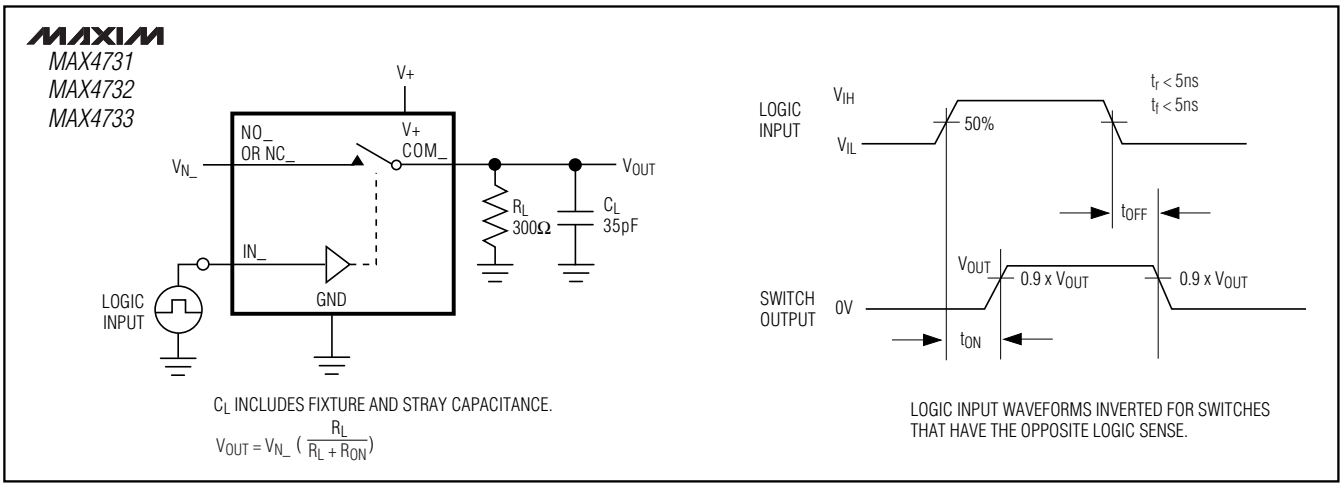


Figure 2. Switching Time

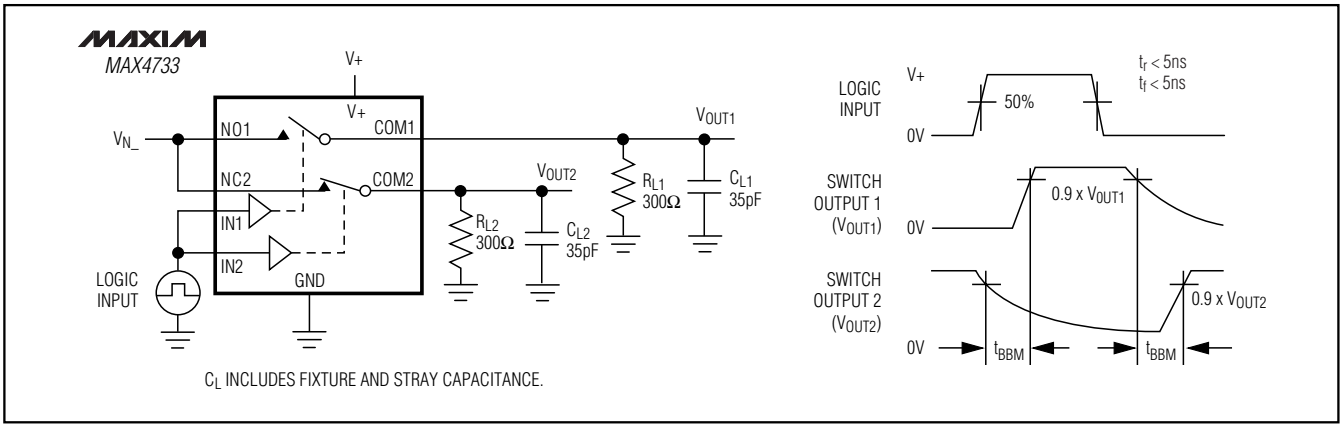


Figure 3. Break-Before-Make Interval (MAX4733 only)

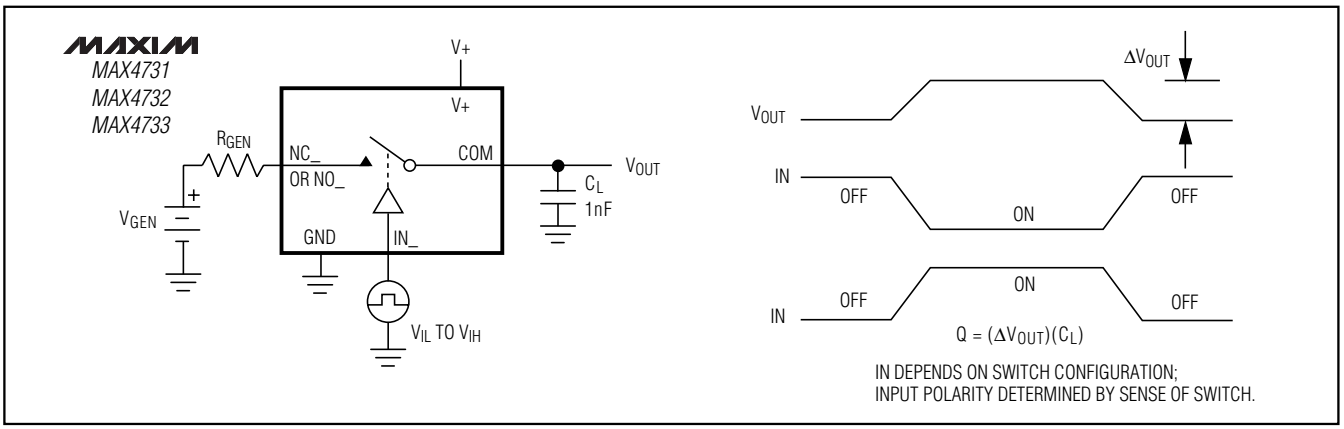


Figure 4. Charge Injection

50Ω, Dual SPST Analog Switches in UCSP

Test Circuits/Timing Diagrams (continued)

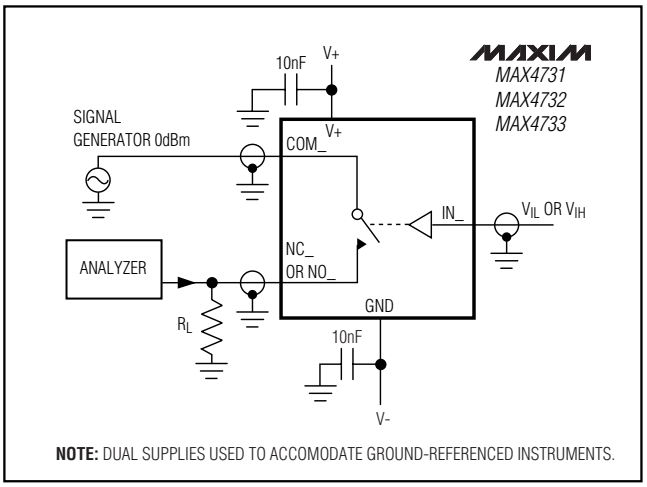


Figure 5. Off-Isolation/On-Channel Bandwidth

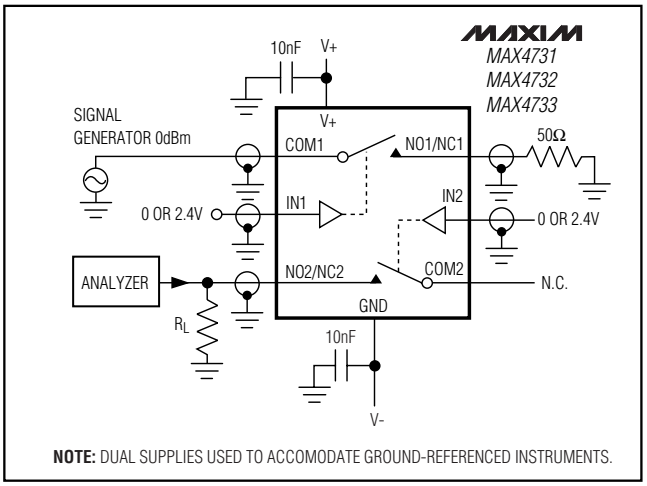


Figure 6. Crosstalk

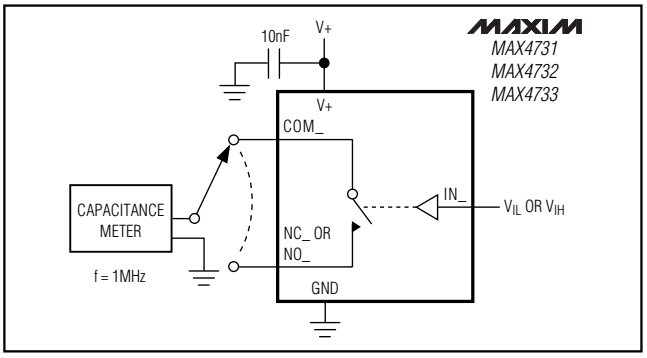


Figure 7. Channel Off/On-Capacitance

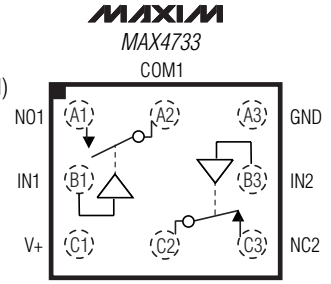
Chip Information

TRANSITOR COUNT: 68

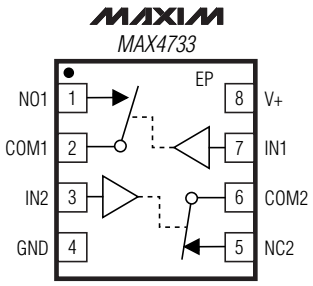
PROCESS: CMOS

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW
(BUMPS
ON BOTTOM)



UCSP



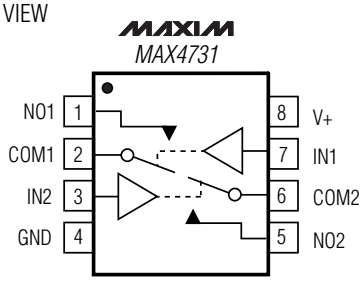
TDFN

EP = EXPOSED PAD

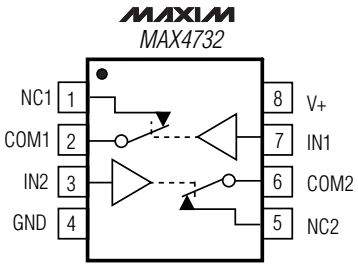
MAX4733		
IN_	**NO1**	**NC2**
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

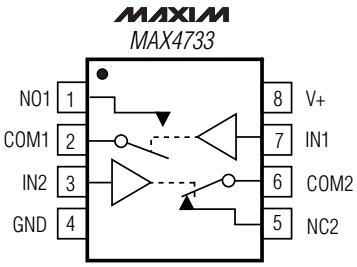
TOP VIEW



µMAX



µMAX



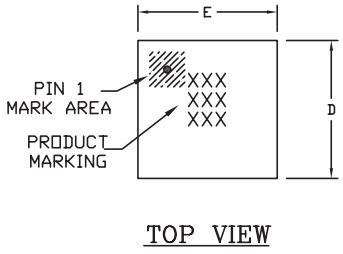
µMAX

50Ω, Dual SPST Analog Switches in UCSP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

9LUCSP, 3x3.EPS

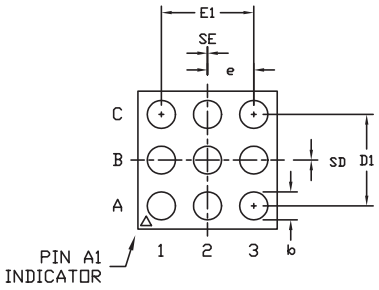


TOP VIEW

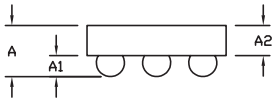
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

-DRAWING NOT TO SCALE-

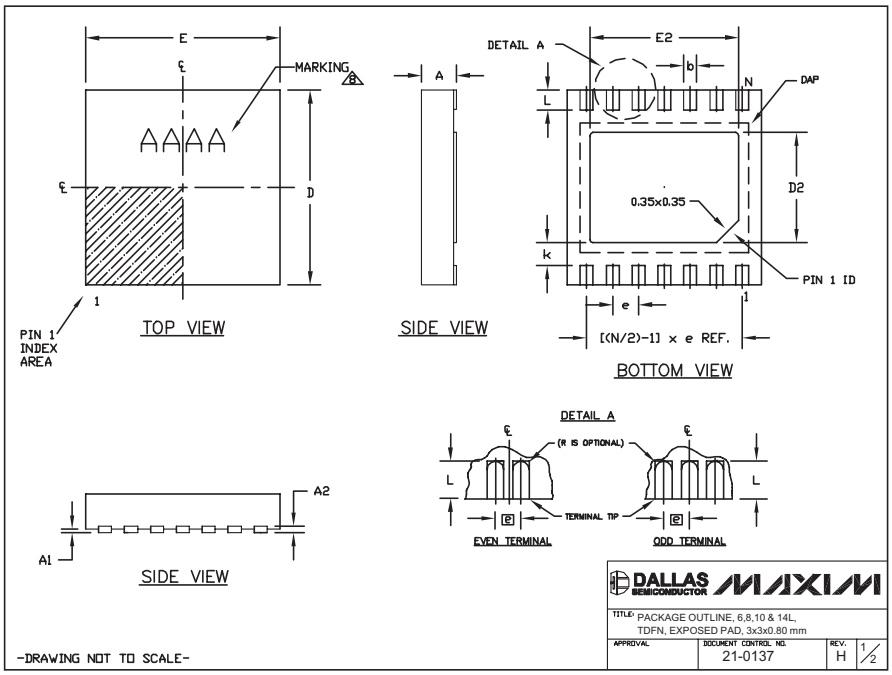
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0093	K	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T633-2	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T833-1	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-2	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-3	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T1033-1	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1033-2	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1433-1	14	1.70–0.10	2.30–0.10	0.40 BSC	- - - -	0.20–0.05	2.40 REF
T1433-2	14	1.70–0.10	2.30–0.10	0.40 BSC	- - - -	0.20–0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. H
2/2

50Ω, Dual SPST Analog Switches in UCSP

Package Information (continued)

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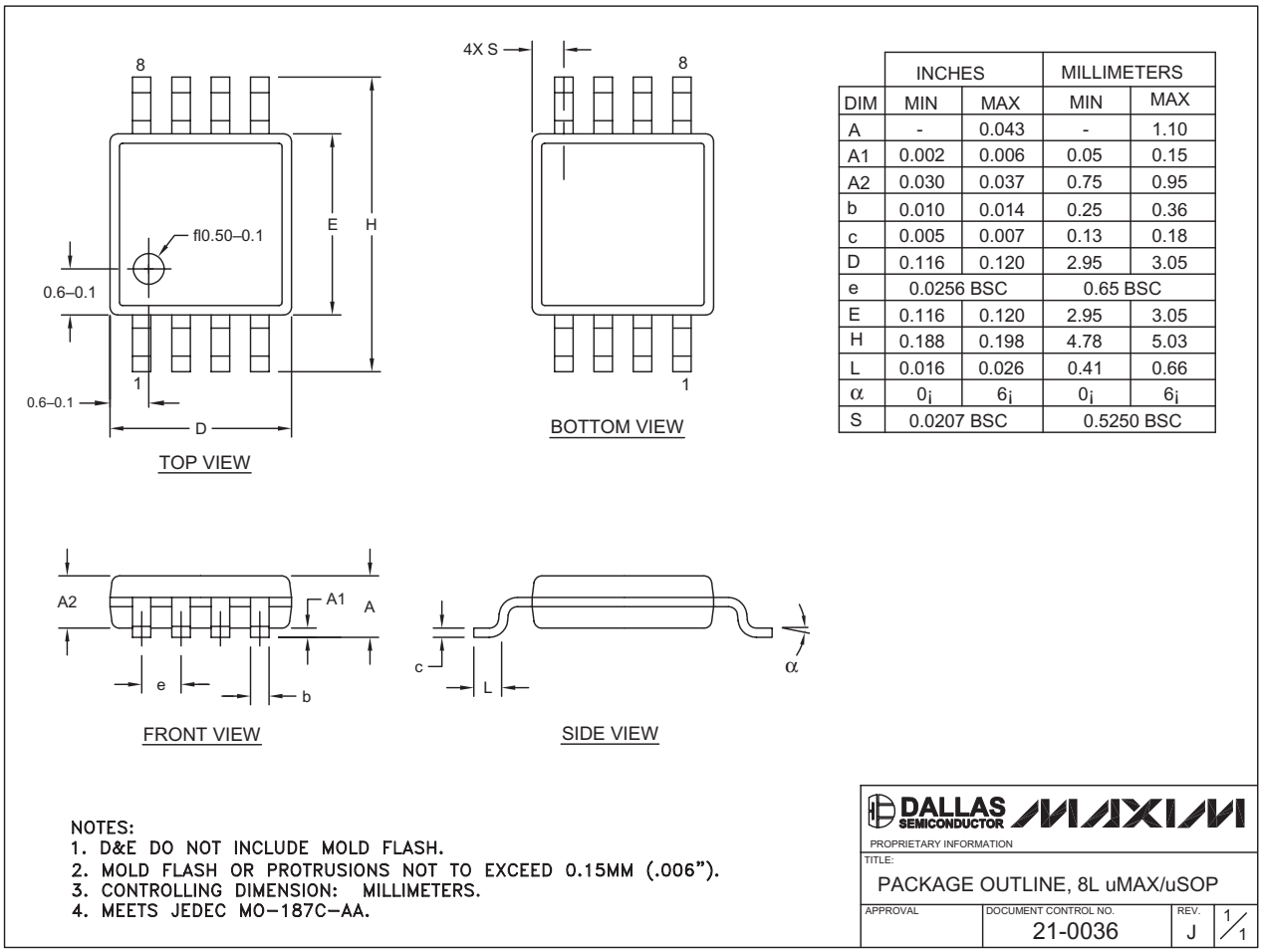

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

Revision History

Pages changed at Rev 2: 1, 2, 7, 8, 11, 14

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