

# High-Current, 25Ω, SPDT, CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

V+ to GND	-0.3V to +44V
V- to GND	-44V to +0.3V
V+ to V-	-0.3V to +44V
All Other Pins to GND (Note 1)	(V- - 0.3V) to (V+ + 0.3V)
Continuous Current COM, NO, NC (MAX4660)	±150mA
Continuous Current COM, NO, NC (MAX4659)	±75mA
Continuous Current IN	±30mA
Peak Current COM, NO, NC	
MAX4660 (pulsed at 1ms, 10% duty cycle)	±200mA
MAX4659 (pulsed at 1ms, 10% duty cycle)	±150mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
8-Pin μMAX-EP (derate 10.3mW/°C above +70°C)	
MAX4660	825mW

8-Pin μMAX (derate 4.50mW/°C above +70°C)	
MAX4659	362mW
8-Pin SO-EP (derate 18.9mW/°C above +70°C)	
MAX4660	1509mW
8-Pin SO (derate 5.88mW/°C above +70°C)	
MAX4659	471mW
Operating Temperature Ranges	
MAX4659/MAX4660	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

**Note 1:** Signals on NO, NC, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, V<sub>IH</sub> = 2.4V, V<sub>IL</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>			V-		V+	V
On-Resistance	R <sub>ON</sub>	I <sub>COM</sub> = 50mA; V <sub>NO</sub> or V <sub>NC</sub> = ±10V	+25°C		18	25	Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			30	
On-Resistance Matching Between Channels	ΔR <sub>ON</sub>	I <sub>COM</sub> = 50mA; V <sub>NO</sub> or V <sub>NC</sub> = ±10V	+25°C		0.4	1.2	Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			1.5	
On-Resistance Flatness (Note 3)	R <sub>FLAT</sub> (ON)	I <sub>COM</sub> = 50mA; V <sub>NO</sub> or V <sub>NC</sub> = -5V, 0, +5V	+25°C		0.5	1.5	Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			2	
NO or NC Off-Leakage Current (Note 4)	I <sub>NO</sub> (OFF) or I <sub>NC</sub> (OFF)	V <sub>COM</sub> = -14.5V, +14.5V; V <sub>NO</sub> or V <sub>NC</sub> = +14.5V, -14.5V	+25°C	-1	0.01	1	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-10		10	
COM On-Leakage Current (Note 4)	I <sub>COM</sub> (ON)	V <sub>COM</sub> = +14.5V, -14.5V; V <sub>NO</sub> or V <sub>NC</sub> = +14.5V, -14.5V, or floating	+25°C	-2	0.02	2	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-20		20	
DYNAMIC CHARACTERISTICS							
Transition Time	t <sub>TRANS</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 10V; R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF; Figure 3	+25°C		85	150	ns
			T <sub>MIN</sub> to T <sub>MAX</sub>			200	
Break-Before-Make Delay	t <sub>BBM</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 10V; R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF; Figure 3	+25°C	10	20		ns
			T <sub>MIN</sub> to T <sub>MAX</sub>	5			

# High-Current, 25Ω, SPDT, CMOS Analog Switches

MAX4659/MAX4660

## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, V<sub>IH</sub> = 2.4V, V<sub>IL</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
Charge Injection	Q	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0, C <sub>L</sub> = 1nF, Figure 4	+25°C		1.5		pC
-3dB Bandwidth	BW		+25°C		225		MHz
Off-Isolation (Note 5)	V <sub>ISO</sub>	f = 1MHz, R <sub>L</sub> = 50Ω, Figure 5	+25°C		-70		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V <sub>NL</sub> = 5Vp-p, R <sub>L</sub> = 600Ω	+25°C		0.005		%
Crosstalk	V <sub>CROSS</sub>	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, f = 1MHz, Figure 6	+25°C		-76		dB
NO or NC Off-Capacitance	C <sub>NO(OFF)</sub> , C <sub>NC(OFF)</sub>	f = 1MHz, Figure 7	+25°C		6		pF
COM On-Capacitance	C <sub>COM(ON)</sub>	f = 1MHz, Figure 8	+25°C		25		pF
<b>DIGITAL I/O</b>							
Input Logic High	V <sub>IH</sub>		T <sub>MIN</sub> to T <sub>MAX</sub>	2.4			V
Input Logic Low	V <sub>IL</sub>		T <sub>MIN</sub> to T <sub>MAX</sub>			0.8	V
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0.8V or 2.4V	T <sub>MIN</sub> to T <sub>MAX</sub>	-1		1	μA
<b>POWER SUPPLY</b>							
Power-Supply Range			T <sub>MIN</sub> to T <sub>MAX</sub>	±4.5		±20	V
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 or 5V, V <sub>NL</sub> = 3V, I <sub>SWITCH</sub> = 100mA, MAX4660; I <sub>SWITCH</sub> = 50mA, MAX4659	+25°C		135	200	μA
			T <sub>MIN</sub> to T <sub>MAX</sub>			300	
Negative Supply Current	I <sub>-</sub>	V <sub>IN</sub> = 0 or 5V, V <sub>NL</sub> = 3V, I <sub>SWITCH</sub> = 100mA, MAX4660; I <sub>SWITCH</sub> = 50mA, MAX4659	+25°C		30	50	μA
			T <sub>MIN</sub> to T <sub>MAX</sub>			75	
Ground Current	I <sub>GND</sub>	V <sub>IN</sub> = 0 or 5V, V <sub>NL</sub> = 3V, I <sub>SWITCH</sub> = 100mA, MAX4660; I <sub>SWITCH</sub> = 50mA, MAX4659	+25°C		100	175	μA
			T <sub>MIN</sub> to T <sub>MAX</sub>			225	

# High-Current, 25Ω, SPDT, CMOS Analog Switches

## ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0, V<sub>IH</sub> = 2.4V, V<sub>IL</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V <sub>IN</sub>		T <sub>MIN</sub> to T <sub>MAX</sub>	0		V+	V
On-Resistance	R <sub>ON</sub>	I <sub>COM</sub> = 25mA; V <sub>NO</sub> or V <sub>NC</sub> = +10V	+25°C	38	50		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>		60		
On-Resistance Matching Between Channels	ΔR <sub>ON</sub>	I <sub>COM</sub> = 25mA; V <sub>NO</sub> or V <sub>NC</sub> = ±10V	+25°C	0.4	2		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>		2.5		
On-Resistance Flatness (Note 3)	R <sub>FLAT</sub> (ON)	I <sub>COM</sub> = 25mA; V <sub>NO</sub> or V <sub>NC</sub> = +2V, +6V, +10V	+25°C	4	7		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>		9		
DYNAMIC CHARACTERISTICS							
Transition Time	t <sub>TRANS</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 10V; R <sub>L</sub> = 300Ω; C <sub>L</sub> = 35pF, Figure 2	+25°C	120	200		ns
			T <sub>MIN</sub> to T <sub>MAX</sub>		250		
Break-Before-Make Delay	t <sub>BBM</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 10V; R <sub>L</sub> = 300 Ω; C <sub>L</sub> = 35pF, Figure 2	+25°C	20	50		ns
			T <sub>MIN</sub> to T <sub>MAX</sub>	10			
Charge Injection	Q	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0, C <sub>L</sub> = 1nF, Figure 4	+25°C	1			pC
POWER SUPPLY							
Power-Supply Range	V+			+9		+40	V
Positive Supply Current	I+	V <sub>IN</sub> = 0 or 12V, V <sub>N-</sub> = 3V; I <sub>SWITCH</sub> = 50mA, MAX4660; I <sub>SWITCH</sub> = 25mA, MAX4659	+25°C	50	100		μA
			T <sub>MIN</sub> to T <sub>MAX</sub>		125		
		V <sub>IN</sub> = 5V, V <sub>N-</sub> = 3V; I <sub>SWITCH</sub> = 50mA, MAX4660; I <sub>SWITCH</sub> = 25mA, MAX4659	+25°C	70	125		
			T <sub>MIN</sub> to T <sub>MAX</sub>		150		

**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

**Note 3:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

**Note 4:** Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at T<sub>A</sub> = +25°C.

**Note 5:** Off-isolation = 20log<sub>10</sub> [V<sub>COM</sub> / (V<sub>NC</sub> or V<sub>NO</sub>)], V<sub>COM</sub> = output, V<sub>NC</sub> or V<sub>NO</sub> = input to off switch.

**Note 6:** -40°C specifications are guaranteed by design.

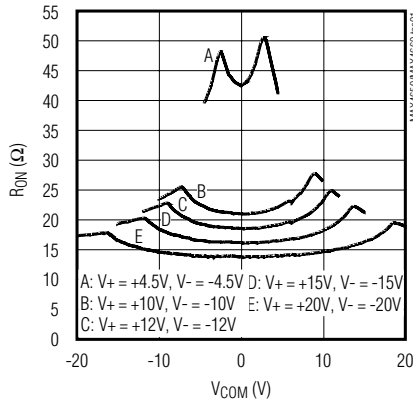
# High-Current, 25Ω, SPDT, CMOS Analog Switches

## Typical Operating Characteristics

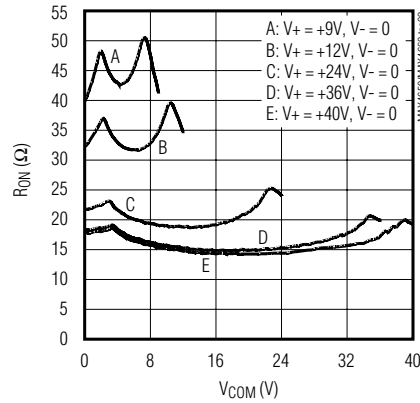
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

MAX4659/MAX4660

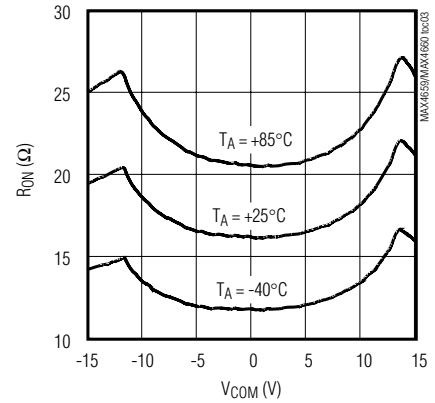
**ON-RESISTANCE vs.  $V_{COM}$  (DUAL SUPPLIES)**



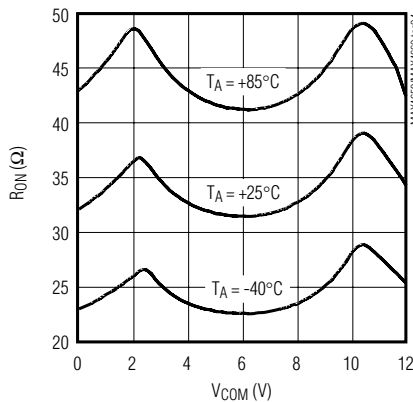
**ON-RESISTANCE vs.  $V_{COM}$  (SINGLE SUPPLY)**



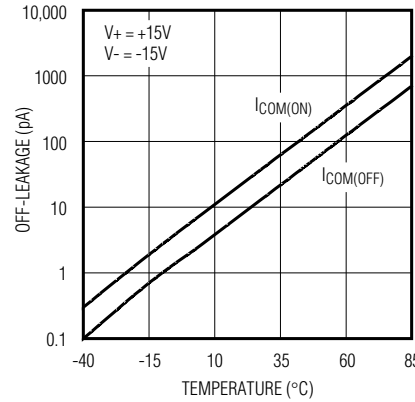
**ON-RESISTANCE vs.  $V_{COM}$  AND TEMPERATURE (DUAL SUPPLIES)**



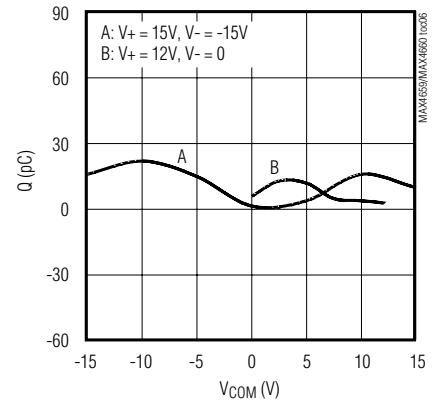
**ON-RESISTANCE vs.  $V_{COM}$  AND TEMPERATURE (SINGLE SUPPLY)**



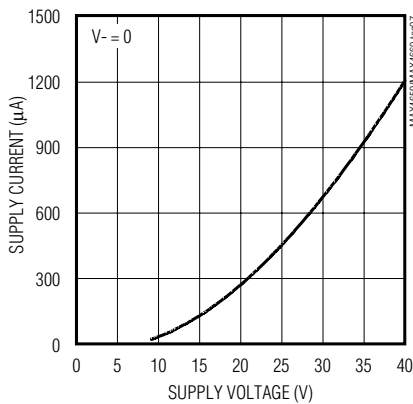
**LEAKAGE CURRENT vs. TEMPERATURE**



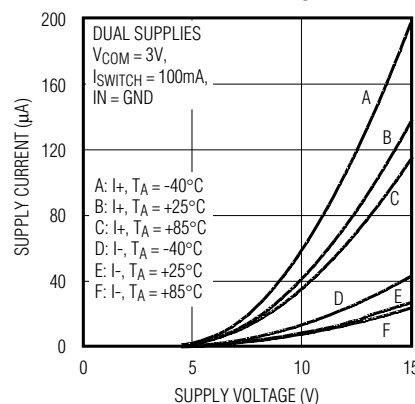
**CHARGE INJECTION vs.  $V_{COM}$**



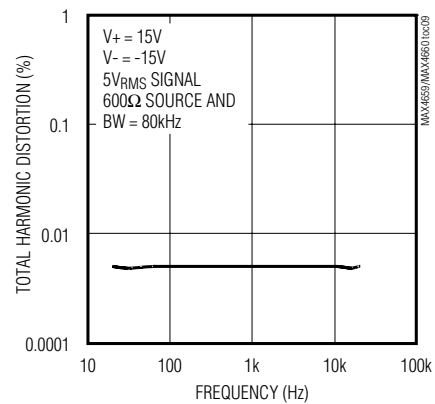
**SUPPLY CURRENT vs. SUPPLY VOLTAGE (SINGLE SUPPLY)**



**SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE**



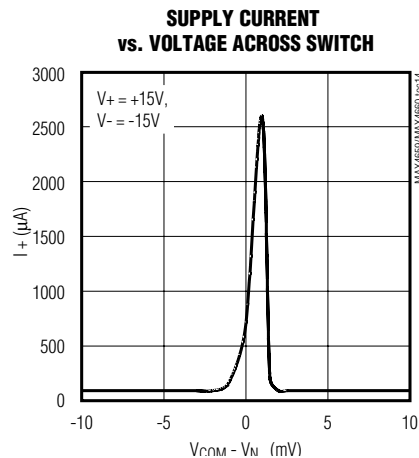
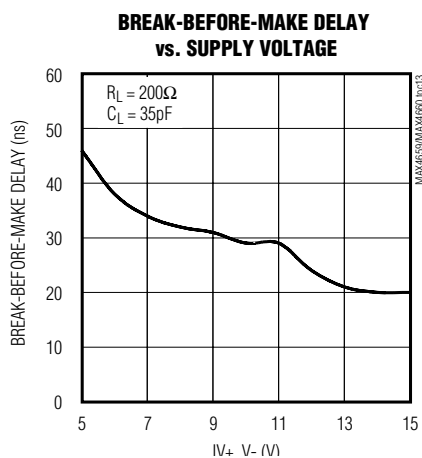
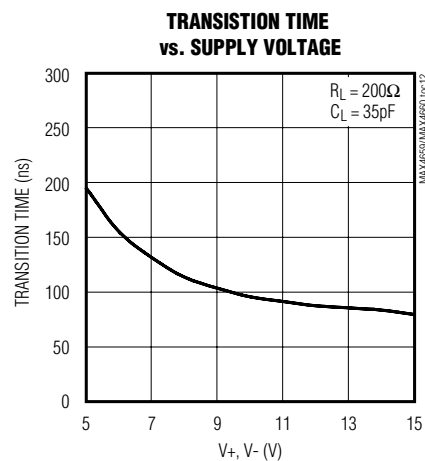
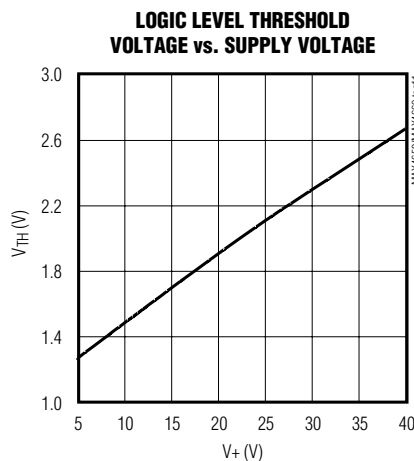
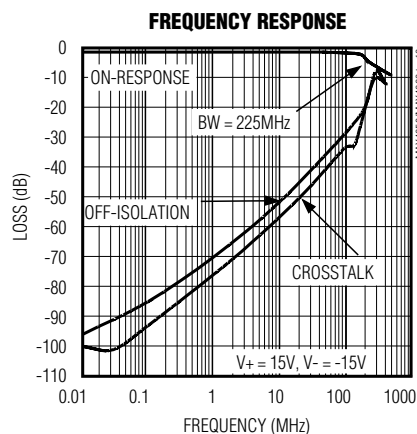
**TOTAL HARMONIC DISTORTION vs. FREQUENCY**



# High-Current, 25 $\Omega$ , SPDT, CMOS Analog Switches

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



## Pin Description

PIN	NAME	FUNCTION
1	COM	Analog Switch Common
2	NC	Normally Closed Switch Terminal. NC is connected to COM when IN is low.
3	GND	Ground
4	$V_+$	Positive Supply Voltage Input
5	N.C.	No Connection
6	IN	Digital Control Input
7	$V_-$	Negative Supply Voltage Input
8	NO	Normally Open Switch Terminal. NO is connected to COM when IN is high.
—	EP	Exposed Paddle. Connect EP to $V_+$ or leave unconnected.

# High-Current, 25 $\Omega$ , SPDT, CMOS Analog Switches

## Detailed Description

The MAX4659/MAX4660 are single, single-pole/double-throw (SPDT) CMOS analog switches. The CMOS switch construction provides rail-to-rail signal handling while consuming very little power. The switch is controlled by a TTL/CMOS level compatible digital input. The MAX4659/MAX4660 have a normally open switch and a normally closed switch.

These devices can be operated with either single power supplies or dual power supplies. Operation at up to  $\pm 20\text{V}$  supplies allows users a wide switching dynamic range. Additionally, asymmetrical operation is possible to tailor performance to a particular application.

These switches have been specifically designed to handle high switch currents, up to 200mA peak current and 150mA continuous currents. In order to do this, a new technique is used to drive the body of the output N-channel device. (Note: The basic switch between the input, NC/NO terminal and the output common terminal consists of an N-channel MOSFET and a P-channel MOSFET in parallel.) The standard method limits operation to approximately a 600mV drop across the switch. More than 600mV causes an increase in  $I_{\text{DON}}$  leakage current (due to the turn-on of on-chip parasitic diodes), and an increase in  $V_+$  supply current. With this new sensing method, there is no limitation to the voltage drop across the switch. Current and voltage are limited only by the power dissipation rating of the package and the absolute maximum ratings of the switch.

When the analog input voltage drop is approximately 7mV there is an increase in power supply current from 90 $\mu\text{A}$  to 2mA (typ) within a 1mV to 7mV range, caused by the new sensing/driving circuitry.

## Applications Information

### Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. First, connect GND, followed by  $V_+$ ,  $V_-$ , and the remaining pins. If power-supply sequencing is not possible, add two small-signal diodes (D1, D2) in series with

supply pins (Figure 1). Adding diodes reduces the analog signal range to one diode drop below  $V_+$  and one diode drop above  $V_-$ , but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between  $V_+$  and  $V_-$  should not exceed 44V. The protection diode for the negative supply is not required when  $V_-$  is connected to GND.

### Off-Isolation at High Frequencies

In 50 $\Omega$  systems, the high-frequency on-response of these parts extends from DC to above 100MHz, with a typical loss of -2dB. When the switch is turned off, however, it behaves like a capacitor and off-isolation decreases with increasing frequency. This effect is more pronounced with higher source and load impedances. Above 5MHz, circuit board layout becomes critical. The graphs shown in the *Typical Operating Characteristics* were taken using a 50 $\Omega$  source and load connected with BNC connectors.

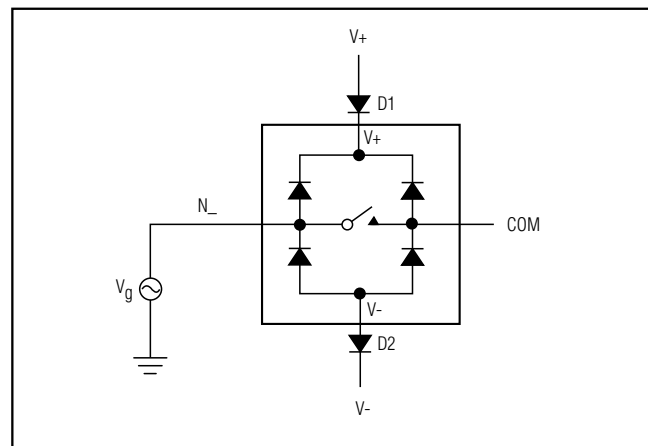


Figure 1. Overvoltage Protection Using Blocking Diodes

# High-Current, 25Ω, SPDT, CMOS Analog Switches

## Test Circuits/Timing Diagrams

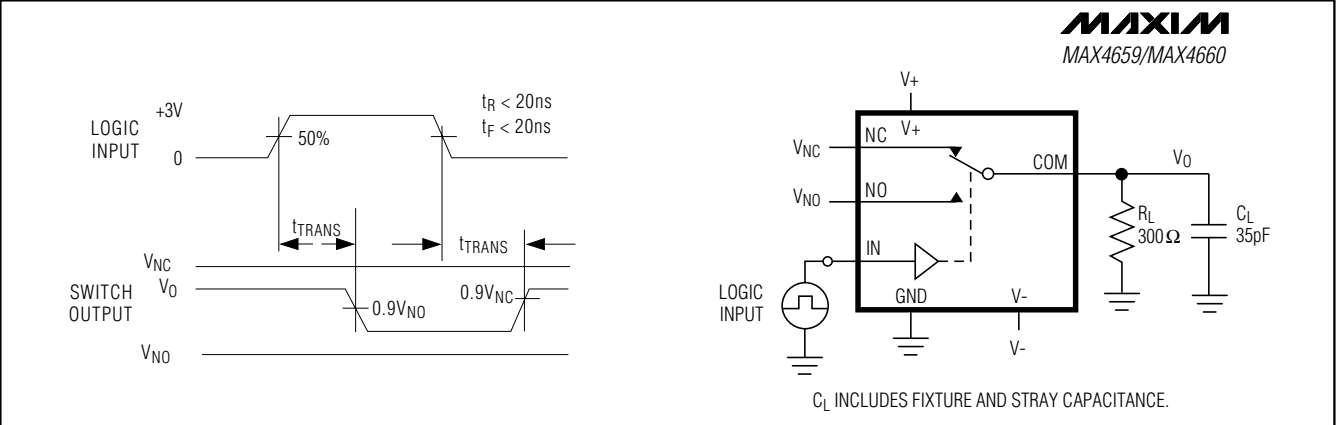


Figure 2. Functional Diagram

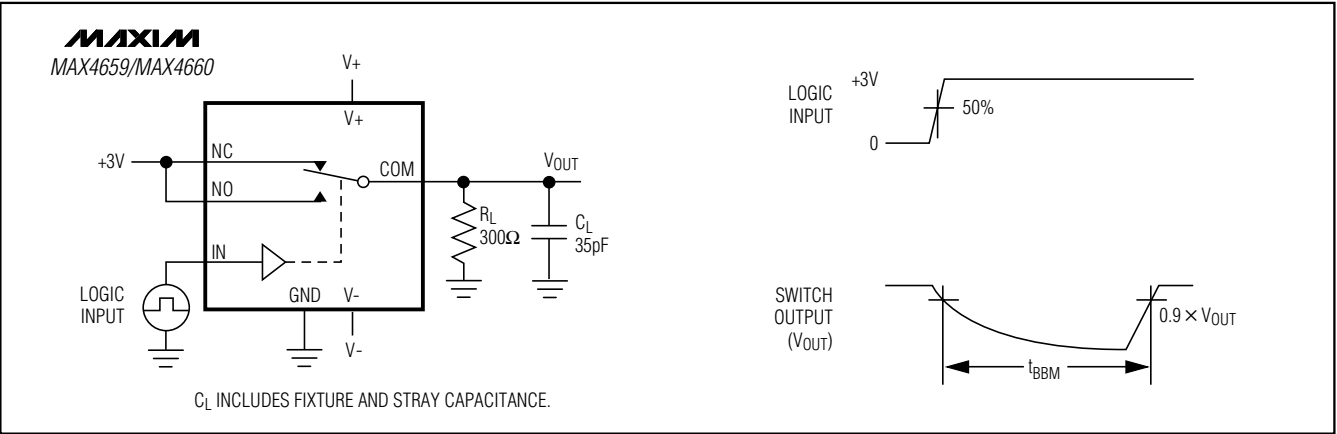


Figure 3. Break-Before-Make Time

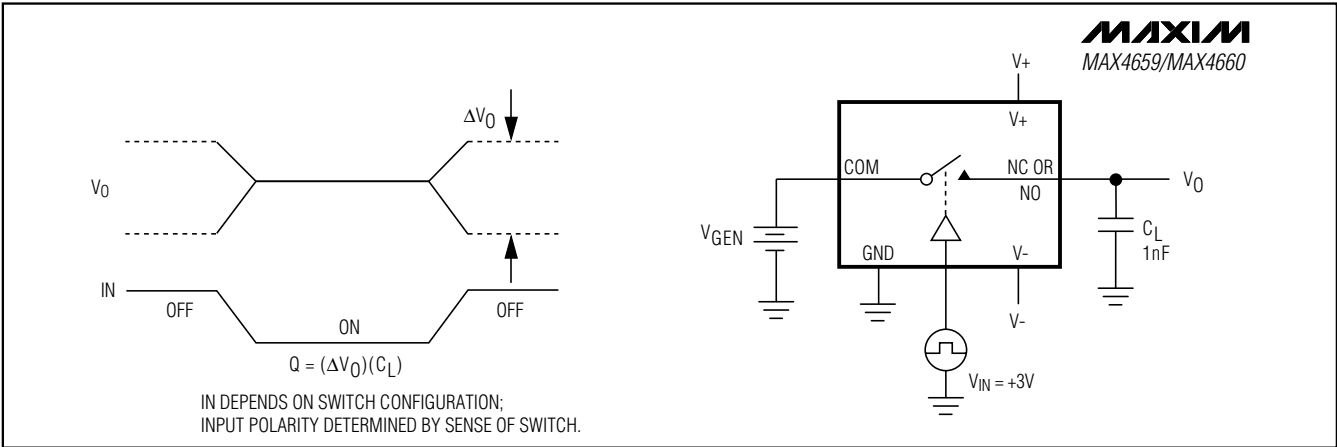


Figure 4. Charge Injection

# High-Current, 25 $\Omega$ , SPDT, CMOS Analog Switches

## Test Circuits/Timing Diagrams (continued)

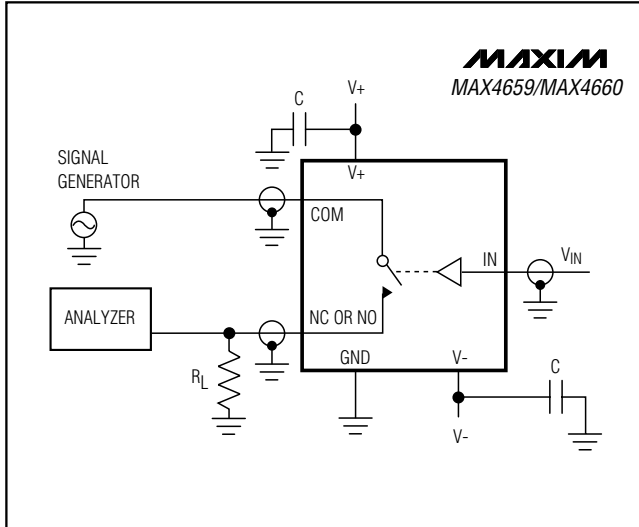


Figure 5. Off-Isolation

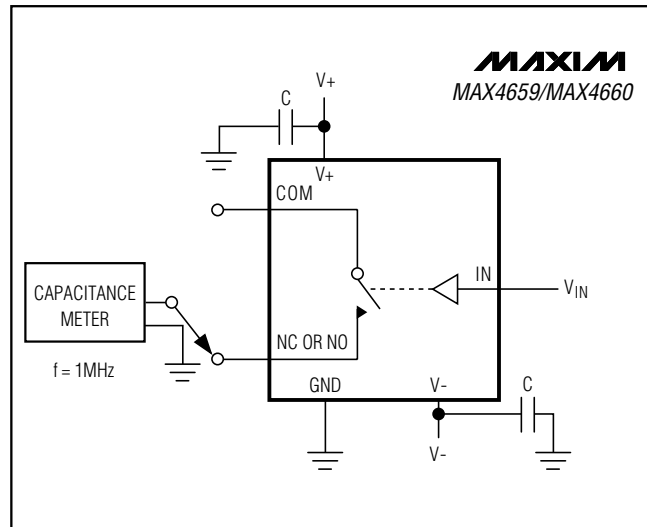


Figure 7. Channel Off-Capacitance

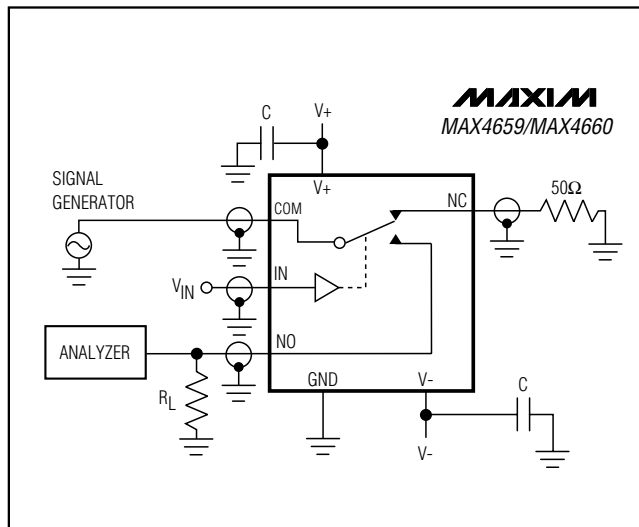


Figure 6. Crosstalk

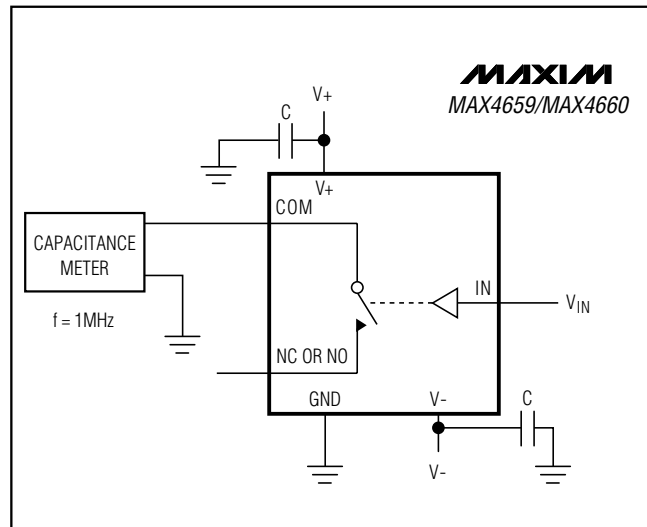


Figure 8. Channel On-Capacitance

## Chip Information

TRANSISTOR COUNT: 45

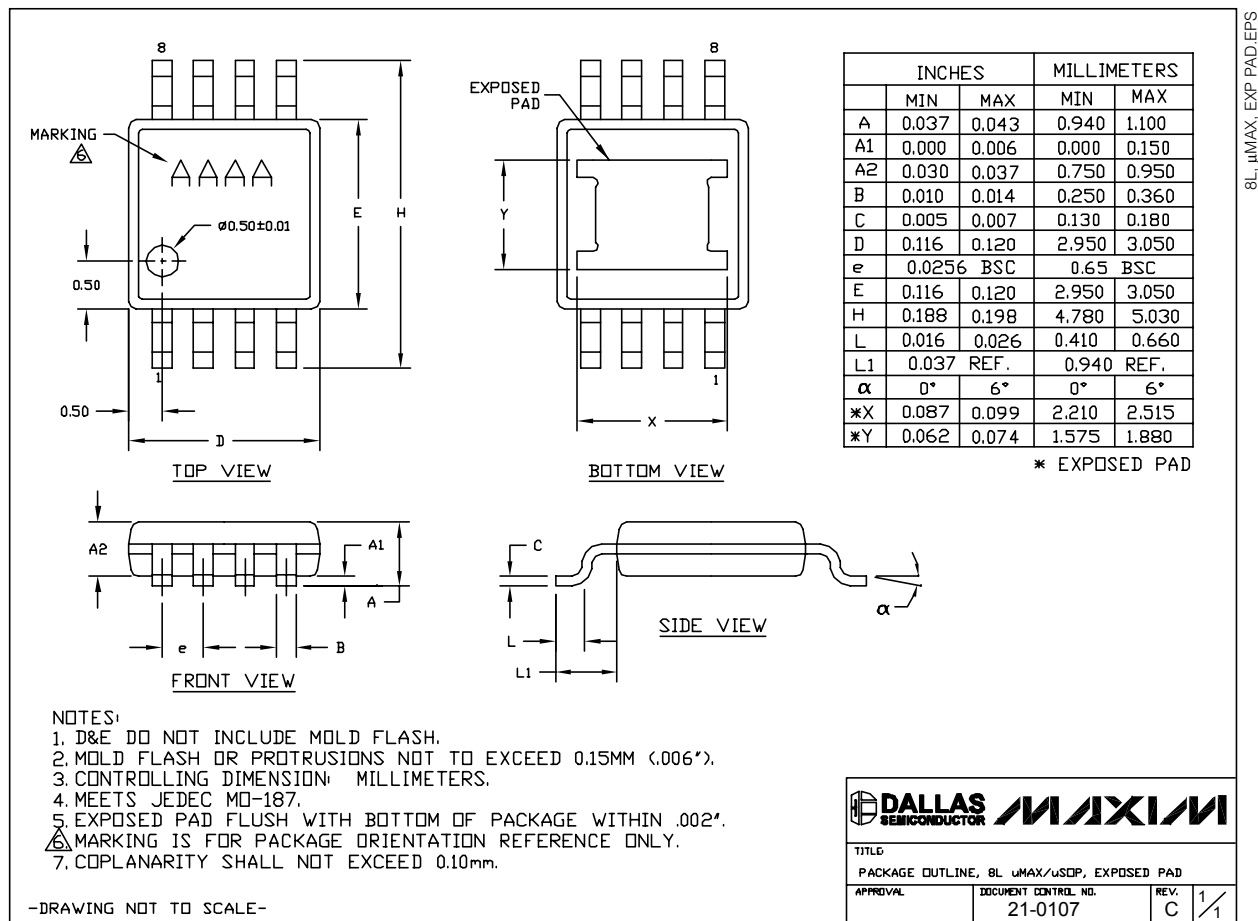
PROCESS: CMOS



# High-Current, 25 $\Omega$ , SPDT, CMOS Analog Switches

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

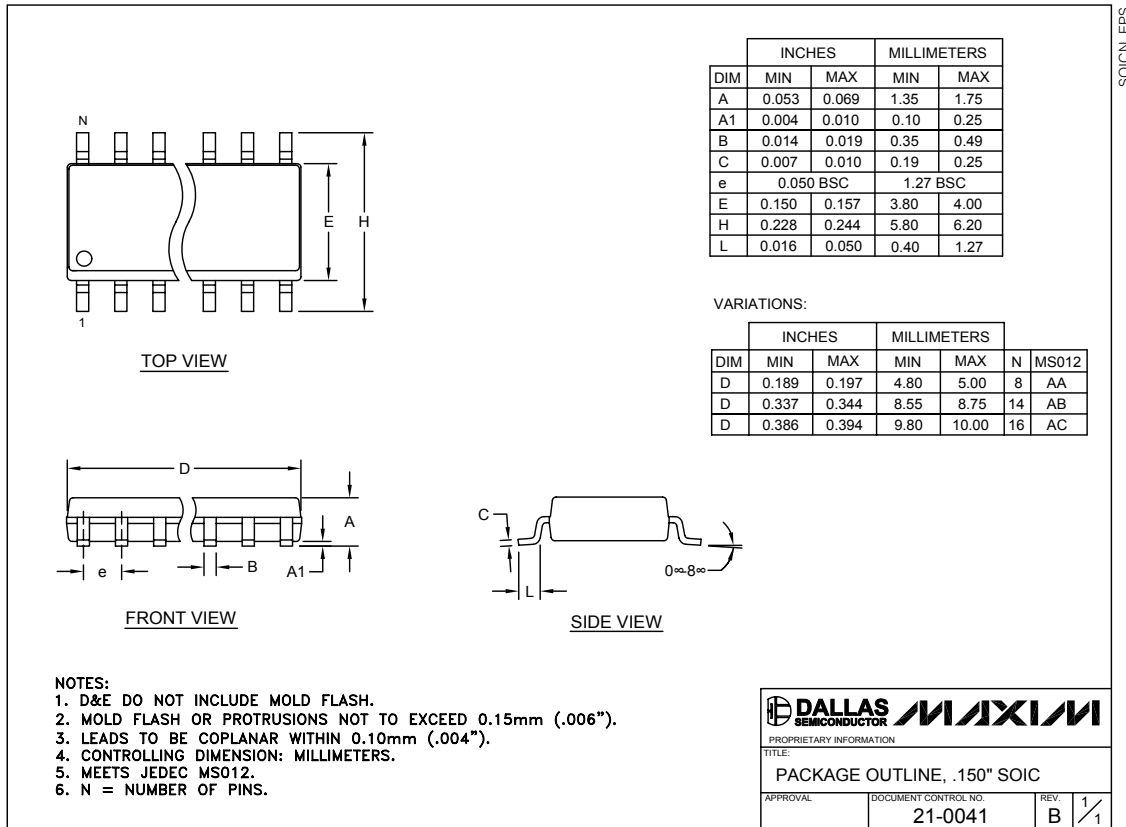


8L,  $\mu$ MAX, EXP PAD EPS

# High-Current, 25Ω, SPDT, CMOS Analog Switches

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

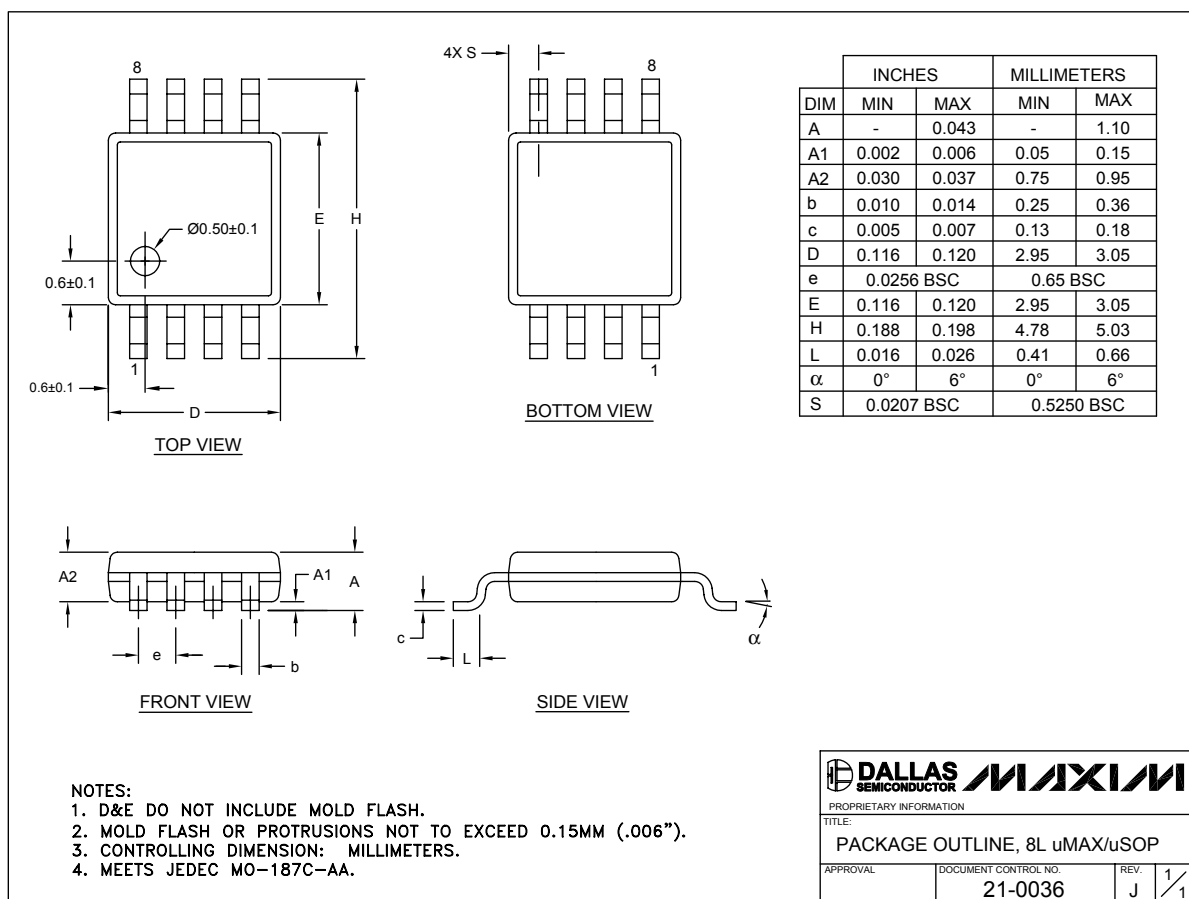


MAX4659/MAX4660

# High-Current, 25 $\Omega$ , SPDT, CMOS Analog Switches

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



8L uMAXD EPS

## Revision History

Pages changed at Rev 1: 1, 6, 12

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