Low-Voltage SIM/Smart Card Level Translators in µMAX

ABSOLUTE MAXIMUM RATINGS

DV_{CC}, V_{CC} to GND .....-0.3V to +6.0V
RIN, CIN, DATA, DDRV, $\overline{SHDN}$ to GND .....-0.3V to (DV_{CC} + 0.3V)
RST, CLK, IO to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Figure 1, DV_{CC} = +1.8V; V_{CC} = +1.8V, +3.0V, or +5.0V; $\overline{SHDN}$ = DV_{CC}, CIN = RIN = GND or DV_{CC}, IO = V_{CC}, DATA = DDRV = DV_{CC}, C_{IO} = C_{CLK} = C_{RST} = C_{DATA} = 30pF, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
DV_{CC} Operating Range	DV_{CC}		1.4		5.5	V
V_{CC} Operating Range	V_{CC}		1.7		5.5	V
DV_{CC} Operating Current	I_{DVCC}	CIN static		0.1	0.5	µA
		CIN clocked at 1.625MHz from GND to DV_{CC} with 50% duty cycle		2.5		
		CIN clocked at 3.25MHz from GND to DV_{CC} with 50% duty cycle		5		
V_{CC} Operating Current	I_{VCC}	CIN static		0.9	3.0	µA
		CIN clocked at 1.625MHz from GND to DV_{CC} with 50% duty cycle		0.4		mA
		CIN clocked at 3.25MHz from GND to DV_{CC} with 50% duty cycle		0.8		
Total Shutdown Current	I_{SHDN}	I_{OFF} = I_{VCC} + I_{DVCC}, $\overline{SHDN}$ = GND (MAX1840 only), or DV_{CC} = GND or V_{CC} = GND		0.01	1	µA
CIN, RIN, $\overline{SHDN}$, DDRV LOGIC INPUTS						
Digital Input Low Threshold	V_{IL}		0.2 × DV_{CC}			V
Digital Input High Threshold	V_{IH}				0.7 × DV_{CC}	V
Input Leakage Current				0.01	1	µA
CLK, RST OUTPUTS						
Digital Output Low Level	V_{OL}	I_{SINK} = 200µA			0.4	V
Digital Output High Level	V_{OH}	I_{SOURCE} = 20µA	0.9 × V_{CC}			V
		I_{SOURCE} = 200µA	0.8 × V_{CC}			
DATA INPUT/OUTPUT						
DATA Pullup Resistance	R_{DATA}	Between DATA and DV_{CC}	13	20	28	kΩ
Input Low Threshold	$V_{IL(DATA)}$	(Note 2)	0.3			V
Input High Threshold	$V_{IH(DATA)}$	(Note 3)			DV_{CC} - 0.6	V
Input Low Current	I_{IL}	V_{CC} = 5.0V			1	mA
Input High Current	I_{IH}				2	µA

ELECTRICAL CHARACTERISTICS (continued)

(Figure 1, DV_{CC} = +1.8V; V_{CC} = +1.8V, +3.0V, or +5.0V; $\overline{SHDN}$ = DV_{CC}, CIN = RIN = GND or DV_{CC}, IO = V_{CC}, DATA = DDRV = DV_{CC}, C_{IO} = C_{CLK} = C_{RST} = C_{DATA} = 30pF, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Level	$V_{OL(DATA)}$	IO = GND, I_{SINK} = 100µA			0.4	V
		DV_{CC} = 3.0V, IO = GND, I_{SINK} = 200µA			0.4	
Output High Level	$V_{OH(DATA)}$	I_{SOURCE} = 10µA	0.7 × DV_{CC}			V
		DV_{CC} = 3.0V, I_{SOURCE} = 20µA	0.7 × DV_{CC}			
IO (INPUT/OUTPUT)						
IO Pullup Resistance	R_{IO}	Between IO and V_{CC}	6.5	10	14	kΩ
Input Low Threshold	$V_{IL(IO)}$	$I_{IL(MAX)}$ = 1mA (Note 2)	0.3			V
Input High Threshold	$V_{IH(IO)}$	$I_{IH(MAX)}$ = ±20µA (Note 3)			0.7 × V_{CC}	V
Input Low Current	I_{IL}				1	mA
Input High Current	I_{IH}				20	µA
Output Low Level	$V_{OL(IO)}$	DATA = GND or DDRV = GND, I_{SINK} = 200µA			0.4	V
Output High Level	$V_{OH(IO)}$	I_{SOURCE} = 20µA	0.8 × V_{CC}			V
SHUTDOWN OUTPUT LEVELS						
Shutdown Output Levels (IO, CLK, RST)		I_{SINK} = 200µA, $\overline{SHDN}$ = GND, DATA = CIN = RIN = DV_{CC} (MAX1840 only)			0.4	V
		I_{SINK} = 200µA, DV_{CC} = GND, $\overline{SHDN}$ (MAX1840) = DDRV (MAX1841) = DATA = CIN = RIN = DV_{CC}			0.4	V
		I_{SINK} = 200µA, V_{CC} = GND, $\overline{SHDN}$ (MAX1840) = DDRV (MAX1841) = DATA = CIN = RIN = DV_{CC}			0.4	V
TIMING						
Maximum CLK Frequency (Notes 4, 5)	f_{CLK}	V_{CC} = 2.7V to 5.5V, DV_{CC} = 1.4V to 2.7V	5	20		MHz
		V_{CC} = 1.7V to 3.6V, DV_{CC} = 1.4V to 2.25V	5	15		

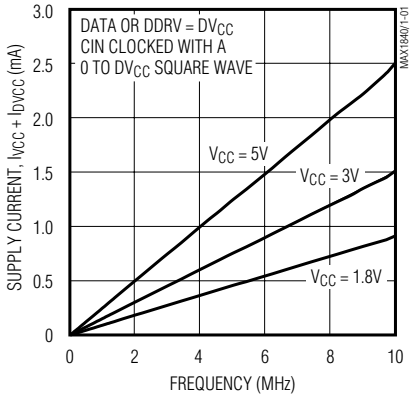
Note 1: Specifications to -40°C are guaranteed by design, not production tested.
Note 2: V_{IL} is defined as the voltage at which the output (DATA/IO) voltage equals 0.5V.
Note 3: V_{IH} is defined as the voltage at which the output (DATA/IO) voltage exceeds the input (IO/DATA) voltage by 100mV.
Note 4: Timing specifications are guaranteed by design, not production tested.
Note 5: The maximum CLK frequency is defined as the output duty cycle remaining in the 40% to 60% range when the 50% CIN is applied. CIN has 5ns rise and fall times; levels are GND to DV_{CC}. Input and output levels are measured at 50% of the waveform.

Low-Voltage SIM/Smart Card Level Translators in µMAX

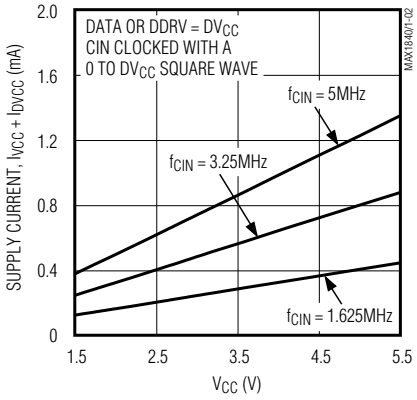
Typical Operating Characteristics

(Circuit of Figure 1, DV_{CC} = 3.0V, V_{CC} = +5.0V, DDRV or DATA = DV_{CC}, RIN = CIN = GND, T_A = +25°C, unless otherwise noted.)

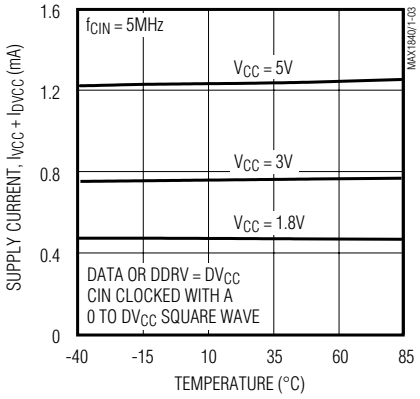
TOTAL OPERATING SUPPLY CURRENT vs. CLOCK FREQUENCY (DATA STATIC)



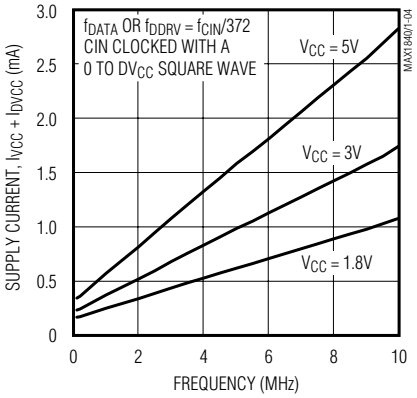
TOTAL OPERATING SUPPLY CURRENT vs. CARD-SIDE SUPPLY VOLTAGE (DATA STATIC)



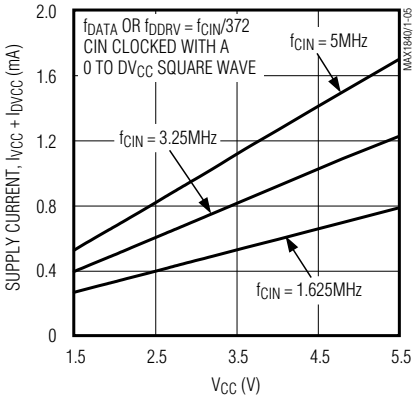
TOTAL OPERATING SUPPLY CURRENT vs. TEMPERATURE (DATA STATIC)



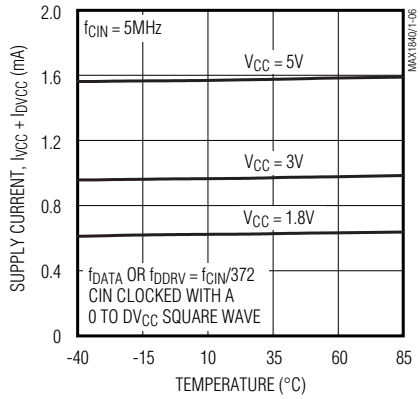
TOTAL OPERATING SUPPLY CURRENT vs. CLOCK FREQUENCY (DATA ACTIVE)



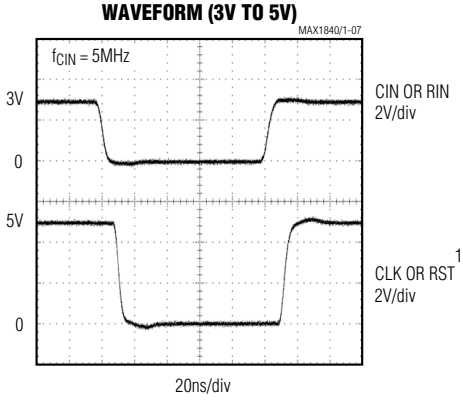
TOTAL OPERATING SUPPLY CURRENT vs. CARD-SIDE SUPPLY VOLTAGE (DATA ACTIVE)



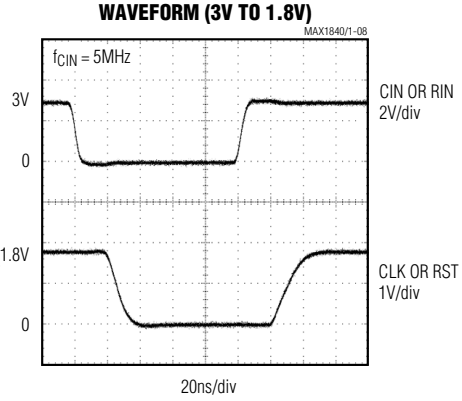
TOTAL OPERATING SUPPLY CURRENT vs. TEMPERATURE (DATA ACTIVE)



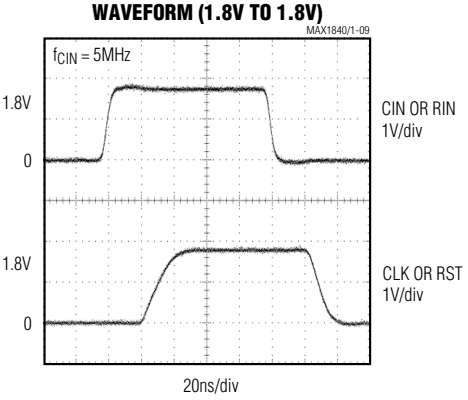
CIN TO CLK OR RIN TO RST WAVEFORM (3V TO 5V)



CIN TO CLK OR RIN TO RST WAVEFORM (3V TO 1.8V)



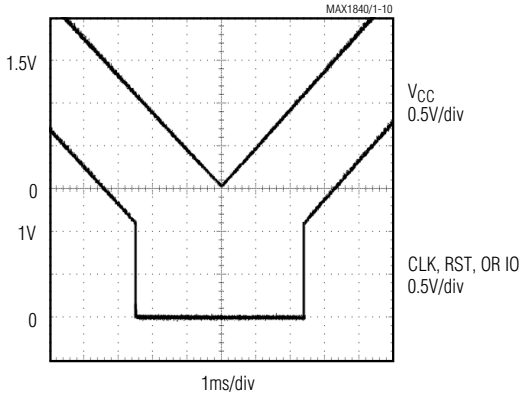
CIN TO CLK OR RIN TO RST WAVEFORM (1.8V TO 1.8V)



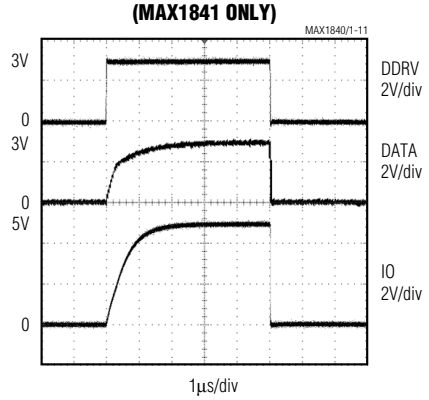
Typical Operating Characteristics (continued)

(Circuit of Figure 1, DV_{CC} = 3.0V, V_{CC} = +5.0V, DDRV or DATA = DV_{CC}, RIN = CIN = GND, T_A = +25°C, unless otherwise noted.)

UNDERVOLTAGE SHUTDOWN WAVEFORM



DDRV TO IO AND DATA WAVEFORM (MAX1841 ONLY)



Pin Description

PIN		NAME	FUNCTION
MAX1840	MAX1841		
1	1	DATA	System Controller Data Input/Output. An open-drain IO with a 20kΩ pull-up resistor to DV_{CC}. For bidirectional data transfer, connect to an open-drain controller output capable of sinking 1mA while pulling DATA low. If the controller is not open-drain, use DDRV to send data and DATA to receive data.
2	2	DV_{CC}	Supply Voltage for System Controller Digital Pins. Set at +1.4V to +5.5V.
3	3	CIN	System Controller Clock Input
4	4	RIN	System Controller Reset Input
—	5	DDRV	Optional System Controller Data Input. Connect to controllers without an open-drain output. When not used, connect DDRV to DV_{CC}.
5	—	$\overline{SHDN}$	Shutdown Mode Input. Driving $\overline{SHDN}$ low reduces the total supply current to less than 1µA. In shutdown mode, RST, CLK, and IO are actively pulled low and the transfer gate between DATA and IO is disabled. When not used, connect $\overline{SHDN}$ to DV_{CC}.
6	6	GND	System Controller and Card Ground
7	7	RST	Reset Output to Card. Actively pulled low during shutdown.
8	8	CLK	Clock Output to Card. Actively pulled low during shutdown.
9	9	V_{CC}	Supply Voltage for Card-Side Digital Pins. Set at +1.7V to +5.5V. Proper supply bypassing is required to meet ±10kV ESD specifications.
10	10	IO	Card-Side Bidirectional Input/Output. An open-drain output with a 10kΩ pull-up resistor to V_{CC}. For bidirectional data transfer, connect to an open-drain card output capable of sinking 1mA while pulling IO low. Actively pulled low during shutdown.

Low-Voltage SIM/Smart Card Level Translators in µMAX

Detailed Description

The MAX1840/MAX1841 provide the necessary level translation for interfacing with SIMs and smart cards in multivoltage systems. These devices operate with logic supply voltages between +1.4V and +5.5V on the controller side (DV_{CC}) and between +1.7V and +5.5V on the card side (V_{CC}). The total supply current (I_{DVCC} + I_{VCC}) is 1µA while operating in an idle state (see *Electrical Characteristics*). Figure 1 shows the MAX1840/MAX1841 test circuit. The *Typical Application Circuit* appears at the end of this data sheet.

Level Translation

The MAX1840/MAX1841 provide level translators for a clock input, a reset input, and a bidirectional data IO. The clock and reset inputs (CIN and RIN) are level shifted from the controller-side supply rails (DV_{CC} to GND) to the card-side supply rails (V_{CC} to GND). When connected to an open-drain controller output, DATA and IO provide bidirectional level translation. All level translation is valid for $DV_{CC} \geq V_{CC}$ or $DV_{CC} \leq V_{CC}$. The MAX1840/MAX1841 contain internal pull up resistors from DATA to the controller-side supply (DV_{CC}) and from IO to the card-side supply (V_{CC}). For push-pull controller outputs, see the *Data Driver* section for bidirectional data translation.

Data Driver (MAX1841 Only)

When using a microcontroller (µC) without an open-drain output, use the data driver (DDRV) input to send data to the SIM/smart card, while DATA provides the controller-side output for bidirectional data transfer. When not used, connect DDRV to DV_{CC} to reduce total supply current.

Shutdown Mode

For the MAX1840, drive $\overline{SHDN}$ low to activate shutdown. Connect $\overline{SHDN}$ to DV_{CC} or drive high for normal operation. To allow for card insertion and removal, shutdown mode actively pulls CLK, RST, and IO low; it also disconnects the internal 10kΩ pull up resistor from V_{CC} to prevent excessive current draw. Shutdown mode reduces the total supply current (I_{DVCC} + I_{VCC}) to 0.01µA.

SIM/Smart Card Insertion/Removal

The SIM/smart card specifications require that the card-side pins (V_{CC}, CLK, RST, IO) be at ground potential prior to inserting the SIM/smart card. For applications using the MAX1686H (Figure 3), the easiest way to achieve this is by shutting down the MAX1686H or by driving SHDN (MAX1840 only) low. If specific sequencing is desired, pull IO low by driving either DATA or DDRV (MAX1841 only) low, and pull CLK and RST low by driving CIN and RIN low, respectively.

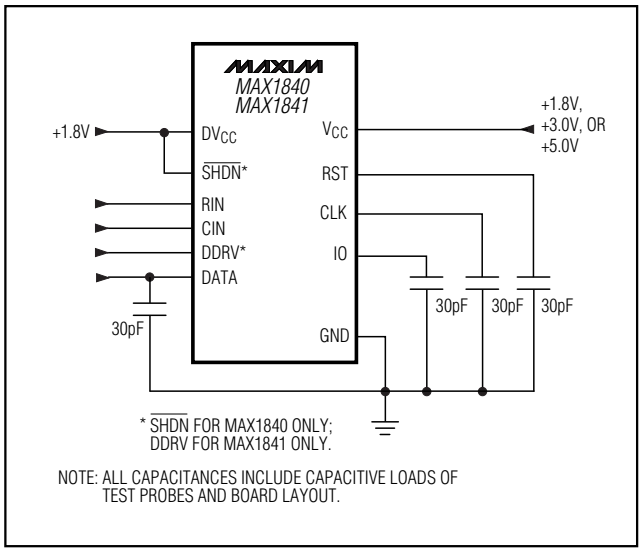


Figure 1. MAX1840/MAX1841 Test Circuit

ESD Protection

As with all Maxim devices, ESD-protection structures on all pins protect against ESDs encountered during handling and assembly. For further protection during card insertion and removal, the pins that connect to the card socket (CLK, RST, IO, V_{CC}, and GND) provide protection against ±10kV of ESD. The ESD structures withstand high ESD in all states: normal operation, shutdown, and power-down. After an ESD event, the MAX1840/MAX1841 continue working without latchup. A 1µF bypass capacitor from V_{CC} to GND is required to exceed ±10kV ESD specifications.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report documenting test setup, test methodology, and test results.

Applications Information

SIM/Smart Card Interface

To provide 5V when interfacing with a 5V SIM/smart card, +3V systems require a DC-DC converter. The MAX1686H +5V regulating charge pump for SIM cards provides

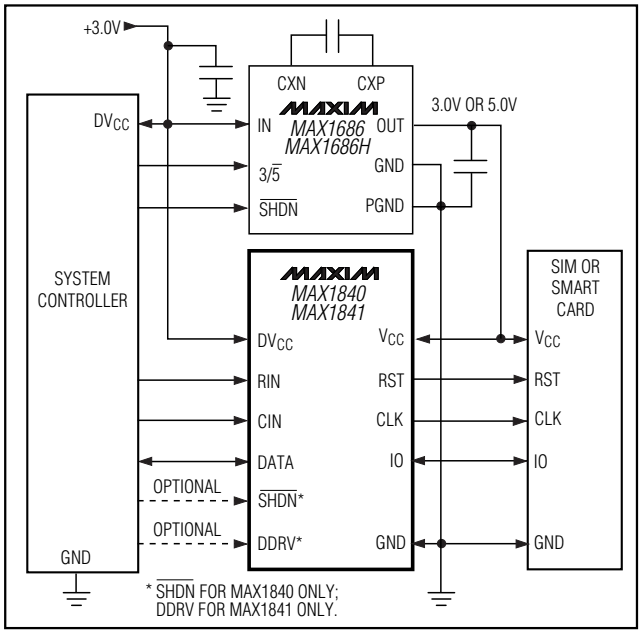


Figure 2. Using MAX1840/MAX1841 and MAX1686/MAX1686H Charge Pump for SIM Card Applications

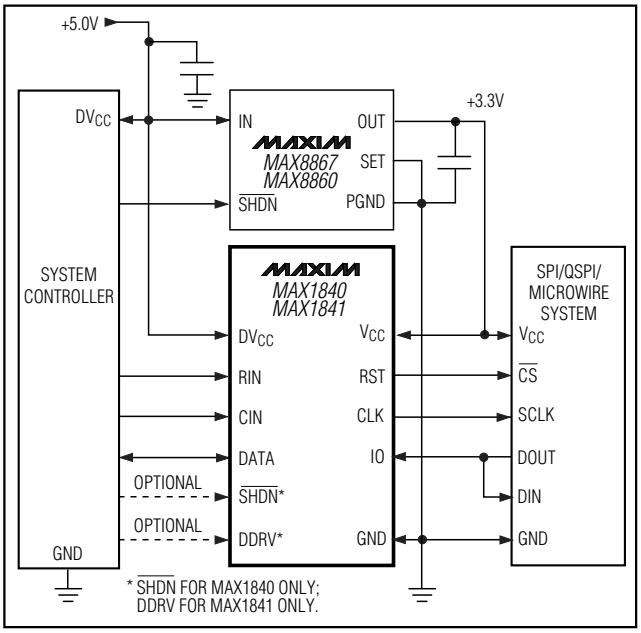


Figure 3. MAX1840/MAX1841 with SPI/QSPI/MICROWIRE Interfaces

0V/3V/5V for full compatibility with SIM/smart-card specifications. Figure 2 shows the charge pump for SIM card applications. Alternatively, the MAX619 generates a regulated 5V from input voltages as low as 2V.

SPI/QSPI/MICROWIRE Interface

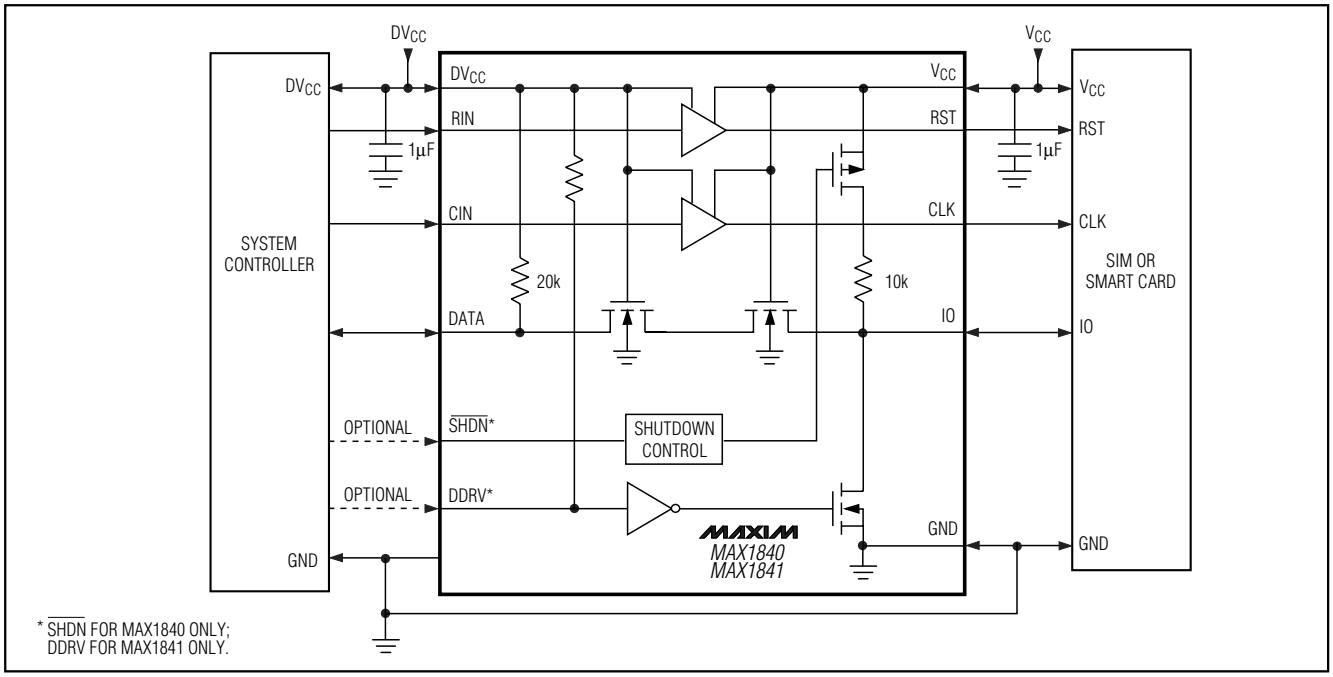
The MAX1840/MAX1841 are also useful as 3V/5V level shifters in SPI, QSPI, and MICROWIRE applications (Figure 3). On the slave side, connect CLK to SCLK, RST to $\overline{CS}$, and IO to DOUT and DIN. The unidirectional level shifters transfer chip select and clock signals to the slave device(s), while the bidirectional level shifter transfers data.

Chip Information

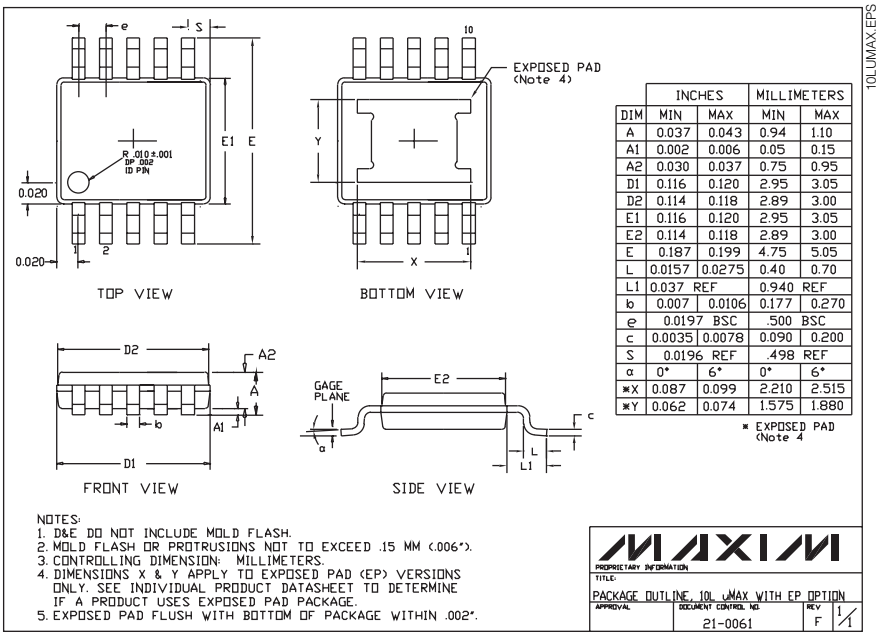
TRANSISTOR COUNT: 211

Low-Voltage SIM/Smart Card Level Translators in µMAX

Typical Application Circuit



Packaging Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.037	0.043	0.94	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
E	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°
*X	0.087	0.099	2.210	2.515
*Y	0.062	0.074	1.575	1.880

* EXPOSED PAD (Note 4

Note: *The MAX1840/MAX1841 do not have an exposed pad.*