Absolute Maximum Ratings

IN to SGND .....-0.3V to +30V
BST to SGND .....-0.3V to +35V
BST to LX .....-0.3V to +6V
DH to LX.....-0.3V to (V_{BST} - V_{LX}) + 0.3V
DL to PGND .....-0.3V to (V_{DD} + 0.3V)
V_{CC} to SGND .....-0.3V to +6V
V_{CC}, V_{DD} to PGND.....-0.3V to +6V
SGND to PGND.....-0.3V to +0.3V
V_{CC} Current 300mA

All Other Pins to SGND.....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN 5mm x 5mm (derate 34.5mW/°C above +70°C) 2758mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 5V, V_{DD} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Voltage Range	V_{IN}	Internal LDO on	7		28	V
		Internal LDO off (V_{CC} connected to V_{IN})	4.75		5.50	
Quiescent Supply Current	I_Q	V_{EN} = V_{CC} or SGND, no switching		2.7	5.5	mA
LED CURRENT REGULATOR						
Differential Set Value (V_{SENSE}+ to V_{SENSE}-) (Note 2)		V_{IN} = V_{CC} = 4.75V to 5.5V, f_{SW} = 500kHz (MAX16821A)	0.594	0.600	0.606	V
		V_{IN} = 7V to 28V, f_{SW} = 500kHz (MAX16821A)	0.594	0.600	0.606	
		V_{IN} = V_{CC} = 4.75V to 5.5V, f_{SW} = 500kHz (MAX16821B)	0.098	0.100	0.102	
		V_{IN} = 7V to 28V, f_{SW} = 500kHz (MAX16821B)	0.098	0.100	0.102	
		V_{IN} = V_{CC} = 4.75V to 5.5V, f_{SW} = 500kHz (MAX16821C)	0.028	0.030	0.032	
		V_{IN} = 7V to 28V, f_{SW} = 500kHz (MAX16821C)	0.028	0.030	0.032	
Soft-Start Time	t_{SS}			1024		Clock Cycles
STARTUP/INTERNAL REGULATOR						
V_{CC} Undervoltage Lockout (UVLO)	UVLO	V_{CC} rising	4.1	4.3	4.5	V
UVLO Hysteresis		V_{CC} falling		200		mV
V_{CC} Output Voltage		V_{IN} = 7V to 28V, I_{SOURCE} = 0 to 60mA	4.85	5.10	5.30	V
MOSFET DRIVER						
Output Driver Impedance		Low or high output, $I_{SOURCE/SINK}$ = 20mA		1.1	3	Ω
Output Driver Source/Sink Current	I_{DH}, I_{DL}			4		A
Nonoverlap Time	t_{NO}	$C_{DH/DL}$ = 5nF		35		ns

Electrical Characteristics (continued)

(V_{CC} = 5V, V_{DD} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Switching Frequency Range			125		1500	kHz
Switching Frequency	f_{SW}	R_T = 500kΩ	120	125	130	kHz
		R_T = 120kΩ	495	521	547	
		R_T = 39.9kΩ	1515	1620	1725	
Switching Frequency Accuracy		120kΩ < R_T ≤ 500kΩ	-5		+5	%
		40kΩ ≤ R_T ≤ 120kΩ	-8		+8	
CLKOUT Phase Shift with Respect to DH (Rising Edges)		f_{SW} = 125kHz, MODE connected to SGND		180		degrees
CLKOUT Phase Shift with Respect to DL (Rising Edges)		f_{SW} = 125kHz, MODE connected to V_{CC}		180		
CLKOUT Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
CLKOUT Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA	4.5			V
SYNC Input High Pulse Width	t_{SYNC}		200			ns
SYNC Input Clock High Threshold	V_{SYNCH}		2			V
SYNC Input Clock Low Threshold	V_{SYNCL}				0.4	V
SYNC Pullup Current	I_{SYNC_OUT}	$V_{RT/SYNC}$ = 0V		250	500	µA
SYNC Power-Off Level	V_{SYNC_OFF}				0.4	V
INDUCTOR CURRENT LIMIT						
Average Current-Limit Threshold	V_{CL}	CSP to CSN	26.4	27.5	33.0	mV
Reverse Current-Limit Threshold	V_{CLR}	CSP to CSN		-2.0		mV
Cycle-by-Cycle Current Limit		CSP to CSN		60		mV
Cycle-by-Cycle Overload		V_{CSP} to V_{CSN} = 75mV		260		ns
CURRENT-SENSE AMPLIFIER						
CSP to CSN Input Resistance	R_{CS}			4		kΩ
Common-Mode Range	$V_{CMR(CS)}$	V_{IN} = 7V to 28V	0		5.5	V
Input Offset Voltage	$V_{OS(CS)}$			0.1		mV
Amplifier Voltage Gain	$A_{V(CS)}$			34.5		V/V
3dB Bandwidth	f_{3dB}			4		MHz
CURRENT-ERROR AMPLIFIER (TRANSCONDUCTANCE AMPLIFIER)						
Transconductance	g_m			550		µS
Open-Loop Gain	$A_{VL(CE)}$			50		dB

Electrical Characteristics (continued)

(V_{CC} = 5V, V_{DD} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED CURRENT SIGNAL DIFFERENTIAL VOLTAGE AMPLIFIER (DIFF)						
Common-Mode Voltage Range	$V_{CMR (DIFF)}$		0		1.0	V
DIFF Output Voltage	V_{CM}	V_{SENSE+} = V_{SENSE-} = 0V		0.6		V
Input Offset Voltage	$V_{OS(DIFF)}$	MAX16821A	-3.7		+3.7	mV
		MAX16821B/MAX16821C	-1.5		+1.5	
Amplifier Voltage Gain	$A_{V(DIFF)}$	MAX16821A	0.992	1	1.008	V/V
		MAX16821B	5.85	6	6.1	
		MAX16821C	18.5	20	21.5	
3dB Bandwidth	f_{3dB}	MAX16821A, C_{DIFF} = 20pF		1.7		MHz
		MAX16821B, C_{DIFF} = 20pF		1600		kHz
		MAX16821C, C_{DIFF} = 20pF		550		
SENSE+ to SENSE- Input Resistance	R_{VS}	MAX16821A	50	100		kΩ
		MAX16821B	30	60		
		MAX16821C	10	20		
OUTV AMPLIFIER						
Gain-Bandwidth Product		V_{OUTV} = 2V		4		MHz
3dB Bandwidth		V_{OUTV} = 2V		1		MHz
Output Sink Current			30			µA
Output Source Current			80			µA
Maximum Load Capacitance				50		pF
OUTV to (CSP - CSN) Transfer Function		4mV ≤ C_{SP} – C_{SN} ≤ 32mV	132.5	135	137.7	V/V
Input Offset Voltage				1		mV
VOLTAGE-ERROR AMPLIFIER (EAOUT)						
Open-Loop Gain	A_{VOLEA}			70		dB
Unity-Gain Bandwidth	f_{GBW}			3		MHz
EAN Input Bias Current	$I_{B(EA)}$	V_{EAN} = 2V	-0.2	+0.03	+0.2	µA
Error Amplifier Output Clamping Voltage	$V_{CLAMP (EA)}$	With respect to V_{CM}	905	930	940	mV
INPUTS (MODE AND OVI)						
MODE Input-Voltage High			2			V
MODE Input-Voltage Low					0.8	V
MODE Pulldown Current			4	5	6	µA
OVI Trip Threshold	OVP_{TH}		1.244	1.276	1.308	V
OVI Hysteresis	OVI_{HYS}			200		mV
OVI Input Bias Current	I_{OVI}	V_{OVI} = 1V		0.2		µA

Electrical Characteristics (continued)

(V_{CC} = 5V, V_{DD} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

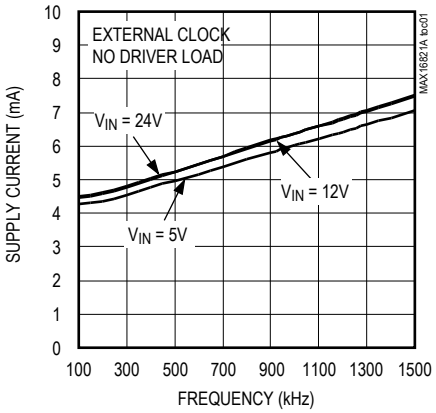
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE INPUT (EN)						
EN Input-Voltage High		EN rising	2.437	2.5	2.562	V
EN Input Hysteresis				0.28		V
EN Pullup Current	I_{EN}		13.5	15	16.5	µA
THERMAL SHUTDOWN						
Thermal Shutdown				165		°C
Thermal-Shutdown Hysteresis				20		°C

Note 1: All devices are 100% production tested at +25°C. Limits over temperature are guaranteed by design.
Note 2: Does not include an error due to finite error amplifier gain. See the *Voltage-Error Amplifier* section.

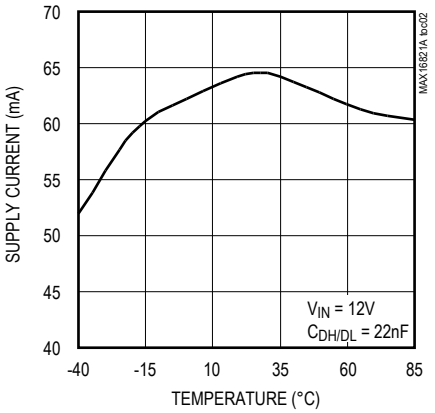
Typical Operating Characteristics

(V_{IN} = 12V, V_{DD} = V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

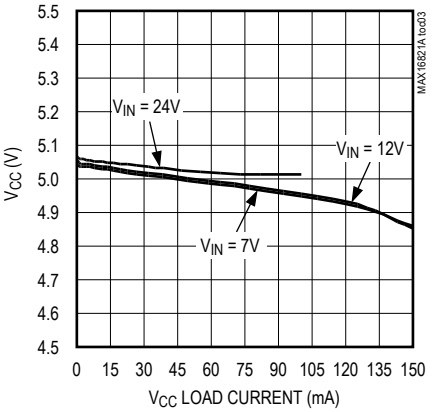
SUPPLY CURRENT (IQ) vs. FREQUENCY



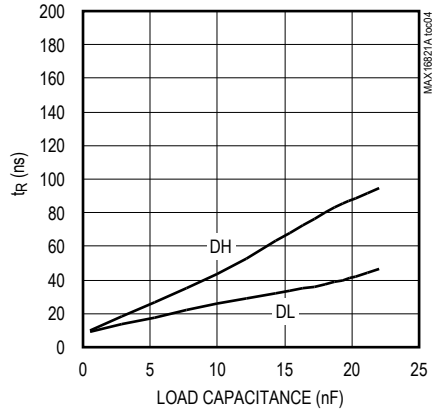
SUPPLY CURRENT vs. TEMPERATURE



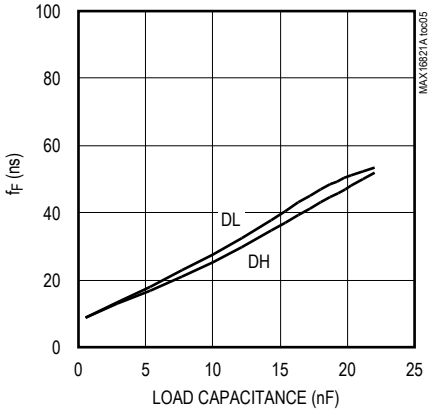
VCC LOAD REGULATION vs. VIN



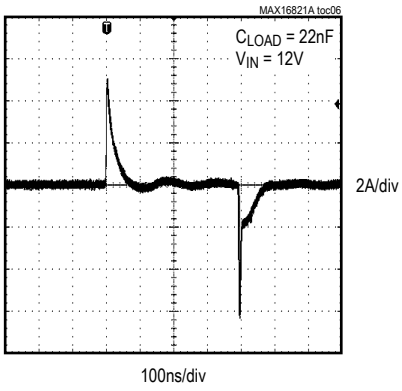
DRIVER RISE TIME
vs. DRIVER LOAD CAPACITANCE



DRIVER FALL TIME
vs. DRIVER LOAD CAPACITANCE



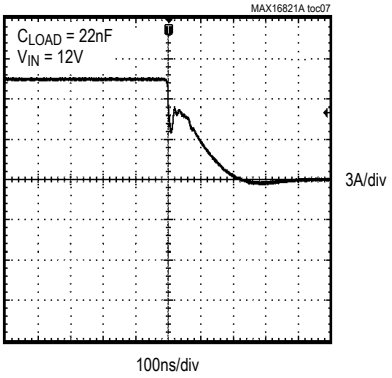
HIGH-SIDE DRIVER (DH) SINK
AND SOURCE CURRENT



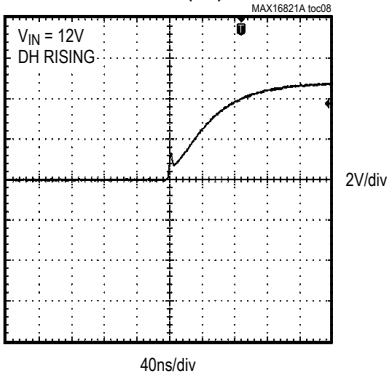
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{DD} = V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

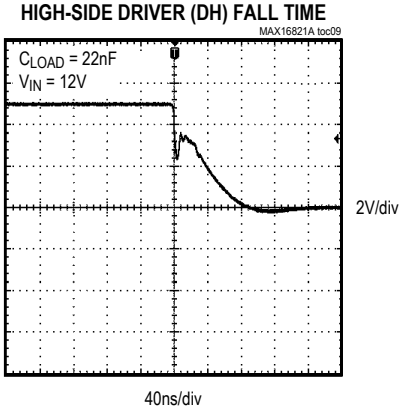
LOW-SIDE DRIVER (DL) SINK AND SOURCE CURRENT



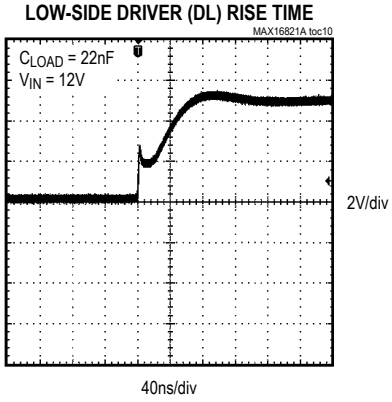
HIGH-SIDE DRIVER (DH) RISE TIME



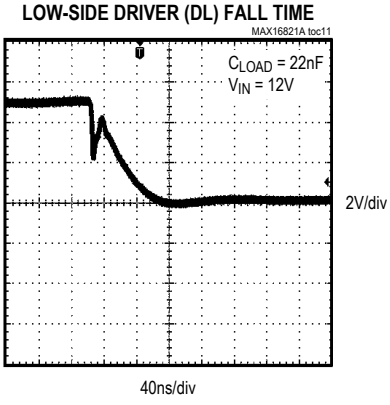
HIGH-SIDE DRIVER (DH) FALL TIME



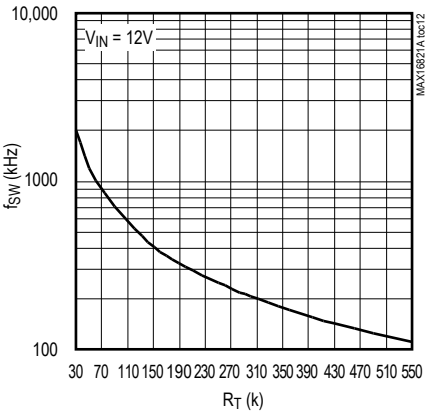
LOW-SIDE DRIVER (DL) RISE TIME



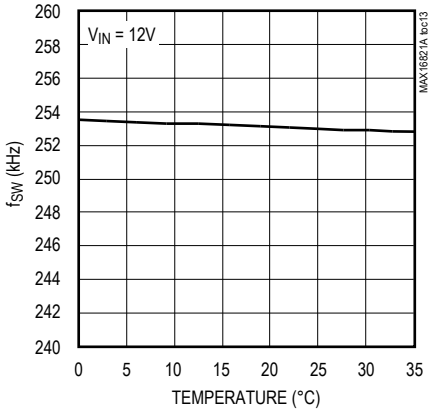
LOW-SIDE DRIVER (DL) FALL TIME



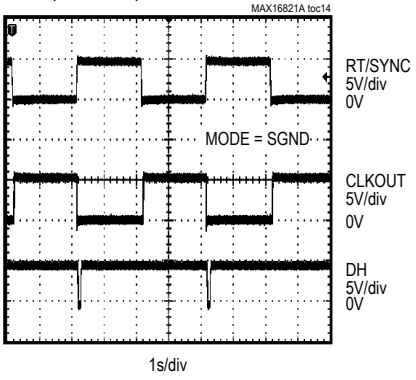
FREQUENCY vs. R_T



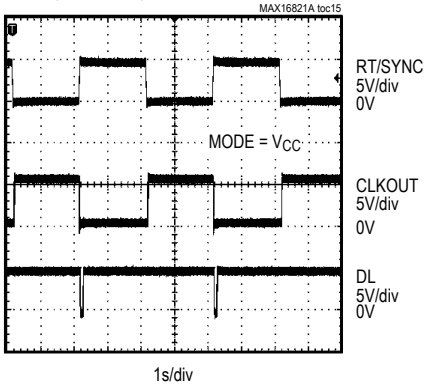
FREQUENCY vs. TEMPERATURE



SYNC, CLKOUT, AND DH WAVEFORMS



SYNC, CLKOUT, AND DL WAVEFORMS



Pin Description

PIN	NAME	FUNCTION
1	PGND	Power-Supply Ground
2, 7	N.C.	No Connection. Not internally connected.
3	DL	Low-Side Gate-Driver Output
4	BST	Boost-Flying Capacitor Connection. Reservoir capacitor connection for the high-side MOSFET driver supply. Connect a ceramic capacitor between BST and LX.
5	LX	High-Side MOSFET Source Connection
6	DH	High-Side Gate-Driver Output
8, 22, 25	SGND	Signal Ground. SGND is the ground connection for the internal control circuitry. Connect SGND and PGND together at one point near the IC.
9	CLKOUT	Oscillator Output. If MODE is low, the rising edge of CLKOUT phase shifts from the rising edge of DH by 180°. If MODE is high, the rising edge of CLKOUT phase shifts from the rising edge of DL by 180°.
10	MODE	Buck/Boost Mode Selection Input. Drive MODE low for low-side buck mode operation. Drive MODE high for boost or high-side buck mode operation. MODE has an internal 5µA pulldown current to ground.
11	EN	Output Enable. Drives EN high or leave unconnected for normal operation. Drive EN low to shut down the power drivers. EN has an internal 15µA pullup current.
12	RT/SYNC	Switching Frequency Programming. Connect a resistor from RT/SYNC to SGND to set the internal oscillator frequency. Drive RT/SYNC to synchronize the switching frequency with an external clock.
13	OUTV	Inductor Current-Sense Output. OUTV is an amplifier output voltage proportional to the inductor current. The voltage at OUTV = 135 x (V_{CSP} - V_{CSN}).
14	I.C.	Internally Connected. Connect to SGND for proper operation.
15	OVI	Overvoltage Protection. When OVI exceeds the programmed output voltage by 12.7%, the low-side and the high-side drivers are turned off. When OVI falls 20% below the programmed output voltage, the drivers are turned on after power-on reset and soft-start cycles are completed.
16	CLP	Current-Error-Amplifier Output. Compensate the current loop by connecting an RC network to ground.
17	EAOUT	Voltage-Error-Amplifier Output. Connect EAOUT to the external gain-setting network.
18	EAN	Voltage-Error-Amplifier Inverting Input
19	DIFF	Differential Remote-Sense Amplifier Output. DIFF is the output of a precision amplifier with SENSE+ and SENSE- as inputs.
20	CSN	Current-Sense Differential Amplifier Negative Input. The differential voltage between CSN and CSP is amplified internally by the current-sense amplifier (Gain = 34.5) to measure the inductor current.
21	CSP	Current-Sense Differential Amplifier Positive Input. The differential voltage between CSP and CSN is amplified internally by the current-sense amplifier (Gain = 34.5) to measure the inductor current.
23	SENSE-	Differential LED Current-Sensing Negative Input. Connect SENSE- to the negative side of the LED current- sense resistor or to the negative feedback point.
24	SENSE+	Differential LED Current-Sensing Positive Input. Connect SENSE+ to the positive side of the LED current- sense resistor, or to the positive feedback point.
26	IN	Supply Voltage Input. Connect IN to V_{CC}, for a 4.75V to 5.5V input supply range.
27	V_{CC}	Internal +5V Regulator Output. V_{CC} is derived from V_{IN}. Bypass V_{CC} to SGND with 4.7µF and 0.1µF ceramic capacitors.
28	V_{DD}	Low-Side Driver Supply Voltage
—	EP	Exposed Pad. EP is internally connected to SGND. Connect EP to a large-area ground plane for effective power dissipation. Connect EP to SGND. Do not use as a ground connection.

Detailed Description

The MAX16821A, MAX16821B, and MAX16821C are high-performance average current-mode PWM controllers for high-power and high-brightness LEDs (HB LEDs). The average current-mode control technique offers inherently stable operation, reduces component derating and size by accurately controlling the inductor current. The devices achieve high efficiency at high currents (up to 30A) with a minimum number of external components. A logic input (MODE) allows the LED driver to switch between buck and boost modes of operation.

The MAX16821A–MAX16821C feature a CLKOUT output 180° out-of-phase with respect to either the high-side or low-side driver, depending on MODE's logic level. CLKOUT provides the drive for a second out-of-phase LED driver for applications requiring reduced input capacitor ripple current while operating another LED driver.

The MAX16821A–MAX16821C consist of an inner average current regulation loop controlled by an outer loop. The combined action of the inner current loop and outer voltage loop corrects the LED current errors by adjusting the inductor current resulting in a tightly regulated LED current. The differential amplifier (SENSE+ and SENSE- inputs) senses the LED current using a resistor in series with the LEDs and produces an amplified version of the sense voltage at DIFF. The resulting amplified sensed voltage is compared against an internal 0.6V reference at the error amplifier input.

Input Voltage

The MAX16821A–MAX16821C operate with a 4.75V to 5.5V input supply range when the internal LDO is disabled (V_{CC} connected to IN) or a 7V to 28V input supply range when the internal LDO is enabled. For a 7V to 28V input voltage range, the internal LDO provides a regulated 5V output with 60mA of sourcing capability. Bypass V_{CC} to SGND with 4.7µF and 0.1µF low-ESR ceramic capacitors.

The MAX16821A–MAX16821C's V_{DD} input provides supply voltage for the low-side and the high-side MOSFET drivers. Connect V_{DD} to V_{CC} using an R-C filter to isolate the analog circuits from the MOSFET drivers. The internal LDO powers up the MAX16821A–MAX16821C. For applications utilizing a 5V input voltage, disable the internal LDO by connecting IN and V_{CC} together. The 5V power source must be in the 4.75V to 5.5V range of for proper operation of the MAX16821A–MAX16821C.

Undervoltage Lockout (UVLO)

The MAX16821A–MAX16821C include UVLO and a 2048 clock-cycle power-on-reset circuit. The UVLO rising threshold is set to 4.3V with 200mV hysteresis. Hysteresis at UVLO eliminates chattering during startup. Most of the internal circuitry, including the oscillator, turns on when the input voltage reaches 4V. The MAX16821A–MAX16821C draw up to 3.5mA of quiescent current before the input voltage reaches the UVLO threshold.

Soft-Start

The MAX16821A–MAX16821C include an internal soft-start for a glitch-free rise of the output voltage. After 2048 power-on-reset clock cycles, a 0.6V reference voltage connected to the positive input of the internal error amplifier ramps up to its final value after 1024 clock cycles. Soft-start reduces inrush current and stress on system components. During soft-start, the LED current will ramp monotonically towards its final value.

Internal Oscillator

The internal oscillator generates a clock with the frequency inversely proportional to the value of R_T (see the *Typical Operating Circuit*). The oscillator frequency is adjustable from 125kHz to 1.5MHz range using a single resistor connected from RT/SYNC to SGND. The frequency accuracy avoids the overdesign, size, and cost of passive filter components like inductors and capacitors. Use the following equation to calculate the oscillator frequency:

For 120kΩ ≤ R_T ≤ 500kΩ:

$$f_{SW} = \frac{6.25 \times 10^{10}}{R_T} (Hz)$$

For 40kΩ ≤ R_T ≤ 120kΩ:

$$f_{SW} = \frac{6.40 \times 10^{10}}{R_T} (Hz)$$

The oscillator also generates a $2V_{P-P}$ ramp signal for the PWM comparator and a 180° out-of-phase clock signal at CLKOUT to drive a second out-of-phase LED current regulator.

Synchronization

The MAX16821A–MAX16821C synchronize to an external clock connected to RT/SYNC. The application of an external clock at RT/SYNC disables the internal oscillator.

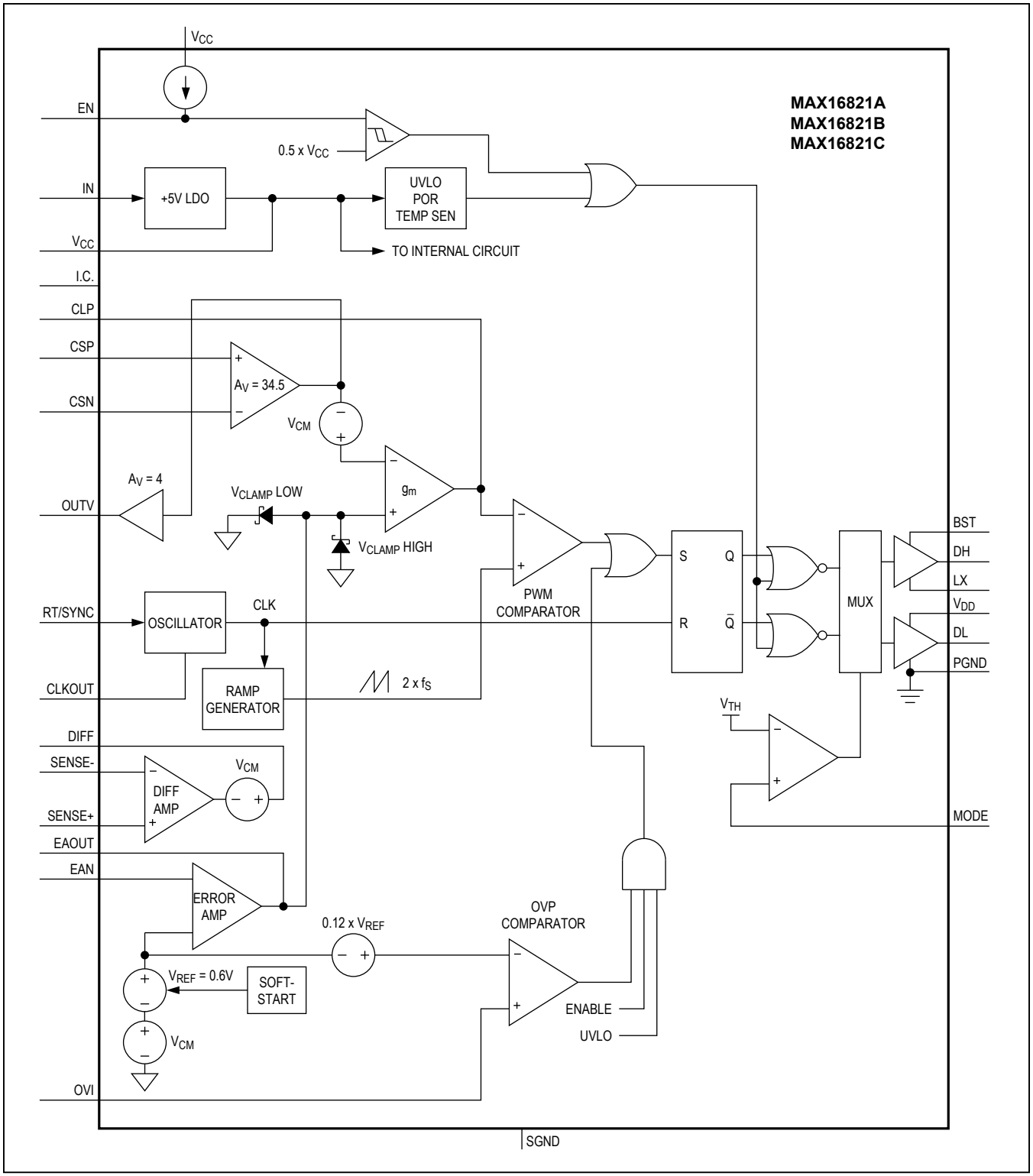


Figure 1. Internal Block Diagram

Once the MAX16821A–MAX16821C are synchronized to an external clock, the external clock cannot be removed if reliable operation is to be maintained.

Control Loop

The MAX16821A–MAX16821C use an average current-mode control scheme to regulate the output current (Figure 2). The main control loop consists of an inner current regulation loop for controlling the inductor current and an outer current regulation loop for regulating the LED current. The inner current regulation loop absorbs the double pole of the inductor and output capacitor combination reducing the order of the outer current regulation loop to that of a single-pole system. The inner current regulation loop consists of a current-sense resistor (R_S), a current-sense amplifier (CSA), a current-error amplifier (CEA), an oscillator providing the carrier ramp, and a PWM comparator (CPWM) (Figure 2). The MAX16821A–MAX16821C outer LED-current control loop consists of a differential amplifier (DIFF), a reference voltage, and a voltage-error amplifier (VEA).

Inductor Current-Sense Amplifier

The differential current-sense amplifier (CSA) provides a 34.5V/V DC gain. The typical input offset voltage of the current-sense amplifier is 0.1mV with a 0 to 5.5V common-mode voltage range (V_{IN} = 7V to 28V). The current-sense amplifier senses the voltage across R_S. The maximum common-mode voltage is 3.2V when V_{IN} = 5V.

Inductor Peak-Current Comparator

The peak-current comparator provides a path for fast cycle-by-cycle current limit during extreme fault conditions, such as an inductor malfunction (Figure 3). Note the average current-limit threshold of 27.5mV still limits the output current during short-circuit conditions. To prevent inductor saturation, select an inductor with a saturation current specification greater than the average current limit. The 60mV threshold for triggering the peak-current limit is twice the full-scale average current-limit voltage threshold. The peak-current comparator has only a 260ns delay.

Current-Error Amplifier

The MAX16821A–MAX16821C include a transconductance current-error amplifier with a typical g_m of 550µS and 320µA output sink and source capability. The current-

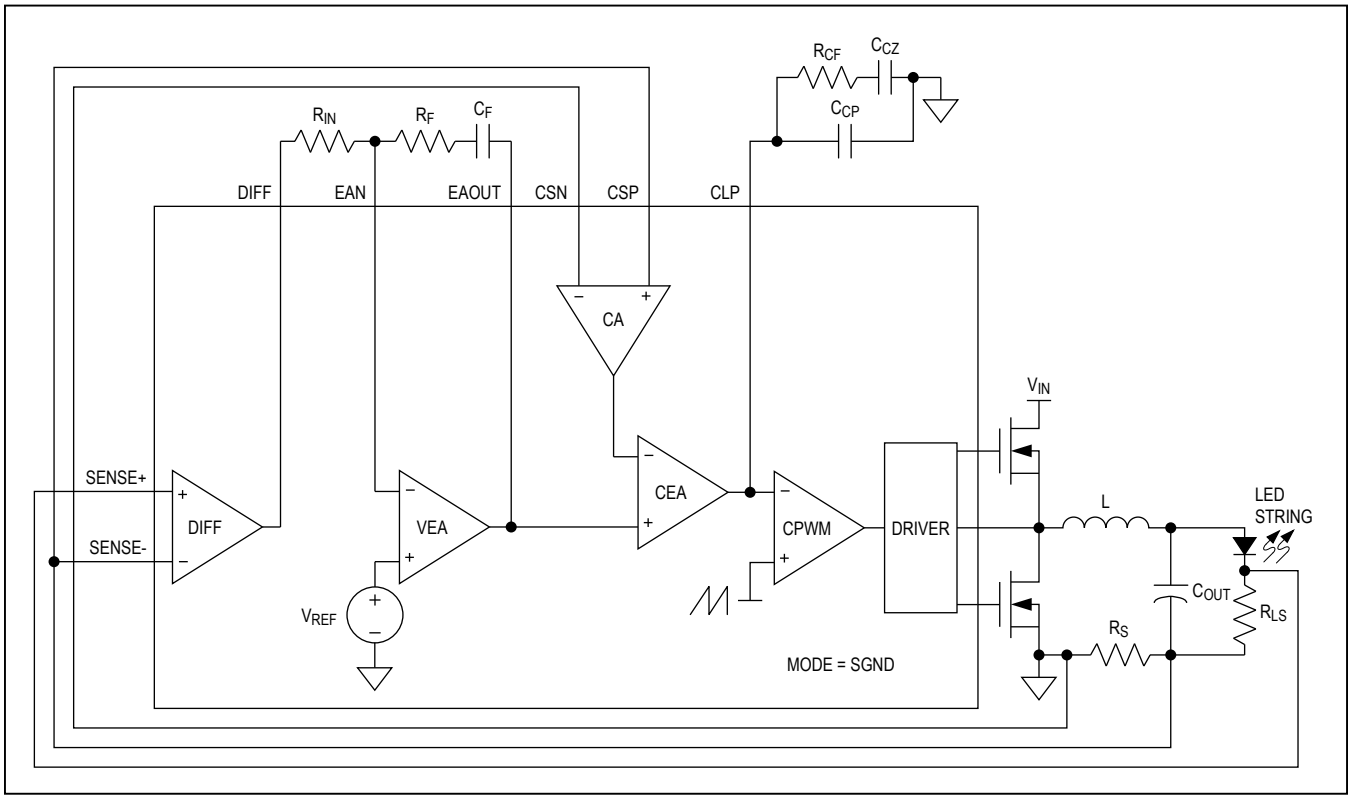


Figure 2. MAX16821A–MAX16821C Control Loop

error amplifier output (CLP) is connected to the inverting input of the PWM comparator. CLP is also externally accessible to provide frequency compensation for the inner current regulation loop (Figure 2). Compensate CEA so the inductor current negative slope, which becomes the positive slope to the inverting input of the PWM comparator, is less than the slope of the internally generated voltage ramp (see the *Compensation* section). In applications without synchronous rectification, the LED driver can be turned off and on instantaneously by shorting or opening the CLP to ground.

PWM Comparator and R-S Flip-Flop

An internal PWM comparator sets the duty cycle by comparing the output of the current-error amplifier to a $2V_{P-P}$ ramp signal. At the start of each clock cycle, an R-S flip-flop resets and the high-side driver (DH) turns on if MODE is connected to SGND, and DL turns on if MODE is connected to V_{CC}. The comparator sets the flip-flop as soon as the ramp signal exceeds the CLP voltage, thus terminating the ON cycle. See Figure 3.

Differential Amplifier

The differential amplifier (DIFF) allows LED current sensing (Figure 2). It provides true-differential LED current sensing, and amplifies the sense voltage by a factor of 1 (MAX16821A), 6 (MAX16821B), and 20 (MAX16821C), while rejecting common-mode voltage errors. The VEA provides the difference between the differential amplifier output (DIFF) and the desired LED current-sense voltage. The differential amplifier has a bandwidth of 1.7MHz (MAX16821A), 1.6MHz (MAX16821B), and 550kHz (MAX16821C). The difference between SENSE+ and SENSE- is regulated to +0.6V (MAX16821A), +0.1V (MAX16821B), or +0.03V (MAX16821C).

Voltage-Error Amplifier (VEA)

The VEA sets the gain of the voltage control loop, and determines the error between the differential amplifier

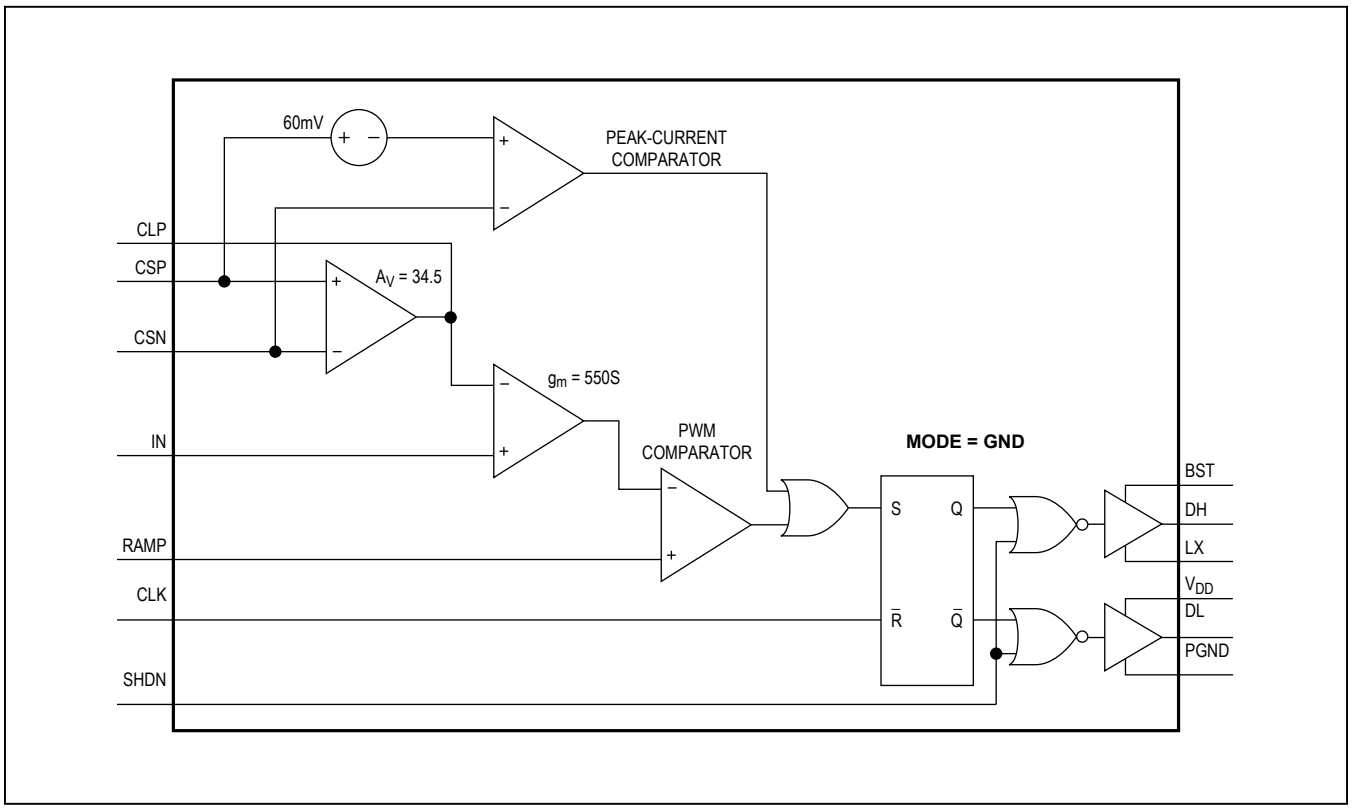


Figure 3. MAX16821A–MAX16821C Phase Circuit

output and the internal reference voltage. The VEA output clamps to 0.93V relative to the internal common- mode voltage, V_{CM} (+0.6V), limiting the average maximum current. The maximum average current-limit threshold is equal to the maximum clamp voltage of the VEA divided by the gain (34.5) of the current-sense amplifier. This results in accurate settings for the average maximum current.

MOSFET Gate Drivers

The high-side (DH) and low-side (DL) drivers drive the gates of external n-channel MOSFETs. The drivers' 4A peak sink- and source-current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced cross-conduction losses. Size the high-side and low-side MOSFETs to handle the peak and RMS currents during overload conditions. The driver block also includes a logic circuit that provides an adaptive nonoverlap time to prevent shoot-through currents during transition. The typical nonoverlap time is 35ns between the high-side and low-side MOSFETs.

BST

The MAX16821A–MAX16821C provide power to the low-side and high-side MOSFET drivers through V_{DD}. A bootstrap capacitor from BST to LX provides the additional boost voltage necessary for the high-side driver. V_{DD} supplies power internally to the low-side driver. Connect a 0.47µF low-ESR ceramic capacitor between BST and LX and a Schottky diode from BST to V_{DD}.

Protection

The MAX16821A–MAX16821C include output overvoltage protection (OVP). During fault conditions when the load goes to high impedance (output opens), the controller attempts to maintain LED current. The OVP disables the MAX16821A–MAX16821C whenever the output voltage exceeds the OVP threshold, protecting the external circuits from undesirable voltages.

Current Limit

The error amplifier (VEA) output is clamped between -0.050V and +0.93V with respect to common-mode voltage (V_{CM}). Average current-mode control limits the average current sourced by the converter during a fault condition. When a fault condition occurs, the VEA output clamps to +0.93V with respect to the common-mode voltage (0.6V) to limit the maximum current sourced by the converter to $I_{LIMIT} = 0.0275 / R_S$.

Overvoltage Protection

The OVP comparator compares the OVI input to the overvoltage threshold. The overvoltage threshold is typically 1.127 times the internal 0.6V reference voltage plus V_{CM} (0.6V). A detected overvoltage event trips the comparator output turning off both high-side and low-side MOSFETs. Add an RC delay to reduce the sensitivity of the overvoltage circuit and avoid unnecessary tripping of the converter (Figure 4). After the OVI voltage falls below 1.076V (typ.), high-side and low-side drivers turn on only after a 2048 clock-cycle POR and a 1024 clock-cycle soft-start have elapsed. Disable the overvoltage function by connecting OVI to SGND.

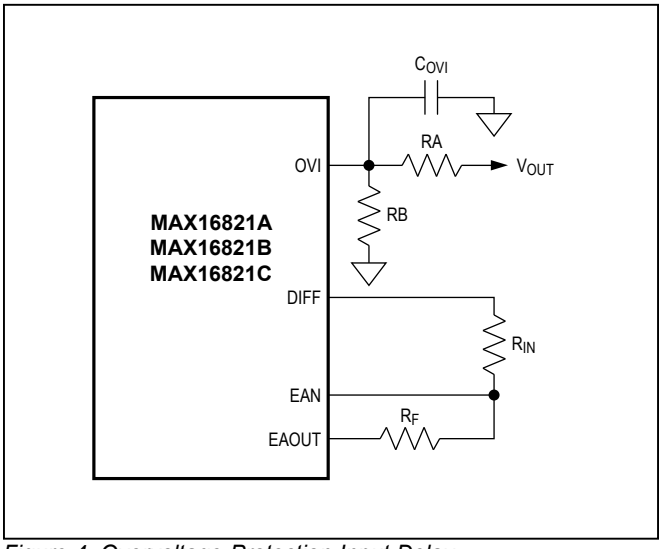


Figure 4. Overvoltage-Protection Input Delay

Applications Information

Boost LED Driver

Figure 5 shows the MAX16821A–MAX16821C configured as a synchronous boost converter with MODE connected to V_{CC}. During the on-time, the input voltage charges the inductor. During the off-time, the inductor discharges to the output. The output voltage cannot go below the input voltage in this configuration. Resistor R1 senses the inductor current and resistor R2 senses the LED current. The outer LED current regulation loop programs the average current in the inductor, thus achieving tight LED current regulation.

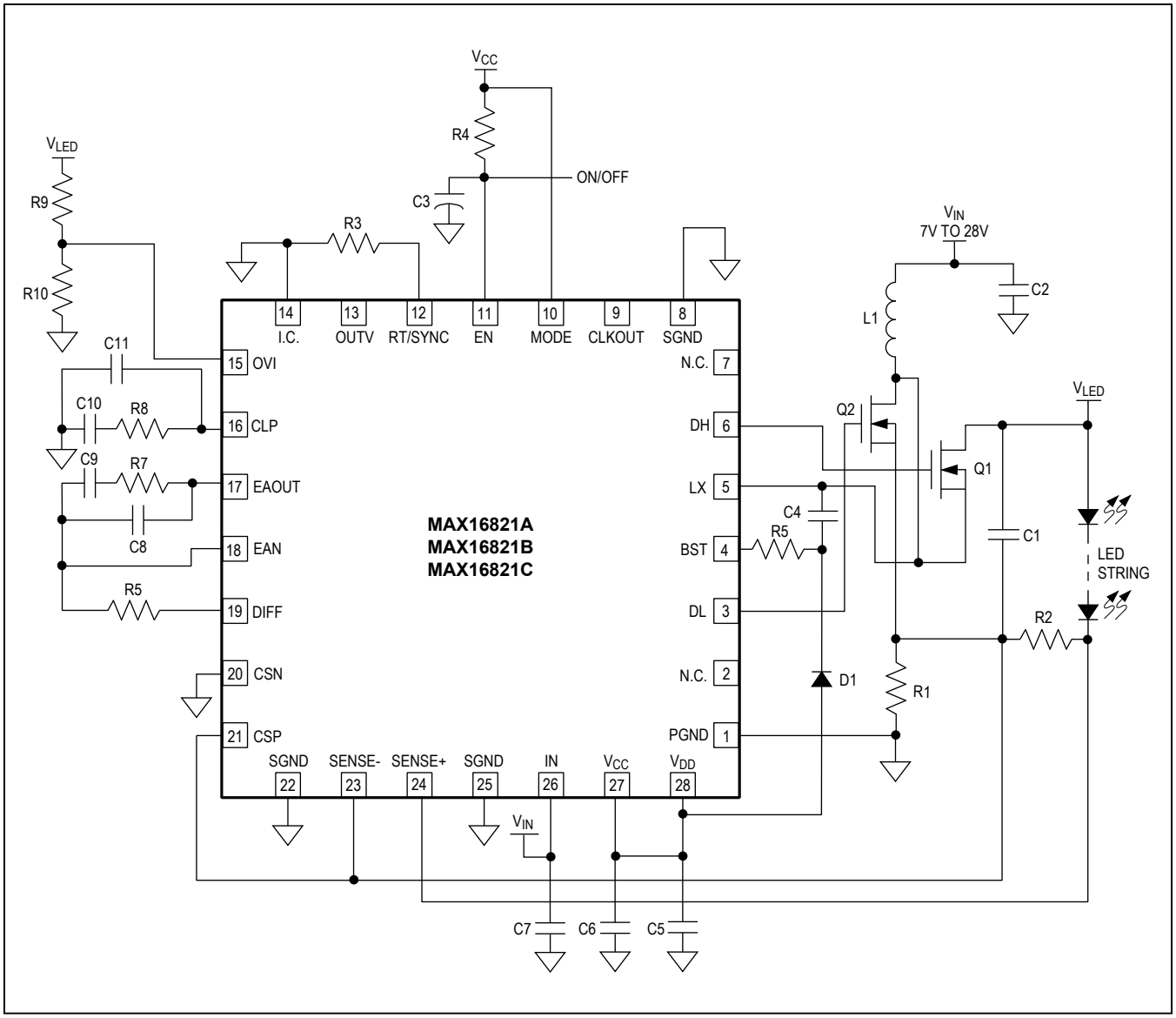


Figure 5. Synchronous Boost LED Driver (Output Voltage Not to Exceed 28V)

Input-Referenced Buck-Boost LED Driver

The circuit in Figure 6 shows a step-up/step-down regulator. It is similar to the boost converter in Figure 5 in that the inductor is connected to the input and the MOSFET is essentially connected to ground. However, rather than going from the output to ground, the LEDs span from the output to the input. This effectively removes the boost-only restriction of the regulator in Figure 5, allowing the voltage across the LED to be greater or less than the input voltage. LED current-sensing is not ground-referenced, so a high-side current-sense amplifier is used to measure current.

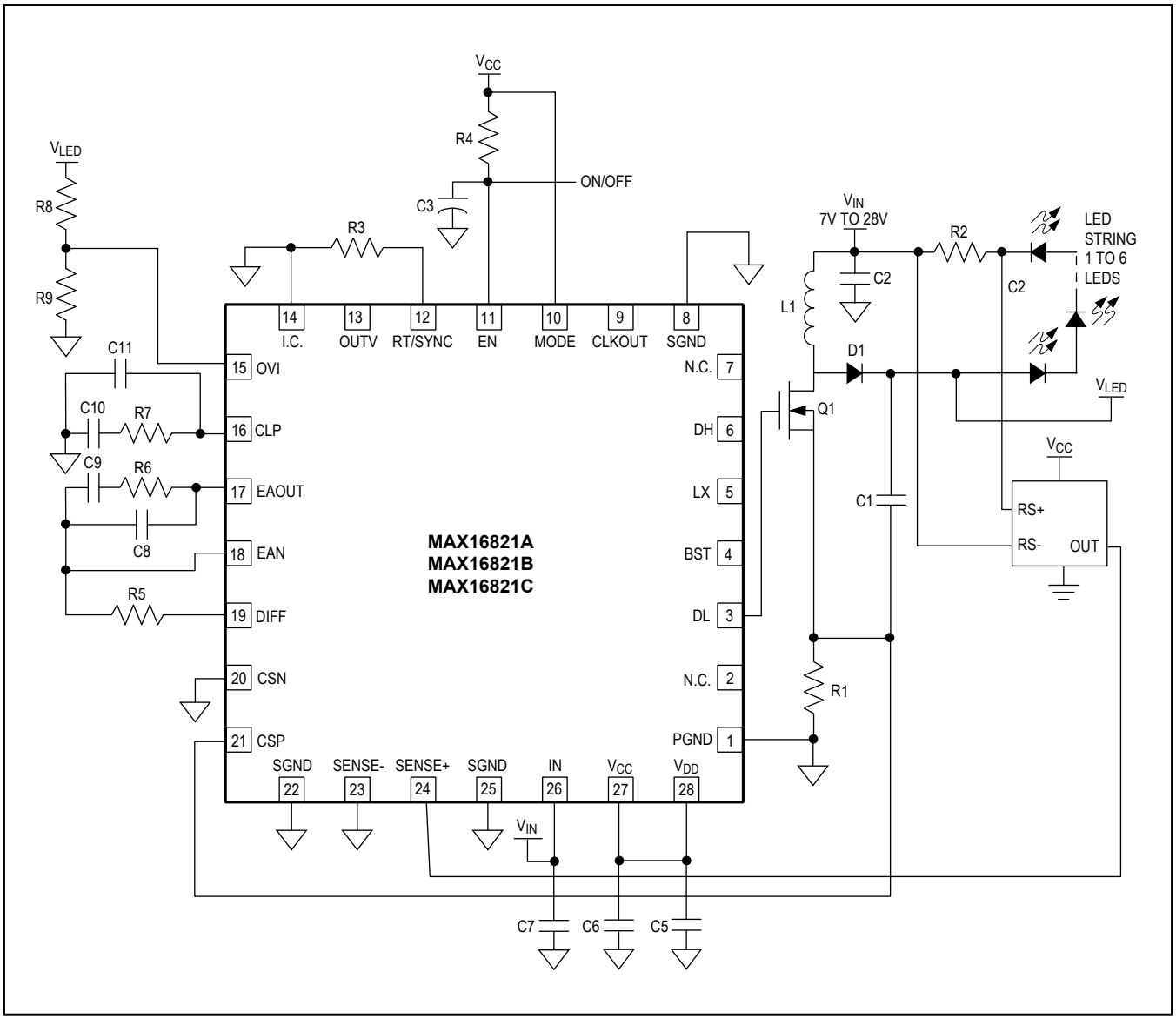


Figure 6. Typical Application Circuit for an Input-Referred Buck-Boost LED Driver (7V to 28V Input)

SEPIC LED Driver

Figure 7 shows the MAX16821A–MAX16821C configured as a SEPIC LED driver. While buck topologies produce an output always lower than the input, and boost topologies produce an output always greater than the input, a SEPIC topology allows the output voltage to be greater than, equal to, or less than the input. In a SEPIC topology, the voltage across C3 is the same as the input voltage, and L1 and L2 have the same inductance. Therefore, when Q1 turns on (on-time), the currents in both inductors (L1 and L2) ramp up at the same rate. The output capacitor supports the output voltage during this time. When Q1 turns off (off-time), L1 current recharges C3 and combines with L2 to provide current to recharge C1 and supplies the load current. Since the voltage waveform across L1 and L2 are exactly the same, it is possible to wind both inductors on the same core (a coupled inductor). Although voltages on L1 and L2 are the same, RMS currents can be quite different so the windings may require a different gauge wire. Because of the dual inductors and segmented energy transfer, the efficiency of a SEPIC converter is lower than the standard buck or boost configurations. As in the boost driver, the current-sense resistor connects to ground, allowing the output voltage of the LED driver to exceed the rated maximum voltage of the MAX16821A–MAX16821C.

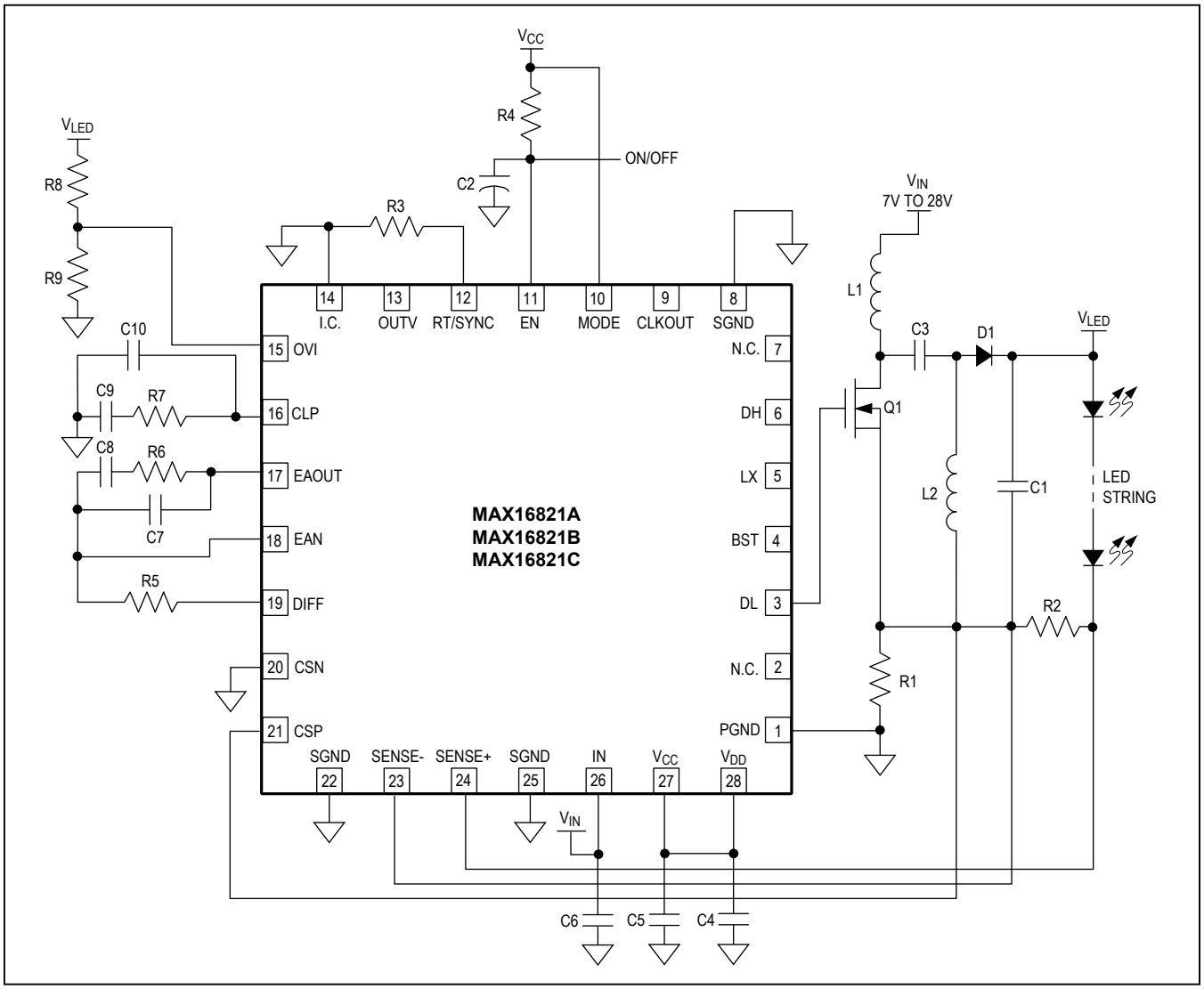


Figure 7. Typical Application Circuit for a SEPIC LED Driver

Low-Side Buck Driver with Synchronous Rectification

In Figure 8, the input voltage goes from 7V to 28V and, because of the ground-based current-sense resistor, the output voltage can be as high as the input. The synchronous MOSFET keeps the power dissipation to a minimum, especially when the input voltage is large compared to the voltage on the LED string. For the inner average current-loop inductor, current is sensed by resistor R1. To regulate the LED current, R2 creates a voltage that the differential amplifier compares to 0.6V. Capacitor C1 is small and helps reduce the ripple current in the LEDs. Omit C1 in cases where the LEDs can tolerate a higher ripple current. The average current-mode control scheme converts the input voltage to a current source feeding the LED string.

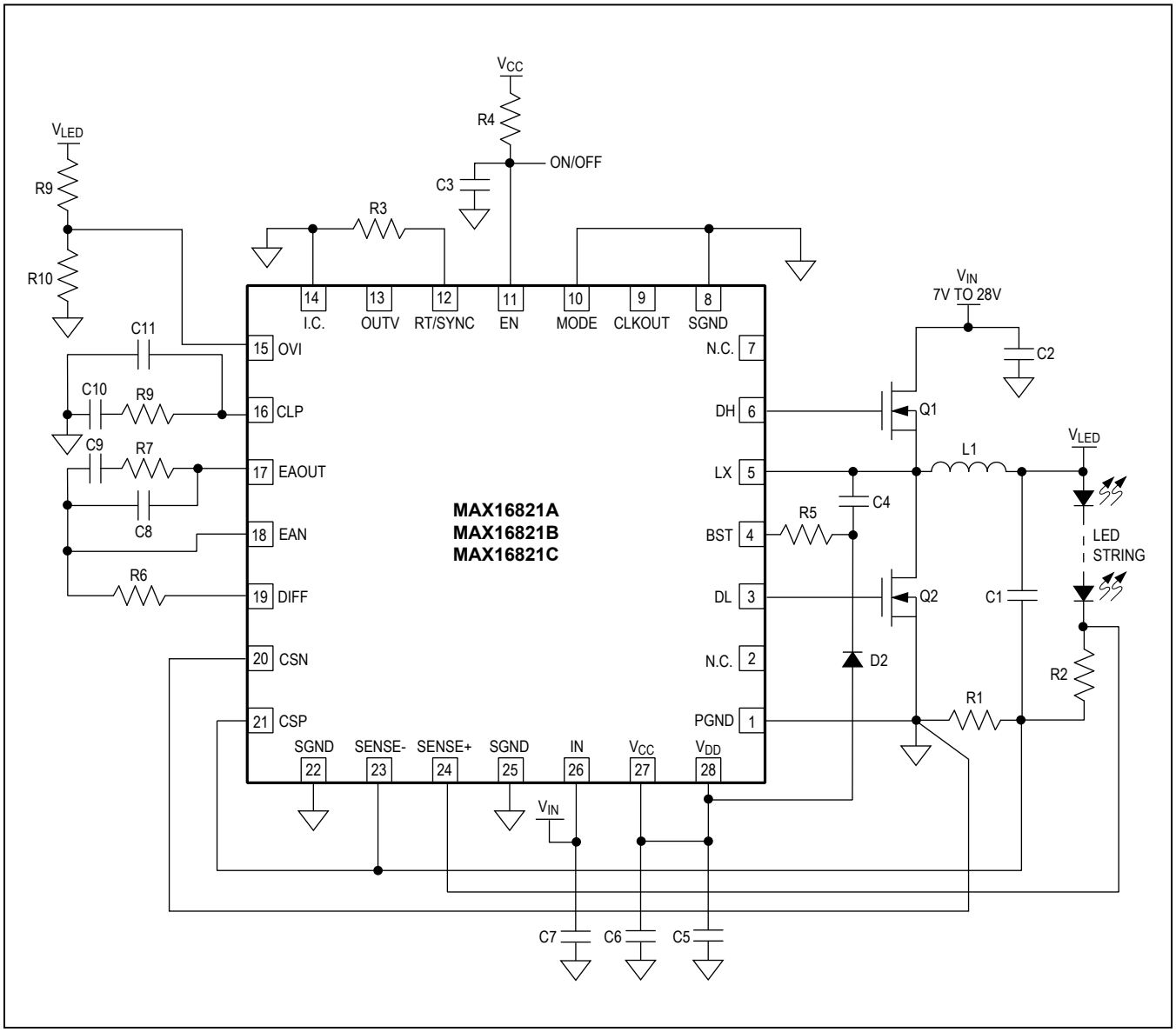


Figure 8. Application Circuit for a Low-Side Buck LED Driver

High-Side Buck Driver with Synchronous Rectification

In Figure 9, the input voltage goes from 7V to 28V, the LED load is connected from the positive side to the current-sense resistor (R1) in series with the inductor, and MODE is connected to V_{CC}. For the inner average current-loop inductor, current is sensed by resistor R1 and is then transferred to the low side by the high-side current-sense amplifier, U2. The voltage appearing across resistor R11 becomes the average inductor current-sense voltage for the inner average current loop. To regulate the LED current, R2 creates a voltage that the differential amplifier compares to its internal reference. Capacitor C1 is small and is added to reduce the ripple current in the LEDs. In cases where the LEDs can tolerate a higher ripple current, capacitor C1 can be omitted.

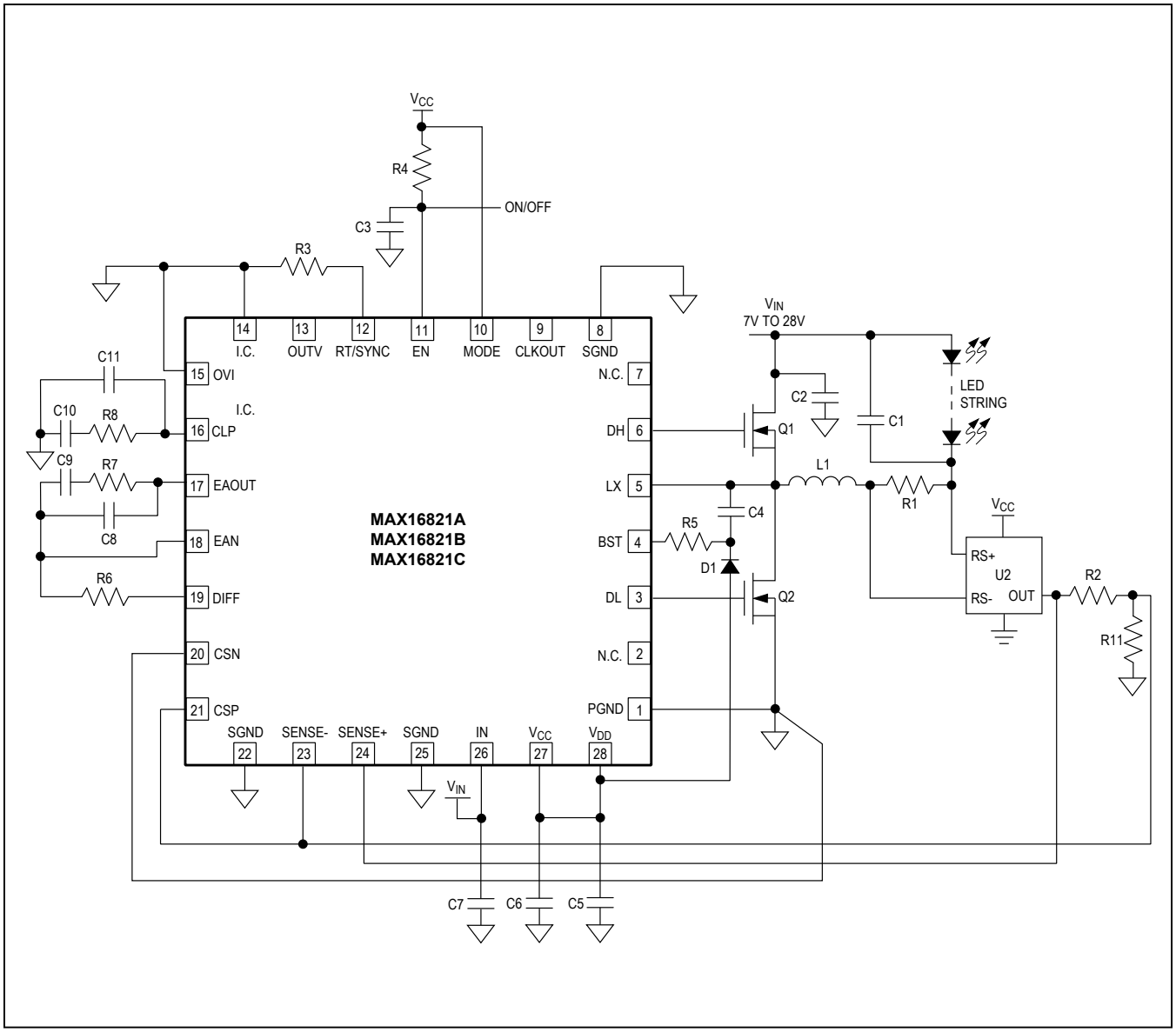


Figure 9. Application Circuit for a High-Side Buck LED Driver

Inductor Selection

The switching frequency, peak inductor current, and allowable ripple at the output determine the value and size of the inductor. Selecting higher switching frequencies reduces inductance requirements, but at the cost of efficiency. The charge/discharge cycle of the gate and drain capacitance in the switching MOSFETs create switching losses worsening at higher input voltages, since switching losses are proportional to the square of the input voltage. The MAX16821A–MAX16821C operate up to 1.5MHz.

Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. Particular applications may require custom-made inductors. Use high-frequency core material for custom inductors. High ΔI_L causes large peak-to-peak flux excursion increasing the core losses at higher frequencies. The high-frequency operation coupled with high ΔI_L reduces the required minimum inductance and makes the use of planar inductors possible.

The following discussion is for buck or continuous boost-mode topologies. Discontinuous boost, buck-boost, and SEPIC topologies are quite different in regards to component selection. Use the following equations to determine the minimum inductance value:

Buck regulators:

$$L_{MIN} = \frac{(V_{INMAX} - V_{LED}) \times V_{LED}}{V_{INMAX} \times f_{SW} \times \Delta I_L}$$

Boost regulators:

$$L_{MIN} = \frac{(V_{LED} - V_{INMAX}) \times V_{INMAX}}{V_{LED} \times f_{SW} \times \Delta I_L}$$

where V_{LED} is the total voltage across the LED string.

The average current-mode control feature of the MAX16821A–MAX16821C limits the maximum peak inductor current and prevents the inductor from saturating. Choose an inductor with a saturating current greater than the worst-case peak inductor current. Use the following equation to determine the worst-case current in the average current-mode control loop.

$$I_{LPEAK} = \frac{V_{CL}}{R_S} + \left(\frac{\Delta I_{CL}}{2}\right)$$

where R_S is the sense resistor and V_{CL} = 0.030V. For the buck converter, the sense current is the inductor current and for the boost converter, the sense current is the input current.

Switching MOSFETs

When choosing a MOSFET for voltage regulators, consider the total gate charge, RDS(ON), power dissipation, and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications. The average current from the MAX16821A–MAX16821C gate-drive output is proportional to the total capacitance it drives from DH and DL. The power dissipated in the MAX16821A–MAX16821C is proportional to the input voltage and the average drive current. The gate charge and drain capacitance losses (CV2), the cross-conduction loss in the upper MOSFET due to finite rise/fall time, and the I2R loss due to RMS current in the MOSFET $R_{DS(ON)}$ account for the total losses in the MOSFET. Estimate the power loss ($PD_{MOS\_}$) in the high-side and low-side MOSFETs using the following equations:

$$PD_{MOS\_HI} = (Q_G \times V_{DD} \times f_{SW}) + \left[\frac{V_{IN} \times I_{LED} \times (t_R + t_F) \times f_{SW}}{2}\right] + R_{DS(ON)} \times I^2_{RMS-HI}$$

where Q_G, $R_{DS(ON)}$, t_R, and t_F are the upper-switching MOSFET's total gate charge, on-resistance, rise time, and fall time, respectively.

$$I_{RMS-HI} = \sqrt{\left(I^2_{VALLEY} + I^2_{PK} + I_{VALLEY} \times I_{PK}\right) \times \frac{D}{3}}$$

For the buck regulator, D is the duty cycle, I_{VALLEY} = (I_{OUT} - ΔI_L / 2) and I_{PK} = (I_{OUT} + ΔI_L / 2).

$$PD_{MOS\_LO} = (Q_G \times V_{DD} \times f_{SW}) + R_{DS(ON)} \times I^2_{RMS-LO}$$

$$I_{RMS-LO} = \sqrt{\left(I^2_{VALLEY} + I^2_{PK} + I_{VALLEY} \times I_{PK}\right) \times \frac{(1-D)}{3}}$$

Input Capacitors

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor).

Use low-ESR ceramic capacitors with high ripple-current capability at the input. In the case of the boost topology where the inductor is in series with the input, the ripple current in the capacitor is the same as the inductor ripple and the input capacitance is small.

Output Capacitors

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most of the applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance.

In a buck configuration, the output capacitance, C_{OUT}, is calculated using the following equation:

$$C_{OUT} \geq \frac{(V_{INMAX} - V_{LED}) \times V_{LED}}{\Delta V_R \times 2 \times L \times V_{INMAX} \times f_{SW}^2}$$

where ΔV_R is the maximum allowable output ripple.

In a boost configuration, the output capacitance, C_{OUT}, is calculated as:

$$C_{OUT} \geq \frac{(V_{LED} - V_{INMIN}) \times 2 \times I_{LED}}{\Delta V_R \times V_{LED} \times f_{SW}}$$

where I_{LED} is the output current.

In a buck-boost configuration, the output capacitance, C_{OUT} is:

$$C_{OUT} \geq \frac{2 \times V_{LED} \times I_{LED}}{\Delta V_R \times (V_{LED} + V_{INMIN}) \times f_{SW}}$$

where V_{LED} is the voltage across the load and I_{LED} is the output current.

Average Current Limit

The average current-mode control technique of the MAX16821A–MAX16821C accurately limits the maximum output current in the case of the buck configuration. The MAX16821A–MAX16821C sense the voltage across the sense resistor and limit the peak inductor current (I_{L-PK}) accordingly. The on-cycle terminates when the current-sense voltage reaches 26.4mV (min). Use the following equation to calculate the maximum current-sense resistor value:

$$R_{SENSE} = \left(\frac{0.0264}{I_{LED}}\right)$$

Select a 5% lower value of R_S to compensate for any parasitics associated with the PCB. Select a non-inductive resistor with the appropriate wattage rating. In the case of the boost configuration, the MAX16821A–MAX16821C accurately limits the maximum input current. Use the following equation to calculate the current-sense resistor value:

$$R_{SENSE} = \left(\frac{0.0264}{I_{IN}}\right)$$

where I_{IN} is the input current.

Compensation

The main control loop consists of an inner current loop (inductor current) and an outer LED current regulation loop. The MAX16821A–MAX16821C use an average current-mode control scheme to regulate the LED current (Figure 2). The VEA output provides the controlling voltage for the current source. The inner current loop absorbs the inductor pole reducing the order of the LED current loop to that of a single-pole system. The major consideration when designing the current control loop is making certain that the inductor downslope (which becomes an upslope at the output of the CEA) does not exceed the internal ramp slope. This is a necessary condition to avoid subharmonic oscillations similar to those in peak current mode with insufficient slope compensation. This requires that the gain at the output of the CEA be limited based on the following equation:

Buck:

$$R_{CF} \leq \frac{V_{RAMP} \times f_{SW} \times L}{A_V \times R_S \times V_{LED} \times g_m}$$

where V_{RAMP} = 2V, g_m = 550µS, A_V = 34.5V/V, and V_{LED} is the voltage across the LED string.

The crossover frequency of the inner current loop is given by:

$$f_C = \frac{R_S}{V_{RAMP}} \times \frac{V_{IN}}{2 \times \pi \times L} \times 34.5 \times g_m \times R_{CF}$$

For adequate phase margin place the zero formed by R_{CF} and C_{CZ} at least 3 to 5 times below the crossover frequency. The pole formed by R_{CF} and C_{CP} may not be required in most applications but can be added to minimize noise at a frequency at or above the switching frequency.

Boost:

$$R_{CF} \le \frac{V_{RAMP} \times f_{SW} \times L}{A_V \times R_S \times (V_{LED} - V_{IN}) \times g_m}$$

The crossover frequency of the inner current loop is given by:

$$f_C = \frac{R_S}{V_{RAMP}} \times \frac{V_{LED}}{2 \times \pi \times L} \times 34.5 \times g_m \times R_{CF}$$

For adequate phase margin at crossover, place the zero formed by R_{CF} and C_{CZ} at least 3 to 5 times below the crossover frequency. The pole formed by R_{CF} and C_{CP} is added to eliminate noise spikes riding on the current waveform and is placed at the switching frequency.

PWM Dimming

Even though the MAX16821A–MAX16821C do not have a separate PWM input, PWM dimming can be easily achieved by means of simple external circuitry. See Figures 10 and 11.

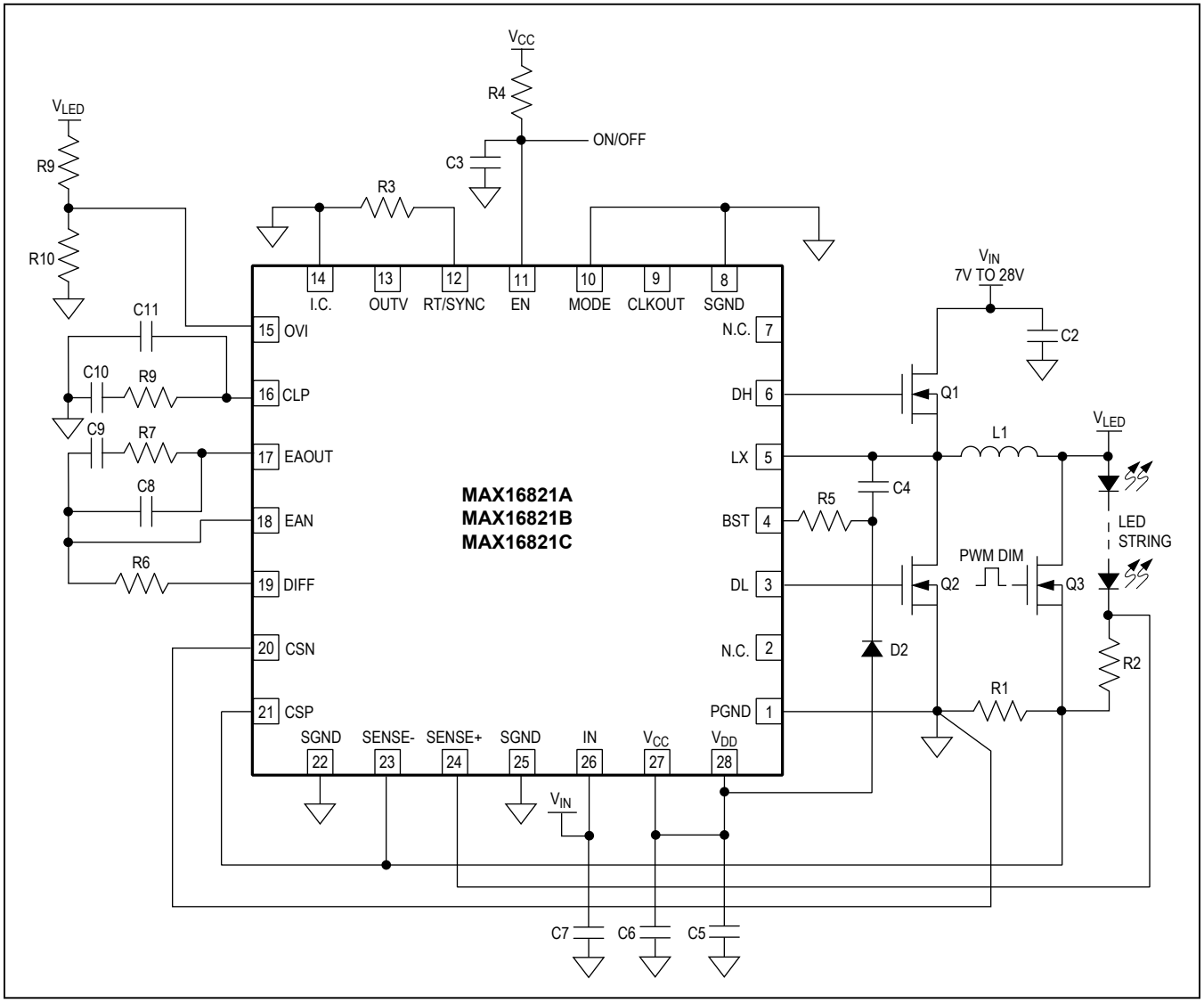


Figure 10. Low-Side Buck LED Driver with PWM Dimming

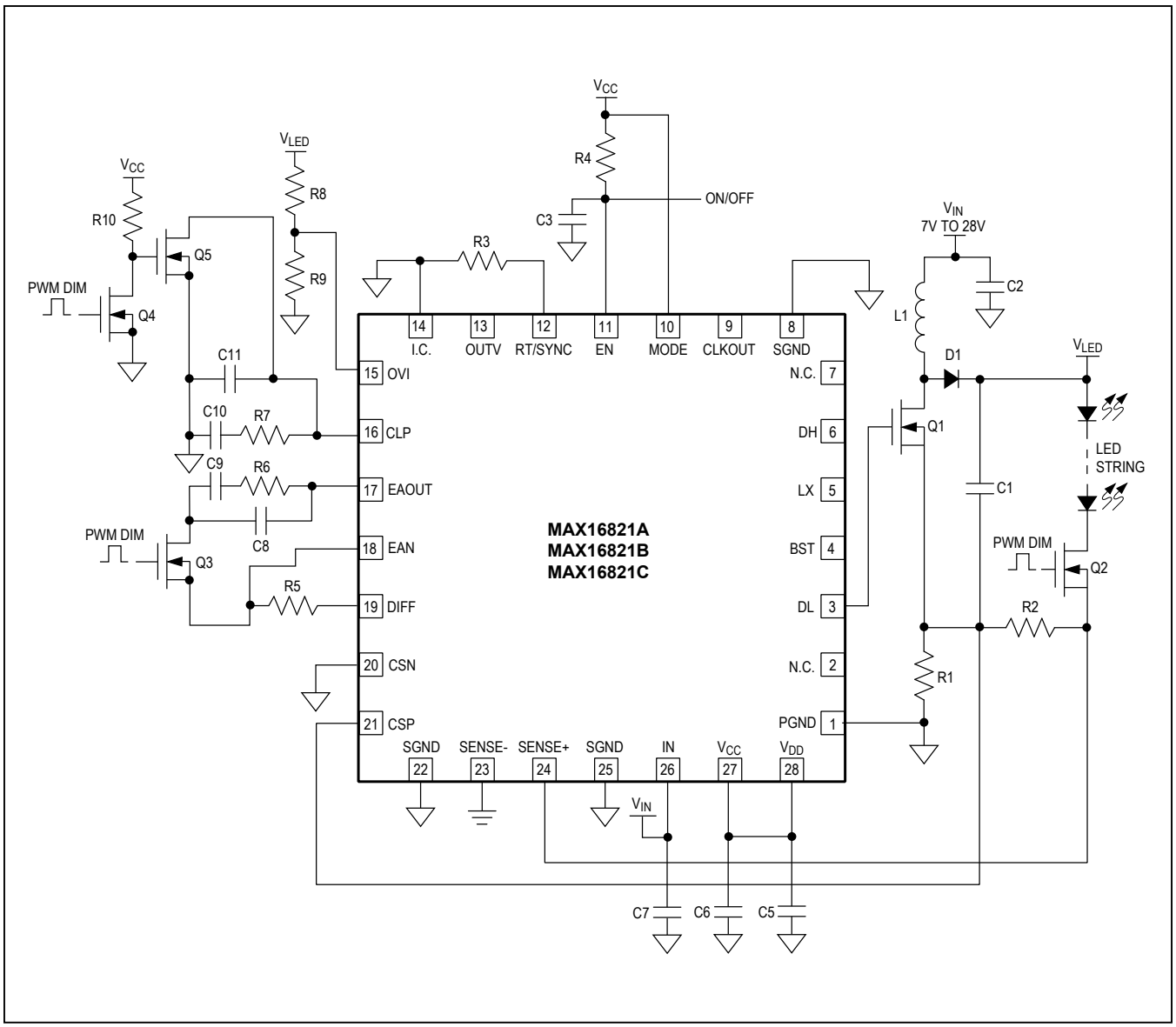


Figure 11. Boost LED Driver with PWM Dimming

Power Dissipation

Calculate power dissipation in the MAX16821A–MAX16821C as a product of the input voltage and the total V_{CC} regulator output current (I_{CC}). I_{CC} includes quiescent current (I_Q) and gate-drive current (I_{DD}):

$$P_D = V_{IN} \times I_{CC}$$

$$I_{CC} = I_Q + [f_{SW} \times (Q_{G1} + Q_{G2})]$$

where Q_{G1} and Q_{G2} are the total gate charge of the low-side and high-side external MOSFETs at V_{GATE} = 5V, I_Q is the supply current, and f_{SW} is the switching frequency of the LED driver.

Use the following equation to calculate the maximum power dissipation (P_{DMAX}) in the chip at a given ambient temperature (T_A):

$$P_{DMAX} = 34.5 \times (150 - T_A)\ mW$$

PCB Layout

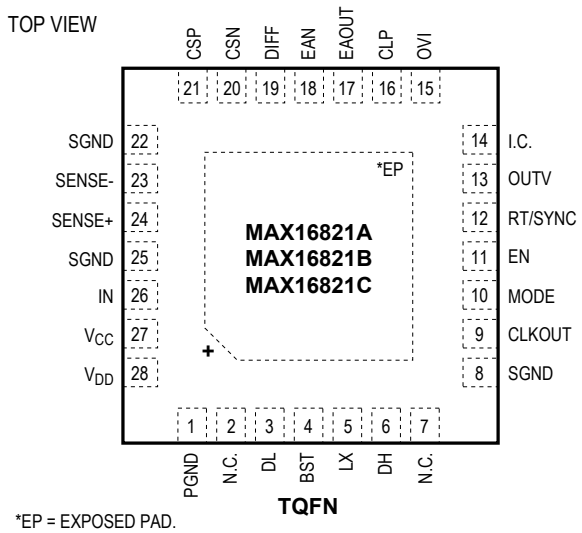
Use the following guidelines to layout the LED driver.

1) Place the IN, V_{CC}, and V_{DD} bypass capacitors close to the MAX16821A–MAX16821C.
2) Minimize the area and length of the high-current switching loops.
3) Place the necessary Schottky diodes that are connected across the switching MOSFETs very close to the respective MOSFET.
4) Use separate ground planes on different layers of the PCB for SGND and PGND. Connect both of these planes together at a single point and make this connection under the exposed pad of the MAX16821A–MAX16821C.
5) Run the current-sense lines CSP and CSN very close to each other to minimize the loop area. Run the sense lines SENSE+ and SENSE- close to each other. Do not cross these critical signal lines with power circuitry. Sense the current right at the pads of the current-sense resistors. The current-sense signal has a maximum amplitude of 27.5mV. To prevent contamination of this signal from high dv/dt and high di/dt components and traces, use a ground plane layer to separate the power traces from this signal trace.
6) Place the bank of output capacitors close to the load.
7) Distribute the power components evenly across the board for proper heat dissipation.
8) Provide enough copper area at and around the switching MOSFETs, inductor, and sense resistors to aid in thermal dissipation.
9) Use 2oz or thicker copper to keep trace inductances and resistances to a minimum. Thicker copper conducts heat more effectively, thereby reducing thermal impedance. Thin copper PCBs compromise efficiency in applications involving high currents.

Selector Guide

PART	DIFFERENTIAL SET VALUE (VSENSE+ - VSENSE-) (V)	DIFFERENTIAL AMP GAIN (V/V)
MAX16821A	0.60	1
MAX16821B	0.10	6
MAX16821C	0.03	20

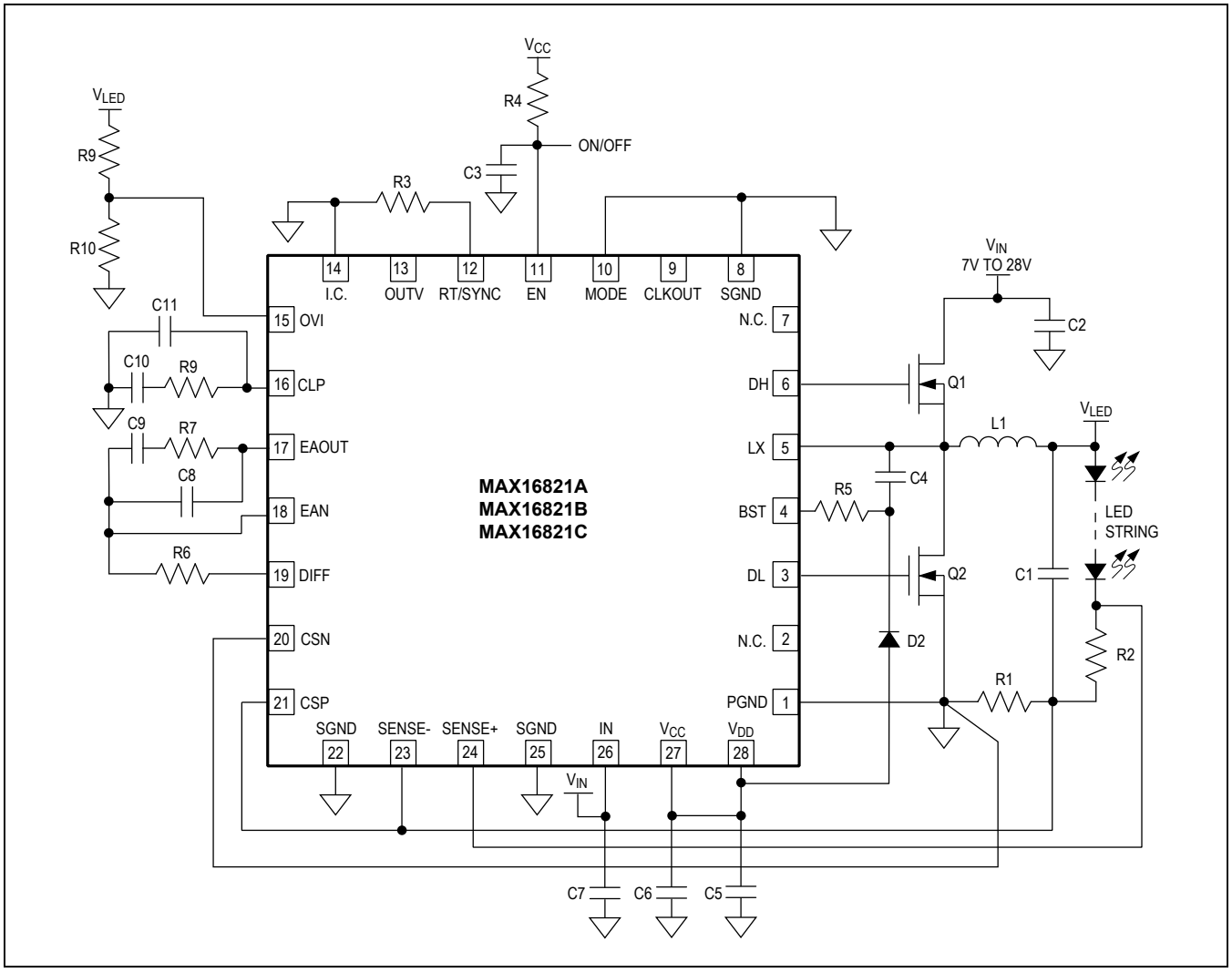
Pin Configuration



Chip Information

PROCESS: BiCMOS

Typical Operating Circuit



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2855+8	21-0140

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/07	Initial release	—
1	3/09	Updated *Electrical Characteristics* table.	3, 4
2	1/10	—	—
3	4/14	No /V OPNs; removed automotive references from *Applications* section	1
4	4/18	Added label above part number indicating parts are not recommended for new designs and to refer to the MAX20078	1