Absolute Maximum Ratings

(All pins referenced to GND.)
IN .....-36V to +90V
$\overline{SHDN}$ .....-0.3V to max (0V, V_{IN} + 0.3V)
TERM .....-0.3V to max (0V, V_{IN} + 0.3V)
SRC, GATE .....-36V to +45V
SRC to GATE .....-36V to +36V
OUT .....-0.3V to +45V
$\overline{FLAG}$ .....-0.3V to +45V
OVSET, UVSET.....-0.3V to +6V

Continuous Sink/Source (all pins).....±100mA
Continuous Power Dissipation (T_A = +70°C) (multilayer board)
TQFN (derate 14.7mW/°C above +70°C).....1176.5mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....46.91°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....5.27°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 12V, $C_{GATE-SOURCE}$ = 1nF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Operating range		3		30	V
		Protection range		-36		+90	
Input Supply Current	I_{IN}	$\overline{SHDN}$ = high	V_{IN} = V_{SRC} = V_{OUT} = 12V		224	360	µA
			V_{IN} = V_{SRC} = V_{OUT} = 30V		260	400	
		$\overline{SHDN}$ = low	V_{IN} = 12V		34	60	
			V_{IN} = 30V		64	100	
SRC Input Current	I_{SRC}	V_{SRC} = V_{IN} = 12V, $\overline{SHDN}$ = high			136	200	µA
		V_{SRC} = V_{IN} = 30V, $\overline{SHDN}$ = high			240	350	
IN Undervoltage Lockout	V_{UVLO}	V_{IN} rising				2.92	V
OVSET/UVSET Input Current	$I_{UVSET/OVSET}$					100	nA
OVSET/UVSET Threshold (Rising)	V_{TH}	V_{IN} rising		1.2	1.225	1.25	V
OVSET/UVSET Threshold Hysteresis	V_{TH-HYS}				0.05 x V_{TH}		V
POK Threshold Rising	V_{POK+}				0.9 x V_{IN}		V
POK Threshold Falling	V_{POK-}				0.87 x V_{IN}		V
TERM On-Resistance	R_{TERM}				0.7	1.2	kΩ

Electrical Characteristics (continued)

(V_{IN} = 12V, $C_{GATE-SOURCE}$ = 1nF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Startup Response Time	t_{START}	(Note 3)		150		µs
Autoretry Timeout	t_{RETRY}			150		ms
GATE Rise Time	t_{RISE}	V_{GATE} rising (GND to V_{SRC} + 8V)		1		ms
OVSET-to-GATE Propagation Delay	t_{OVG}	V_{OVSET} rising (V_{TH} - 100mV to V_{TH} + 100mV)			0.55	µs
UVSET-to-GATE Propagation Delay	t_{UVG}	V_{UVSET} falling (V_{TH} + 100mV to V_{TH} - 100mV)		20		µs
Output Input Resistance to GND	R_{OUT}	MAX16126		4		MΩ
		MAX16127		2		
OVSET-to-FLAG Propagation Delay	t_{OV}	V_{OVSET} rising (V_{TH} - 100mV to V_{TH} + 100mV)		0.3		µs
GATE Output Voltage High Above V_{SRC}	V_{GS}	V_{IN} = V_{SRC} = V_{OUT} = 3V, I_{GATE} = -1µA	4.25	5	5.5	V
		V_{IN} = V_{SRC} = V_{OUT} = 12V, I_{GATE} = -1µA	8	9	10	
		V_{IN} = V_{SRC} = V_{OUT} = 24V, I_{GATE} = -1µA	7	8.5	10	
		V_{IN} = V_{SRC} = V_{OUT} = 30V, I_{GATE} = -1µA	6.25	8	9.5	
GATE Pulldown Current	I_{PD}	V_{GATE} = 12V	8.8			mA
GATE Charge-Pump Current	I_{GATE}	V_{IN} = V_{GATE} = V_{SRC} = 12V		180		µA
Thermal Shutdown	T_+			+145		°C
Thermal-Shutdown Hysteresis	ΔT			15		°C
$\overline{SHDN}$ Logic-High Input Voltage	V_{IH}		1.4			V
$\overline{SHDN}$ Logic-Low Input Voltage	V_{IL}				0.4	V
$\overline{SHDN}$ Input Pulse Width	t_{PW}		6			µs
$\overline{SHDN}$ Input Pulldown Current	I_{SPD}			0.8	1.2	µA
$\overline{FLAG}$ Output Voltage Low	V_{OL}	$\overline{FLAG}$ sinking 1mA			0.4	V
$\overline{FLAG}$ Leakage Current	I_{IL}	$V_{\overline{FLAG}}$ = 12V			0.5	µA

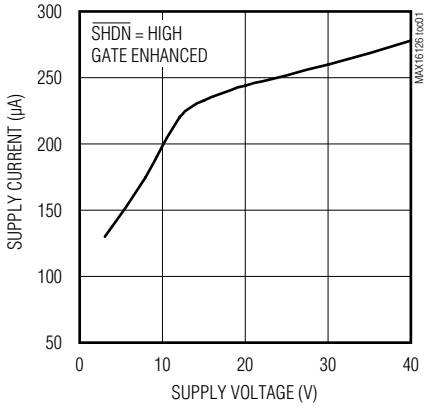
Note 2: All parameters are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 3: The MAX16126/MAX16127 power up with the external MOSFETs in off mode (V_{GATE} = V_{SRC}). The external MOSFETs turn on t_{START} after the IC is powered up and all input conditions are valid.

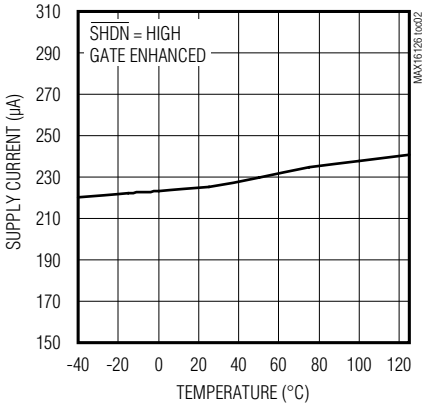
Typical Operating Characteristics

(V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

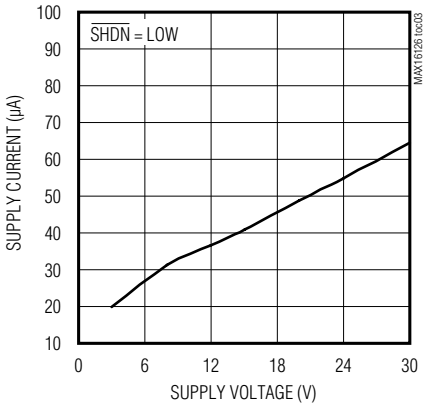
SUPPLY CURRENT vs. SUPPLY VOLTAGE



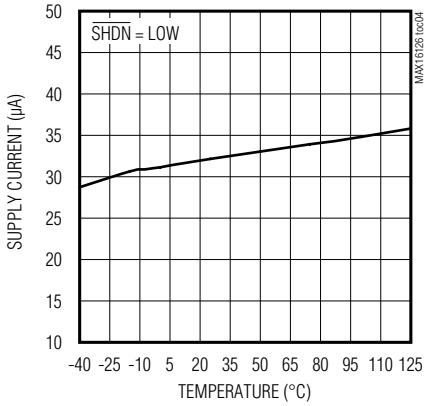
SUPPLY CURRENT vs. TEMPERATURE



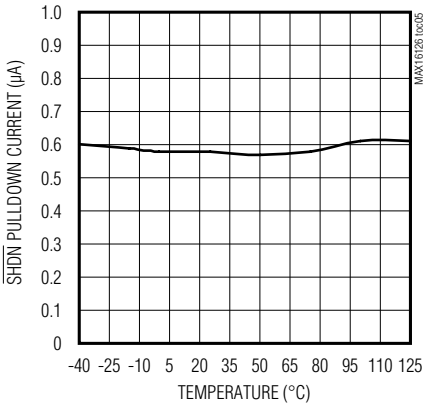
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



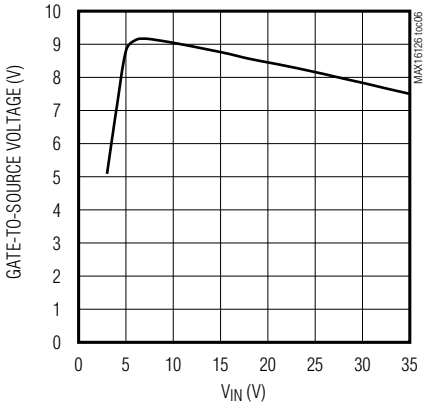
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



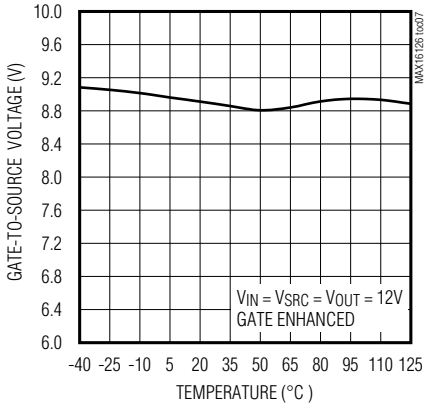
SHDN PULLDOWN CURRENT vs. TEMPERATURE



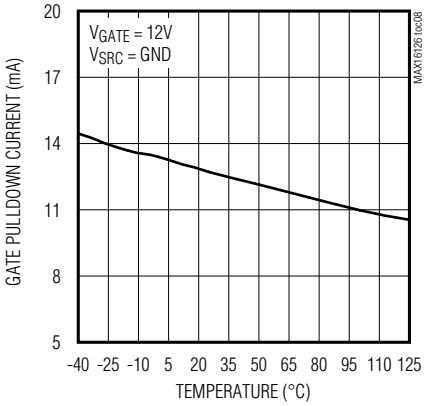
GATE-TO-SOURCE VOLTAGE vs. SUPPLY VOLTAGE



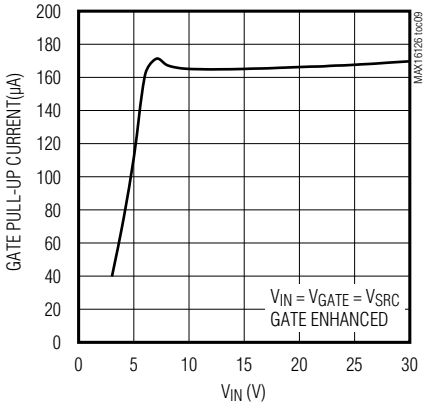
GATE-TO-SOURCE VOLTAGE vs. TEMPERATURE



GATE PULLDOWN CURRENT vs. TEMPERATURE



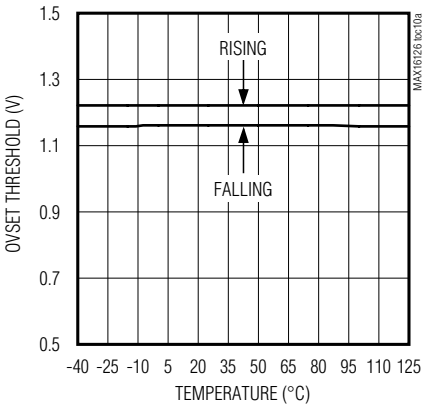
GATE-PULLUP CURRENT vs. SUPPLY VOLTAGE



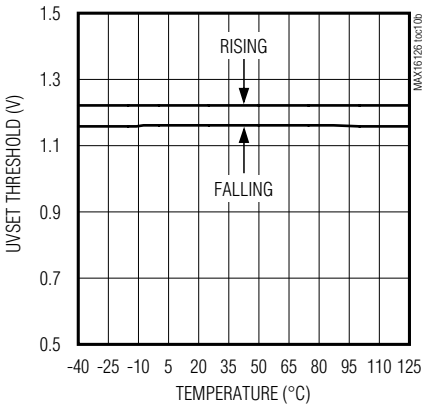
Typical Operating Characteristics (continued)

(V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

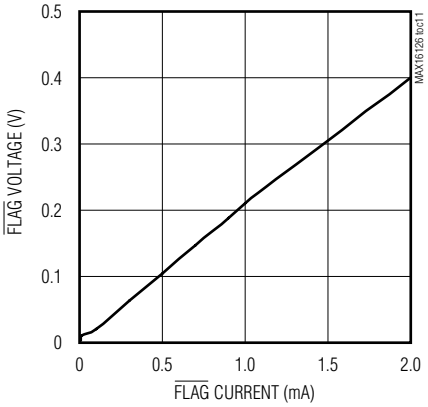
OVSET THRESHOLD vs. TEMPERATURE



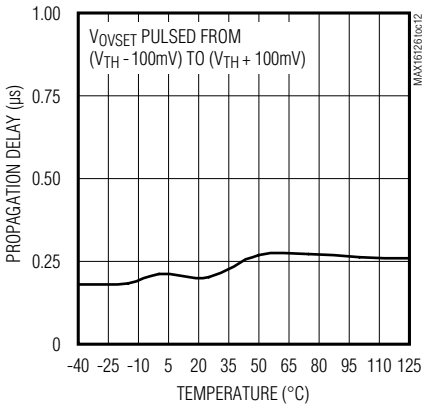
UVSET THRESHOLD vs. TEMPERATURE



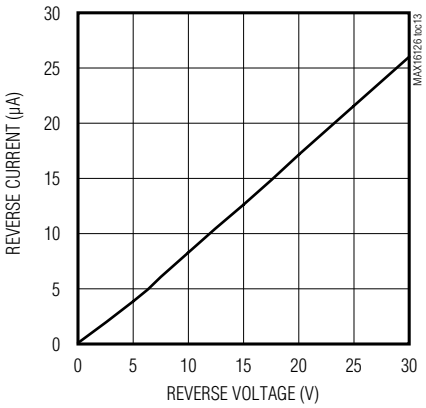
$\overline{FLAG}$ OUTPUT LOW VOLTAGE vs. CURRENT



OVERVOLTAGE FAULT TO GATE PROPAGATION DELAY vs. TEMPERATURE



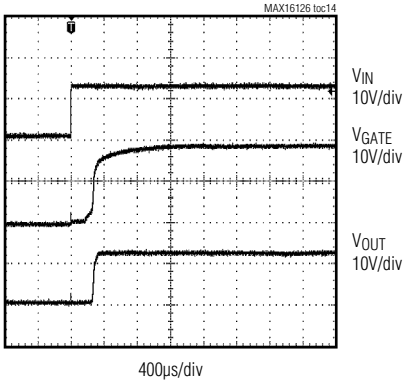
REVERSE CURRENT vs. REVERSE VOLTAGE



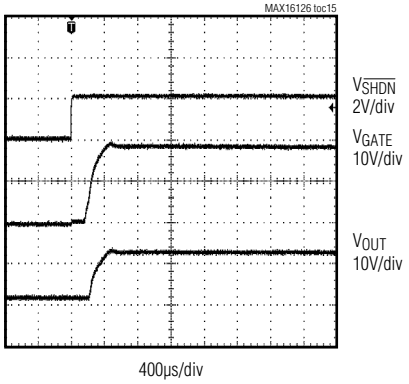
Typical Operating Characteristics (continued)

(V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

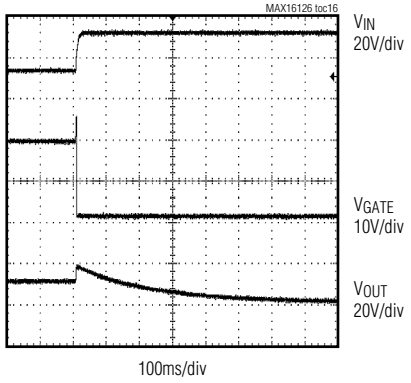
STARTUP WAVEFORM
(V_{IN} = 0 TO 12V, R_L = 100Ω, C_{IN} = 0.1µF, C_{OUT} = 100µF)



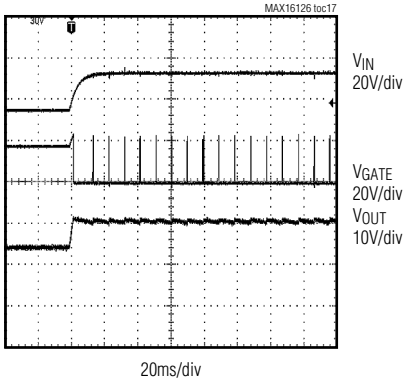
STARTUP FROM SHUTDOWN
($\overline{SHDN}$ RISING 0 TO 2V, V_{IN} = 12V, R_{LOAD} = 100Ω, C_{IN} = 0.1µF)



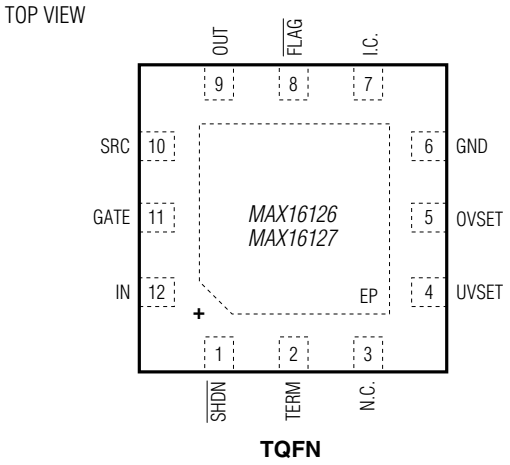
OVERVOLTAGE SWITCH FAULT
(V_{OV} = 20V, C_{IN} = 0.1µF, C_{OUT} = 100µF)



OVERVOLTAGE LIMITER
(V_{UV} = 4V, V_{OV} = 20V, C_{IN} = 0.1µF, C_{OUT} = 100µF)



Pin Configuration



TQFN

Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to force GATE and $\overline{FLAG}$ low and turn off the external n-channel MOSFETs. Connect a 100kΩ resistor from $\overline{SHDN}$ to IN for normal operation.
2	TERM	Voltage-Divider Termination Output. TERM is internally connected to IN. TERM is high impedance when $\overline{SHDN}$ is low, forcing the current to zero in the resistive-divider connected to TERM.
3	N.C.	No Connection. Not internally connected.
4	UVSET	Undervoltage Threshold Adjustment Input. Connect UVSET to the external resistive voltage-divider network to adjust the desired input undervoltage threshold. Connect the resistive divider to TERM.
5	OVSET	Overvoltage Threshold Adjustment Input. Connect OVSET to an external resistive voltage-divider network to adjust the desired overvoltage disable or overvoltage limit threshold. Connect the resistive divider to TERM for overvoltage switch-mode applications or to OUT for overvoltage limiting applications.
6	GND	Ground
7	I.C.	Internally Connected. Connect to GND.
8	$\overline{FLAG}$	$\overline{FLAG}$ Output. During startup, $\overline{FLAG}$ is low as long as V_{OUT} is lower than 90% of V_{IN} and after that it is high impedance. It asserts low during shutdown mode, an overvoltage, thermal shutdown, or undervoltage fault or when V_{OUT} falls below 90% of V_{IN}.
9	OUT	Output Voltage-Sense Input. Connect OUT to the load with a 100Ω series resistor. Bypass the load with a minimum 10µF capacitor to GND.
10	SRC	Source Input. Connect SRC to the common source connection of the external MOSFETs. When the MOSFETs are turned off, this connection is clamped to GND. An external zener diode between SRC and GATE protects the gates of the external MOSFETs.
11	GATE	Gate-Driver Output. Connect GATE to the gates of the external n-channel MOSFETs. GATE is the charge-pump output during normal operation. GATE is quickly pulled low during a fault condition or when $\overline{SHDN}$ is pulled low.
12	IN	Positive Supply Input Voltage. Connect IN to the positive side of the input voltage. Bypass IN with a 0.1µF ceramic capacitor to GND.
—	EP	Exposed Pad. Can be connected to GND or left unconnected.

Detailed Description

The MAX16126/MAX16127 transient protection circuits are suitable for automotive and industrial applications where high-voltage transients are commonly present on supply voltage inputs. The devices monitor the input voltage and control two external common-source n-channel MOSFETs to protect downstream voltage regulators during load-dump events or other automotive pulse conditions.

The devices feature an overvoltage and an undervoltage comparator for voltage window detection. A flag output ($\overline{FLAG}$) asserts when a fault event occurs.

Two external back-to-back n-channel MOSFETs provide reverse-voltage protection and also prevent reverse current during a fault condition. Compared to a traditional reverse-battery diode, this approach minimizes power dissipation and voltage drop, and allows the circuit to operate at very low cold-crank voltages (3V minimum).

The MAX16127 provides a limiter-mode fault management for overvoltage and thermal shutdown conditions, whereas the MAX16126 provides switch-mode fault management for overvoltage and thermal shutdown conditions. In the limiter mode, the MOSFETs cycle on and off so the output voltage is limited. In the switch mode, the external MOSFETs are switched off, disconnecting the load from the input. In both cases, $\overline{FLAG}$ asserts to indicate a fault.

Gate Charge Pump

The MAX16126/MAX16127 use a charge pump to generate the GATE to SRC voltage and enhance the external MOSFETs. After the input voltage exceeds the input

undervoltage threshold, the charge pump turns on after a 150µs delay.

During a fault condition, GATE is pulled to ground with a 8.8mA (min) pulldown current. Note that an external zener diode is required to be connected between the gate and source of the external MOSFETs. See the *Applications Information* section.

Overvoltage Protection

The MAX16126/MAX16127 detect overvoltage conditions using a comparator that is connected through an external resistive divider to the input or output voltage. An overvoltage condition causes the GATE output to go low, turning off the external MOSFETs. $\overline{FLAG}$ also asserts to indicate the fault condition.

Overvoltage Limiter (MAX16127)

In overvoltage limiter mode, the output voltage is regulated at the overvoltage threshold voltage and continues to supply power to downstream devices. In this mode, the device operates like a voltage regulator.

During normal operation, GATE is enhanced 9V above SRC. The output voltage is monitored through a resistive divider between OUT and OVSET. When OUT rises above the overvoltage threshold, GATE goes low and the MOSFETs turn off. As the voltage on OUT falls below the overvoltage threshold minus the threshold hysteresis, GATE goes high and the MOSFETs turn back on again, regulating OUT in a switched-linear mode at the overvoltage threshold.

The switching frequency depends on the gate charge of the MOSFETs, the charge-pump current, the output load current, and the output capacitance.

Caution must be exercised when operating the MAX16127 in voltage-limiting mode for long durations. Since MOSFETs can dissipate power continuously during this interval, proper heat sinking should be implemented to prevent damage to them.

Overvoltage Switch (MAX16126)

In the overvoltage switch mode, the internal overvoltage comparator monitors the input voltage and the load is completely disconnected from the input during an overvoltage event. When the input voltage exceeds the overvoltage threshold, GATE goes low and the MOSFETs turn off, disconnecting the input from the load. After that, for the autoretry mode version, the autoretry timer starts, while for the latched mode version a power cycle to IN or a cycle on $\overline{SHDN}$ is needed to turn the external MOSFETs back on.

The MAX16126 can be configured to latch off (suffix **D**) even after the overvoltage condition ends. The latch is cleared by cycling IN below the undervoltage threshold or by toggling $\overline{SHDN}$.

The devices can also be configured to retry:

- One time, then latch off (suffix B)
- Three times, then latch off (suffix C)
- Always retry and never latch off (suffix A)

There is a fixed 150ms (typ) delay between each retry attempt. If the overvoltage fault condition is gone when a retry is attempted, GATE goes high and power is restored to the downstream circuitry.

Undervoltage Protection

The MAX16126/MAX16127 monitor the input voltage for undervoltage conditions. If the input voltage is below the undervoltage threshold ($V_{IN} < V_{TH} - V_{TH-HYS}$), GATE goes low, turning off the external MOSFETs and $\overline{FLAG}$ asserts. When the input voltage exceeds the undervoltage threshold ($V_{IN} > V_{TH}$), GATE goes high after a 150µs delay (typ).

For the MAX16126/MAX16127, an external resistive divider connected between TERM, UVSET, and GND sets the undervoltage threshold (TERM is connected to IN when $\overline{SHDN}$ is high).

Thermal Shutdown

The MAX16126/MAX16127 thermal shutdown feature turns off the MOSFETs if the internal die temperature exceeds +145°C (T_J). By ensuring good thermal coupling between the MOSFETs and the MAX16126/MAX16127, the thermal shutdown can turn off the MOSFETs if they overheat.

When the junction temperature exceeds T_J = +145°C (typ), the internal thermal sensor signals the shutdown logic, pulling the GATE voltage low and allowing the device to cool. When T_J drops by 15°C (typ), GATE goes high and the MOSFETs turn back on. Do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

Flag Output ($\overline{FLAG}$)

An open-drain $\overline{FLAG}$ output indicates fault conditions. During startup, $\overline{FLAG}$ is initially low and goes high impedance when V_{OUT} is greater than 90% of V_{IN} if no fault conditions are present. $\overline{FLAG}$ asserts low during shutdown mode, an overvoltage, thermal shutdown, or undervoltage fault, or when V_{OUT} falls below 90% of V_{IN}.

TERM Connection

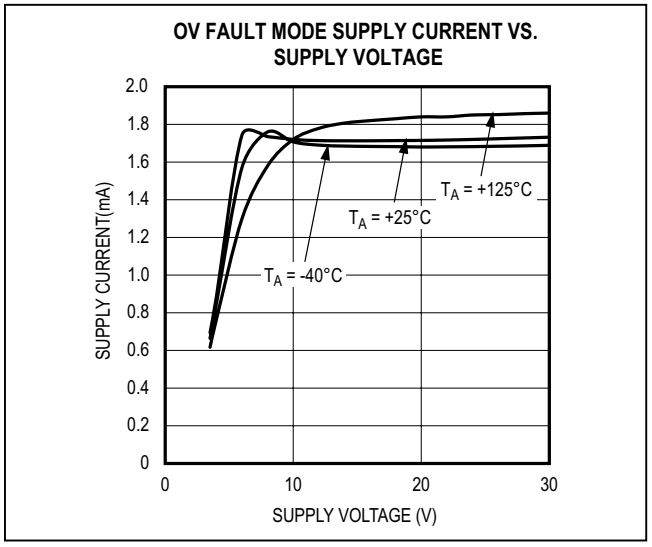
The TERM connection has an internal switch to IN. In shutdown ($\overline{SHDN}$ = GND), this switch is open. By connecting the voltage threshold resistive divider to TERM instead of directly to IN, power dissipation in the resistive divider can be eliminated and the shutdown supply current reduced.

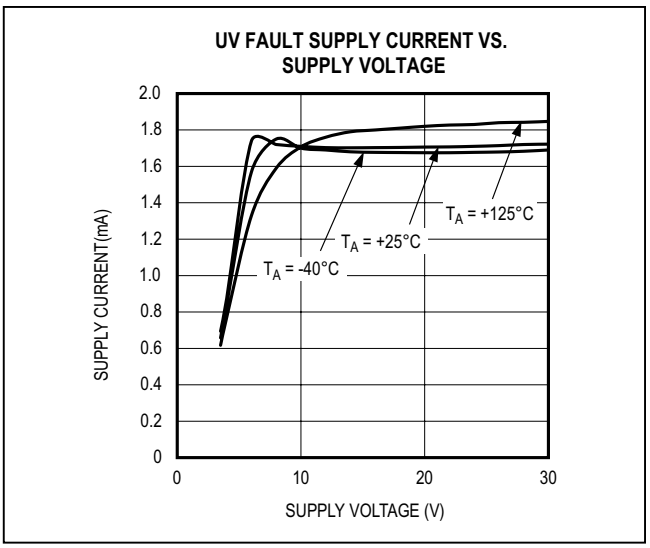
Reverse-Voltage Protection

The MAX16126/MAX16127 integrate reverse-voltage protection, preventing damage to the downstream circuitry caused by battery reversal or negative transients. The devices can withstand reverse voltage to -36V without damage to themselves or the load. During a reverse-voltage condition, the two external n-channel MOSFETs are turned off, protecting the load. Connect a 0.1µF ceramic capacitor from IN to GND, connect 10µF from the load to GND, and minimize the parasitic capacitance from GATE to GND to have a fast reserve-battery voltage-transient protection. During normal operation, both MOSFETs are turned on and have a minimal forward voltage drop, providing lower power dissipation and a much lower voltage drop than a reverse-battery protection diode.

Supply Current During Fault Conditions

During fault conditions, the MAX16126/MAX16127 supply current is higher than normal operation. When a fault condition occurs, the MAX16126/MAX16127 pulls the gate low but keeps the charge pump active. This results in increased supply because the charge pump tries hard to bring up the gate. See Figures below for supply current during overvoltage and undervotlage fault conditions.





Applications Information

Automotive Electrical Transients (Load Dump)

Automotive circuits generally require supply voltage protection from various transient conditions that occur in automotive systems. Several standards define various pulses that can occur. Table 1 summarizes the pulses from the ISO 7637-2 and ISO 16750-2 specification.

Most of the pulses can be mitigated with capacitors and zener clamp diodes (see the *Typical Operating Characteristics* and also the *Increasing the Input Voltage Protection Range* section). The load dump (pulse 5a and 5b) occurs when the alternator is charging the battery and a battery terminal gets disconnected. Due to the sudden change in load, the alternator goes out of regulation and the bus voltage spikes. The pulse has a rise time of about 10ms and a fall time of about 400ms, but can extend out to 1s or more depending on the characteristics of the charging system. The magnitude of the pulse depends on the bus voltage and whether the system is unsuppressed or uses central load-dump suppression (generally implemented using very large clamp diodes built into the alternator). Table 1 lists the worst-case values from the ISO 7637-2 specification.

Cold crank (pulse 4) occurs when activating the starter motor in cold weather with a marginal battery. Due to the large load imposed by the starter motor, the bus voltage sags. Since the MAX16126/MAX16127 can operate down to 3V, the downstream circuitry can continue to operate through a cold-crank condition. If desired, the undervoltage threshold can be increased so that the MOSFETs turn

Table 1. Summary of ISO 7637 and ISO 16750-2 Pulses

NAME	DESCRIPTION	PEAK VOLTAGE (V) (max)*	DURATION
		12V SYSTEM	
Pulse 1	Inductive load disconnection	-100	1ms to 2ms
Pulse 2a	Inductive wiring disconnection	50	0.05ms
Pulse 3a	Switching transients	-150	0.2µs
Pulse 3b		100	
Pulse 4	Cold crank	-7	100ms (initial)
		-6	Up to 20s
Pulse 5a	Load dump (unsuppressed)	87	400ms (single)
Pulse 5b	Load dump (suppressed)	(Varies, but less than pulse 5a)	

**Relative to system voltage.*

off during a cold crank, disconnecting the downstream circuitry. An output reservoir capacitor can be connected from OUT to GND to provide energy to the circuit during the cold-crank condition.

Refer to the ISO 7637-2 specification for details on pulse waveforms, test conditions, and test fixtures.

Setting Overvoltage and Undervoltage Thresholds (MAX16126)

The MAX16126 uses an external resistive divider to set the overvoltage and undervoltage thresholds. The MAX16126 operates in switch mode in which the internal overvoltage comparator monitors the input voltage. It uses three resistors in a single resistive divider to set the undervoltage and overvoltage thresholds. The top of the resistive divider connects to TERM (see Figure 1).

The MAX16126 includes internal undervoltage and overvoltage comparators for window detection. GATE is enhanced and the n-channel MOSFETs are on when the IN voltage is within the selected window. When the monitored voltage falls below the lower limit ($V_{TRIPLOW}$) or exceeds the upper limit ($V_{TRIPHIGH}$) of the window, the GATE voltage goes to GND, turning off the MOSFETs. The circuit in Figure 1 shows the MAX16126 enabling the DC-DC converter when the monitored voltage is in the selected window.

The resistor values R1, R2, and R3 can be calculated as follows:

$$V_{TRIPLOW} = (V_{TH} - V_{TH-HYS})\left(\frac{R_{TOTAL}}{R2 + R3}\right)$$

$$V_{TRIPHIGH} = V_{TH}\left(\frac{R_{TOTAL}}{R3}\right)$$

where R_{TOTAL} = R1 + R2 + R3, V_{TH} is the 1.225V OVSET/UVSET threshold, and V_{TH-HYS} is the hysteresis.

Use the following steps to determine the values for R1, R2, and R3:

1) Choose a value for R_{TOTAL}, the sum of R1, R2, and R3.
2) Calculate R3 based on R_{TOTAL} and the desired upper trip point:

$$R3 = \frac{V_{TH} \times R_{TOTAL}}{V_{TRIPHIGH}}$$

3) Calculate R2 based on R_{TOTAL}, R3, and the desired lower trip point:

$$R2 = \frac{(V_{TH} - V_{TH-HYS}) \times R_{TOTAL}}{V_{TRIPLOW}} - R3$$

4) Calculate R1 based on R_{TOTAL}, R2, and R3:

$$R1 = R_{TOTAL} - R2 - R3$$

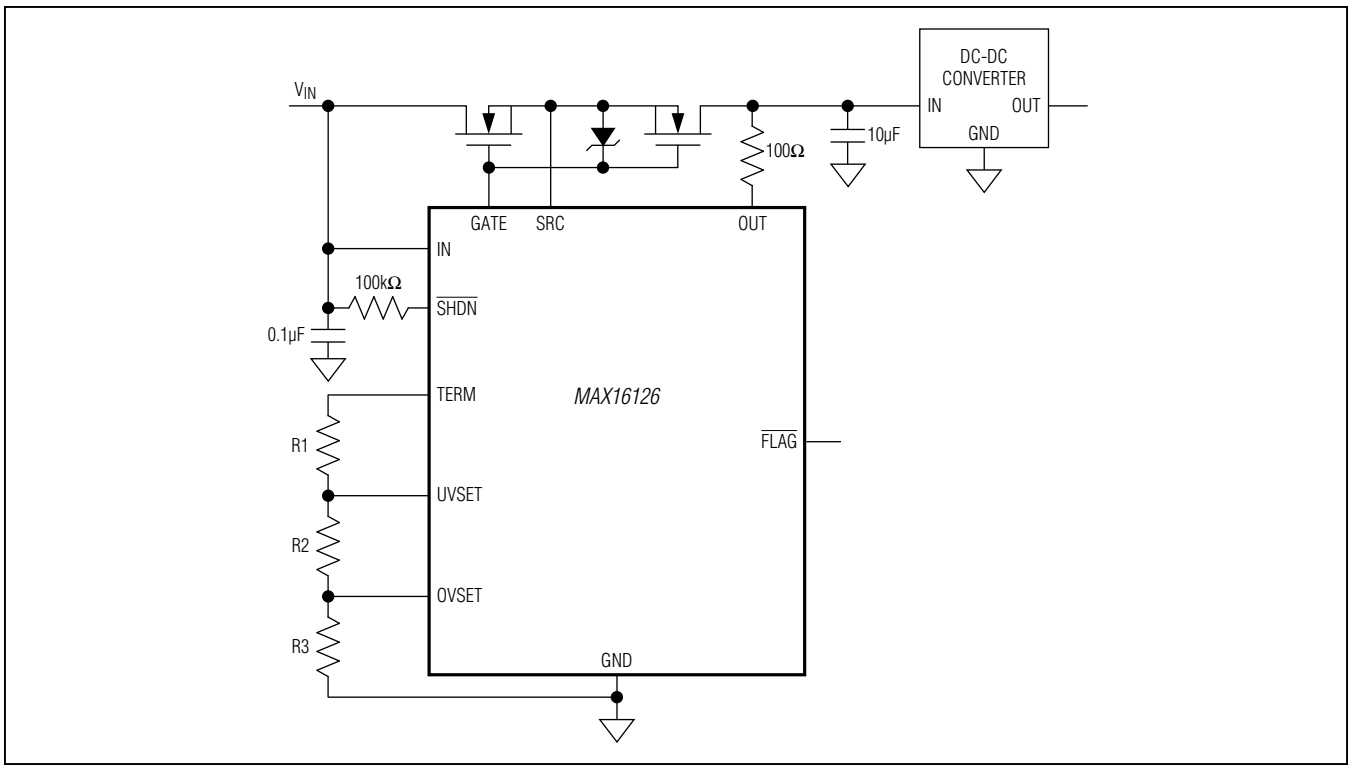


Figure 1. Overvoltage and Undervoltage Window Detector Circuit (MAX16126)

Setting Overvoltage and Undervoltage Thresholds (MAX16127)

The MAX16127 operates in limiter mode and uses separate resistive dividers to set the undervoltage and overvoltage thresholds. The top of the overvoltage divider connects to OUT and the top of the undervoltage divider connects to TERM (see Figure 2).

Use the following formula to calculate R4:

$$R4 = V_{TH} \times \frac{R_{TOTAL\_OV}}{V_{OV}}$$

where R_{TOTAL_OV} = R3 + R4, V_{TH} is the 1.225V OVSET rising threshold, and V_{OV} is the desired overvoltage threshold. The falling threshold of V_{TH} is 5% below the rising threshold.

Similarly, to calculate the values of R1 and R2:

$$R2 = (V_{TH} - V_{TH\text{-}HYS}) \times \frac{R_{TOTAL\_UV}}{V_{UV}}$$

where R_{TOTAL_UV} = R1 + R2, V_{TH} is the 1.225V UVSET rising threshold, $V_{TH\text{-}HYS}$ is the hysteresis, and V_{UV} is the desired undervoltage threshold.

Use the nearest standard-value resistor that is less than the calculated value. A lower value for total resistance dissipates more power, but provides slightly better accuracy.

MOSFET Selection

MOSFET selection is critical to design a proper protection circuit. Several factors must be taken into account: the gate capacitance, the drain-to-source voltage rating, the on-resistance ($R_{DS(ON)}$), the peak power dissipation capability, and the average power dissipation limit. In general, both MOSFETs should have the same part number. For size-constrained applications, a dual MOSFET can save board area. Select the drain-to-source voltage so that the MOSFETs can handle the highest voltage that might be applied to the circuit. Gate capacitance is not as critical, but it does determine the maximum turn-on and turn-off time. MOSFETs with more gate capacitance tend to respond more slowly.

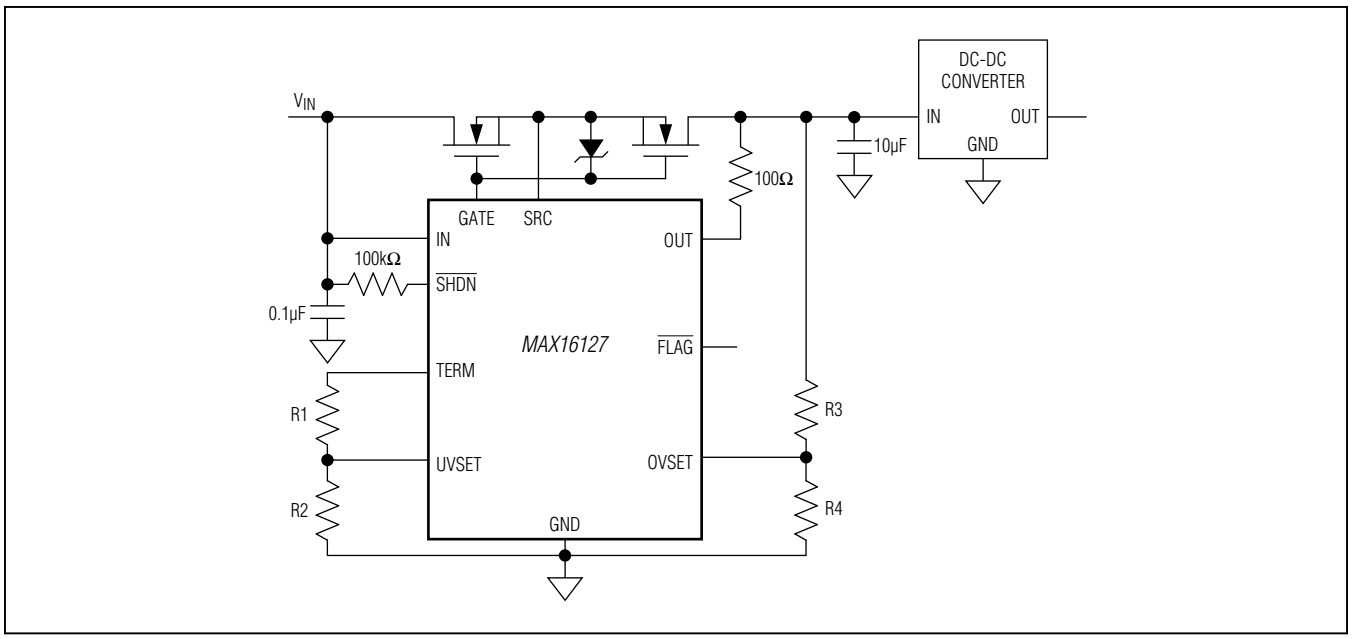


Figure 2. Overvoltage and Undervoltage Limiter Protection Configuration (MAX16127)

MOSFET Power Dissipation

The $R_{DS(ON)}$ must be low enough to limit the MOSFET power dissipation during normal operation. Power dissipation (per MOSFET) during normal operation can be calculated using this formula:

$$P = I_{LOAD}^2 \times R_{DS(ON)}$$

where P is the power dissipated in each MOSFET and I_{LOAD} is the average load current.

During a fault condition in switch mode, the MOSFETs turn off and do not dissipate power. Limiter mode imposes the worst-case power dissipation. The average power can be computed using the following formula:

$$P = I_{LOAD} \times (V_{IN} - V_{OUT})$$

where P is the average power dissipated in both MOSFETs, I_{LOAD} is the average load current, V_{IN} is the input voltage, and V_{OUT} is the average limited voltage on the output. In limiter mode, the output voltage is a sawtooth wave with characteristics determined by the $R_{DS(ON)}$ of the MOSFETs, the output load current, the output capacitance, the gate charge of the MOSFETs, and the GATE charge-pump current.

Since limiter mode can involve high switching currents when the GATE is turning on at the start of a limiting cycle (especially when the output capacitance is high), it is important to ensure the circuit does not violate the peak power rating of the MOSFETs. Check the pulse power ratings in the MOSFET data sheet.

MOSFET Gate Protection

To protect the gate of the MOSFETs, connect a zener clamp diode from the gate to the source. The cathode connects to the gate, and the anode connects to the source. Choose the zener clamp voltage to be above 10V and below the MOSFET V_{GS} maximum rating.

Increasing the Input Voltage Protection Range

The MAX16126/MAX16127 can tolerate -36V to +90V. To increase the positive input voltage range protection, connect two back-to-back zener diodes from IN to system ground, and connect a resistor in series with IN and the power-supply input to limit the current drawn by the zener diodes (see Figure 3).

Zener diode D1 clamps positive voltage excursions and D2 clamps negative voltage excursions. Set the zener voltages so the worst-case voltages do not exceed the ratings of the part. Also ensure that the zener diode power ratings are not exceeded. The combination of the series resistor and the zener diodes also help snub pulses on the supply voltage input and can aid in clamping the low-energy ISO 7637-2 pulses.

It is important to compute the peak power dissipation in the series resistor. Most standard surface-mount resistors cannot withstand the peak power dissipation during certain pulse events. Check the resistor data sheets for pulse power derating curves. If necessary, connect multiple resistors in parallel or use automotive-rated resistors.

The shutdown input needs a series resistor to limit the current if V_{IN} exceeds the clamped voltage on IN. A good starting point is 100kΩ

Increasing the Input Voltage Operating Range

With proper external component selection, the MAX16126/MAX16127's input voltage operating range can be extended beyond 30V. Normally the input voltage can swing up to 90V in protection mode, but normal operation is listed in the electrical characteristics table to 30V. Higher voltage operation is permissible so long as the resulting GATE bias voltage does not exceed 45V with respect to GND.

To enable operating voltages above 30V, a 6.8V Zener diode clamp can be added GATE-to-SRC to the external switches to limit the maximum GATE voltage. The circuit in Figure 4 shows the recommended arrangement. When V_{IN} = 35V, V_{GATE} = 35V + 6.8V or 41.8V. When V_{IN} > 35V, the MAX16126/MAX16127 detects the input over voltage condition by sensing the voltage at the OVSET pin and turns off the charge pump. The resistive voltage divider on OVSET must be selected to disable the circuit before the gate voltage reaches 45V. The MAX16126TCA/MAX16127TCA automatically reenable GATE drive when the input voltage drops 5% below the overvoltage threshold. For the MAX16126TCD, the latch-mode option, GATE drive is enabled by either power cycling the IN voltage below UVLO threshold or by toggling $\overline{SHDN}$. See the *Ordering Information* section for other available options.

Output Reservoir Capacitor

The output capacitor can be used as a reservoir capacitor to allow downstream circuitry to ride out fault transient conditions. Since the voltage at the output is protected from input voltage transients, the capacitor voltage rating can be less than the expected maximum input voltage.

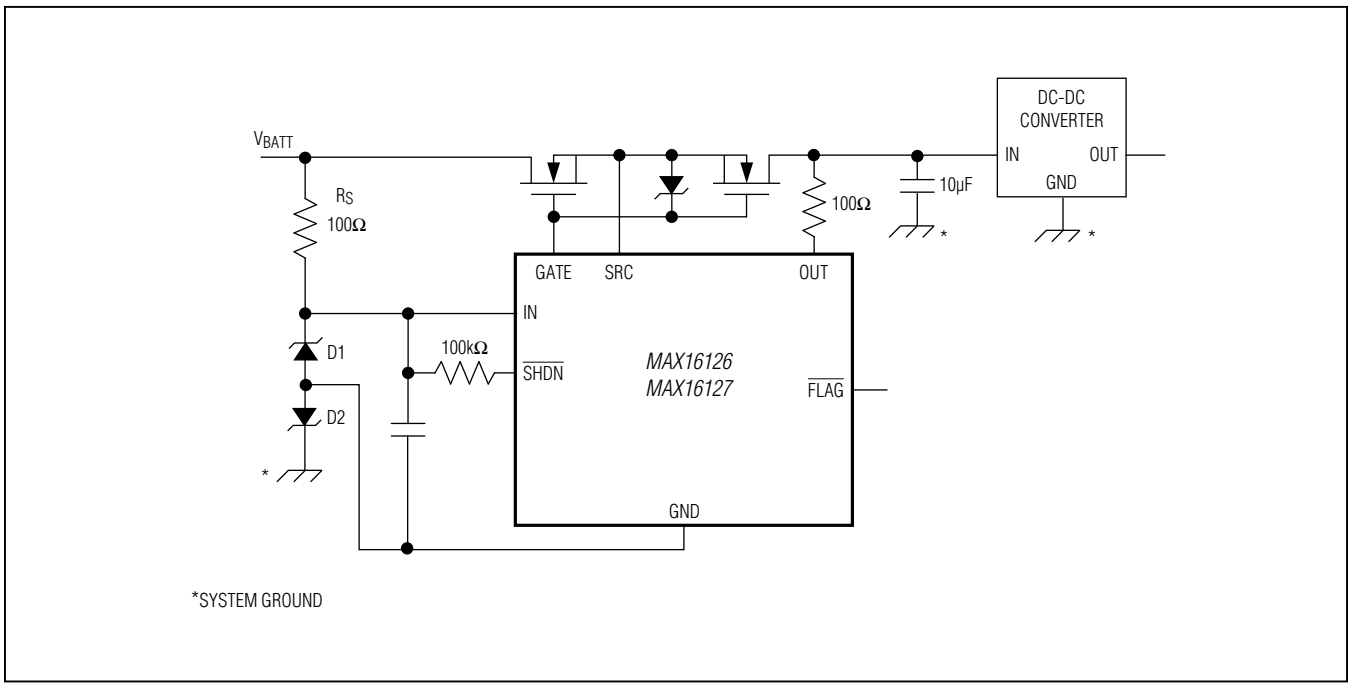


Figure 3. Circuit to Increase Input Voltage Protection Range

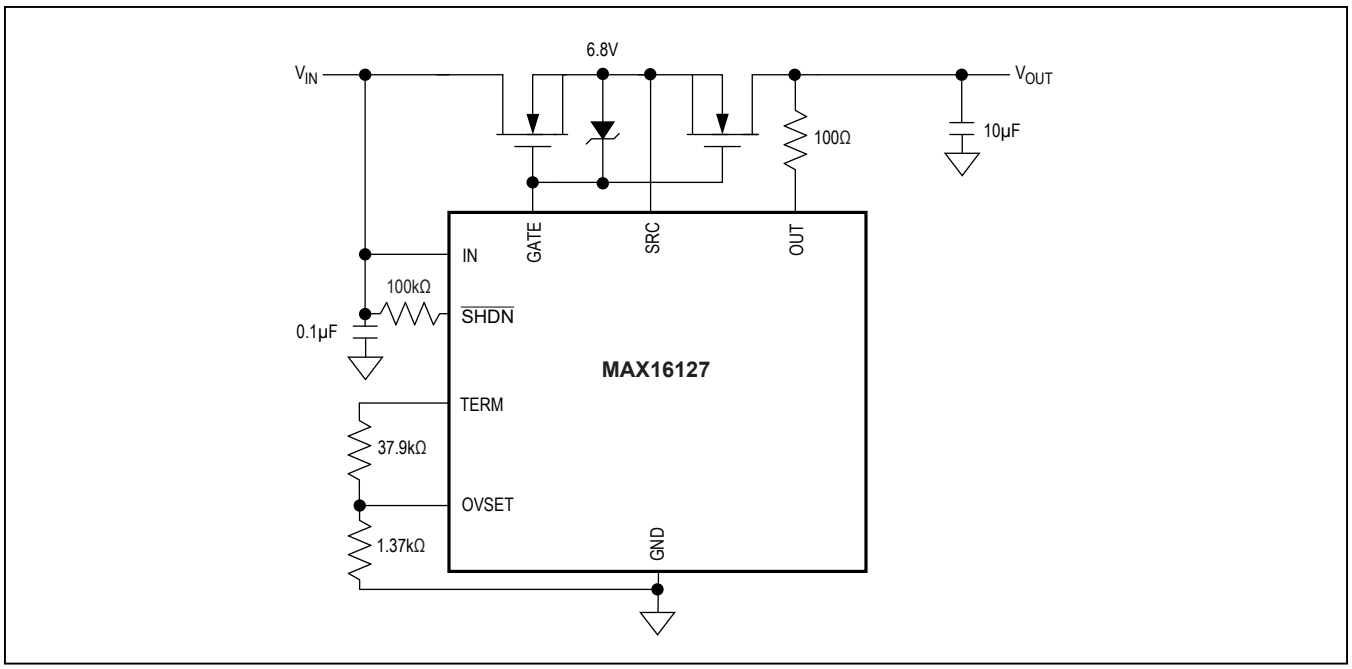


Figure 4. Use of a 6.8V Zener Clamp to Enable Operation with V_{IN} Up to 35V

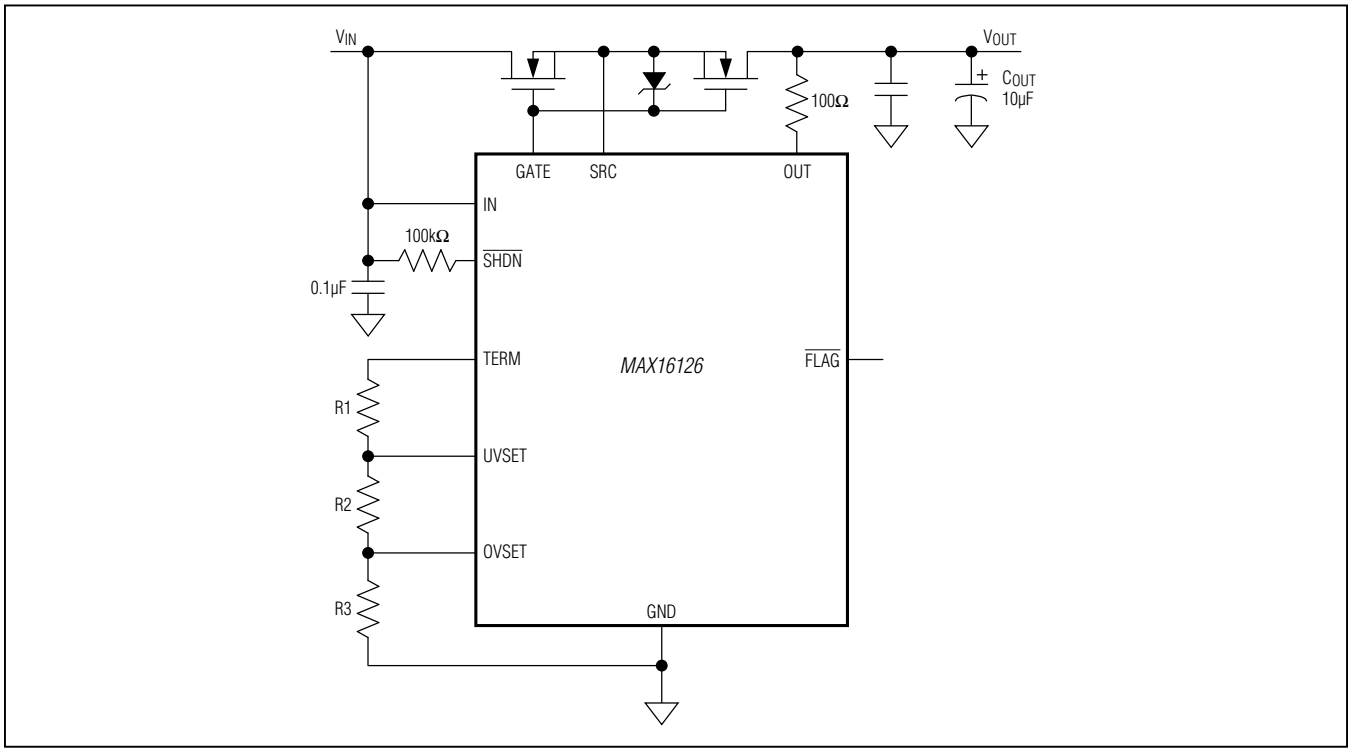


Figure 5. MAX16126 Typical Operating Circuit

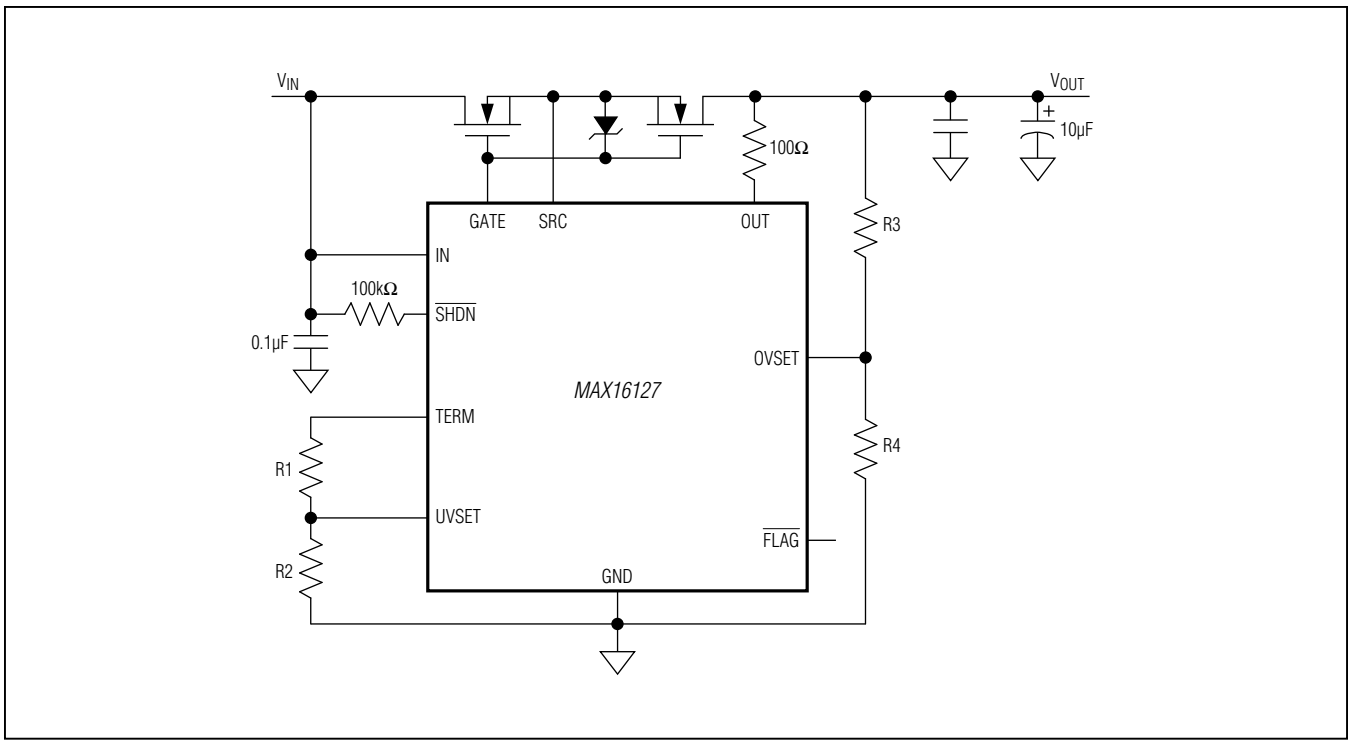


Figure 6. MAX16127 Typical Operating Circuit

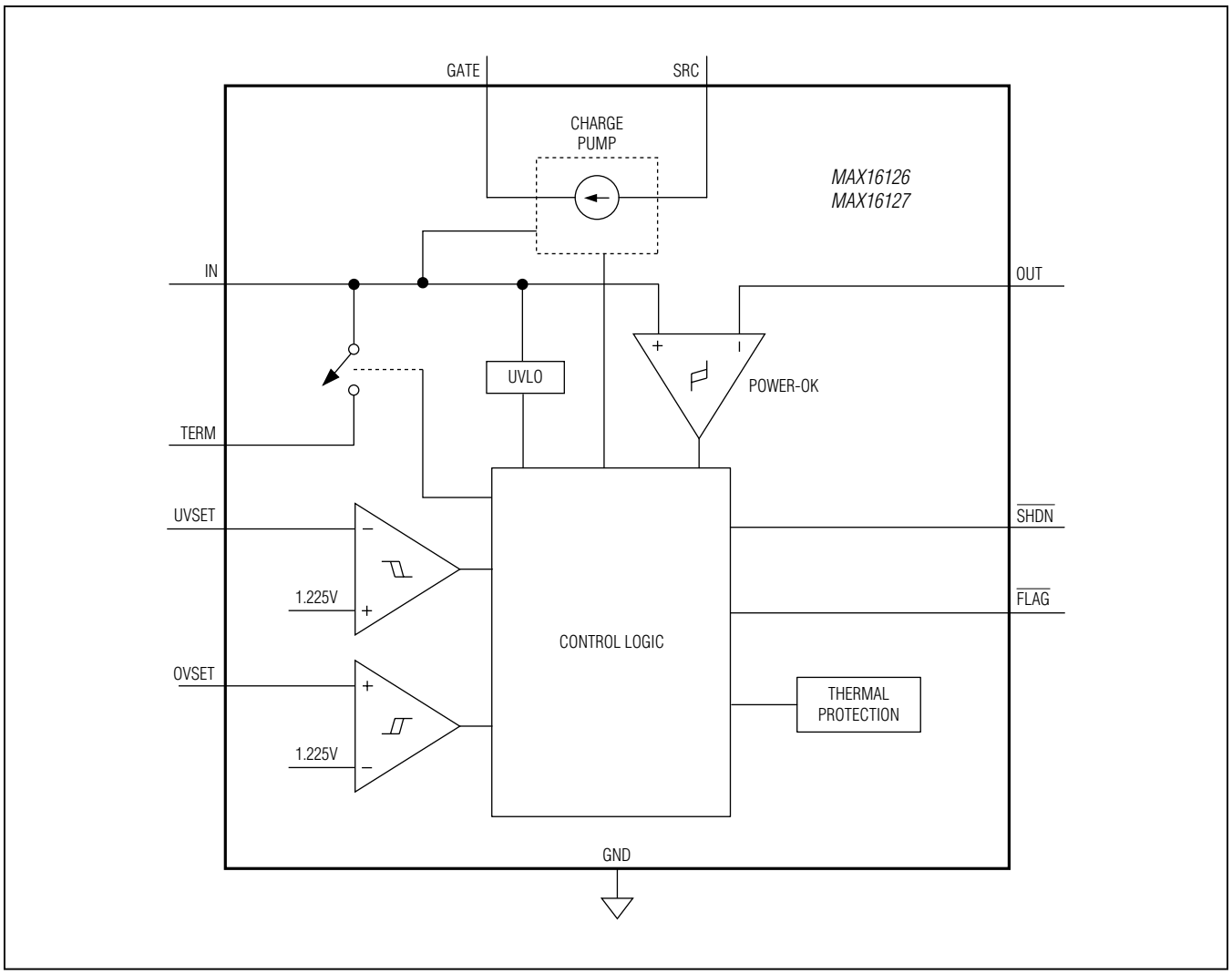


Figure 7. MAX16126/MAX16127 Functional Diagram

Ordering Information

PART	PIN-PACKAGE	TOP MARK	PACKAGE CODE	FUNCTION	
MAX16126TCA+	12 TQFN-EP	+ABV	T1233+4	Switch mode	Always autoretry
MAX16126TCA/V+	12 TQFN-EP	+ACR	T1233+4		
MAX16126TCA/VY+*	12 TQFN-EP	+ACR	T1233Y+4		
MAX16126TCB+	12 TQFN-EP	+ABX	T1233+4		One retry, then latch
MAX16126TCB/V+	12 TQFN-EP	+ADT	T1233+4		
MAX16126TCC+	12 TQFN-EP	+ABY	T1233+4		Three retries, then latch
MAX16126TCC/V+	12 TQFN-EP	+ADU	T1233+4		
MAX16126TCD+	12 TQFN-EP	+ABZ	T1233+4		Latch mode
MAX16126TCD/V+*	12 TQFN-EP	+ADH	T1233+4		
MAX16127TC+	12 TQFN-EP	+ABW	T1233+4	Limiter mode	
MAX16127TC/V+	12 TQFN-EP	+AGC	T1233+5	Limiter mode	

Note: *All devices are specified over the -40°C to +125°C temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
**Future product—contact factory for availability.*
EP = Exposed pad.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 TQFN-EP	T1233+4	**21-0136**	**90-0019**
12 TQFN-EP	T1233Y+4	**21-100171**	**90-100060**
12 TQFN-EP	T1233+5	**21-100319**	**90-0019**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/11	Initial release	—
1	6/12	Revised the *Electrical Characteristics*, *Typical Operating Characteristics*, the *Overvoltage Limiter (MAX16127)*, *Reverse-Voltage Protection*, and the *Increasing the Input Voltage Protection Range* sections and Figure 3.	1–3, 4, 9, 10, 14
2	12/12	Updated Input Supply Current, SRC Input Current, and GATE Output Voltage High Above V_{SRC} conditions in the *Electrical Characteristics* and updated Figure 3	2, 3, 14
3	12/13	Updated Figure 3	12
4	1/14	Added /V automotive OPNs to *Ordering Information*	18
5	10/14	Added *Increasing the Input Voltage Operating Range* section and new Figure 4	14–17
6	3/15	Updated *Benefits and Features* section	1
7	8/17	Corrected *Ordering Information* table	18
8	4/18	Added *Supply Current During Fault Conditions* section	10
9	9/18	Updated the *Pin Description* table and *Reverse-Voltage Protection* section. Added MAX16127TC/V+* to *Ordering Information* and package code T1233+5 to the *Package Information*.	8, 10, 18
10	12/18	Updated *Electrical Characteristics*, *Ordering Information*, and *Package Information*	2, 3, 18
11	6/19	Updated *Package Thermal Characteristics*	2
12	8/19	Updated *Electrical Characteristics*, *Detailed Description, Applications Information*, and *Ordering Information*	2, 3, 9–16, 18

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