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1 Summary description

The M27C801 is an 8 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for applications where fast turn-around and pattern experimentation are important requirements and is organized as 1,048,576 by 8 bits.

The FDIP32W (window ceramic frit-seal package) has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C801 is offered in PDIP32, PLCC32 and TSOP32 (8 x 20 mm) packages.

In order to meet environmental requirements, ST offers the M27C801 in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at: www.st.com.

See *Figure 1: Logic Diagram* and *Table 1: Signal descriptions* for a brief overview of the signals connected to this device.

Figure 1. Logic Diagram

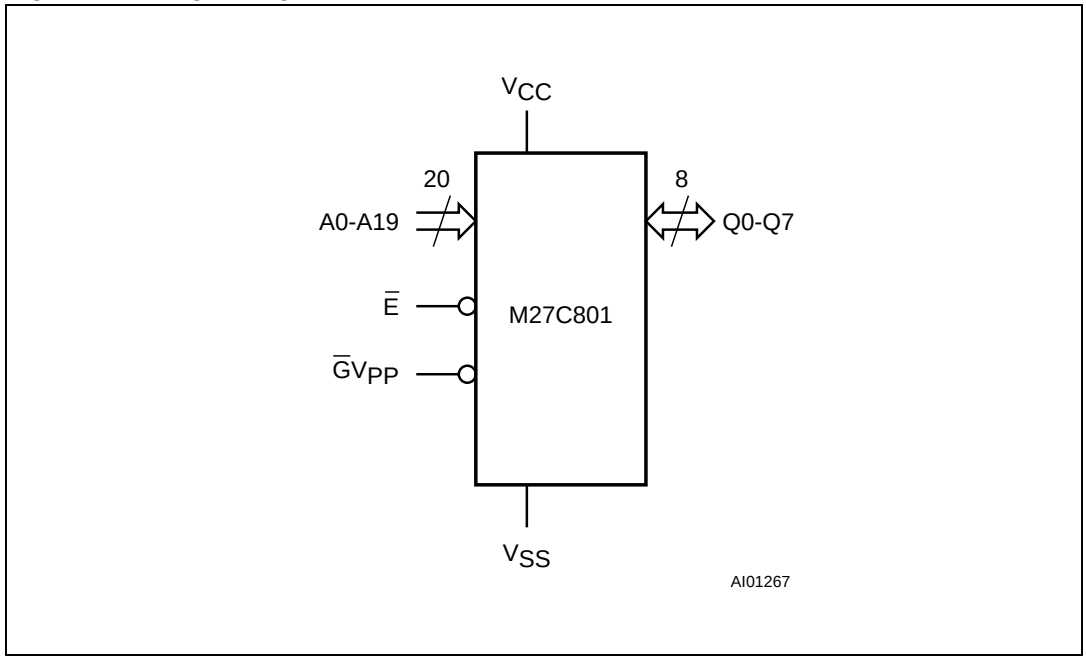


Table 1. Signal descriptions

Signal	Description
A0-A19	Address Inputs
Q0-Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. DIP connections

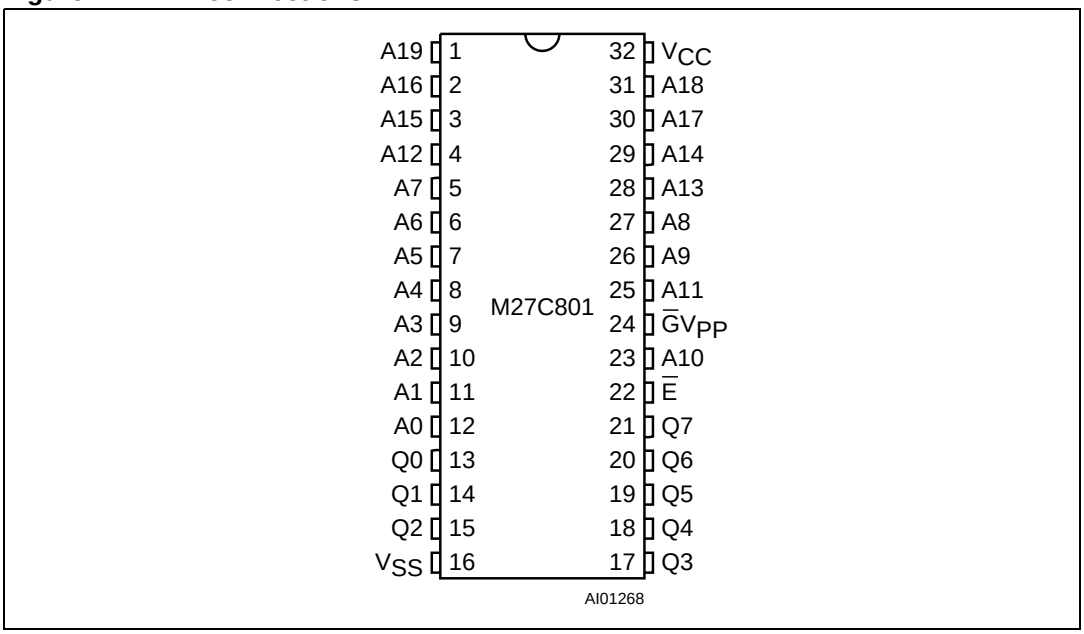


Figure 3. PLCC connections

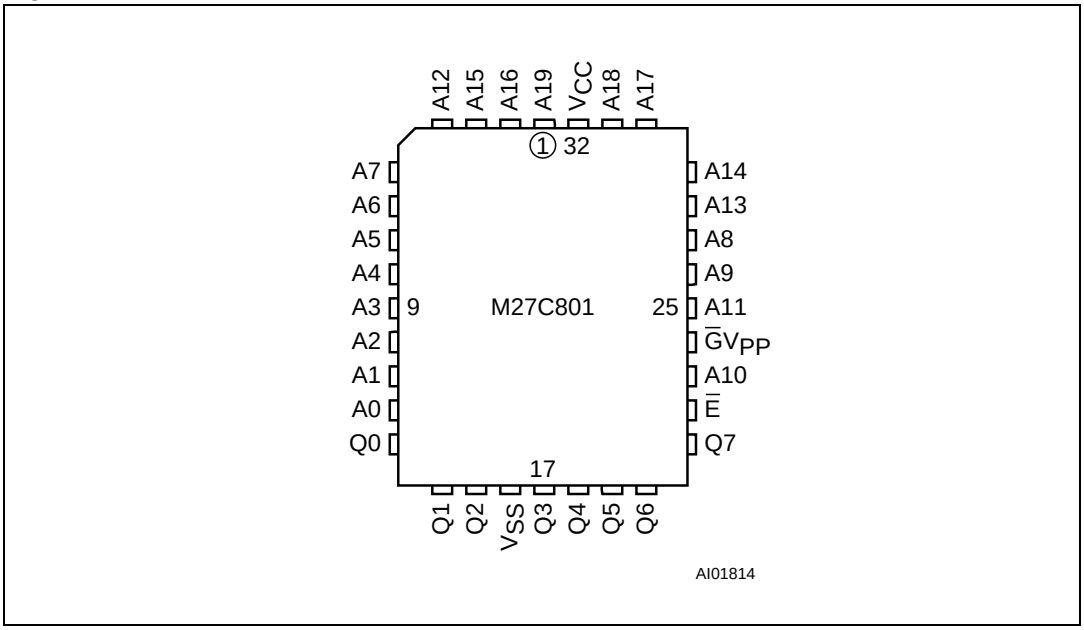
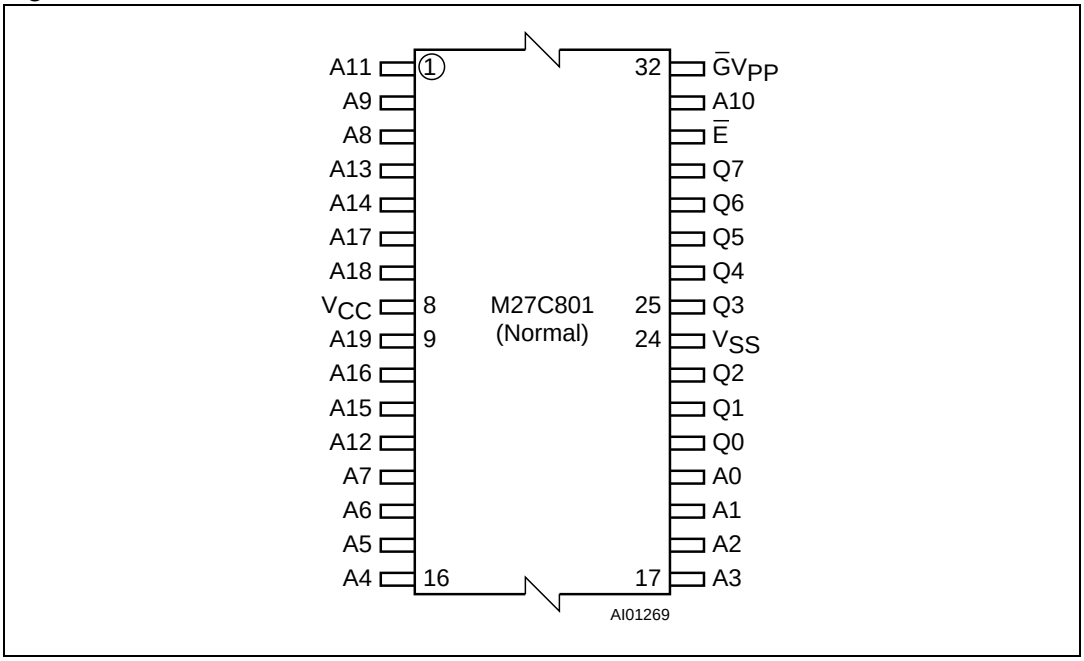


Figure 4. TSOP connections



2 Device description

The operating modes of the M27C801 are listed in the Operating Modes table. A single power supply is required in Read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature and Margin Mode Set or Reset.

Table 2. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}V_{pp}$	A9	Q7-Q0
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

1. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

2.1 Read mode

The M27C801 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

2.2 Standby mode

The M27C801 has a standby mode which reduces the supply current from 35mA to 100µA.

The M27C801 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

2.3 Two-line output control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This

ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

2.4 System considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

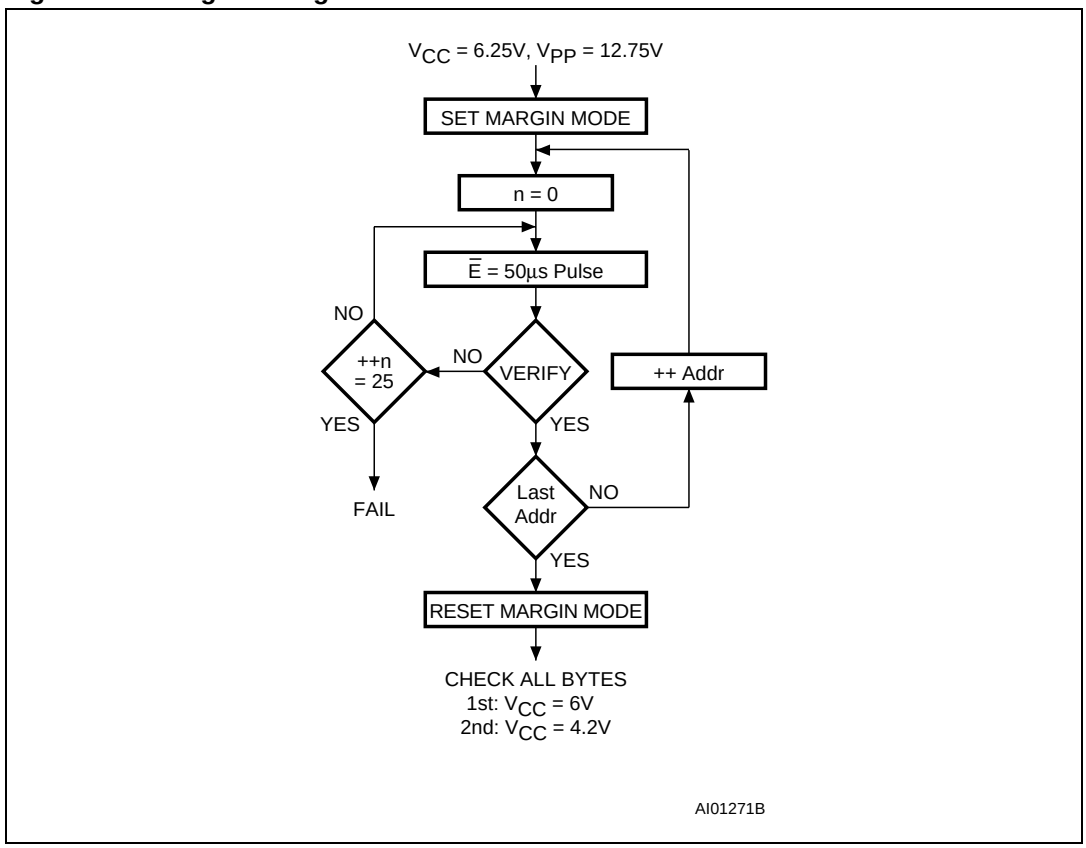
2.5 Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C801 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0' will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27C801 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is pulsed to V_{IL}. The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

2.6 Presto IIB programming algorithm

Presto IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. This can be achieved with STMicroelectronics M27C801 due to several design innovations to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal Margin Mode circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 50 µs program pulses are applied to each byte until a correct Verify occurs (see *Figure 5*). No overprogram pulses are applied since the Verify in Margin Mode provides the necessary margin.

Figure 5. Programming flowchart



2.7 Program Inhibit

Programming of multiple M27C801s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27C801 may be common. A TTL low level pulse applied to a M27C801's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C801. A high level $\overline{E}$ input inhibits the other M27C801s from being programmed.

2.8 Program Verify

A Verify (Read) should be performed on the programmed bits to determine that they were correctly programmed. The Verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

2.9 Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C801. To activate

the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C801. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the STMicroelectronics M27C801, these two identifier bytes are given in *Table 3* and can be read-out on outputs Q7 to Q0.

Table 3. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	1	0	42h

2.10 Erasure operation (applies to UV EPROM)

The erasure characteristics of the M27C801 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C801 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C801 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C801 window to prevent unintentional erasure. The recommended erasure procedure for the M27C801 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 30 W-sec/cm^2. The erasure time with this dosage is approximately 30 to 40 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C801 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

3 Maximum ratings

Table 4. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (2)	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (3)	Input or Output Voltage (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (3)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is VCC +0.5V with possible overshoot to VCC +2V for a period less than 20ns.

4 DC and AC characteristics

T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%

Table 5. Read Mode DC Characteristics (1)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		35	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7		V

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V

Table 6. Programming Mode DC Characteristics (1)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. AC Measurement Conditions

Parameter	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns (10% to 90%)
Input Pulse Voltages	0 to 3V	0.4 to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8 and 2V

T_A = 25 °C, f = 1 MHz

Table 8. Capacitance (1)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

1. Sampled only, not 100% tested.

Figure 6. AC Testing Input Output Waveform

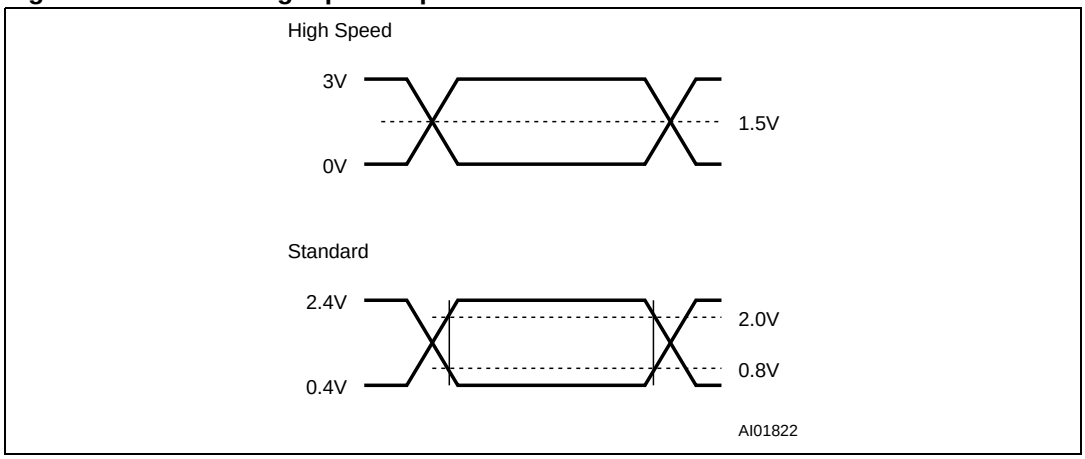
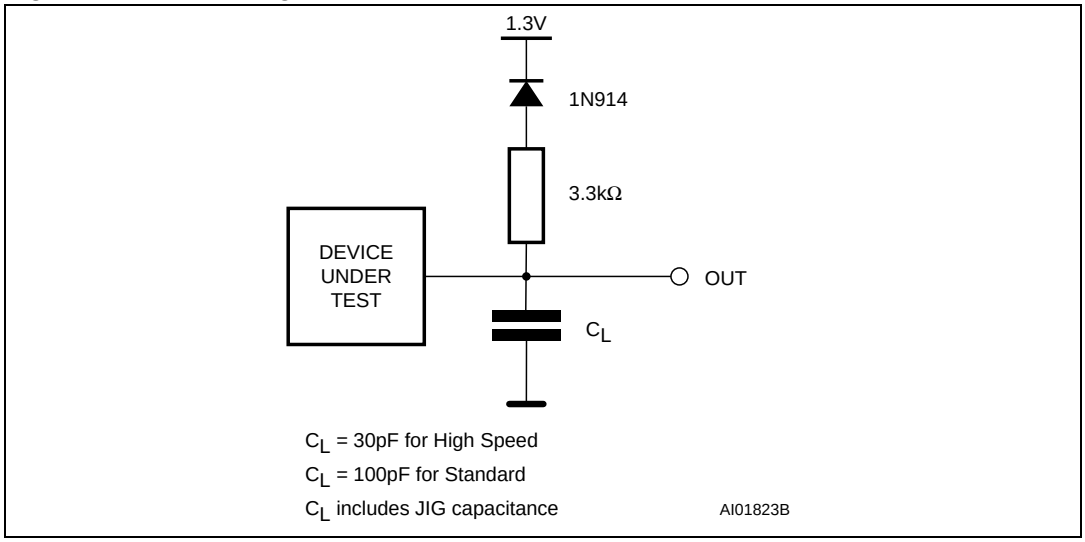


Figure 7. AC Testing Load Circuit



T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%

Table 9. Read Mode AC Characteristics (1)

Symbol	Alt	Parameter	Test Condition	-45 (2)		-55 (2)		-60		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}		45		55		60	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}V_{PP}$ = V_{IL}		45		55		60	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		25		30		30	ns
t_{EHQZ} (3)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}V_{PP}$ = V_{IL}	0	25	0	25	0	25	ns
t_{GHQZ} (3)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	25	0	25	0	25	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}	0		0		0		ns

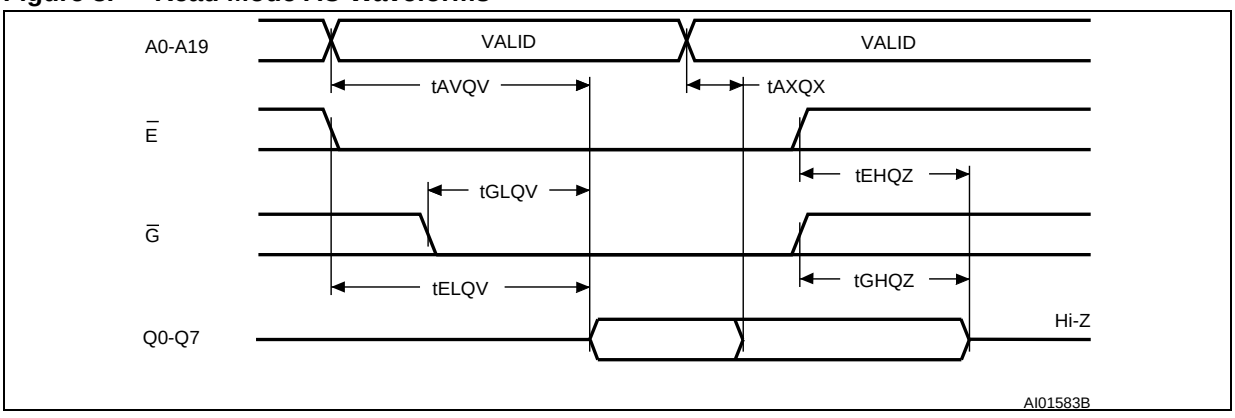
1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Speed obtained with High Speed AC measurement conditions.
3. Sampled only, not 100% tested.

Table 10. Read Mode AC Characteristics (1)

Symbol	Alt	Parameter	Test Condition	-70		-80		-100/-120/-150		Unit
				Min.	Max.	Min.	Max.	Min	Max.	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}		70		80		100	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}V_{PP}$ = V_{IL}		70		80		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}V_{PP}$ = V_{IL}	0	30	0	35	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}	0		0		0		ns

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 8. Read Mode AC Waveforms



T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V

Table 11. Margin Mode AC Characteristics (1)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	V_{A9} High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	V_{A10} High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	V_{A10} Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to V_{A10} Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to V_{A9} Transition		2		µs

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 9. Margin Mode AC Waveforms

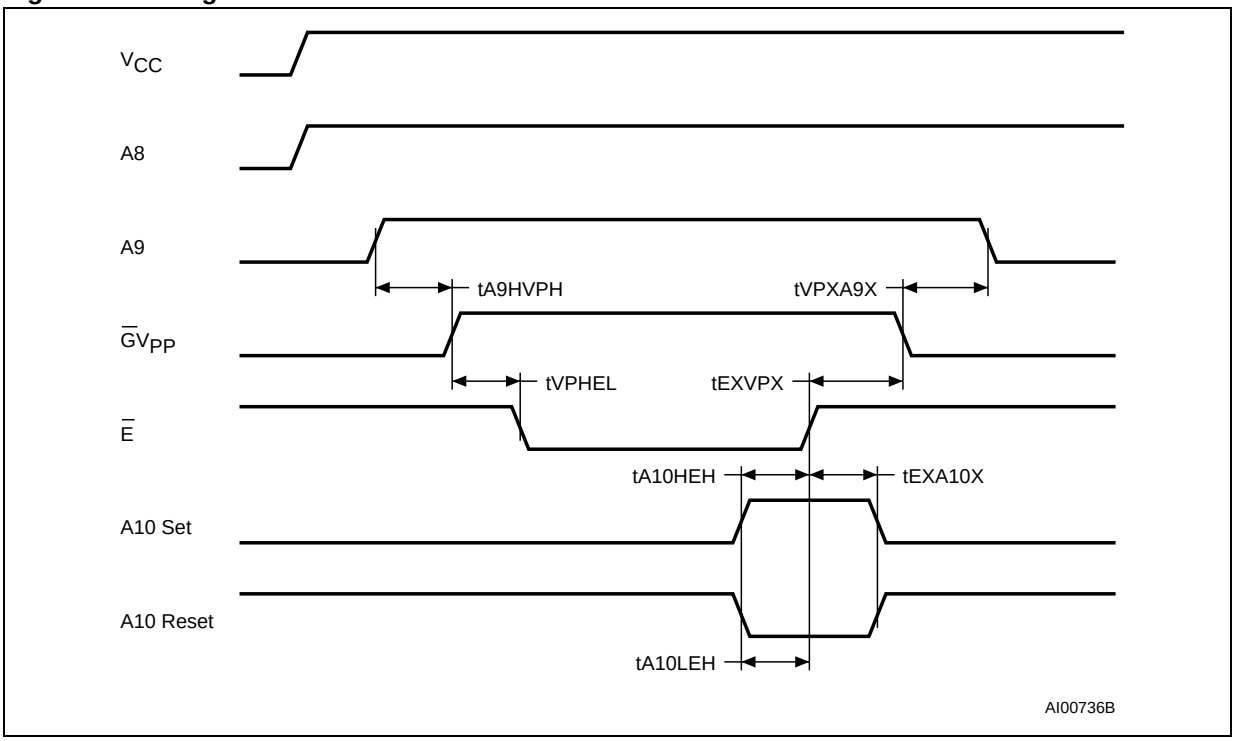
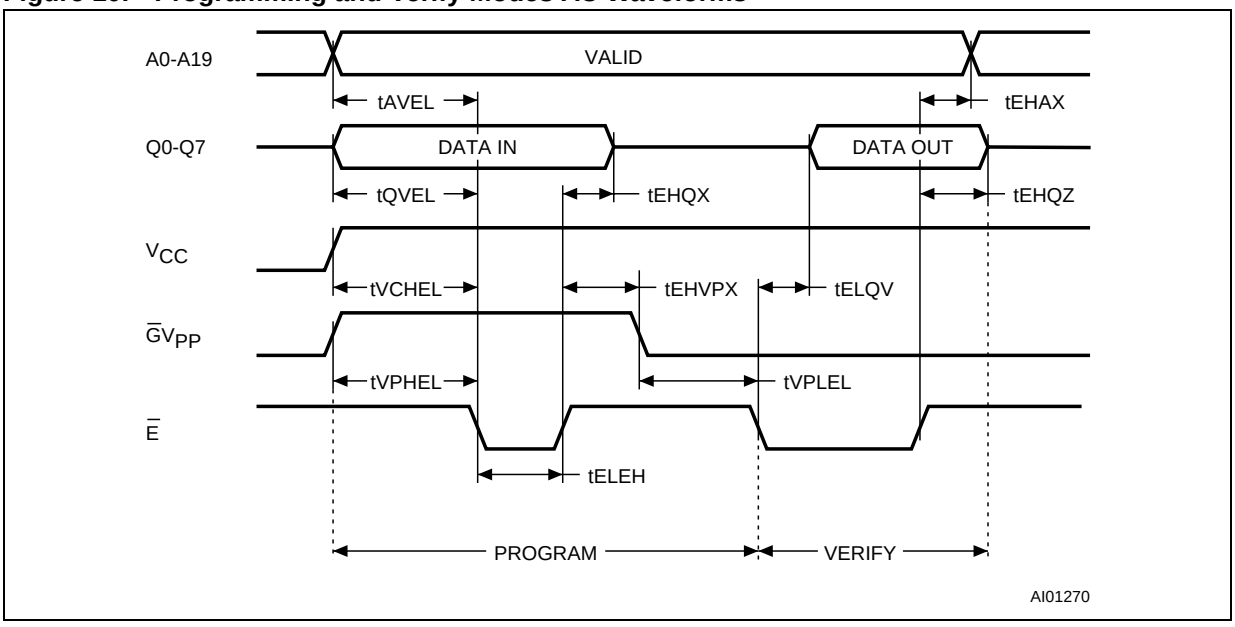


Table 12. Programming Mode AC Characteristics (1)

Symbol	Alt	Parameter	Test Condition	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		45	55	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 10. Programming and Verify Modes AC Waveforms



5 Package mechanical data

5.1 32-pin Ceramic Frit-seal DIP, with round window (FDIP32WA)

Figure 11. FDIP32WA package outline

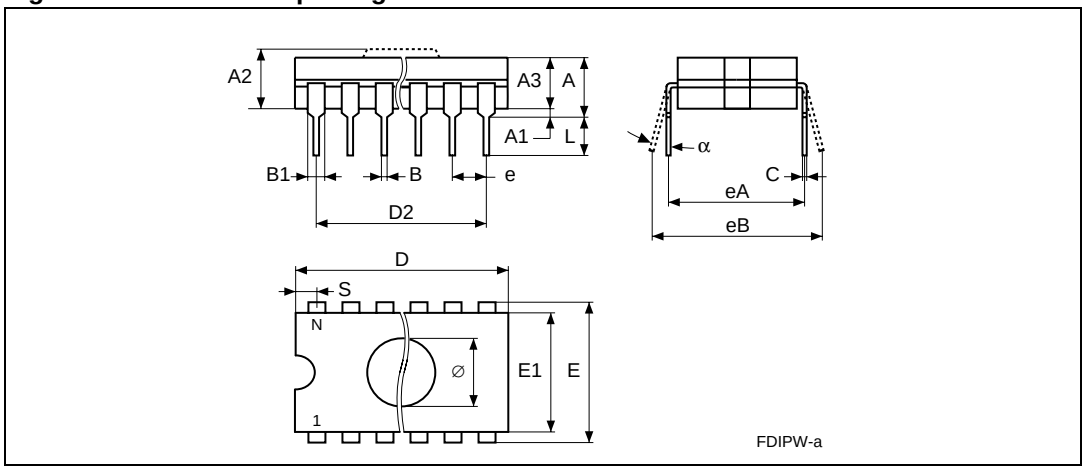


Table 13. FDIP32WA package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.72			0.225
A1	0.51		1.40	0.020		0.055
A2	3.91		4.57	0.154		0.180
A3	3.89		4.50	0.153		0.177
B	0.41		0.56	0.016		0.022
B1		1.45			0.057	
C	0.23		0.30	0.009		0.012
D	41.73		42.04	1.643		1.655
D2		38.10			1.500	
e		2.54			0.100	
E		15.24			0.600	
E1	13.06		13.36	0.514		0.526
eA		14.99			0.590	
eB	16.18		18.03	0.637		0.710
L	3.18		4.10	0.125		0.161
N		32			32	
S	1.52		2.49	0.060		0.098
Ø		7.11			0.280	
α	4°		11°	4°		11°

5.2 32-pin Plastic DIP, 600 mils width (PDIP32)

Figure 12. PDIP32 package outline

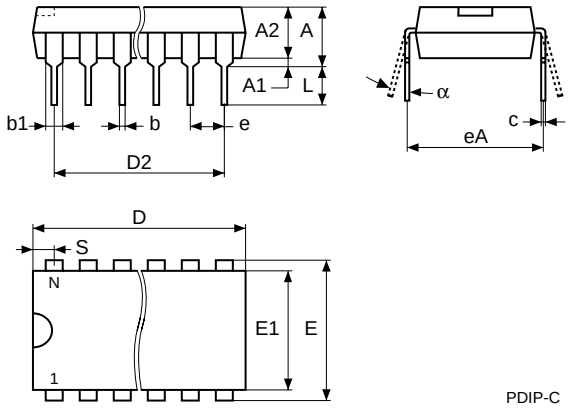


Table 14. PDIP32 package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			4.83			0.190
A1	0.38			0.015		
A2		3.81			0.150	
b	0.41		0.53	0.016		0.021
b1	1.14		1.65	0.045		0.065
c	0.23		0.38	0.009		0.015
D	41.78		42.29	1.645		1.665
D2		38.10			1.500	
eA		15.24			0.600	
e		2.54			0.100	
E	15.24		15.88	0.600		0.625
E1	13.46		13.97	0.530		0.550
S	1.65		2.21	0.065		0.087
L	3.05		3.56	0.120		0.140
α	0°		15°	0°		15°
N		32			32	

5.3 32-lead Rectangular Plastic Leaded Chip Carrier (PLCC32)

Figure 13. PLCC32 package outline

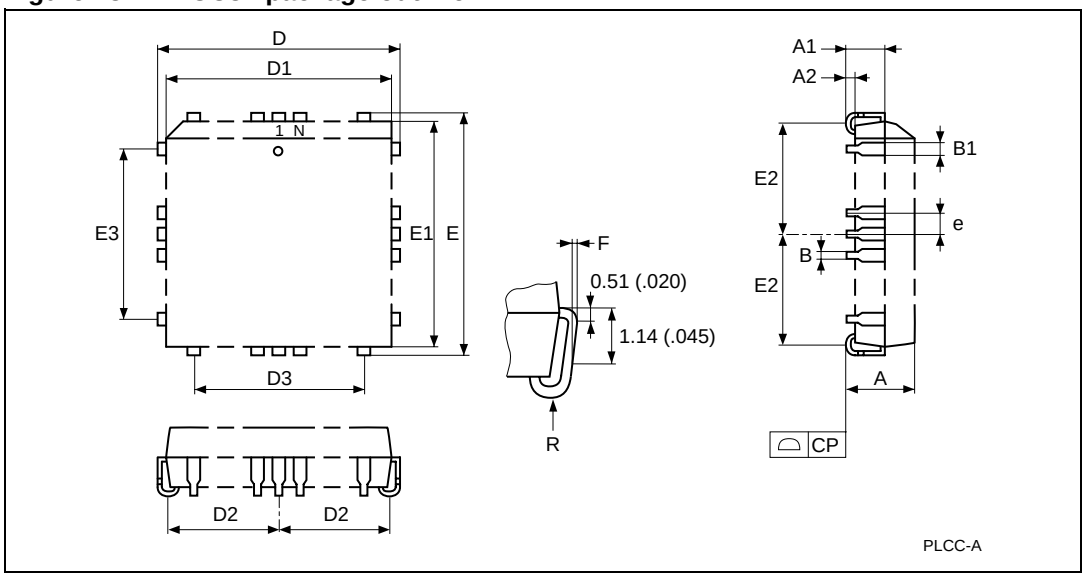


Table 15. PLCC32 package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.18		3.56	0.125		0.140
A1	1.53		2.41	0.060		0.095
A2	0.38		–	0.015		–
B	0.33		0.53	0.013		0.021
B1	0.66		0.81	0.026		0.032
CP			0.10			0.004
D	12.32		12.57	0.485		0.495
D1	11.35		11.51	0.447		0.453
D2	4.78		5.66	0.188		0.223
D3		7.62			0.300	
E	14.86		15.11	0.585		0.595
E1	13.89		14.05	0.547		0.553
E2	6.05		6.93	0.238		0.273
E3		10.16			0.400	
e		1.27			0.050	
F	0.00		0.13	0.000		0.005
R		0.89			0.035	
N		32			32	

5.4 32-lead Plastic Thin Small Outline, 8x20 mm (TSOP32)

Figure 14. TSOP32 package outline

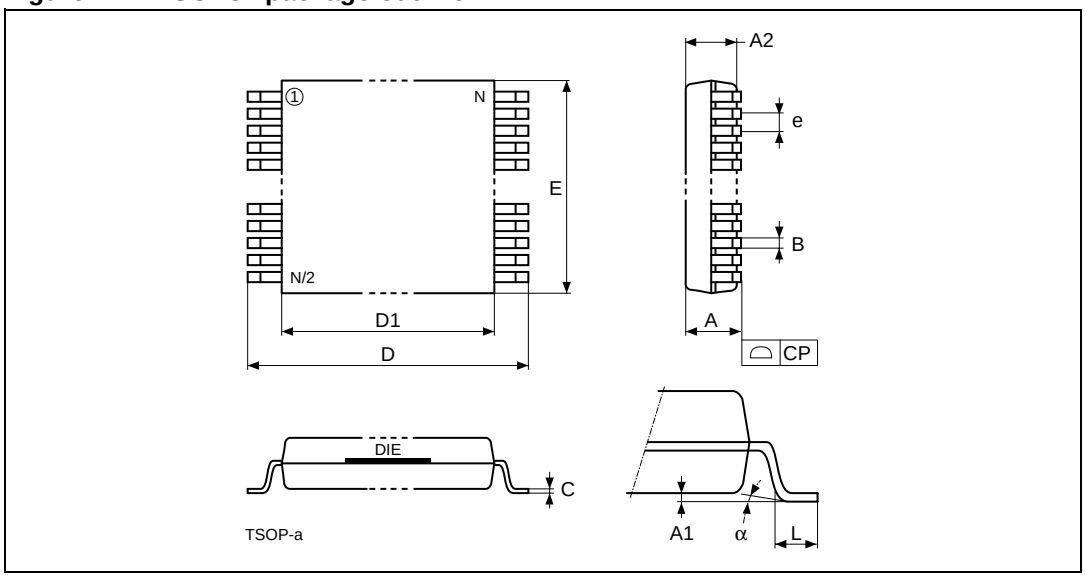


Table 16. TSOP32 package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.200			0.0472
A1	0.050		0.150	0.0020		0.0059
A2	0.950		1.050	0.0374		0.0413
B	0.170		0.250	0.0067		0.0098
C	0.100		0.210	0.0039		0.0083
CP			0.100			0.0039
D	19.800		20.200	0.7795		0.7953
D1	18.300		18.500	0.7205		0.7283
e		0.500			0.0197	
E	7.900		8.100	0.3110		0.3189
L	0.500		0.700	0.0197		0.0276
N		32			32	
α	0°		5°	0°		5°

6 Part numbering

Table 17. Ordering Information Scheme

Example: M27C801 -45 K 1

Device Type

M27

Supply Voltage

C = 5V ±10%

Device Function

801 = 8Mbit (1Mb x8)

Speed

-45 (1) = 45 ns	-80 = 80 ns
-55 (1) = 55 ns	-100 = 100 ns
-60 = 60 ns	-120 = 120 ns
-70 = 70 ns	-150 = 150 ns

Package

F = FDIP32W

B = PDIP32

K = PLCC32

N = TSOP32: 8 x 20 mm

Temperature Range

1 = 0 to 70 °C

6 = –40 to 85 °C

1. High Speed, see AC Characteristics section for further information.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
10-Sept-1998	1	First Issue
21-Mar-2000	2	FDIP32W Package changed
25-Sep-2000	3	AN620 Reference removed
12-Jul-2002	4	55ns speed class added PLCC32 Package mechanical drawing and data clarified
12-Apr-2006	5	Converted to new template. Added ECOPACK® information. Removed Tape & Reel Packing option.

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