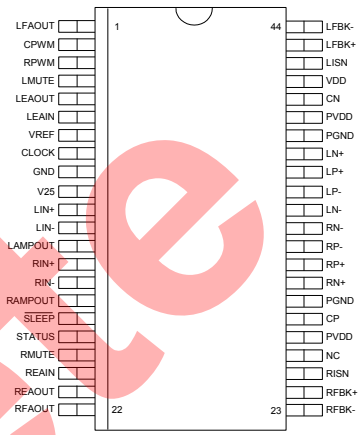
THERMAL DATA

DB 44-PIN QSSOP PACKAGE

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	50°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



DB PACKAGE
(Top View)

DESCRIPTION (CONTINUTED)

The stereo output controller is available in either an LX1722 high power version (>65Wrms, 4Ω) with a supply voltage range of 7V-25V or an LX1721 high fidelity version (better SNR performance) with a supply voltage range of 7V-15V. The current rating of the external MOSFET's, the available supply voltage, and speaker load primarily limits the maximum output power. The amplifier provides high fidelity performance and is designed to operate over the full 20Hz to 20kHz audio band. Signal distortion measurements yield.

THD+N levels of 0.06%(1kHz, 1Wrms). Efficiency is greater than 80% typical, which eliminates the need for heatsinks in most applications. The AudioMAX™ solution requires a single supply voltage, simplifying input power requirements where a dual supply may not be available. To minimize potential environmental noise issues and ease the integration of the amplifier into a variety of applications, features such as a balanced/differential audio input and a high power supply rejection ratio help reduce the effects of noise from the audio signal or power supply.

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FUNCTIONAL PIN DESCRIPTION

PIN NAME	DESCRIPTION	PIN NAME	DESCRIPTION
LFAOUT	Left Feedback Amplifier Output	LFBK-	Left Feedback Amplifier Inverting Input
CPWM	PWM Capacitor Connection	LFBK+	Left Feedback Amplifier Non-Inverting Input
RPWM	PWM Resistor Connection	LISN	Left Current Limit Sense Input
LMUTE	Left Mute Input (Active High)	VDD	Analog Supply Voltage
LEAOUT	Left Error Amplifier Output	CN	Supply Decoupling for NFET Drivers
LEAIN	Left Inverting Input of Error Amplifier	PVDD	Output Driver Supply Voltage
VREF	5V Reference	PGND	Output Driver High Current Ground
CLOCK	Input / Output Clock for Synch Operation	LN+	Left Drive for NFET on Positive Half of Bridge
GND	Low Current Ground	LP+	Left Drive for PFET on Positive Half of Bridge
V25	2.5V Reference	LP-	Left Drive for PFET on Negative Half of Bridge
LIN+	Left Positive Audio Input	LN-	Left Drive for NFET on Negative Half of Bridge
LIN-	Left Negative Audio Input	RN-	Right Drive for NFET on Negative Half of Bridge
LAMPOUT	Left Input Amplifier Output	RP-	Right Drive for PFET on Negative Half of Bridge
RIN+	Right Positive Audio Input	RP+	Right Drive for PFET on Positive Half of Bridge
RIN-	Right Negative Audio Input	RN+	Right Drive for NFET on Positive Half of Bridge
RAMPOUT	Right Input Amplifier Output	PGND	Output Driver High Current Ground
$\overline{\text{SLEEP}}$	Sleep Input (active low)	CP	Supply Decoupling for PFET Drivers
STATUS	UVLO Indicator (Open Collector Output)	PVDD	Output Driver Supply Voltage
RMUTE	Right Mute Input (Active High)	NC	No Connect
REAIN	Right Inverting Input of Error Amplifier	RISN	Right Current Limit Sense Input
REAOUT	Right Error Amplifier Output	RFBK+	Left Feedback Amplifier Non-Inverting Input
RFAOUT	Right Feedback Amplifier Output	RFBK-	Right Feedback Amplifier Inverting Input

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (PVDD, VDD) ..... -0.3V to 30V
$\overline{\text{SLEEP}}$, STATUS, R/LFBK+, R/LFBK- ..... -0.3V to VDD +0.3V
R/LISN ..... PVDD –2 to PVDD to +0.3V
RPWM, CPWM, R/LMUTE ..... -0.3V to VREF +0.3V
R/LIN+, R/LIN-, R/LAMPOUT ..... -0.3V to VREF +0.3V
R/LEAIN, R/LEAOUT, R/LFAOUT ..... -0.3V to VREF + 0.3V
CLOCK ..... -0.3V to CN +0.3V
Operating Junction Temperature Plastic ..... 125°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -20°C < T_A < 70°C (NOTE 2).
Test conditions: RPWM = 34.8k, CPWM = 100pF, VDD = PVDD = 15V

Parameter		Symbol	Test Conditions	LX1721 / 1722 Min	LX1721 / 1722 Typ	LX1721 / 1722 Max	Units
Evaluation Module (See LXE1721)							
Supply Voltage	LX1721	V_{DD}		7		15	V
	LX1722			7		25	
Power Supply Rejection Ratio		PSRR	V_{IN} = 15V, V_{RIPPLE} = 1V_{RMS}, 20Hz to 20kHz		-70		dB
Output Power (Per Channel)		P_O	V_{IN} = 15V, R_L=4Ω, THD+N=1%, 10Hz to 22kHz		25		W
			V_{IN} = 25V, R_L=4Ω, THD+N=1%, 10Hz to 22kHz		60		
Efficiency			V_{IN} = 15V, f_{IN} = 1kHz, P_O = 10W		82		%
			V_{IN} = 15V, f_{IN} = 1kHz, P_O = 20W		85		
Total Harmonic Distortion Plus Noise		THD+N	f_{IN} = 1kHz, P_O = 1W		.06		%
			f_{IN} = 20Hz to 20kHz, P_O = 1W			.2	
Signal-To-Noise Ratio		SNR	R_L = 4Ω, P_O = 1W		81		dBr
Oscillator Section							
Oscillator Frequency		F_{OSC}			450		kHz
Charge Current		I_{CHG}	(varies with V_{DD} pin voltage)		-225		µA
Discharge Current		I_{DIS}	(varies with V_{DD} pin voltage)		225		µA
Oscillator Peak Voltage		V_{PK}	(varies with V_{DD} pin voltage)		3.6		V
Oscillator Valley Voltage		V_{VAL}	(varies with V_{DD} pin voltage)		1.4		V
Voltage Stability			V_{DD} = 8V to 25V		0.6	2	%
Temperature Stability			T_A = 0°C to 70°C		1.0	2	%
Error Amplifier							
Input Offset Voltage		V_{IO}			5		mV
DC Open Loop Gain		A_{OL}			60		dB
Unity Gain Bandwidth		UGBW			7		MHz
High Output Voltage		V_{OH}	I_{OUT} = -100µA	3.5			V
Low Output Voltage		V_{OL}	I_{OUT} = +100µA			100	mV
Input Bias Current		I_{IN}	V_{IN} = 1V to 4V		1		µA
Input Amplifier							
Stage Gain			Set by Internal Resistors	3.465	3.5	3.535	V/V
Output Voltage, High		V_{OH}	I_{OUT} = -100µA	3.85			V
Output Voltage, Low		V_{OL}	I_{OUT} = +100µA			1.3	V
Input Impedance					180		kΩ
Feedback Amplifier							
Stage Gain	LX1721		Set by Internal Resistors	89	91	93	mV/V
	LX1722		Set by Internal Resistors	56	57	58	mV/V
Input Impedance	LX1721				250		kΩ
	LX1722				400		kΩ

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Test Conditions	LX1721 / 1722 Min	LX1721 / 1722 Typ	LX1721 / 1722 Max	Units
Current Limit Comparator						
Voltage Sense Threshold			190	210	230	mV
Blanking Pulse Delay				500		ns
Response Time		Excluding blanking pulse		250		ns
I_{UM} Pulses required to Current Limit Latch			4	4	4	cycles
Consecutive Clear Pulses required to reset I_{UM} counter			2	2	2	cycles
Reference Voltage Section						
Initial Accuracy (VREF)				5.0		
Voltage Stability (VREF)				± 50	± 100	mV
Initial Accuracy (V25)				2.5		
Voltage Stability (V25)				± 25	± 50	mV
Temperature Stability		T_A = 0°C to 70°C		2	5	mV
Line Regulation		V_{DD} = 9V to 15V		0.5		mV
Load Regulation		I_{OUT} = 0 to 10mA		5		mV
Under Voltage Lockout Section						
Start Threshold Voltage				6		V
UV Lockout Hysteresis				250		mV
UVLO Delay To Output Enable				62,500		clkcyc
Supply Current						
Sleep Current		$\overline{SLEEP}$ Input = 0V, T_A = 25°C		30		µA
Operating Current		$\overline{SLEEP}$ Input = 2V, V_{IN} = 15V, No MOSFETs connected		8	11	mA
Sleep to Output Enable				62,500		clkcyc
Sleep Threshold			1.45	1.6	1.75	V
Mute Section						
Mute Threshold			1.2	1.35	1.5	V
Output Drivers For N-Channel MOSFETs						
NFET Drivers, Low Level Voltage	V_{OL}	I_{SINK} = 3mA		30	100	mV
		I_{SINK} = 100mA		0.3	1.0	V
NFET Drivers, High Level Voltage	V_{OH}	I_{SOURCE} = 3mA, C_N = 5.2V applied externally		30	100	mV
		I_{SOURCE} = 100mA, C_N = 5.2V applied externally		0.3	1.0	V
Output Drives For P-Channel MOSFETs						
PFET Drivers, Low Level Voltage	V_{OL}	I_{SINK} = 3mA		30	100	mV
		I_{SINK} = 100mA		0.5	1.0	V
PFET Drivers, High Level Voltage	V_{OH}	I_{SOURCE} = 3mA, C_P = 5.2V (applied externally)		30	100	mV
		I_{SOURCE} = 100mA, C_P = 5.2V (applied externally)		0.5	1.0	V

Note 2: The LX1721 / 22CDB is guaranteed to meet performance specifications from 0° to 70°C. Specifications over the -20° to 0°C operation temperature range are assured by design, characterization, and statistical process control.

BLOCK DIAGRAM

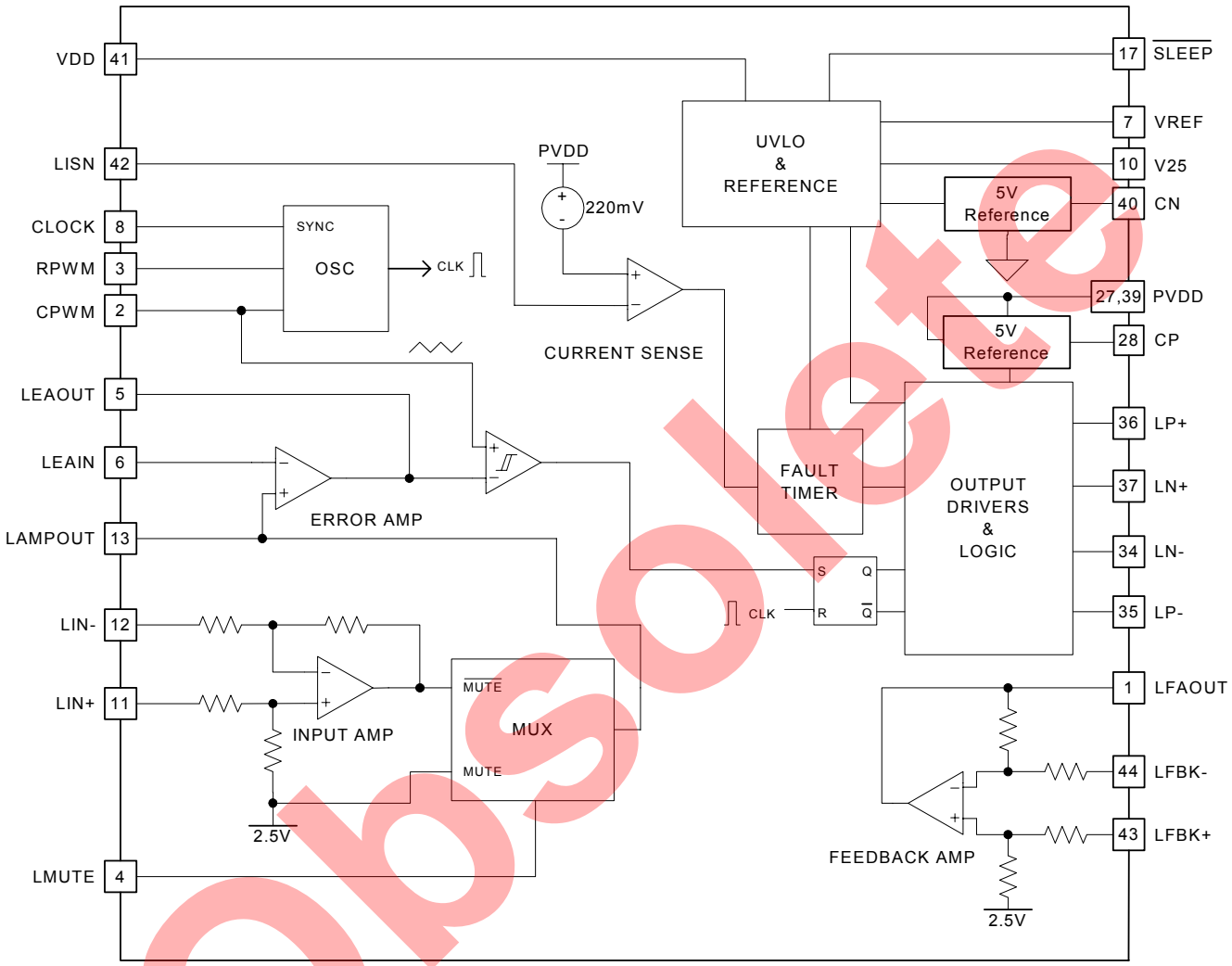

FIGURE 1 – LX1721 / 22 SIMPLIFIED BLOCK DIAGRAM (LEFT CHANNEL CIRCUIT SHOWN)

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APPLICATION INFORMATION

Frequency Synchronization

Two or more LX1721 / LX1722 oscillators can be configured for synchronous operation. One unit, the master, is programmed for the desired frequency with the R_{PWM} and C_{PWM} as usual. Additional units will be slave units, and their oscillators will be disabled by leaving the R_{PWM} pin disconnected. The CLOCK pin and the C_{PWM} pin of the slave units should be tied to the CLOCK pin and the C_{PWM} pin of the master unit respectively. In this configuration, the CLOCK pins of the slave units begin receiving instead of transmitting clock pulses. Also, the C_{PWM} pins quit driving the PWM capacitor in the slave units. Note that for optimum performance, all slave units should be located within a few inches of the master unit.

Oscillator Configuration (R_{PWM} and C_{PWM} selection)

The oscillator is programmed by the external timing components R_{PWM} and C_{PWM}. For a nominal frequency of 333kHz, R_{PWM} and C_{PWM} should be set to 49.9kOhms and 100pF respectively. Note that in order to keep the slope of the PWM ramp voltage proportional to the supply voltage, both the ramp peak and valley voltages, and the charge and discharge currents are proportional to the supply voltage. This keeps the frequency relatively constant while keeping the slope of the PWM ramp proportional to the voltage on the VDD pin. For operating frequencies other than 333kHz, the frequency can be approximated by the following equation:

$$\text{Frequency} = \frac{1}{(0.577)(R_{PWM})(C_{PWM}) + 320ns}$$

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CHARACTERISTIC CURVES

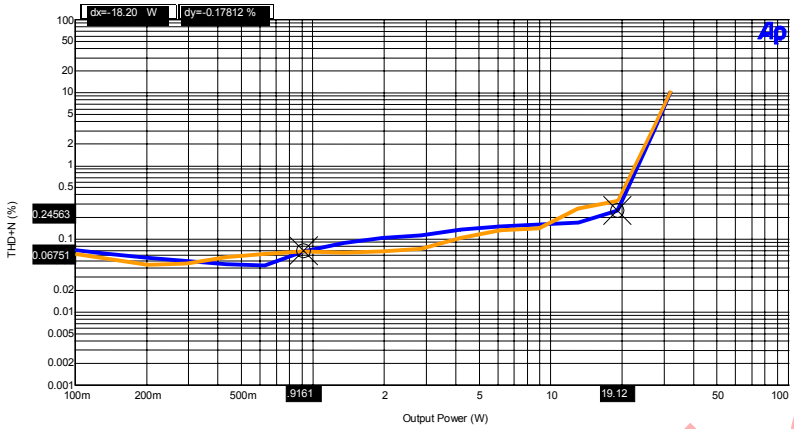

FIGURE 2 – THD+N VS. OUTPUT POWER

V_{IN} = 15V
f_{IN} = 1kHz
R_L = 4Ω

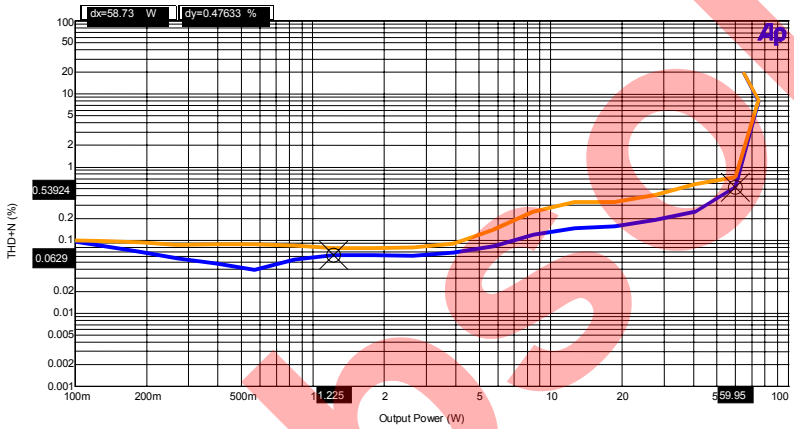

FIGURE 3 – THD+N VS. OUTPUT POWER

V_{IN} = 25V
f_{IN} = 1kHz
R_L = 4Ω

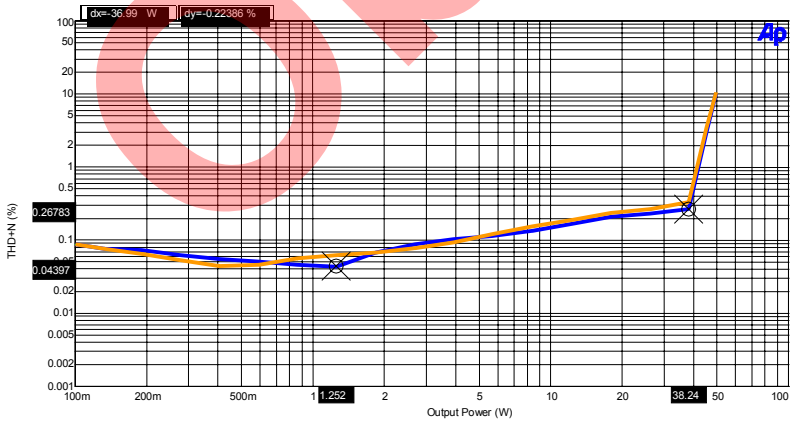

FIGURE 4 – THD+N VS. OUTPUT POWER

V_{IN} = 15V
f_{IN} = 1kHz
R_L = 2Ω

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CHARACTERISTIC CURVES (CONTINUED)

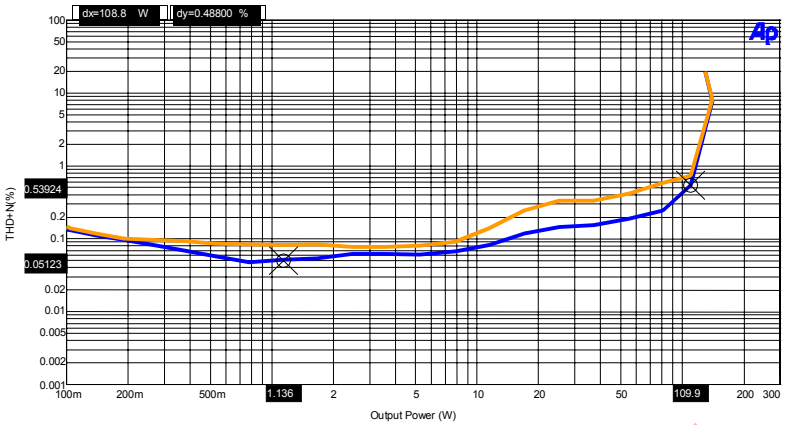


FIGURE 5 – THD+N VS. OUTPUT POWER

V_{IN} = 25V
f_{IN} = 1kHz
R_L = 2Ω

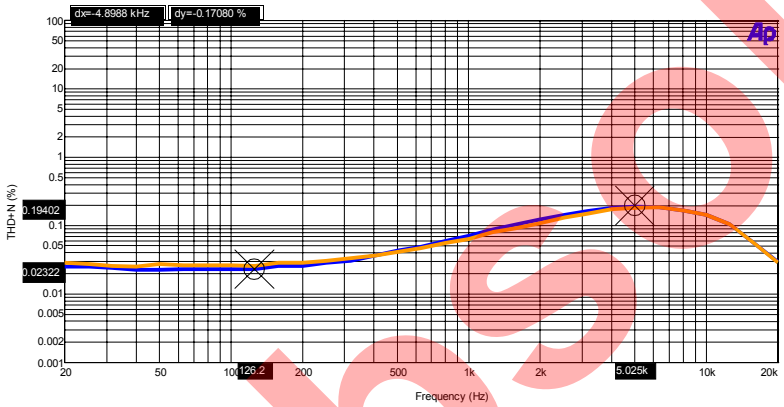


FIGURE 6 – THD+N VS. FREQUENCY

V_{IN} = 15V
R_L = 4Ω
P_O = 1W_{RMS}

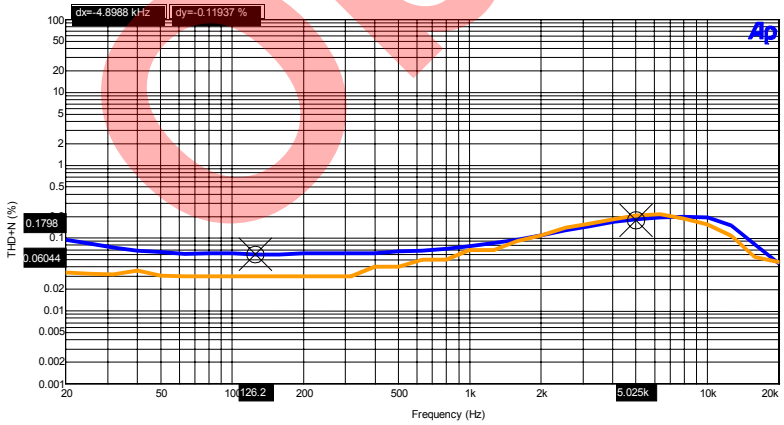


FIGURE 7 – THD+N VS. FREQUENCY

V_{IN} = 25V
R_L = 4Ω
P_O = 1W_{RMS}

CHARACTERISTIC CURVES (CONTINUED)

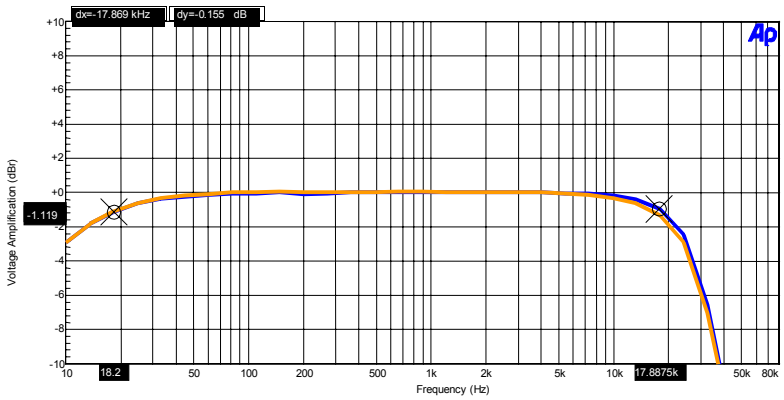


FIGURE 8 – FREQUENCY RESPONSE

V_{IN} = 15V
R_L = 4Ω
P_O = 1W_{RMS}

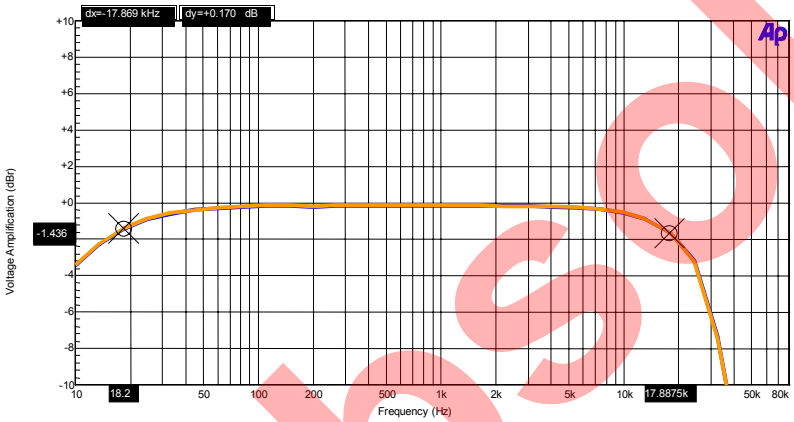


FIGURE 9 – FREQUENCY RESPONSE

V_{IN} = 25V
R_L = 4Ω
P_O = 1W_{RMS}

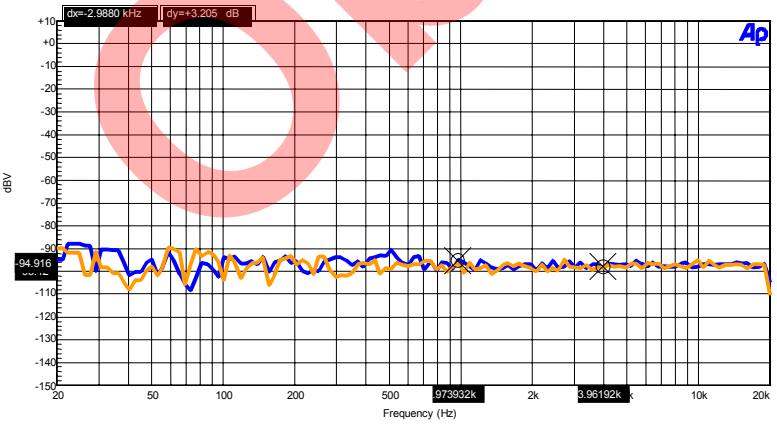


FIGURE 10 – NOISE FLOOR FFT

V_{IN} = 15V
R_L = 4Ω
10Hz – 22kHz Bandwidth
A-weighted

CHARACTERISTIC CURVES (CONTINUED)

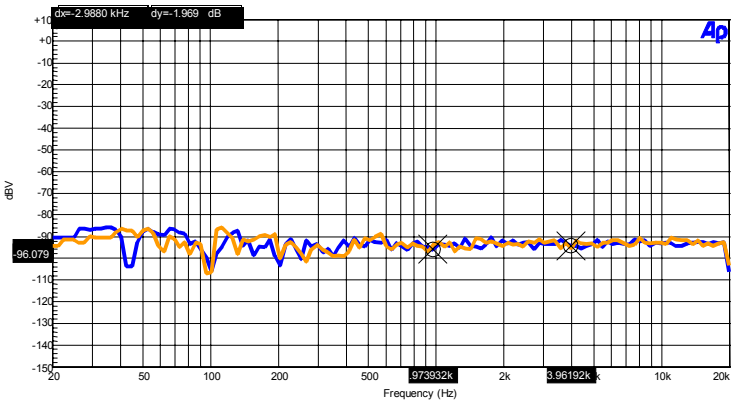


FIGURE 11 – NOISE FLOOR FFT

V_{IN} = 25V
R_L = 4Ω
10Hz – 22kHz Bandwidth
A-Weighted

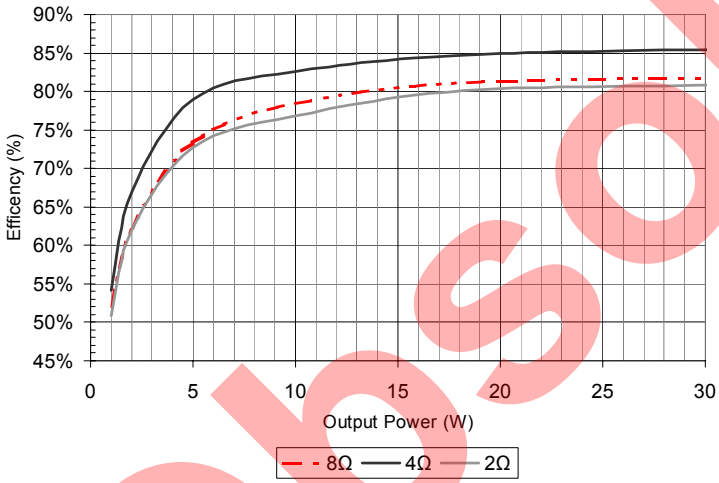


FIGURE 12 – EFFICIENCY VS. OUTPUT POWER

V_{IN} = 15V
f_{IN} = 1kHz

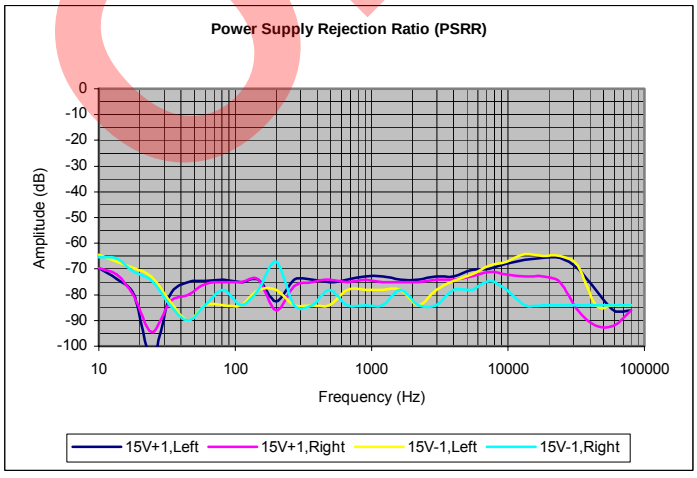


FIGURE 13 – POWER SUPPLY REJECTION RATIO (PSSR)

P_O = 1W_{RMS}
R_L = 4Ω

APPLICATION

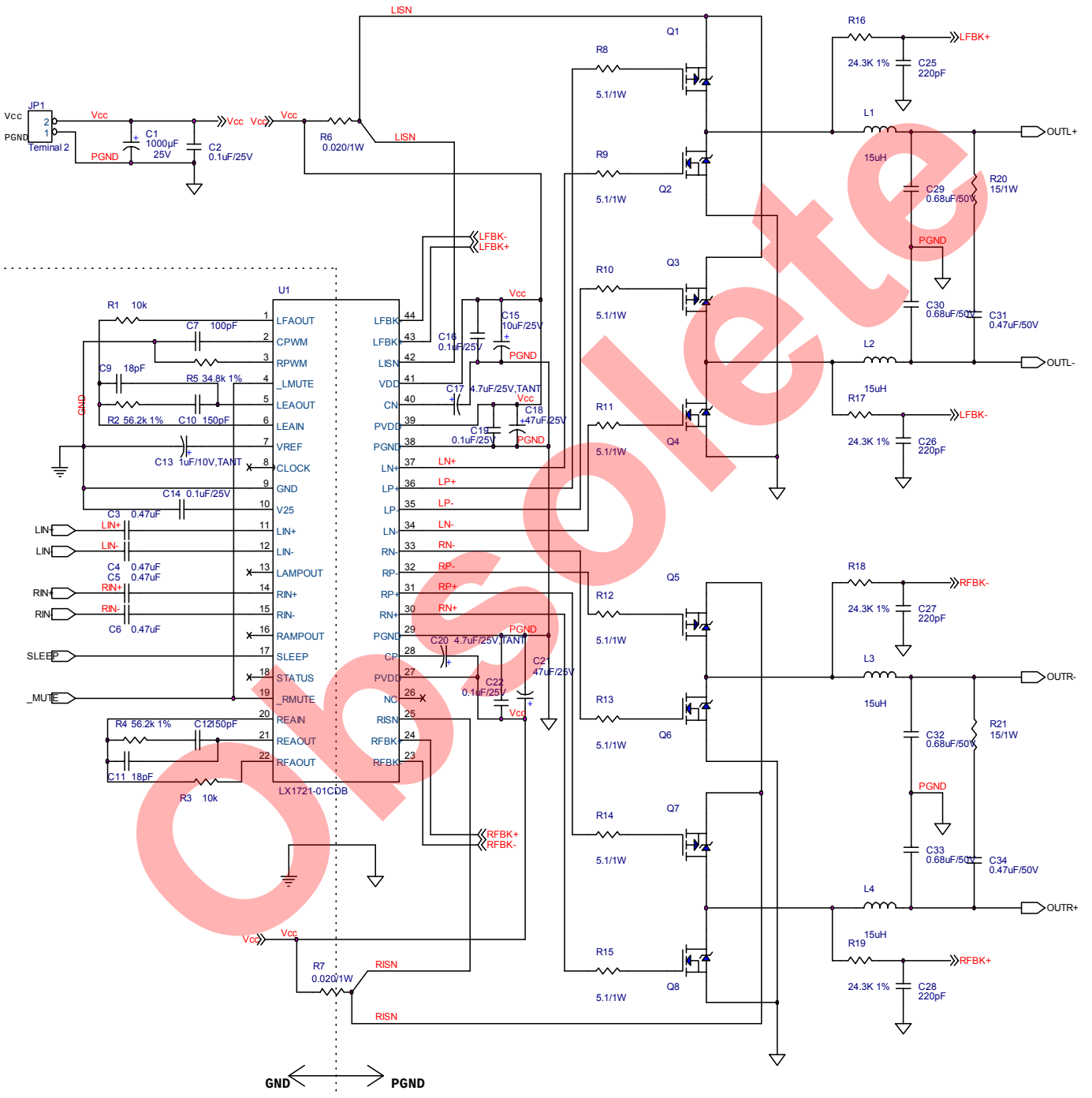
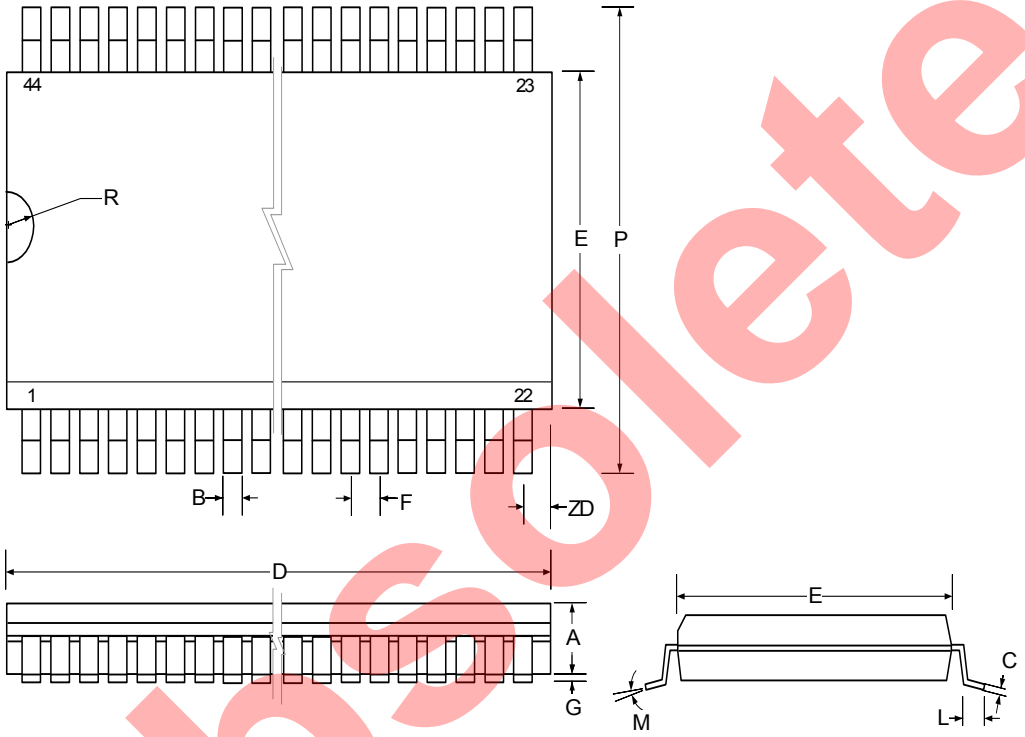


FIGURE 14 – TYPICAL CLASS-D STEREO SWITCHING AMPLIFIER CIRCUIT APPLICATION

MECHANICAL DIMENSIONS

DB 44-Pin Quarter Size Outline Package (QSOP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.44	2.64	0.096	0.104
B	0.28	0.51	0.011	0.020
C	0.23	0.32	0.091	0.0125
D	17.73	17.93	0.698	0.706
E	7.40	7.60	0.291	0.299
F	0.80 BSC		0.0315 BSC	
G	0.10	0.30	0.004	0.012
L	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
P	10.11	10.51	0.396	0.414
R	0.63	0.89	0.025	0.035
ZD	0.51 REF		0.020 REF	
*LC	-	0.10	-	0.004

* Lead Coplanarity

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.15mm (.006") on any side. Lead dimension shall not include solder coverage.

NOTES

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