ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

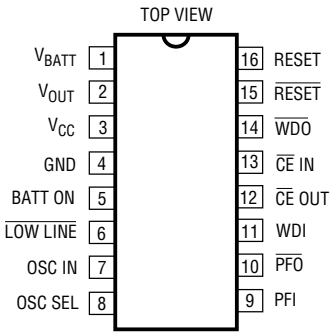
Terminal Voltage
- V_{CC} ..... −0.3V to 6.0V
- V_{BATT} ..... −0.3V to 6.0V
- All Other Inputs ..... −0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

V_{OUT} Output Current ..... Short-Circuit Protected
Power Dissipation 500mW
Operating Temperature Range
- LTC690/91/94/95C ..... 0°C to 70°C
- LTC690/91/94/95I ..... −40°C to 85°C
- LTC690M ..... −55°C to 125°C

Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION (Note 3)

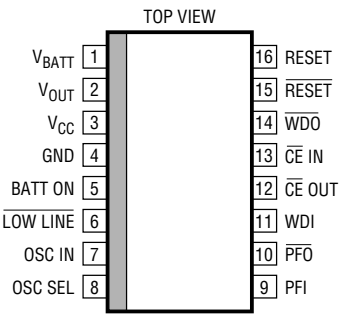


N PACKAGE
16-LEAD PDIP

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC691CN
LTC691IN
LTC695CN
LTC695IN

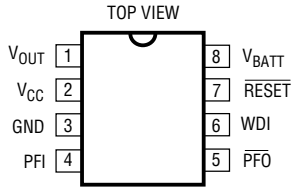


SW PACKAGE
16-LEAD WIDE PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 130°C/W Conditions: PCB mount on FR4 Material, Still Air at 25°C, Copper Trace

ORDER PART NUMBER

LTC691CSW
LTC691ISW
LTC695CSW
LTC695ISW

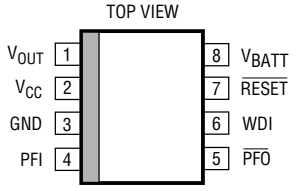


J8 PACKAGE
8-LEAD CERDIP

N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 110°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 110°C, θ_{JA} = 130°C/W (N8)

LTC690CN8
LTC690IN8
LTC690MJ8
LTC694CN8
LTC694IN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 180°C/W Conditions: PCB Mount on FR4 Material, Still Air AT 25°C, Copper Trace

LTC690CS8
LTC690IS8
LTC694CS8
LTC694IS8

S8 PART MARKING

690 694
690I 694I

PRODUCT SELECTION GUIDE

	PINS	RESET	WATCHDOG TIMER	BATTERY BACK-UP	POWER-FAIL WARNING	RAM WRITE PROTECT	PUSH-BUTTON RESET	CONDITIONAL BATTERY BACK-UP
LTC690	**8**	**X**	**X**	**X**	**X**			
LTC691	**16**	**X**	**X**	**X**	**X**	**X**		
LTC694	**8**	**X**	**X**	**X**	**X**			
LTC695	**16**	**X**	**X**	**X**	**X**	**X**		
LTC699	8	X	X					
LTC1232	8	X	X				X	
LTC1235	16	X	X	X	X	X	X	X

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = full operating range, V_{BATT} = 2.8V, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
Battery Back-Up Switching						
Operating Voltage Range	V_{CC} V_{BATT}		4.75 2.00		5.50 4.25	V V
V_{OUT} Output Voltage	I_{OUT} = 1mA	 ●	V_{CC} – 0.05 V_{CC} – 0.10	V_{CC} – 0.005 V_{CC} – 0.005		V V
	I_{OUT} = 50mA		V_{CC} – 0.50	V_{CC} – 0.250		V
V_{OUT} in Battery Back-Up Mode	I_{OUT} = 250µA, V_{CC} < V_{BATT}		V_{BATT} – 0.1	V_{BATT} – 0.02		V
Supply Current (Exclude I_{OUT})	$I_{OUT} \leq$ 50mA	 ●		0.6 0.6	1.5 2.5	mA mA
Supply Current in Battery Back-Up Mode	V_{CC} = 0V, V_{BATT} = 2.8V	 ●		0.04 0.04	1 5	µA µA
Battery Standby Current (+ = Discharge, – = Charge)	5.5 > V_{CC} > V_{BATT} + 0.2V	 ●	–0.1 –1.0		+0.02 +0.10	µA µA
Battery Switchover Threshold, V_{CC} – V_{BATT}	Power Up Power Down			70 50		mV mV
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage (Note 4)	I_{SINK} = 3.2mA				0.4	V
BATT ON Output Short-Circuit Current (Note 4)	BATT ON = V_{OUT} Sink Current			35		m
	BATT ON = 0V Source Current		0.5	1	25	µA
Reset and Watchdog Timer						
Reset Voltage Threshold		●	4.5	4.65	4.75	V
	LTC690M	●	4.4	4.65	4.75	V
Reset Threshold Hysteresis				40		mV
Reset Active Time (LTC690/91) (Note 5)	OSC SEL HIGH, V_{CC} = 5V	 ●	40 35	50 50	60 70	ms ms
Reset Active Time (LTC694/95) (Note 5)	OSC SEL HIGH, V_{CC} = 5V	 ●	160 140	200 200	240 280	ms ms
Watchdog Time-Out Period, Internal Oscillator	Long Period, V_{CC} = 5V	 ●	1.2 1.0	1.6 1.6	2.00 2.25	sec sec
	Short Period, V_{CC} = 5V	 ●	80 70	100 100	120 140	ms ms
Watchdog Time-Out Period, External Clock (Note 6)	Long Period Short Period		4032 960		4097 1025	Clock Cycles Clock Cycles
Reset Active Time PSRR				1		ms/V
Watchdog Time-Out Period PSRR, Internal OSC				1		ms/V
Minimum WDI Input Pulse Width	V_{IL} = 0.4V, V_{IH} = 3.5V	●	200			ns
$\overline{\text{RESET}}$ Output Voltage at V_{CC} = 1V	I_{SINK} = 10µA, V_{CC} = 1V			4	200	mV
$\overline{\text{RESET}}$ and $\overline{\text{LOW LINE}}$ Output Voltage (Note 4)	I_{SINK} = 1.6mA, V_{CC} = 4.25V I_{SOURCE} = 1µA, V_{CC} = 5V		 3.5		0.4	V V
RESET and $\overline{\text{WDO}}$ Output Voltage (Note 4)	I_{SINK} = 1.6mA, V_{CC} = 5V I_{SOURCE} = 1µA, V_{CC} = 4.25V		 3.5		0.4	V V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = full operating range, V_{BATT} = 2.8V, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
RESET, $\overline{\text{RESET}}$, $\overline{\text{WDO}}$, $\overline{\text{LOW LINE}}$ Output Short-Circuit Current (Note 4)	Output Source Current		1	3	25	µA
	Output Sink Current			25		mA
WDI Input Threshold	Logic Low Logic High		 3.5		0.8	V
WDI Input Current	WDI = V_{OUT} WDI = 0V	● ●	 –50	4 –8	50	µA
Power-Fail Detector						
PFI Input Threshold	V_{CC} = 5V	●	1.25	1.3	1.35	V
PFI Input Threshold PSRR				0.3		mV/V
PFI Input Current				±0.01	±25	nA
$\overline{\text{PFO}}$ Output Voltage (Note 4)	I_{SINK} = 3.2mA I_{SOURCE} = 1µA		 3.5		0.4	V
$\overline{\text{PFO}}$ Short-Circuit Source Current (Note 4)	PFI = HIGH, $\overline{\text{PFO}}$ = 0V		1	3	25	µA
	PFI = LOW, $\overline{\text{PFO}}$ = V_{OUT}			25		mA
PFI Comparator Response Time (Falling)	ΔV_{IN} = –20mV, V_{OD} = 15mV			2		µs
PFI Comparator Response Time (Rising) (Note 4)	ΔV_{IN} = 20mV, V_{OD} = 15mV with 10kΩ Pull-Up			40 8		µs
Chip Enable Gating						
$\overline{\text{CE}}$ IN Threshold	V_{IL} V_{IH}		 2.0		0.8	V
$\overline{\text{CE}}$ IN Pull-Up Current (Note 7)				3		µA
$\overline{\text{CE}}$ OUT Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 3.0mA I_{SOURCE} = 1µA, V_{CC} = 0V		 V_{OUT} – 1.50 V_{OUT} – 0.05		0.4	V
$\overline{\text{CE}}$ Propagation Delay	V_{CC} = 5V, C_L = 20pF	 ●		20 20	35 45	ns
$\overline{\text{CE}}$ OUT Output Short-Circuit Current	Output Source Current Output Sink Current			30 35		mA
Oscillator						
OSC IN Input Current (Note 7)				±2		µA
OSC SEL Input Pull-Up Current (Note 7)				5		µA
OSC IN Frequency Range	OSC SEL = 0V	●	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V, C_{OSC} = 47pF			4		kHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: For military temperature range parts or for the LTC692 and LTC693, consult the factory.

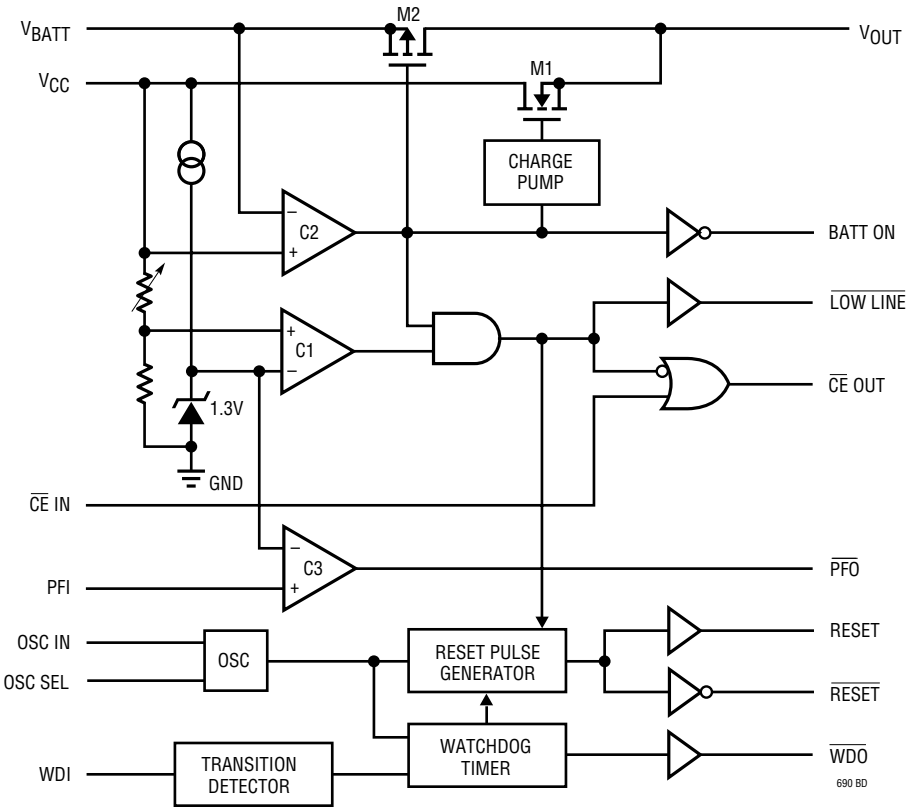
Note 4: The output pins of BATT ON, $\overline{\text{LOW LINE}}$, $\overline{\text{PFO}}$, $\overline{\text{WDO}}$, $\overline{\text{RESET}}$ and RESET have weak internal pull-ups of typically 3µA. However, external pull-up resistors may be used when higher speed is required.

Note 5: The LTC690 and LTC691 have minimum reset active time of 35ms (50ms typically) while the LTC694 and LTC695 have longer minimum reset active time of 140ms (200ms typically). The reset active time of the LTC691 and LTC695 can be adjusted (see Table 2 in Applications Information section).

Note 6: The external clock feeding into the circuit passes through the oscillator before clocking the watchdog timer (See Block Diagram). Variation in the time-out period is caused by phase errors which occur when the oscillator divides the external clock by 64. The resulting variation in the time-out period is 64 clocks plus one clock of jitter.

Note 7: The input pins of $\overline{\text{CE}}$ IN, OSC IN and OSC SEL have weak internal pullups which pull to the supply when the input pins are floating.

BLOCK DIAGRAM



PIN FUNCTIONS

V_{CC}: 5V Supply Input. The V_{CC} pin should be bypassed with a 0.1µF capacitor.

V_{OUT}: Voltage Output for Backed Up Memory. Bypass with a capacitor of 0.1µF or greater. During normal operation, V_{OUT} obtains power from V_{CC} through an NMOS power switch, M1, which can deliver up to 50mA and has a typical on resistance of 5Ω. When V_{CC} is lower than V_{BATT}, V_{OUT} is internally switched to V_{BATT}. If V_{OUT} and V_{BATT} are not used, connect V_{OUT} to V_{CC}.

V_{BATT}: Back-Up Battery Input. When V_{CC} falls below V_{BATT}, auxiliary power, connected to V_{BATT}, is delivered to V_{OUT} through PMOS switch, M2. If back-up battery or auxiliary power is not used, V_{BATT} should be connected to GND.

GND: Ground pin.

BATT ON: Battery On Logic Output from Comparator C2. BATT ON goes low when V_{OUT} is internally connected to V_{CC}. The output typically sinks 35mA and can provide base drive for an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}. BATT ON goes high when V_{OUT} is internally switched to V_{BATT}.

PFI: Power Failure Input. PFI is the noninverting input to the power-fail comparator, C3. The inverting input is internally connected to a 1.3V reference. The power failure output remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. Connect PFI to GND or V_{OUT} when C3 is not used.

PIN FUNCTIONS

$\overline{PFO}$: Power Failure Output from C3. $\overline{PFO}$ remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. When V_{CC} is lower than V_{BATT}, C3 is shut down and $\overline{PFO}$ is forced low.

$\overline{RESET}$: Logic Output for µP Reset Control. Whenever V_{CC} falls below either the reset voltage threshold (4.65V, typically) or V_{BATT}, $\overline{RESET}$ goes active low. After V_{CC} returns to 5V, reset pulse generator forces $\overline{RESET}$ to remain active low for a minimum of 35ms for the LTC690 /LTC691 (140ms for the LTC694/LTC695). When the watchdog timer is enabled but not serviced prior to a preset time-out period, reset pulse generator also forces $\overline{RESET}$ to active low for a minimum of 35ms for the LTC690/LTC691 (140ms for the LTC694/5) for every preset time-out period (see Figure 11). The reset active time is adjustable on the LTC691/LTC695. An external push-button reset can be used in connection with the $\overline{RESET}$ output. See Push-Button Reset in Applications Information section.

RESET: RESET is an active high logic ouput. It is the inverse of $\overline{RESET}$.

$\overline{LOW\ LINE}$: Logic Output from Comparator C1. $\overline{LOW\ LINE}$ indicates a low line condition at the V_{CC} input. When V_{CC} falls below the reset voltage threshold (4.65V typically), $\overline{LOW\ LINE}$ goes low. As soon as V_{CC} rises above the reset voltage threshold, $\overline{LOW\ LINE}$ returns high (see Figure 1). $\overline{LOW\ LINE}$ goes low when V_{CC} drops below V_{BATT} (see Table 1).

WDI: Watchdog Input, WDI, is a three level input. Driving WDI either high or low for longer than the watchdog time-out period, forces both $\overline{RESET}$ and $\overline{WDO}$ low. Floating WDI disables the watchdog timer. The timer resets itself with each transition of the watchdog input (see Figure 11).

$\overline{WDO}$: Watchdog Logic Output. When the watchdog input remains either high or low for longer than the watchdog time-out period, $\overline{WDO}$ goes low. $\overline{WDO}$ is set high whenever there is a transition on the WDI pin, or $\overline{LOW\ LINE}$ goes low. The watchdog timer can be disabled by floating WDI (see Figure 11).

$\overline{CE}$ IN: Logic input to the Chip Enable gating circuit. $\overline{CE}$ IN can be derived from microprocessor's address line and/or decoder output. See Applications Information section and Figure 5 for additional information.

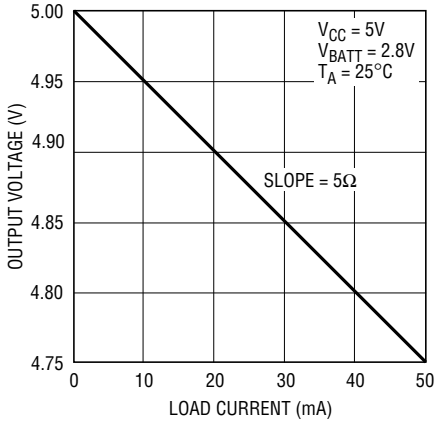
$\overline{CE}$ OUT: Logic Output on the Chip Enable Gating Circuit. When V_{CC} is above the reset voltage threshold, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN. When V_{CC} is below the reset voltage threshold $\overline{CE}$ OUT is forced high (see Figure 5).

OSC SEL: Oscillator Selection Input. When OSC SEL is high or floating, the internal oscillator sets the reset active time and watchdog time-out period. Forcing OSC SEL low, allows OSC IN be driven from an external clock signal or external capacitor be connected between OSC IN and GND.

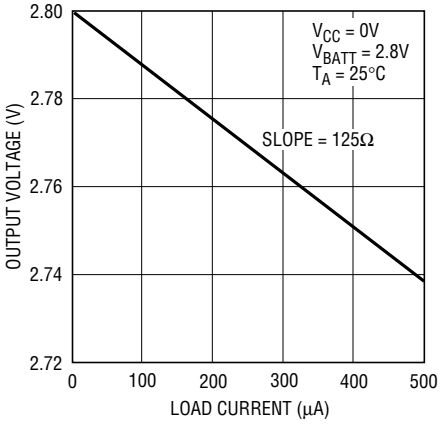
OSC IN: Oscillator Input. OSC IN can be driven by an external clock signal or external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In this configuration the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula (see Applications Information section). When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 50ms typical for the LTC691 and 200ms typical for the LTC695. OSC IN selects between the 1.6 seconds and 100ms typical watchdog time-out periods. In both cases, the time-out period immediately after a reset is 1.6 seconds typical.

TYPICAL PERFORMANCE CHARACTERISTICS

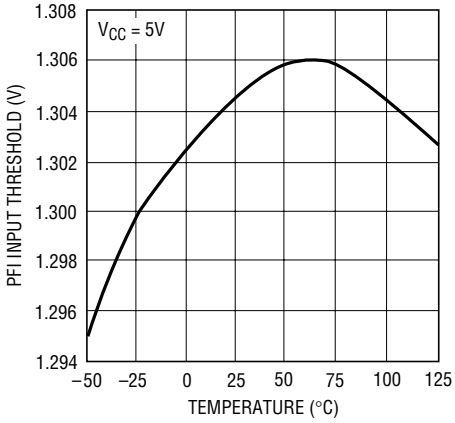
V_{OUT} vs I_{OUT}



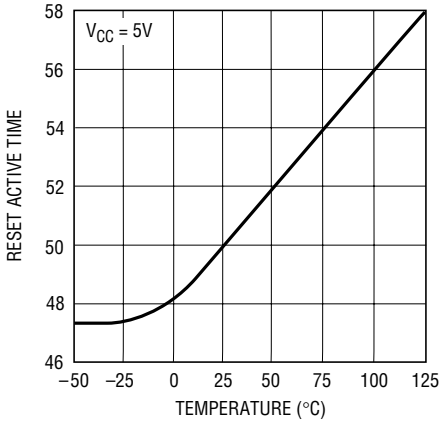
V_{OUT} vs I_{OUT}



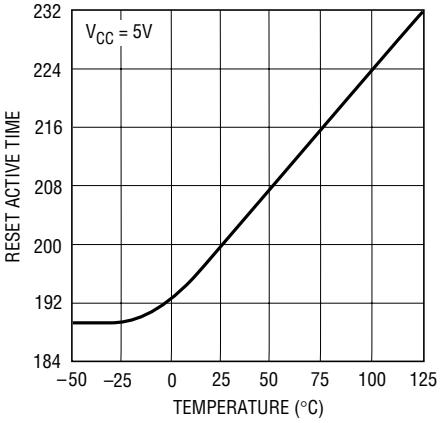
Power Failure Input Threshold vs Temperature



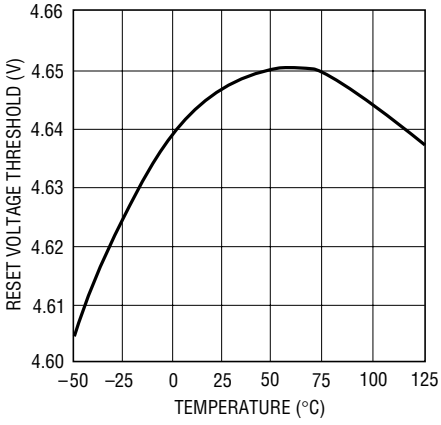
Reset Active Time vs Temperature LTC690-1



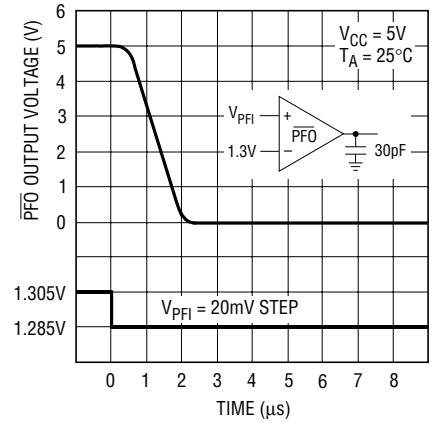
Reset Active Time vs Temperature LTC694-5



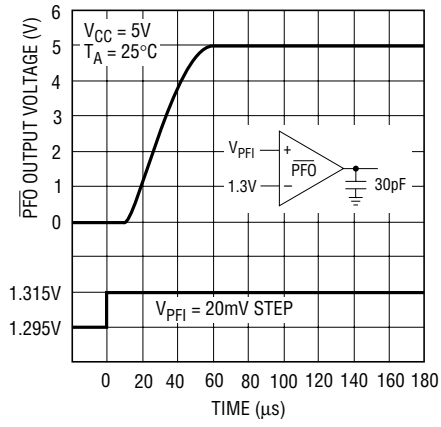
Reset Voltage Threshold vs Temperature



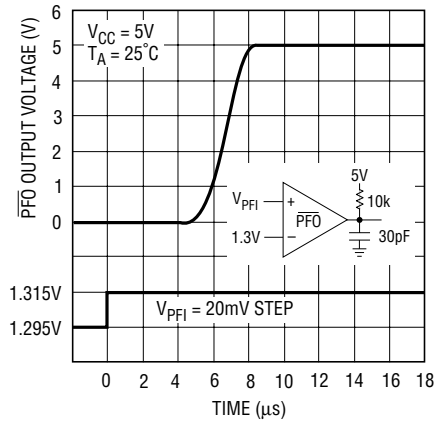
Power-Fail Comparator Response Time



Power-Fail Comparator Response Time



Power-Fail Comparator Response Time with Pull-Up Resistor



APPLICATIONS INFORMATION

Microprocessor Reset

The LTC690 family uses a bandgap voltage reference and a precision voltage comparator C1 to monitor the 5V supply input on V_{CC} (see Block Diagram). When V_{CC} falls below the reset voltage threshold, the $\overline{RESET}$ output is forced to active low state. The reset voltage threshold accounts for a 5% variation on V_{CC}, so the $\overline{RESET}$ output becomes active low when V_{CC} falls below 4.75V (4.65V typical). On power-up, the $\overline{RESET}$ signal is held active low for a minimum of 35ms for the LTC690/LTC691 (140ms for the LTC694/LTC695) after reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. The reset active time is adjustable on the LTC691/LTC695. On power-down, the $\overline{RESET}$ signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the $\overline{RESET}$ signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at V_{CC} pin do not activate the $\overline{RESET}$ output. Response time is typically 10µs. To help prevent mistriggering due to transient loads, V_{CC} pin should be bypassed with a 0.1µF capacitor with the leads trimmed as short as possible.

The LTC691 and LTC695 have two additional outputs: $\overline{RESET}$ and $\overline{LOW\ LINE}$. $\overline{RESET}$ is an active high output and is the inverse of $\overline{RESET}$. $\overline{LOW\ LINE}$ is the output of the precision voltage comparator C1. When V_{CC} falls below the reset voltage threshold, $\overline{LOW\ LINE}$ goes low. $\overline{LOW\ LINE}$ returns high as soon as V_{CC} rises above the reset voltage threshold.

Battery Switchover

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. When V_{CC} rises to 70mV above V_{BATT}, the battery switchover comparator, C2, connects V_{OUT} to V_{CC} through a charge pumped NMOS power switch, M1. When V_{CC} falls to 50mV above V_{BATT}, C2 connects V_{OUT} to V_{BATT} through a PMOS switch, M2. C2 has typically 20mV of hysteresis to prevent spurious switching when V_{CC} remains nearly equal to V_{BATT}. The response time of C2 is approximately 20µs.

During normal operation, the LTC690 family uses a charge pumped NMOS power switch to achieve low dropout and low supply current. This power switch can deliver up to 50mA to V_{OUT} from V_{CC} and has a typical on resistance of 5Ω. The V_{OUT} pin should be bypassed with a capacitor of 0.1µF or greater to ensure stability. Use of a larger bypass capacitor is advantageous for supplying current to heavy transient loads.

When operating currents larger than 50mA are required from V_{OUT}, or a lower dropout (V_{CC}-V_{OUT} voltage differential) is desired, the LTC691 and LTC695 should be used. These products provide BATT ON output to drive the base

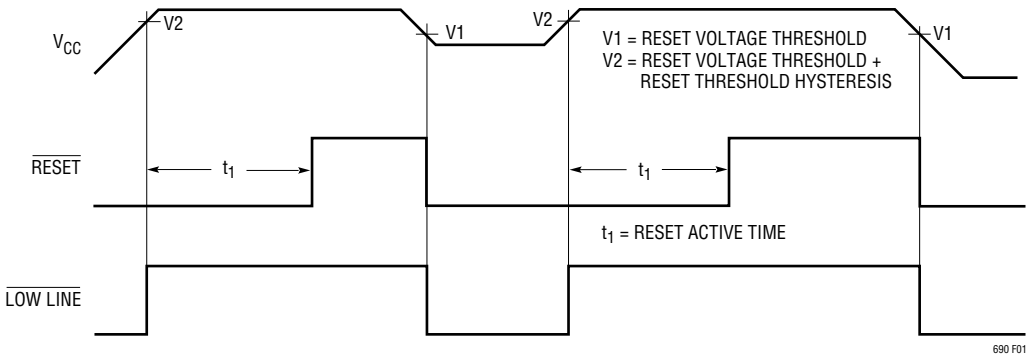


Figure 1. Reset Active Time

APPLICATIONS INFORMATION

of external PNP transistor (Figure 2). If higher currents are needed with the LTC690 and LTC694, a high current Schottky diode can be connected from the V_{CC} pin to the V_{OUT} pin to supply the extra current.

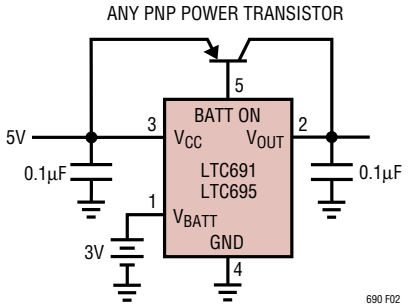


Figure 2. Using BATT ON to Drive External PNP Transistor

The LTC690 family is protected for safe area operation with short-circuit limit. Output current is limited to approximately 200mA. If the device is overloaded for long period of time, thermal shutdown turns the power switch off until the device cools down. The threshhold temperature for thermal shutdown is approximately 155°C with about 10°C of hysteresis which prevents the device from oscillating in and out of shutdown.

The PNP switch used in competitive devices was not chosen for the internal power switch because it injects unwanted current into the substrate. This current is collected by the V_{BATT} pin in competitive devices and adds to the charging current of the battery which can damage lithium batteries. The LTC690 family uses a charge pumped NMOS power switch to eliminate unwanted charging current while achieving low dropout and low supply current. Since no current goes to the substrate, the current collected by V_{BATT} pin is strictly junction leakage.

A 125Ω PMOS switch connects the V_{BATT} input to V_{OUT} in battery back-up mode. The switch is designed for very low dropout voltage (input-to-output differential). This feature is advantageous for low current applications such as battery back-up in CMOS RAM and other low power CMOS circuitry. The supply current in battery back-up mode is 1µA maximum.

The operating voltage at the V_{BATT} pin ranges from 2.0V to 4.25V. High value capacitors, such as electrolytic or farad-size double layer capacitors, can be used for short term memory back-up instead of a battery. The charging resistor for both capacitors and rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists when the resistor is connected to V_{CC} (Figure 3).

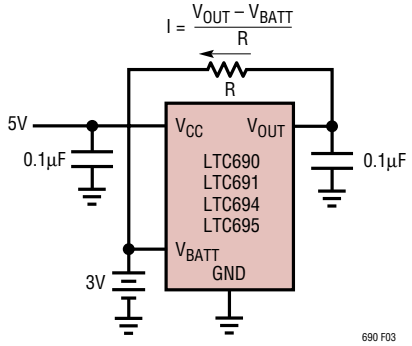


Figure 3. Charging External Battery Through V_{OUT}

Replacing the Back-Up Battery

When changing the back-up battery with system power on, spurious resets can occur while battery is removed due to battery standby current. Although battery standby current is only a tiny leakage current, it can still charge up the stray capacitance on the V_{BATT} pin. The oscillation cycle is as follows: When V_{BATT} reaches within 50mV of V_{CC}, the LTC690 switches to battery back-up. V_{OUT} pulls V_{BATT} low and the device goes back to normal operation. The leakage current then charges up the V_{BATT} pin again and the cycle repeats.

If spurious resets during battery replacement pose no problems, then no action is required. Otherwise, a resistor from V_{BATT} to GND will hold the pin low while changing the battery. For example, the battery standby current is 1µA maximum over temperature and the external resistor required to hold V_{BATT} below V_{CC} is:

$$R \leq \frac{V_{CC} - 50mV}{1\mu A}$$

With V_{CC} = 4.5V, a 4.3M resistor will work. With a 3V battery, this resistor will draw only 0.7µA from the battery, which is negligible in most cases.

APPLICATIONS INFORMATION

If battery connections are made through long wires, a 10Ω to 100Ω series resistor and a 0.1µF capacitor are recommended to prevent any overshoot beyond V_{CC} due to the lead inductance (Figure 4).

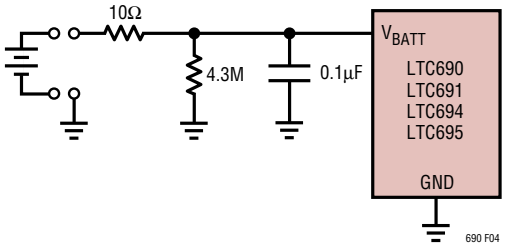


Figure 4. 10Ω/0.1µF Combination Eliminates Inductive Overshoot and Prevents Spurious Resets During Battery Replacement

Table 1 shows the state of each pin during battery back-up. When the battery switchover section is not used, connect V_{BATT} to GND and V_{OUT} to V_{CC}.

Memory Protection

The LTC691 and LTC695 include memory protection circuitry that ensures the integrity of the data in memory by preventing write operations when V_{CC} is at invalid level. Two additional pins, $\overline{CE}$ IN and $\overline{CE}$ OUT, control the Chip Enable or Write inputs of CMOS RAM. When V_{CC} is 5V, $\overline{CE}$ OUT follows $\overline{CE}$ IN with a typical propagation delay of 20ns. When V_{CC} falls below the reset voltage threshold or V_{BATT}, $\overline{CE}$ OUT is forced high, independent of $\overline{CE}$ IN. $\overline{CE}$ OUT is an alternative signal to drive the $\overline{CE}$, $\overline{CS}$, or $\overline{Write}$ input of battery-backed up CMOS RAM. $\overline{CE}$ OUT can also be used to drive the $\overline{Store}$ or $\overline{Write}$ input of an EEPROM, EAROM or NOVRAM to achieve similar protection. Figure 5 shows the timing diagram of $\overline{CE}$ IN and $\overline{CE}$ OUT.

$\overline{CE}$ IN can be derived from the microprocessor's address decoder output. Figure 6 shows a typical nonvolatile CMOS RAM application.

Memory protection can also be achieved with the LTC690 and LTC694 by using $\overline{RESET}$ as shown in Figure 7.

Table 1. Input and Output Status in Battery Back-Up Mode

SIGNAL	STATUS
V_{CC}	C2 monitors V_{CC} for active switchover.
V_{OUT}	V_{OUT} is connected to V_{BATT} through an internal PMOS switch.
V_{BATT}	The supply current is 1µA maximum.
BATT ON	Logic high. The open-circuit output voltage is equal to V_{OUT}.
PFI	Power failure input is ignored.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
RESET	Logic high. The open-circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
WDI	Watchdog input is ignored.
$\overline{WDO}$	Logic high. The open-circuit output voltage is equal to V_{OUT}.
$\overline{CE}$ IN	$\overline{Chip\ Enable}$ Input is ignored.
$\overline{CE}$ OUT	Logic high. The open-circuit output voltage is equal to V_{OUT}.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

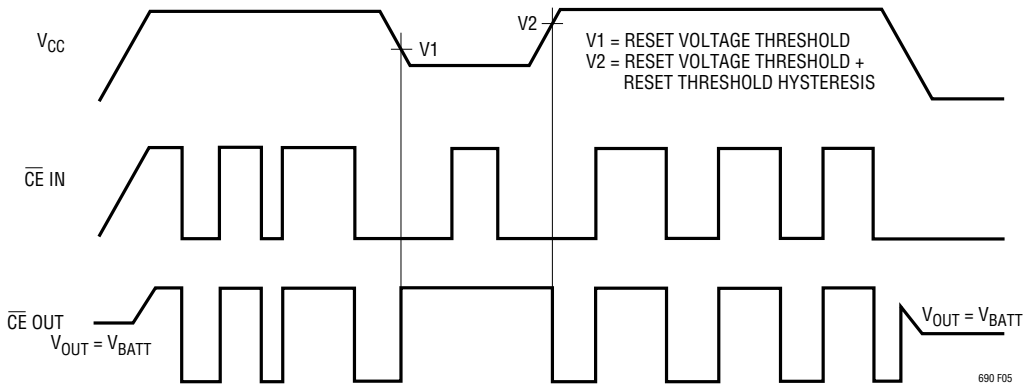


Figure 5. Timing Diagram for $\overline{CE}$ IN and $\overline{CE}$ OUT

APPLICATIONS INFORMATION

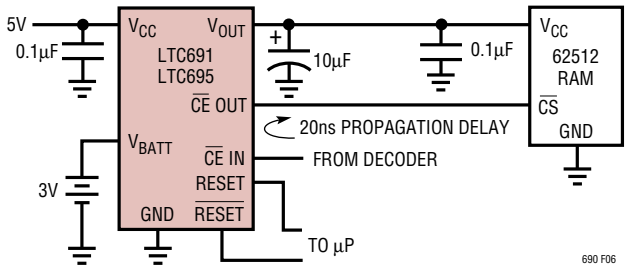


Figure 6. A Typical Nonvolatile CMOS RAM Application

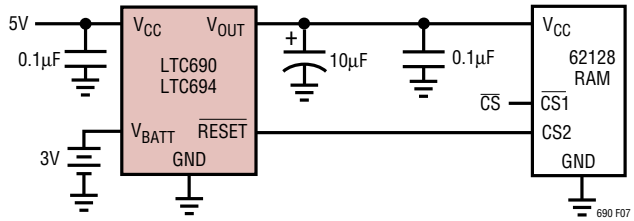


Figure 7. Write Protect for RAM with LTC690 or LTC694

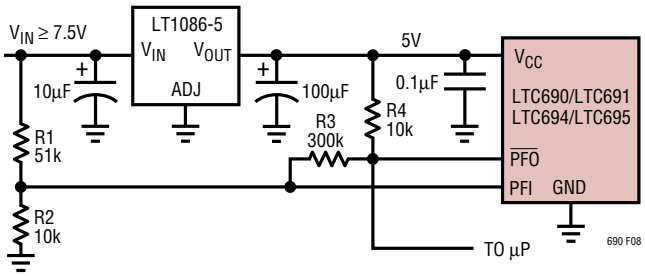


Figure 8. Monitoring *Unregulated* DC Supply with the LTC690's Power-Fail Comparator

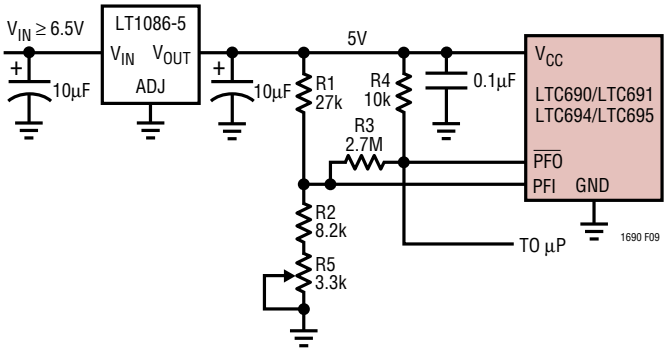


Figure 9. Monitoring *Regulated* DC Supply with the LTC690's Power-Fail Comparator

Power-Fail Warning

The LTC690 family generates a Power Failure Output ($\overline{PFO}$) for early warning of failure in the microprocessor's power supply. This is accomplished by comparing the Power Failure Input (PFI) with an internal 1.3V reference. $\overline{PFO}$ goes low when the voltage at the PFI pin is less than 1.3V. Typically PFI is driven by an external voltage divider (R1 and R2 in Figures 8 and 9) which senses either an unregulated DC input or a regulated 5V output. The voltage divider ratio can be chosen such that the voltage at the PFI pin falls below 1.3V several milliseconds before the 5V supply falls below the maximum reset voltage threshold 4.75V. $\overline{PFO}$ is normally used to interrupt the microprocessor to execute shutdown procedure between $\overline{PFO}$ and $\overline{RESET}$ or RESET.

The power-fail comparator, C3, does not have hysteresis. Hysteresis can be added however, by connecting a resistor between the $\overline{PFO}$ output and the noninverting PFI input pin as shown in Figures 8 and 9. The upper and lower trip points in the comparator are established as follows:

When $\overline{PFO}$ output is low, R3 sinks current from the summing junction at the PFI pin.

$$V_H = 1.3V\left(1+\frac{R1}{R2}+\frac{R1}{R3}\right)$$

When $\overline{PFO}$ output is high, the series combination of R3 and R4 source current into the PFI summing junction.

$$V_L = 1.3V\left(1+\frac{R1}{R2}-\frac{(5V-1.3V)R1}{1.3V(R3+R4)}\right)$$

$$\text{Assuming } R4 << R3, V_{HYSTERESIS} = 5V\frac{R1}{R3}$$

Example 1: The circuit in Figure 8 demonstrates the use of the power-fail comparator to monitor the unregulated power supply input. Assuming the the rate of decay of the supply input V_{IN} is 100mV/ms and the total time to execute a shutdown procedure is 8ms. Also the noise of V_{IN} is 200mV. With these assumptions in mind, we can reasonably set V_L = 7.5V which 1.25V greater than the sum of maximum reset voltage threshold and the dropout voltage

APPLICATIONS INFORMATION

of LT1086-5 (4.75V + 1.5V) and $V_{HYSTERESIS}$ = 850mV.

$$V_{HYSTERESIS} = 5V\frac{R1}{R3} = 850V$$

$$R3 \approx 5.88\ R1$$

Choose R3 = 300k and R1 = 51k. Also select R4 = 10k which is much smaller than R3.

$$7.5V = 1.3V\left(1+\frac{51k}{R2}-\frac{(5V-1.3V)51k}{1.3V(310k)}\right)$$

R2 = 9.7kΩ, Choose nearest 5% resistor 10k and recalculate V_L,

$$V_L = 1.3V\left(1+\frac{51k}{10k}-\frac{(5V-1.3V)51k}{1.3V(310k)}\right) = 7.32V$$

$$V_H = 1.3V\left(1+\frac{51k}{10k}+\frac{51k}{300k}\right) = 8.151V$$

$$\frac{(7.32V-6.25V)}{100mV/ms} = 10.7ms$$

$V_{HYSTERESIS}$ = 8.151V – 7.32V = 831mV

The 10.7ms allows enough time to execute shutdown procedure for microprocessor and 831mV of hysteresis would prevent $\overline{PFO}$ from going low due to the noise of V_{IN}.

Example 2: The circuit in Figure 9 can be used to measure the regulated 5V supply to provide early warning of power failure. Because of variations in the PFI threshold, this circuit requires adjustment to ensure the PFI comparator trips before the reset threshold is reached. Adjust R5 such that the $\overline{PFO}$ output goes low when the V_{CC} supply reaches the desired level (e.g., 4.85V).

Monitoring the Status of the Battery

C3 can also monitor the status of the memory back-up battery (Figure 10). If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high in battery back-up mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

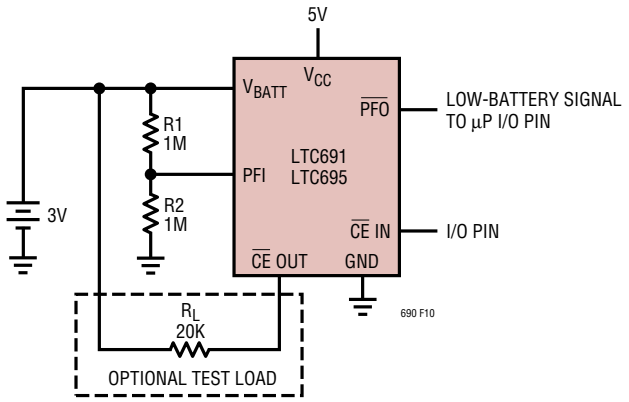


Figure 10. Back-Up Battery Monitor with Optional Test Load

Watchdog Timer

The LTC690 family provides a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within a seleced time-out period, $\overline{RESET}$ is forced to active low for a minimum of 35ms for the LTC690/LTC691 (140ms for the LTC694/LTC695). The reset active time is adjustable on the LTC691/LTC695. Since many systems can not service the watchdog timer immediately after a reset, the LTC691 and LTC695 have longer time-out period (1.0 second minimum) right after a reset is issued. The normal time-out period (70ms minimum) becomes effective following the first transition of WDI after $\overline{RESET}$ is inactive. The watchdog time-out period is fixed at 1.0 second minimum on the LTC690 and LTC694. Figure 11 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as $\overline{RESET}$ is inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog time is reset and begins to time out again. To ensure the watchdog time does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog time can be deactivated by floating the WDI pin. The timer is also disabled when V_{CC} falls below the reset voltage threshold or V_{BATT}.

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The LTC691 and LTC695 provide an additional output (Watchdog Output, $\overline{WDO}$) which goes low if the watchdog timer is allowed to time out and remains low until set high by the next transition on the WDI pin. $\overline{WDO}$ is also set high when V_{CC} falls below the reset voltage threshold or V_{BATT}.

The LTC691 and LTC695 have two additonal pins OSC SEL and OSC IN, which allow reset active time and watchdog time-out period to be adjusted per Table 2. Several configurations are shown in Figure 12.

OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In these configurations, the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula in Table 2. When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 35ms minimum for the LTC691 and 140ms minimum for the LTC695. OSC IN selectes between the 1 second and 70ms minimum normal watchdog time-out periods. In both cases, the time-out period immediately after a reset is at least 1 second.

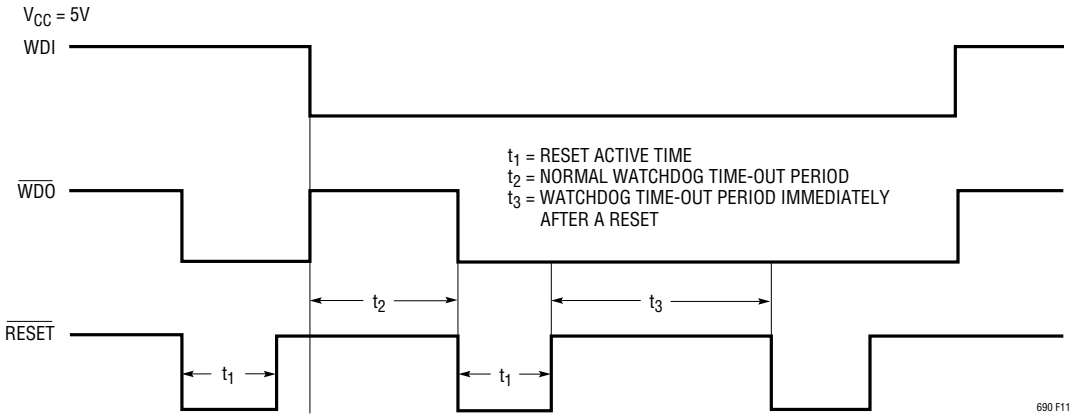


Figure 11. Watchdog Time-Out Period and Reset Active Time

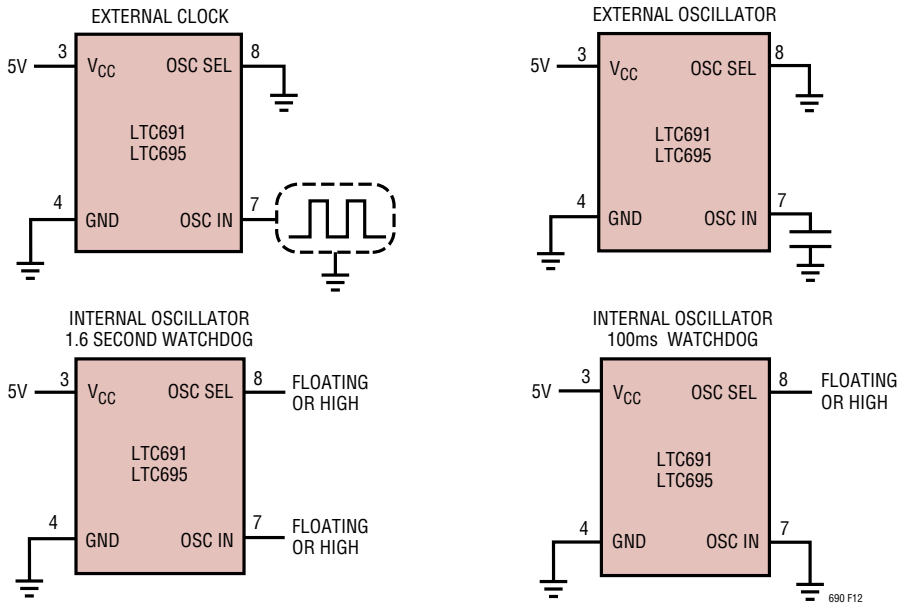


Figure 12. Oscillator Configurations

APPLICATIONS INFORMATION

Table 2. LTC691 and LTC695 Reset Active Time and Watchdog Time-Out Selections

OSC SEL	OSC IN	WATCHDOG TIME-OUT PERIOD		RESET ACTIVE TIME	
		NORMAL (Short Period)	IMMEDIATELY AFTER RESET (Long Period)	LTC691	LTC695
Low	External Clock Input	1024 clks	4096 clks	512 clks	2048 clks
Low	External Capacitor*	$\frac{400ms}{70pF} \bullet C$	$\frac{1.6\ sec}{70pF} \bullet C$	$\frac{200ms}{70pF} \bullet C$	$\frac{800ms}{70pF} \bullet C$
Floating or High	Low	100ms	1.6 sec	50ms	200ms
Floating or High	Floating or High	1.6 sec	1.6 sec	50ms	200ms

*The nominal internal frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is $f_{OSC}\ (Hz) = \frac{184,000}{C(pF) \bullet 1025}$

Push-Button Reset

The LTC690 family does not provide a logic input for direct connection to a pushbutton. However, a push-button in series with a 100Ω resistor connected to the $\overline{RESET}$ output pin (Figure 13) provides an alternative for manual reset. Connecting a 0.1µF capacitor to the $\overline{RESET}$ pin debounces the push-button input.

The 100Ω resistor in series with the push-button is required to prevent the ringing, due to the capacitance and lead inductance, from pulling the $\overline{RESET}$ pins of the MPU and LTC69X below ground.

If a dedicated pushbutton reset input is desired, the LTC1235 is a good choice (Figure 14). It has all the functions of the LTC695 and provides push-button reset as an extra feature. Its push-button is internally debounced and invokes the normal 200ms reset sequence. This eliminates the need for the 100Ω resistor and 0.1µF capacitor. It also provides a more consistent reset pulse.

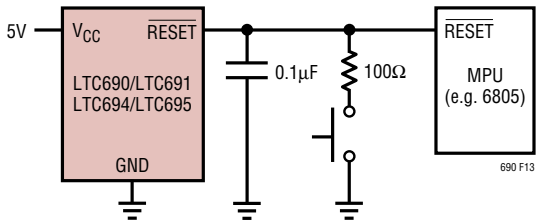


Figure 13. The External Push-Button Reset

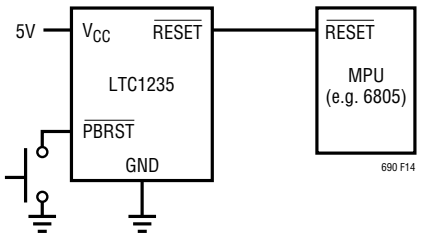
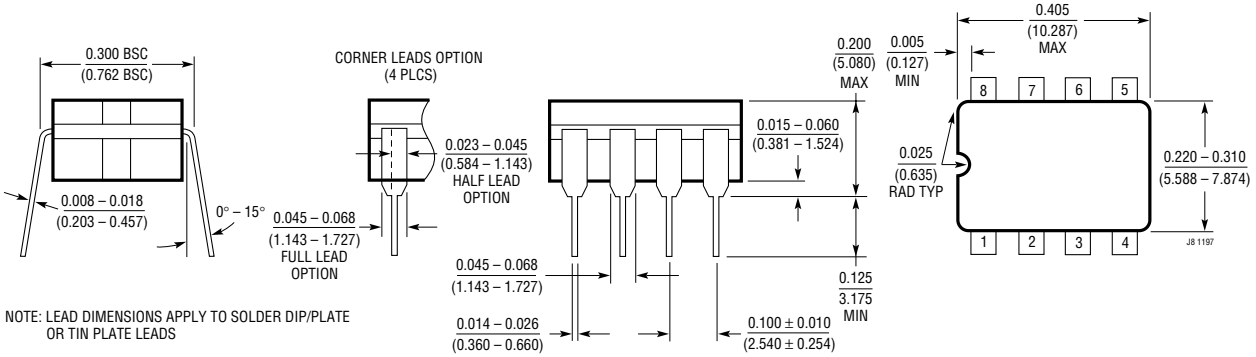


Figure 14. The External Push-Button Reset with the LTC1235

PACKAGE DESCRIPTION

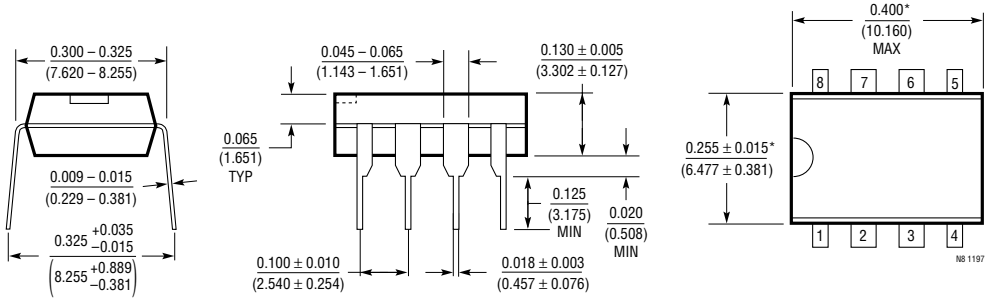
Dimensions in inches (millimeters) unless otherwise noted.

J8 Package 8-Lead CERDIP (Narrow 0.300, Hermetic) (LTC DWG # 05-08-1110)



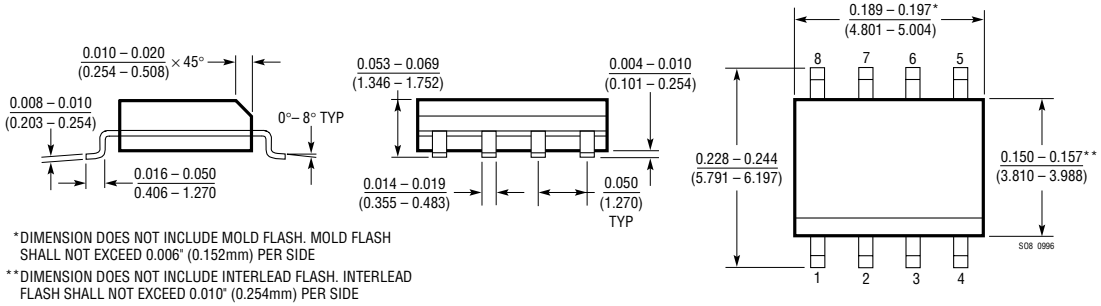
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

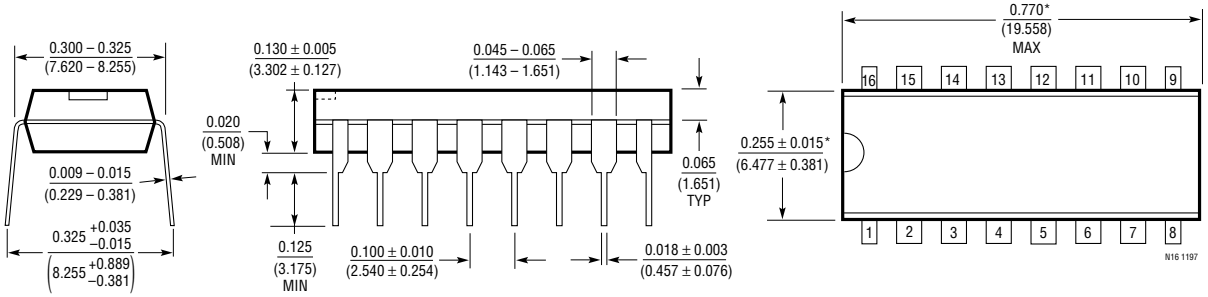
S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

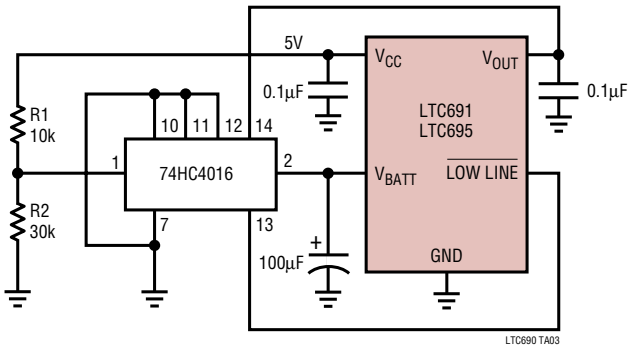
N Package 16-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



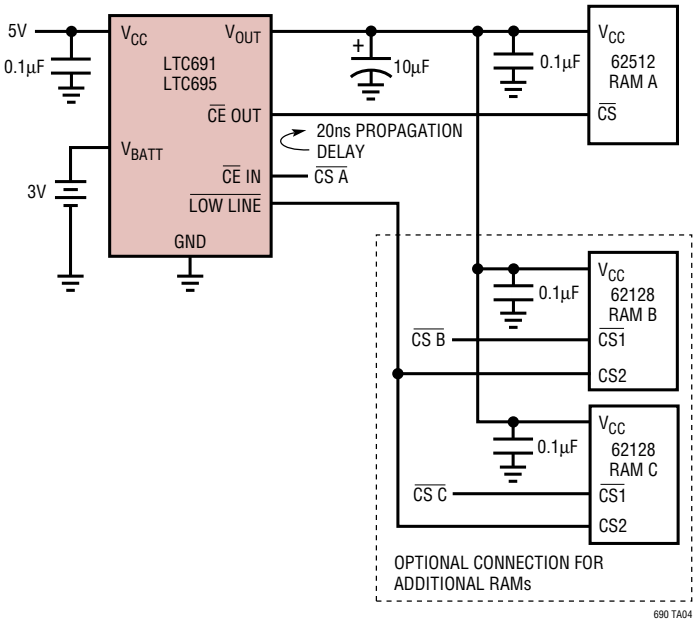
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

TYPICAL APPLICATIONS

Capacitor Back-Up with 74HC4016 Switch



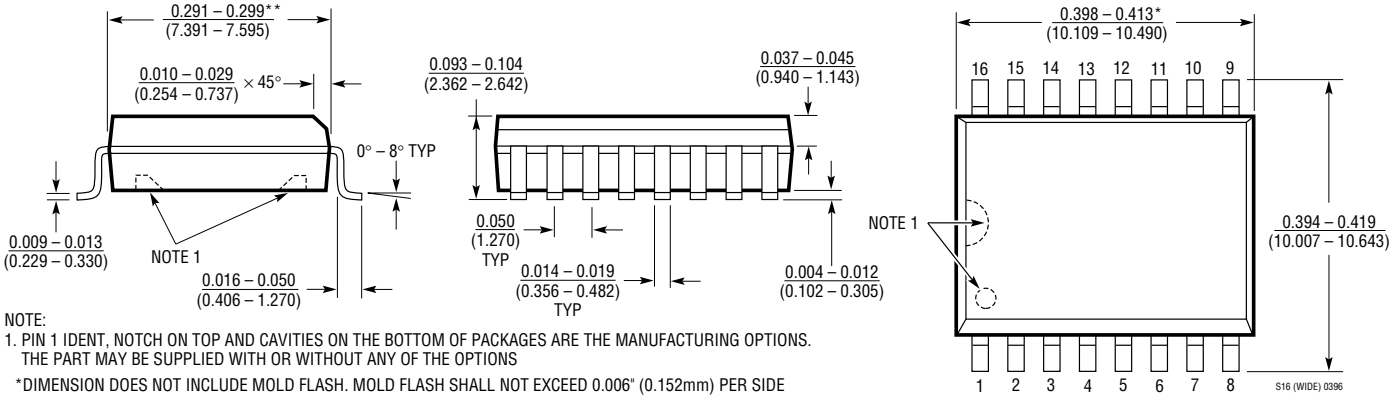
Write Protect for Additional RAMs



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1326	Micropower Precision Triple Supply Monitor	4.725V, 3.118V, 1V Thresholds (±0.75%)
LTC1536	Micropower Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications

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