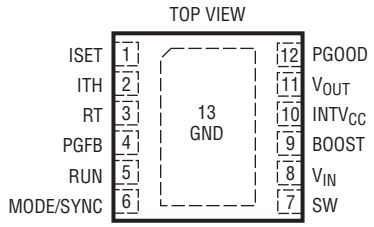
ABSOLUTE MAXIMUM RATINGS (Notes 1, 5)

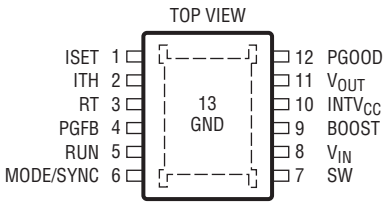
V_{IN}, SW Voltage ..... –0.3V to 16V
SW Transient Voltage (Note 6) .....–2V to 21V
V_{OUT}, ISET Voltage .....0V to V_{IN}
BOOST Voltage .....–0.3V to V_{IN} + $INTV_{CC}$
RUN Voltage.....–0.3V to 12V
$INTV_{CC}$ Voltage .....–0.3V to 7V
ITH, RT Voltage.....–0.3V to $INTV_{CC}$
MODE/SYNC, PGFB, PGOOD Voltage....–0.3V to $INTV_{CC}$
Operating Junction Temperature Range
(Notes 2, 5).....–40°C to 125°C
MSE Package Lead Temperature
(Soldering, 10 sec).....300°C

PIN CONFIGURATION



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 55°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LTC3600#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3600EDD#PBF	LTC3600EDD#TRPBF	LFXB	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3600IDD#PBF	LTC3600IDD#TRPBF	LFXB	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3600EMSE#PBF	LTC3600EMSE#TRPBF	3600	12-Lead Plastic MSOP	–40°C to 125°C
LTC3600IMSE#PBF	LTC3600IMSE#TRPBF	3600	12-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	V_{IN} Supply Range			4		15	V
ISET	I_{SET} Reference Current		 ●	49.5 49.3	50 50	50.5 51	µA µA
	I_{SET} Line Regulation		●		0.02	0.05	%/V
	I_{SET} DROP_OUT Voltage	I_{SET} > 45µA, $V_{IN} - V_{SET}$			340		mV
	I_{SET} Load Regulation	I_{OUT} = 0 to 1.5A			0.25		µA
	Error Amp Input Offset	(Note 4)		–3		3	mV
	Error Amp Load Regulation		●		0.05	0.1	%
	Minimum V_{OUT} Voltage	V_{ISET} = 0, R_{OUT} = 0			10		mV
g_m(EA)	Error Amplifier Transconductance				0.63	0.9	mS
$t_{ON(MIN)}$	Minimum On-Time				30		ns
$t_{OFF(MIN)}$	Minimum Off-Time				130		ns
I_{LIM}	Current Limit		●	1.6	2	2.4	A
	Negative Current Limit				–0.9		A
R_{TOP}	Top Power NMOS On-Resistance				200		mΩ
R_{BOTTOM}	Bottom Power NMOS On-Resistance				100		mΩ
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout Threshold	$INTV_{CC}$ Rising			3.45	3.7	V
	UVLO Hysteresis	$INTV_{CC}$ Falling			150		mV
V_{RUN}	Run Threshold Run Hysteresis	RUN Rising RUN Falling	●		1.55 0.13	1.8	V V
	RUN Pin Leakage	RUN = 12V			0	2	µA
V_{INTVCC}	Internal V_{CC} Voltage	5.5V < V_{IN} < 15V		4.8	5	5.4	V
	$INTV_{CC}$ Load Regulation	I_{LOAD} = 0mA to 20mA			0.3		%
OV	Output Overvoltage PGOOD Upper Threshold	PGFB Rising		0.620	0.645	0.680	V
UV	Output Undervoltage PGOOD Lower Threshold	PGFB Falling		0.520	0.555	0.590	V
	PGOOD Hysteresis	PGFB Returning			10		mV
	PGOOD Pull-Down Resistance	1mA Load			200		Ω
	PGOOD Leakage Current	PGOOD = 5V				1	µA
$V_{MODE/SYNC}$	MODE/SYNC Threshold	MODE $V_{IL(MAX)}$ MODE $V_{IH(MIN)}$ SYNC $V_{IH(MIN)}$ SYNC $V_{IL(MAX)}$		 4.3 2.5		0.4 0.4	V V V V
	MODE/SYNC Pin Current	MODE = 5V			9.5		µA
f_{OSC}	Switching Frequency	R_T = 36.1k	●	0.92	1	1.06	MHz
	V_{OUT} Pin Resistance to Ground				600		kΩ
V_{INOV}	V_{IN} Overvoltage Lockout	V_{IN} Rising V_{IN} Falling			17.5 16		V V
I_Q	Input DC Supply Current Discontinuous Shutdown	(Note 3) Mode = 0, R_T = 36.1k Run = 0			 700 0	 1100 1.5	 µA µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3600 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3600E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3600I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

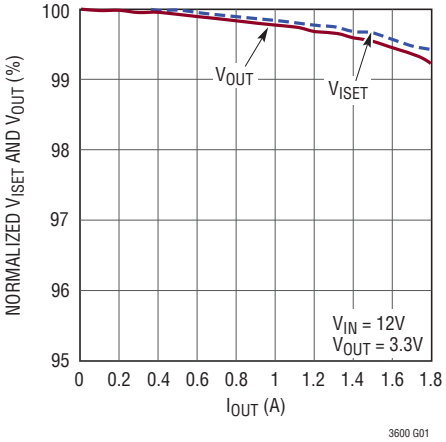
Note 4: The LTC3600 is tested in a feedback loop that adjusts V_{OUT} to achieve a specified error amplifier output voltage (I_{TH}).

Note 5: This IC includes overtemperature protection that is intended protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

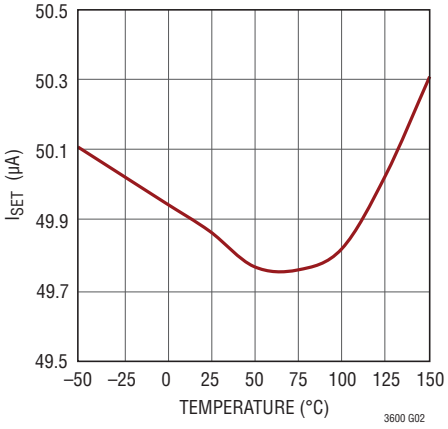
Note 6: Duration of voltage transient is less than 20ns for each switching cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

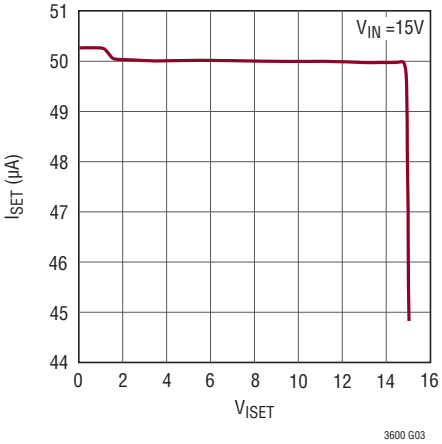
Load Regulation



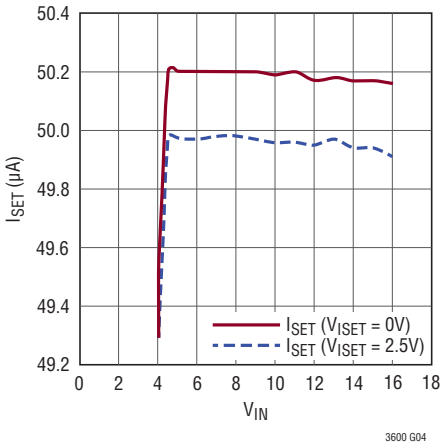
ISET Current vs Temperature



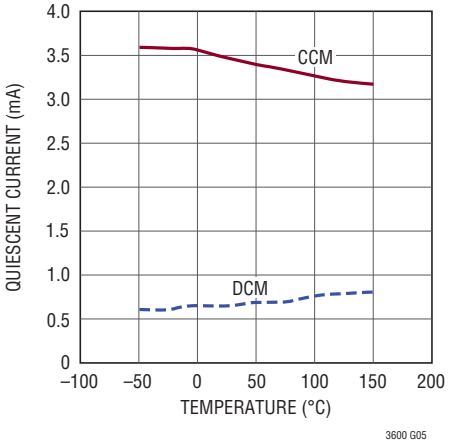
ISET Current vs VISET



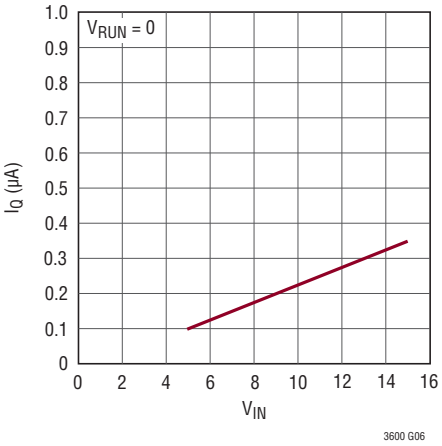
ISET Current Line Regulation



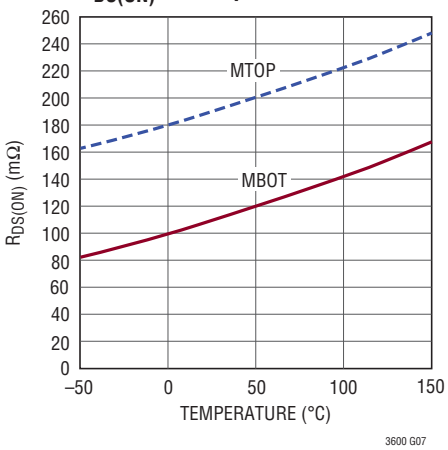
Quiescent Current vs Temperature



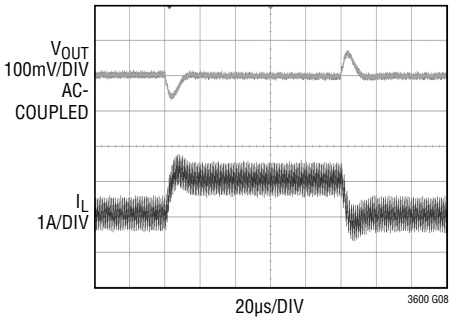
Shutdown IQ vs VIN



RDS(ON) vs Temperature

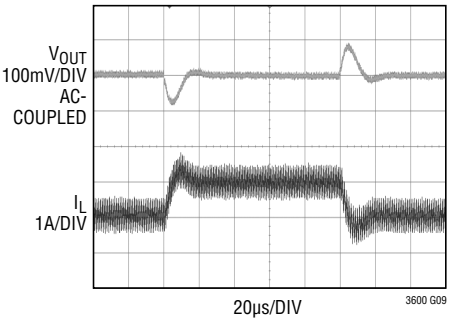


Transient Response CCM Operation, External Compensation



VIN = 12V
VOUT = 3.3V
IOUT = 0A TO 1A
L = 4.7µH
fSW = 1MHz
RITH = 27.5kΩ, CITH = 250pF
MODE = INTVCC
COUT = 47µF

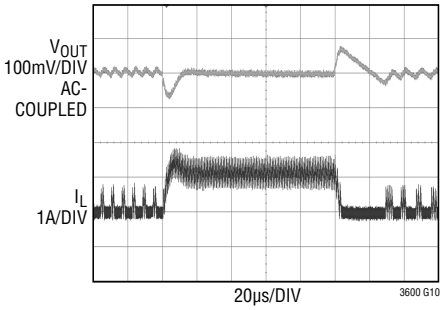
Transient Response CCM Operation, Internal Compensation



VIN = 12V
VOUT = 3.3V
IOUT = 0A TO 1A
L = 4.7µH
fSW = 1MHz
ITH = INTVCC
MODE = INTVCC
COUT = 47µF

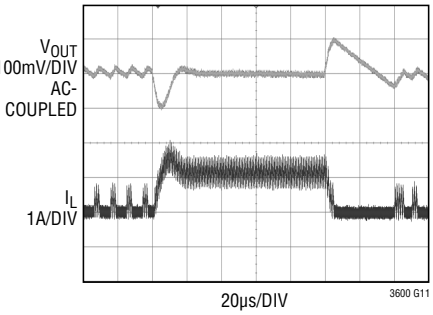
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response DCM, Operation, External Compensation



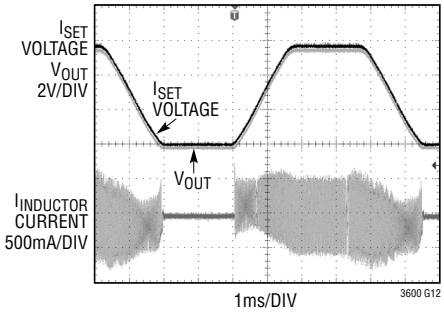
V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 0.1A TO 1A
L = 4.7µH
f_{SW} = 1MHz
R_{ITH} = 27.5kΩ, C_{ITH} = 250pF
MODE = 0
C_{OUT} = 47µF

Transient Response DCM, Operation, Internal Compensation

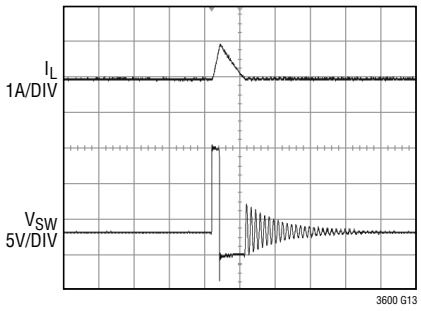


V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 0.1A TO 1A
L = 4.7µH
f_{SW} =1MHz
ITH = $INTV_{CC}$
MODE = 0
C_{OUT} = 47µF

Output Tracking

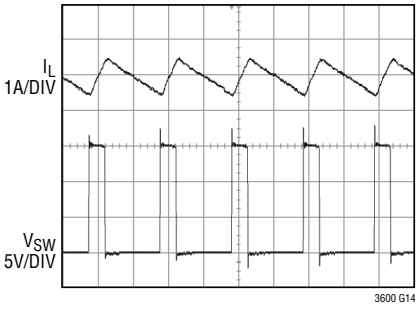


Discontinuous Conduction Mode Operation



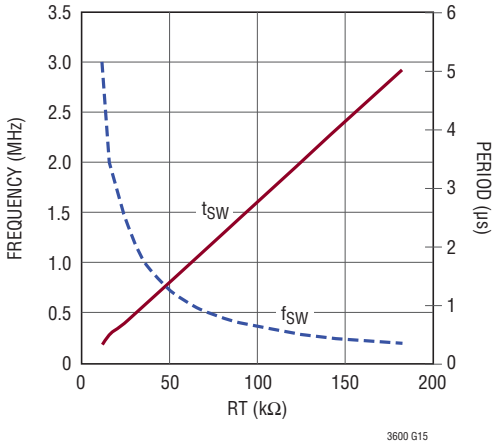
V_{IN} = 15V
V_{OUT} = 2.5V
MODE = 0
L = 2.2µH

Continuous Conduction Mode Operation

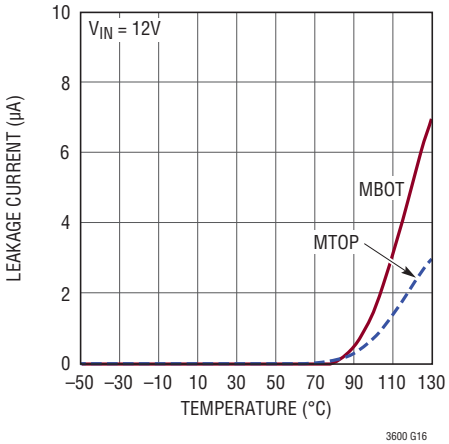


V_{IN} = 15V
V_{OUT} = 2.5V
MODE = $INTV_{CC}$
L = 2.2µH

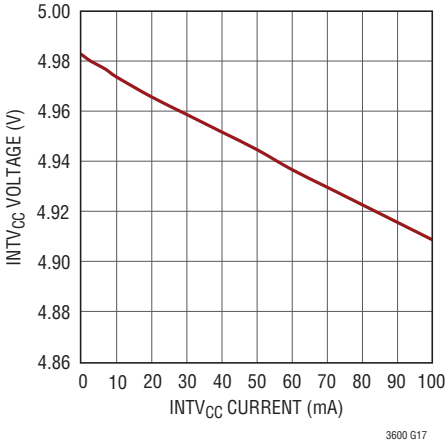
Switching Frequency/Period vs RT



Switch Leakage Current

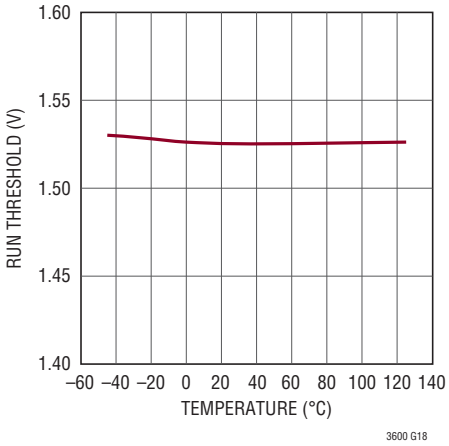


$INTV_{CC}$ Load Regulation

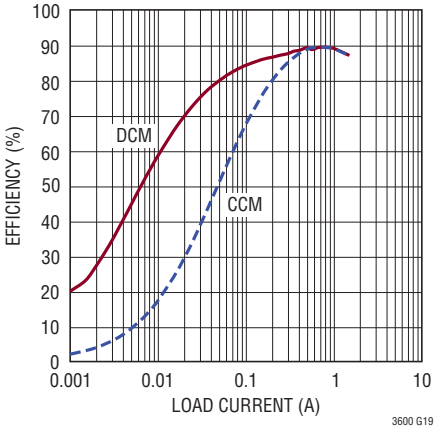


TYPICAL PERFORMANCE CHARACTERISTICS

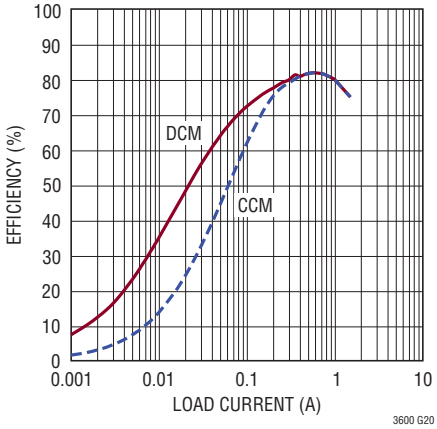
Rising RUN Threshold vs Temperature



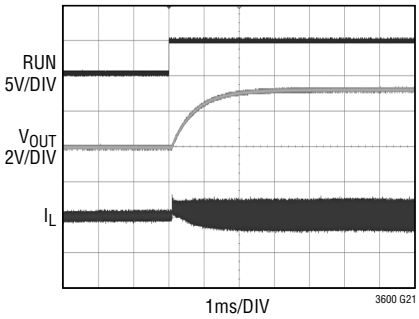
Efficiency vs Load Current V_{OUT} = 3.3V, V_{IN} = 12V



Efficiency vs Load Current V_{OUT} = 1.2V, V_{IN} = 12V

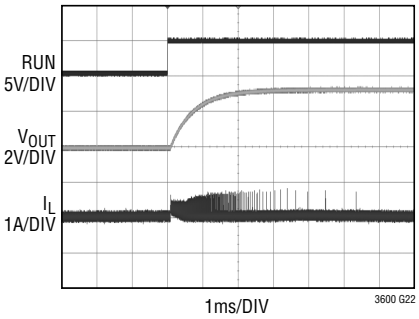


Start-Up Waveform



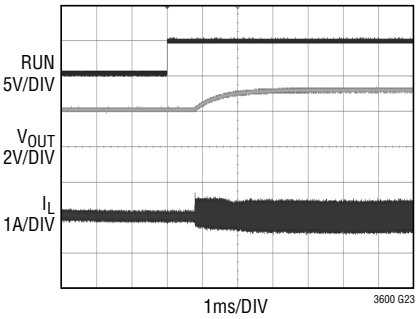
MODE = CCM
NO PREBIASED V_{OUT}
V_{IN} = 12V
V_{OUT} = 3.3V

Start-Up Waveform



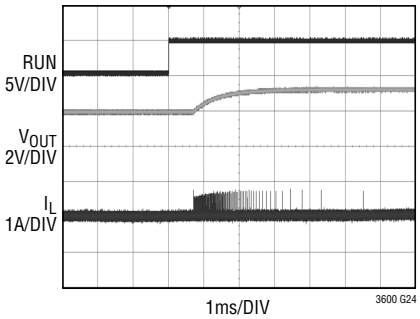
MODE = DCM
NO PREBIASED V_{OUT}
V_{IN} = 12V
V_{OUT} = 3.3V

Start-Up Waveform



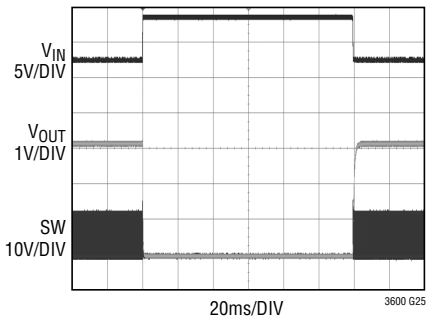
MODE = CCM
V_{OUT} IS PREBIASED TO 2V
V_{IN} = 12V
V_{OUT} = 3.3V

Start-Up Waveform



MODE = DCM
V_{OUT} IS PREBIASED TO 2V
V_{IN} = 12V
V_{OUT} = 3.3V

V_{IN} Overvoltage



V_{IN} = 12V TO 18V TO 12V
V_{OUT} = 3.3V
I_{OUT} = 1A
V_{IN} RESISTOR = 30Ω
MODE = CCM

PIN FUNCTIONS

ISET (Pin 1): Accurate 50µA Current Source. Positive input to the error amplifier. Connect an external resistor from this pin to signal GND to program the V_{OUT} voltage. Connecting an external capacitor from ISET to ground will soft start the output voltage and reduce current inrush when turning on. V_{OUT} can also be programmed by driving ISET directly with an external supply from 0 to V_{IN}, in which case the external supply would be sinking the provided 50µA. Do not drive V_{ISET} above V_{IN} or below GND. Do not float ISET.

ITH (Pin 2): Error Amplifier Output and Switching Regulator Compensation Point. The internal current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 2.4V. For external compensation, tie a resistor (R_{ITH}) in series with a capacitor (C_{ITH}) to signal GND. A separate 10pF high frequency filtering capacitor can also be placed from ITH to signal GND. Tying ITH to $INTV_{CC}$ activates internal compensation.

RT (Pin 3): Switching Frequency Programming Pin. Connect an external resistor (between 200k to 10k) from RT to SGND to program the frequency from 200kHz to 4MHz. Tying the RT pin to $INTV_{CC}$ programs 1MHz operation. Do not float the RT pin.

PGFB (Pin 4): Power Good Feedback. Place a resistor divider on V_{OUT} to detect power good level. If PGFB is more than 0.645V, or less than 0.555V, PGOOD will be pulled down. Tie PGFB to $INTV_{CC}$ to disable the PGOOD function. Tying PGFB to a voltage greater than 0.64V and less than 4V will force continuous synchronous operation regardless of the MODE/SYNC state.

RUN (Pin 5): Run Control Input. Enables chip operation by tying RUN above 1.55V. Tying it below 1V shuts down the switching regulator. Tying it below 0.4V shuts off the entire chip. When tying RUN to more than 12V, place a resistor (100k to 500k) between RUN and the voltage source.

MODE/SYNC (Pin 6): Operation Mode Select. Tie this pin to $INTV_{CC}$ to force continuous synchronous operation at all output loads. Tying it to GND enables discontinuous mode operation at light loads. Applying an external clock signal to this pin will synchronize switching frequency to the external clock. During external clock synchronization, R_T value should be set up such that the free running frequency is within 30% of the external clock frequency.

SW (Pin 7): Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to V_{IN}.

V_{IN} (Pin 8): Input voltage. Must decouple to GND with a capacitor close to the V_{IN} pin.

BOOST (Pin 9): Boosted Floating Driver Supply for Internal Top Power MOSFET. The (+) terminal of the bootstrap capacitor connects here. This pin swings from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

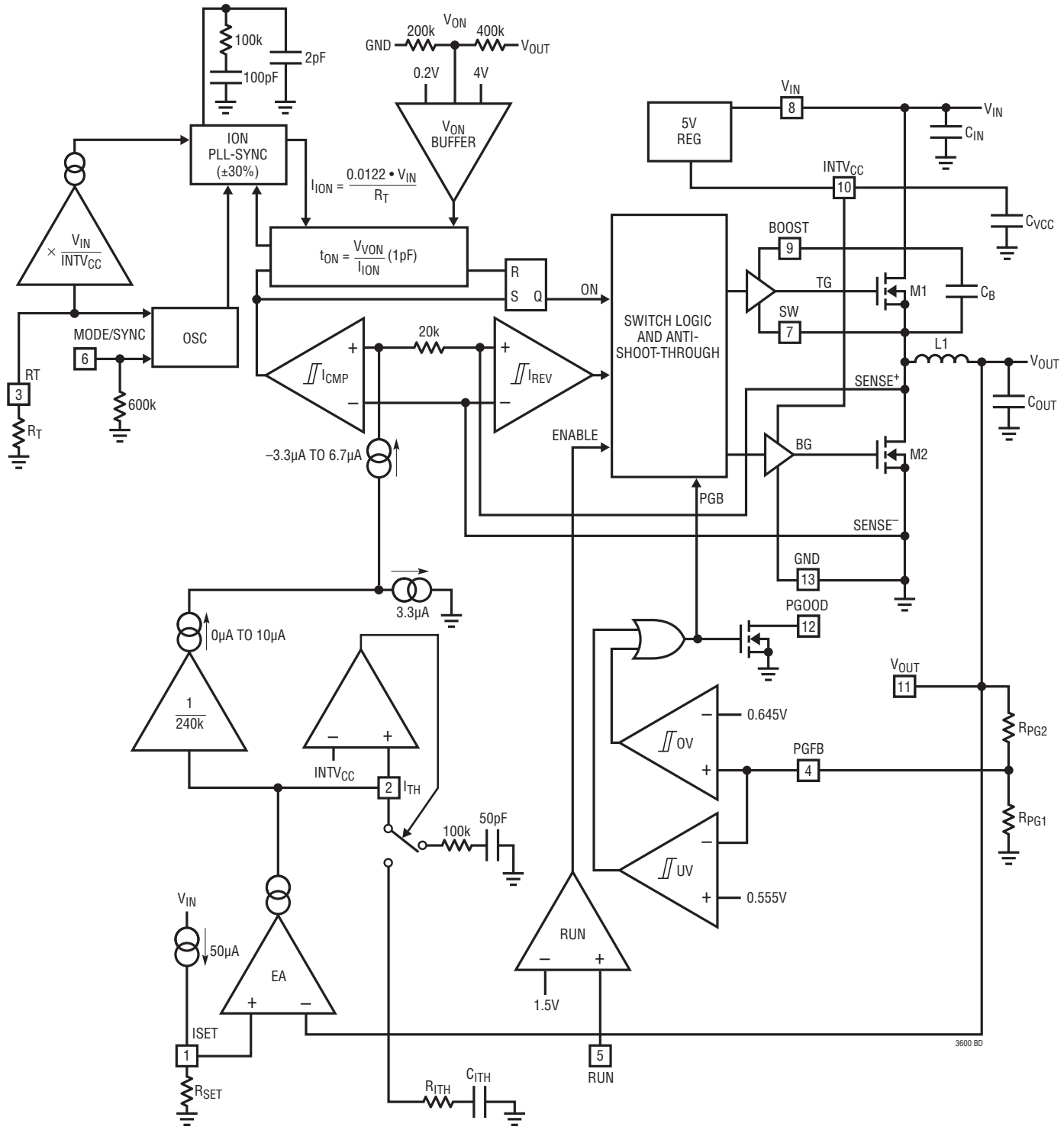
$INTV_{CC}$ (Pin 10): Internal 5V Regulator Output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to GND with a minimum of 1µF low ESR ceramic capacitor.

V_{OUT} (Pin 11): Output Voltage Pin. Output of the LTC3600 voltage regulator. Also the negative input of the error amplifier which is driven to be the same voltage as ISET.

PGOOD (Pin 12): Output Power Good with Open-Drain Logic. PGOOD is pulled to ground when the PGFB pin is more than 0.645V or less than 0.555V. PGOOD open-drain logic will be disabled if PGFB is tied to $INTV_{CC}$.

GND (Exposed Pad Pin 13): Ground. Return path of internal power MOSFETs. Connect the exposed pad to the negative terminal of the input capacitor and output capacitor.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3600 is a current mode monolithic step down regulator. The accurate 50µA current source on the ISET pin allows the user to use just one external resistor to program the output voltage in a unity gain buffer fashion. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a fixed one-shot timer OST. When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator I_{CMP} trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the SW and PGND nodes of the bottom power MOSFET. The voltage on the ITH pin sets the comparator threshold corresponding to inductor valley current. The error amplifier, EA, adjusts this ITH voltage by comparing the V_{OUT} voltage with the voltage on ISET. If the load current increases, it causes a drop in the V_{OUT} voltage relative to V_{ISET}. The ITH voltage then rises until the average inductor current matches that of the load current.

At low load current, the inductor current can drop to zero and become negative. This is detected by current reversal comparator, I_{REV}, which then shuts off the bottom power MOSFET, resulting in discontinuous operation. Both power MOSFETs will remain off with the output capacitor supplying the load current until the ITH voltage rises above the zero current level (0.8V) to initiate another cycle. Discontinuous mode operation is disabled by tying the MODE pin to $INTV_{CC}$, which forces continuous synchronous operation regardless of output load.

The operating frequency is determined by the value of the R_T resistor, which programs the current for the internal oscillator as well as the current for the internal one-shot timer. An internal phase-locked loop servos the switching regulator on-time to track the internal oscillator to force constant switching frequency. If an external synchronization clock is present on the MODE/SYNC pin, the regulator on-time and switching frequency would then track the external clock.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output power good feedback voltage V_{PGFB} exits a 7.5% window around the regulation point. Continuous operation is forced during an OV condition. To defeat the PGOOD function, simply tie PGFB to $INTV_{CC}$.

Pulling the RUN pin to ground forces the LTC3600 into its shutdown state, turning off both power MOSFETs and all of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN voltage above 1.5V turns on the entire chip.

$INTV_{CC}$ Regulator

An internal low drop out (LDO) regulator produces the 5V supply that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply up to 50mA RMS and must be bypassed to ground with a minimum of 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Connecting a load to the $INTV_{CC}$ pin is not recommended since it will further push the LDO into its RMS current rating while increasing power dissipation and die temperature.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3600 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 16V, the regulator suspends operation by shutting off both power MOSFETs and discharges the ISET pin voltage to ground. Once V_{IN} drops below 15V, the regulator immediately resumes normal switching operation by first charging up the ISET pin to its programmed voltage.

Programming Switching Frequency

Connecting a resistor from the RT pin to GND programs the switching frequency from 200kHz to 4MHz according to the following formula:

$$\text{Frequency (Hz)} = \frac{3.6 \bullet 10^{10}\,(1/F)}{R_T\ (\Omega)}$$

For ease of use, the RT pin can be connected directly to the $INTV_{CC}$ pin for 1MHz operation. Do not float the RT pin.

The internal on-time phase-locked loop has a synchronization range of 30% around its programmed frequency. Therefore, during external clock synchronization, the proper

OPERATION

R_T value should be selected such that the external clock frequency is within this 30% range of the R_T programmed frequency.

Output Voltage Tracking and Soft Start

The LTC3600 allows the user to program its output voltage ramp rate by means of the ISET pin. Since V_{OUT} servos its voltage to that of the ISET pin, placing an external capacitor C_{SET} on the ISET pin will program the ramp-up rate of the ISET pin and thus the V_{OUT} voltage.

$$V_{OUT(t)} = I_{ISET} \bullet R_{SET} \left[1 - e^{-\frac{t}{R_{SET} \bullet C_{SET}}}\right]$$

from 0 to 90% V_{OUT}

$$t_{SS} \cong -R_{SET} \bullet C_{SET} \bullet \ell n(1-0.9)$$

$$t_{SS} \simeq 2.3 R_{SET} \bullet C_{SET}$$

The soft-start time t_{SS} (from 0% to 90% V_{OUT}) is 2.3 times of time constant ($R_{SET} \bullet C_{SET}$). The ISET pin can also be driven by an external voltage supply capable of sinking 50µA.

When starting up into a pre-biased V_{OUT}, the LTC3600 will stay in discontinuous mode and keep the power switches off until the voltage on ISET has ramped up to be equal to V_{OUT}, at which point the switcher will begin switching and V_{OUT} will ramp up with ISET.

Output Power Good

When the LTC3600's output voltage is within the 7.5% window of the regulation point, which is reflected back as a V_{PGFB} voltage in the range of 0.555V to 0.645V, the output voltage is in regulation and the PGOOD pin is pulled high with an external resistor connected to $INTV_{CC}$ or another voltage rail. Otherwise, an internal open-drain pull-down device (200Ω) will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3600's PGOOD falling edge includes a blanking delay of approximately 20µs.

Internal/External ITH Compensation

For ease of use, the user can simplify the loop compensation by tying the ITH pin to $INTV_{CC}$ to enable internal compensation. This connects an internal 100k resistor in series with a 50pF capacitor to the output of the error amplifier (internal ITH compensation point). This is a trade-off for simplicity instead of OPTI-LOOP® optimization, where ITH components are external and are selected to optimize the loop transient response with minimum output capacitance.

Minimum Off-Time Considerations

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the LTC3600 is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 130ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \bullet \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 30ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$D_{MIN} = f_{SW} \bullet t_{ON(MIN)}$$

Where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of severe consequences. As the sections on inductor and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \left(\frac{V_{OUT}}{V_{IN}} \right) \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \approx \frac{\Delta I_L}{8 \bullet f_{SW} \bullet C_{OUT}} + \Delta I_L \bullet R_{ESR}$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints. Their relatively low value of bulk capacitance may require multiples in parallel.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, three to four cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about two to three times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} \simeq \frac{2.5 \bullet \Delta I_{OUT}}{f_{SW} \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

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In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 22µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to V_{IN} pin as possible.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Table 1. Inductor Selection Table

INDUCTOR	INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)	MANUFACTURER
IHLP-1616BZ-11 Series	1.0	24	4.5	4.3 × 4.7	2	Vishay
	2.2	61	3.25	4.3 × 4.7	2	www.vishay.com
	4.7	95	1.7	4.3 × 4.7	2	
IHLP-2020BZ-01 Series	1	18.9	7	5.4 × 5.7	2	
	2.2	45.6	4.2	5.4 × 5.7	2	
	3.3	79.2	3.3	5.4 × 5.7	2	
	4.7	108	2.8	5.4 × 5.7	2	
	5.6	113	2.5	5.4 × 5.7	2	
	6.8	139	2.4	5.4 × 5.7	2	
FDV0620 Series	1	18	5.7	6.7 × 7.4	2	Toko
	2.2	37	4	6.7 × 7.4	2	www.toko.com
	3.3	51	3.2	6.7 × 7.4	2	
	4.7	68	2.8	6.7 × 7.4	2	
MPLC0525L Series	1	16	6.4	6.2 × 5.4	2.5	NEC/Tokin
	1.5	24	5.2	6.2 × 5.4	2.5	www.nec-tokin.com
	2.2	40	4.1	6.2 × 5.4	2.5	
HCP0703 Series	1	9	11	7 × 7.3	3	Cooper Bussmann
	1.5	14	9	7 × 7.3	3	www.cooperbussmann.com
	2.2	18	8	7 × 7.3	3	
	3.3	28	6	7 × 7.3	3	
	4.7	37	5.5	7 × 7.3	3	
	6.8	54	4.5	7 × 7.3	3	
	8.2	64	4	7 × 7.3	3	
RLF7030 Series	1	8.8	6.4	6.9 × 7.3	3.2	TDK
	1.5	9.6	6.1	6.9 × 7.3	3.2	www.tdk.com
	2.2	12	5.4	6.9 × 7.3	3.2	
	3.3	20	4.1	6.9 × 7.3	3.2	
	4.7	31	3.4	6.9 × 7.3	3.2	
	6.8	45	2.8	6.9 × 7.3	3.2	
WE-TPC 4828 Series	1.2	17	3.1	4.8 × 4.8	2.8	Würth Elektronik
	1.8	20	2.7	4.8 × 4.8	2.8	www.we-online.com
	2.2	23	2.5	4.8 × 4.8	2.8	
	2.7	27	2.35	4.8 × 4.8	2.8	
	3.3	30	2.15	4.8 × 4.8	2.8	
	3.9	47	1.72	4.8 × 4.8	2.8	
	4.7	52	1.55	4.8 × 4.8	2.8	

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Once the value for L is known, the type of inductor must be selected. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, TDK, and Würth Elektronik. Refer to Table 1 for more details.

Checking Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the ITH pin not only allows optimization of the control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The ITH external components shown in the Figure 1 circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH}. If R_{ITH} is increased by the same factor that C_{ITH} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) load capacitors. The discharged load capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limit, short-circuit protection, and soft-start.

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Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3600 circuits: 1) I^2R losses, 2) transition losses, 3) switching losses, 4) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, the external inductor, R_L, and board trace resistance, R_b. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(D) + (R_{DS(ON)BOT})(1-D)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

   $$I^2R \text{ losses} = I_{OUT}^2 (R_{SW} + R_L + R_b)$$

2. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, internal power MOSFET gate capacitance, internal driver strength, and switching frequency.

3. The $INTV_{CC}$ current is the sum of the power MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f_{SW}$ (QT + QB), where QT and QB are the gate charges of the internal top and bottom power MOSFETs and f_{SW} is the switching frequency. Since $INTV_{CC}$ is a low dropout regulator output powered by V_{IN}, the $INTV_{CC}$ current also shows up as V_{IN} current, unless a separate voltage supply (>5V and <6V) is used to drive $INTV_{CC}$.

4. Other "hidden" losses such as copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these system level losses in the design of a system. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the LTC3600 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed pad DFN or MSOP package. However, in applications where the LTC3600 is running at high ambient temperature, high V_{IN}, high switching frequency and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until temperature is about 15°C cooler.

To avoid the LTC3600 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

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As an example, consider the case when the LTC3600 is used in application where V_{IN} = 12V, I_{OUT} = 1.5A, frequency = 4MHz, V_{OUT} = 1.8V. The equivalent power MOSFET resistance R_{SW} is:

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)BOT} \bullet \frac{V_{IN} - V_{OUT}}{V_{IN}} = 0.2 \bullet \frac{1.8}{12} + 0.1 \bullet \frac{10.2}{12} = 0.115\Omega$$

The V_{IN} current during 4MHz forced continuous operation with no load is about 11mA, which includes switching and internal biasing current loss, transition loss, inductor core loss and other losses in the application. Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet I_{VIN} \text{ (No Load)}$$

$$= 2.25A^2 \bullet 0.115\Omega + 12V \bullet 11mA = 0.39W$$

The DFN 3mm × 3mm package junction-to-ambient thermal resistance, θ_{JA}, is around 55°C/W. Therefore, the junction temperature of the regulator operating in a 50°C ambient temperature is approximately:

$$T_J = 0.39W \bullet 55\frac{°C}{W} + 50°C = 71°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 25% at 71°C yields a new junction temperature of 75°C, which is still very far away from thermal shutdown or maximum allowed junction temperature rating.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3600. Check the following in your layout:

1. Do the capacitors C_{IN} connect to the power V_{IN} and power GND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. Are C_{OUT} and inductor closely connected? The (–) plate of C_{OUT} returns current to PGND and the (–) plate of C_{IN}.
3. The ground terminal of the ISET resistor must be connected to the other quiet signal GND and together connect to the power GND on only one point. The ISET resistor should be placed and routed away from noisy components and traces, such as the SW line, and its trace should be minimized.
4. Keep sensitive components away from the SW pin. The ISET resistor, R_T resistor, the compensation components C_{ITH} and R_{ITH}, and the $INTV_{CC}$ bypass capacitor, should be routed away from the SW trace and the inductor.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the signal GND at one point which is then connected to the power GND at the exposed pad with minimal resistance.

   Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to one of the input supplies: V_{IN} or GND.

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Design Example

As a design example, consider using the LTC3600 in an application with the following specifications:

V_{IN} = 10.8V to 13.2V
V_{OUT} = 1.8V
$I_{OUT(MAX)}$ = 1.5A
$I_{OUT(MIN)}$ = 500mA
f_{SW} = 2MHz

First, R_{SET} is selected based on:

$$R_{SET} = \frac{V_{OUT}}{50\mu A} = \frac{1.8V}{50\mu A} = 36k\Omega$$

For best accuracy, a 0.1% 36.1k resistor is selected.

Because efficiency is important at both high and low load current, discontinuous mode operation will be utilized. Select from the characteristic curves the correct R_T resistor value for 2MHz switching frequency. Based on that, R_T should be 18.2k. Then calculate the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \left(\frac{1.8V}{2MHz \bullet 0.6A}\right)\left(1 - \frac{1.8V}{13.2V}\right) = 1.3\mu H$$

The nearest standard value inductor would be 1.2µH.

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, one 47µF ceramic capacitor will be used.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 1.5A\left(\frac{1.8V}{13.2V}\right)\left(\frac{13.2V}{1.8V} - 1\right)^{1/2} = 0.51A$$

Decoupling the V_{IN} pin with one 22µF ceramic capacitor is adequate for most applications.

TYPICAL APPLICATIONS

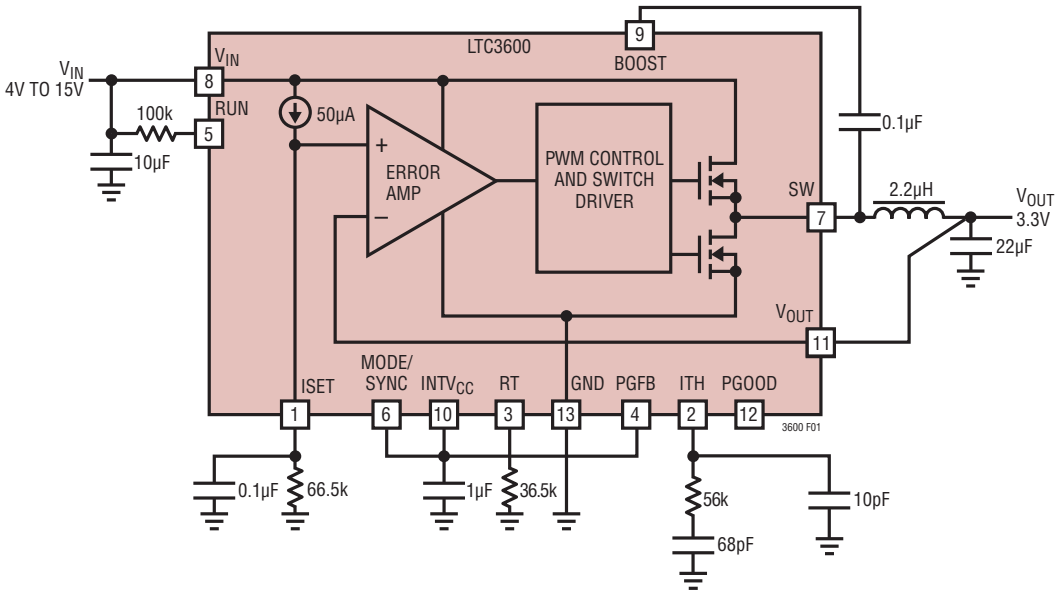
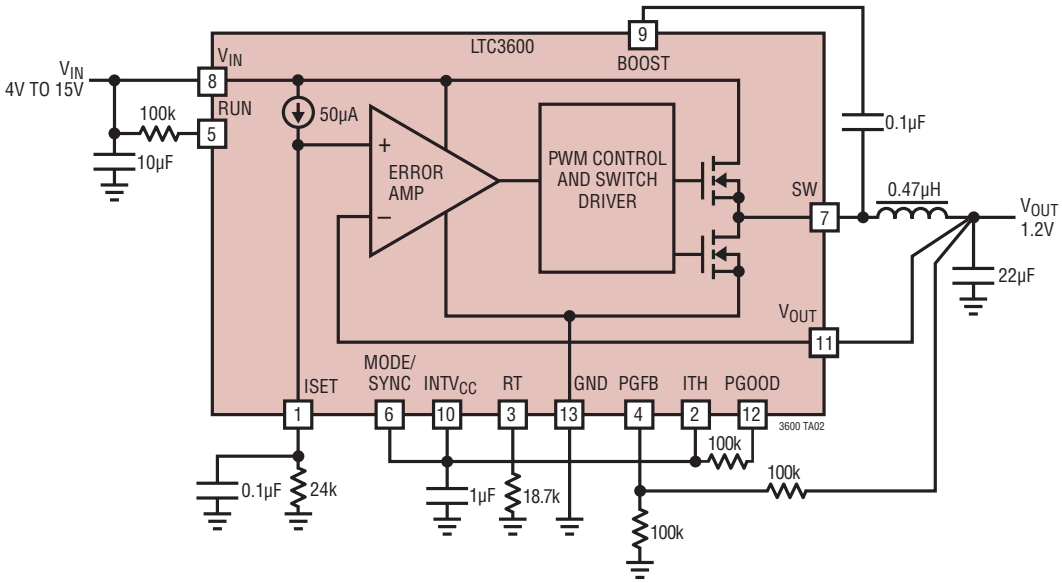


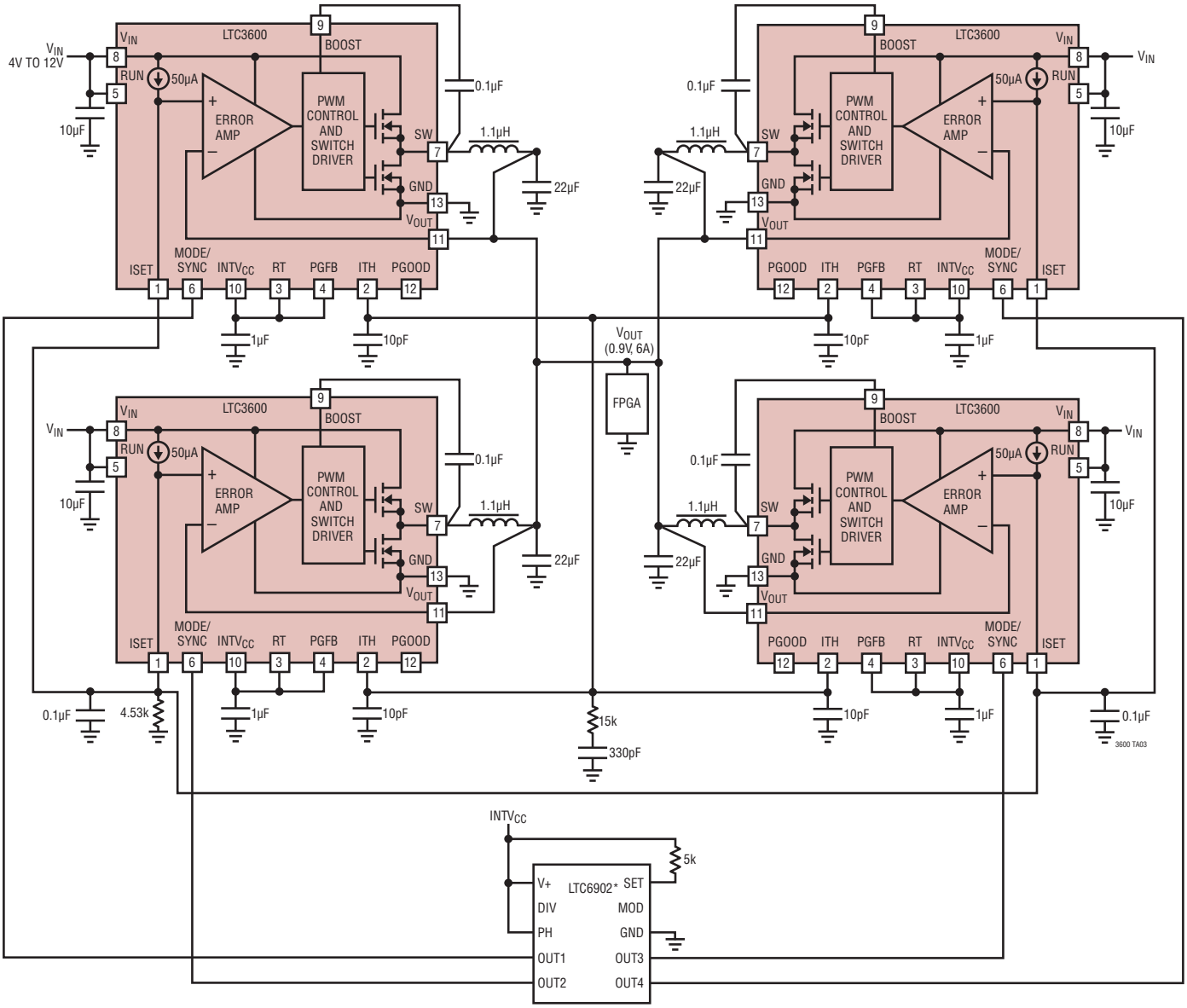
Figure 1. 12V to 3.3V 1MHz Buck Regulator

12V to 1.2V 2MHz Buck Regulator



TYPICAL APPLICATIONS

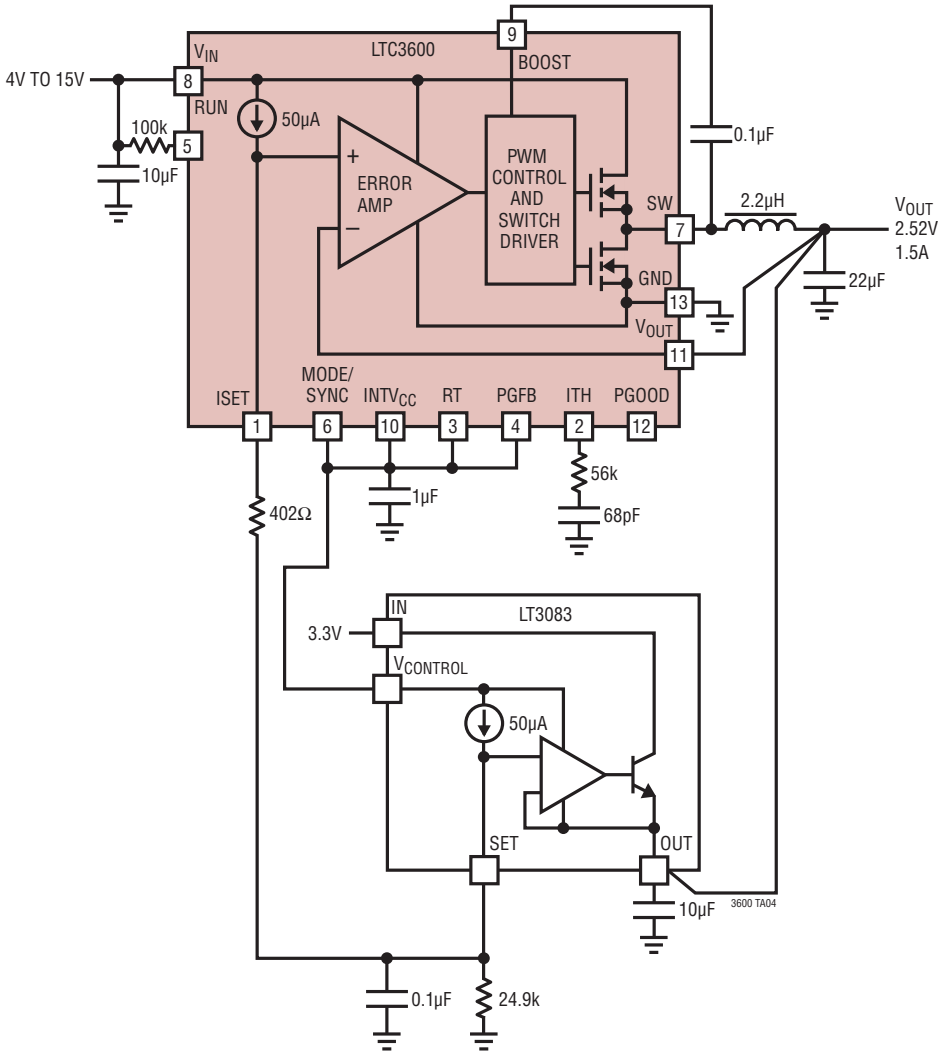
0.9V FPGA Power Supply



*EXTERNAL CLOCK FOR FREQUENCY SYNCHRONIZATION IS RECOMMENDED

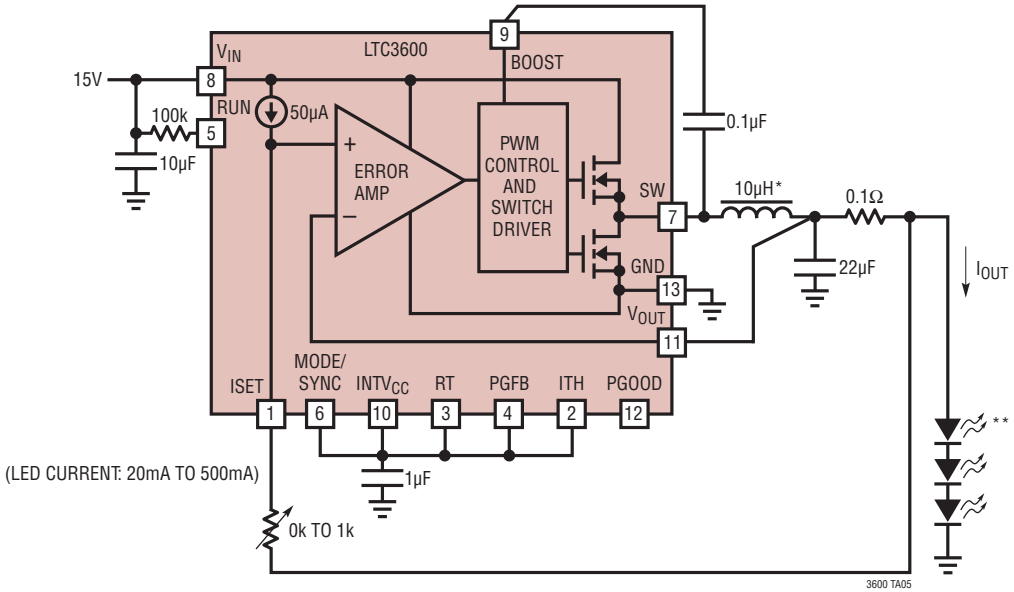
TYPICAL APPLICATIONS

High Efficiency Fast Load Response Power Supply



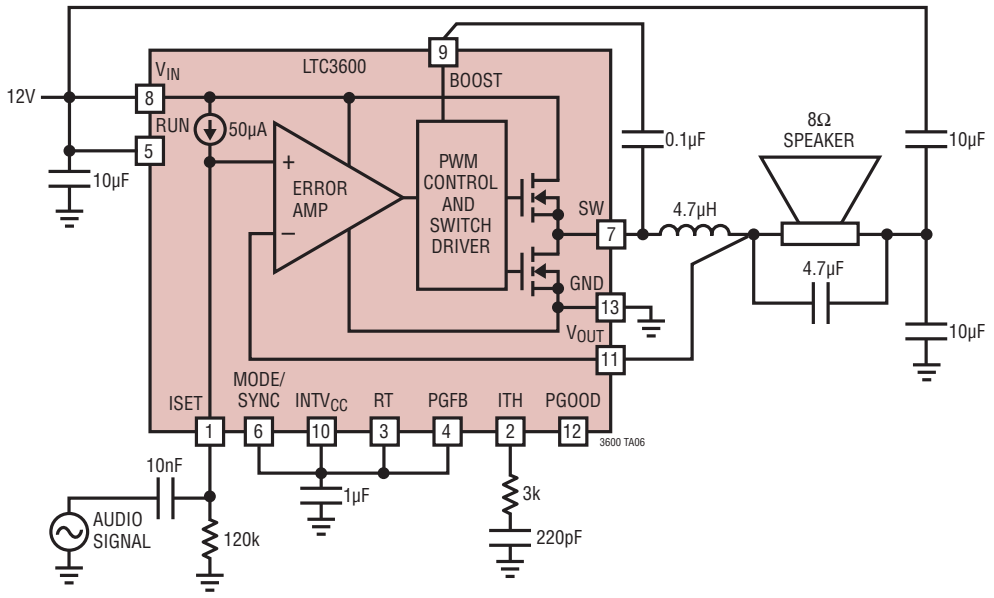
TYPICAL APPLICATIONS

LED Driver with Programmable Dimming Control



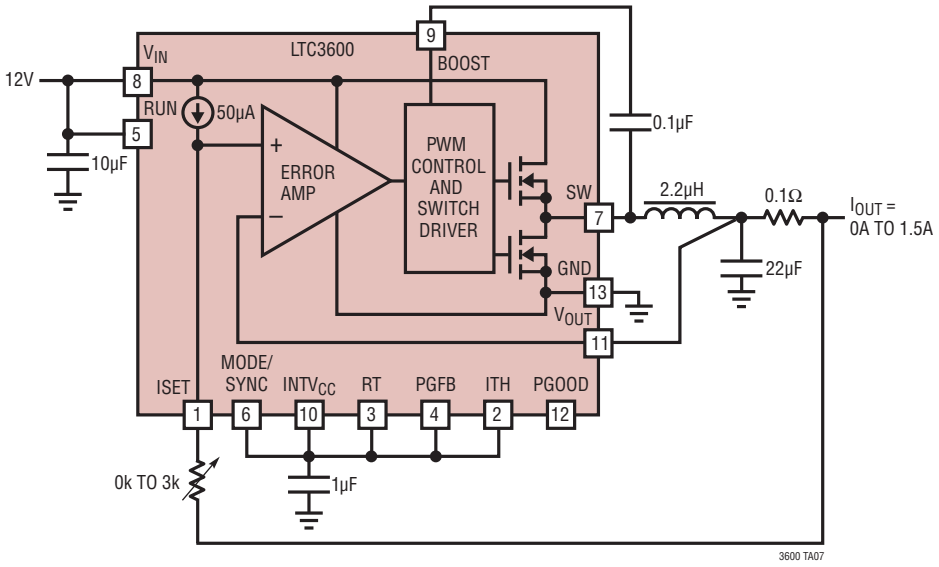
*TDK LTF5022T-100M1R4-LC
**LUXEON LXML-PWN1-0100

High Efficiency 12V Audio Driver

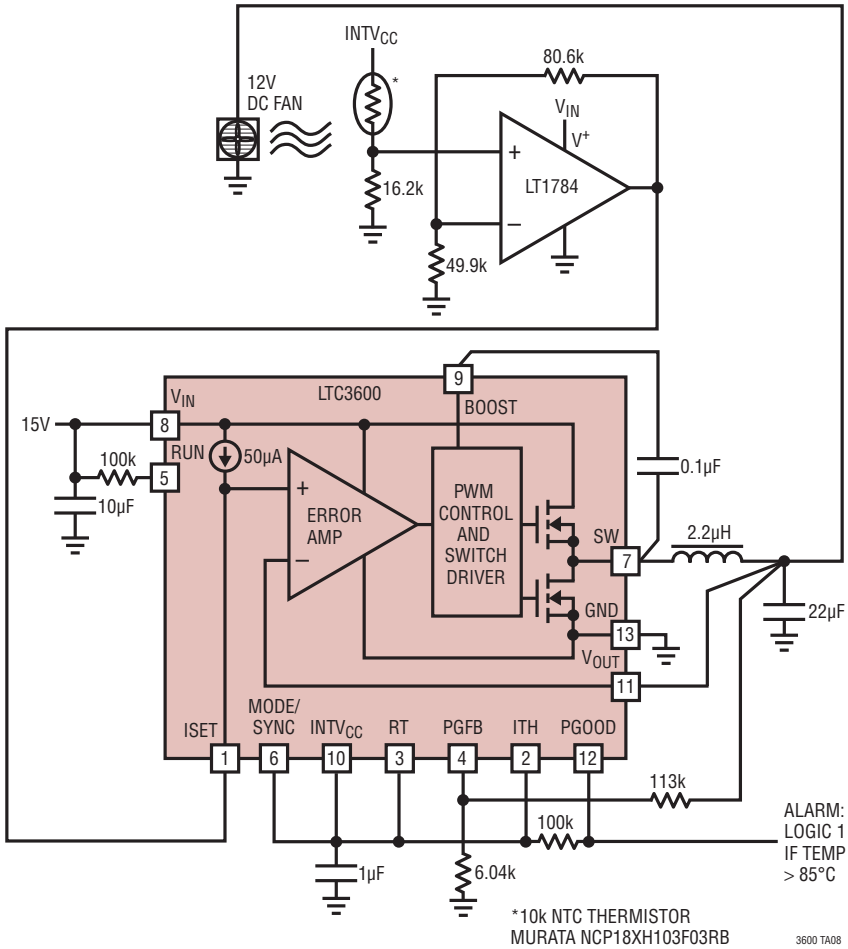


TYPICAL APPLICATIONS

Programmable 1.5A Current Source

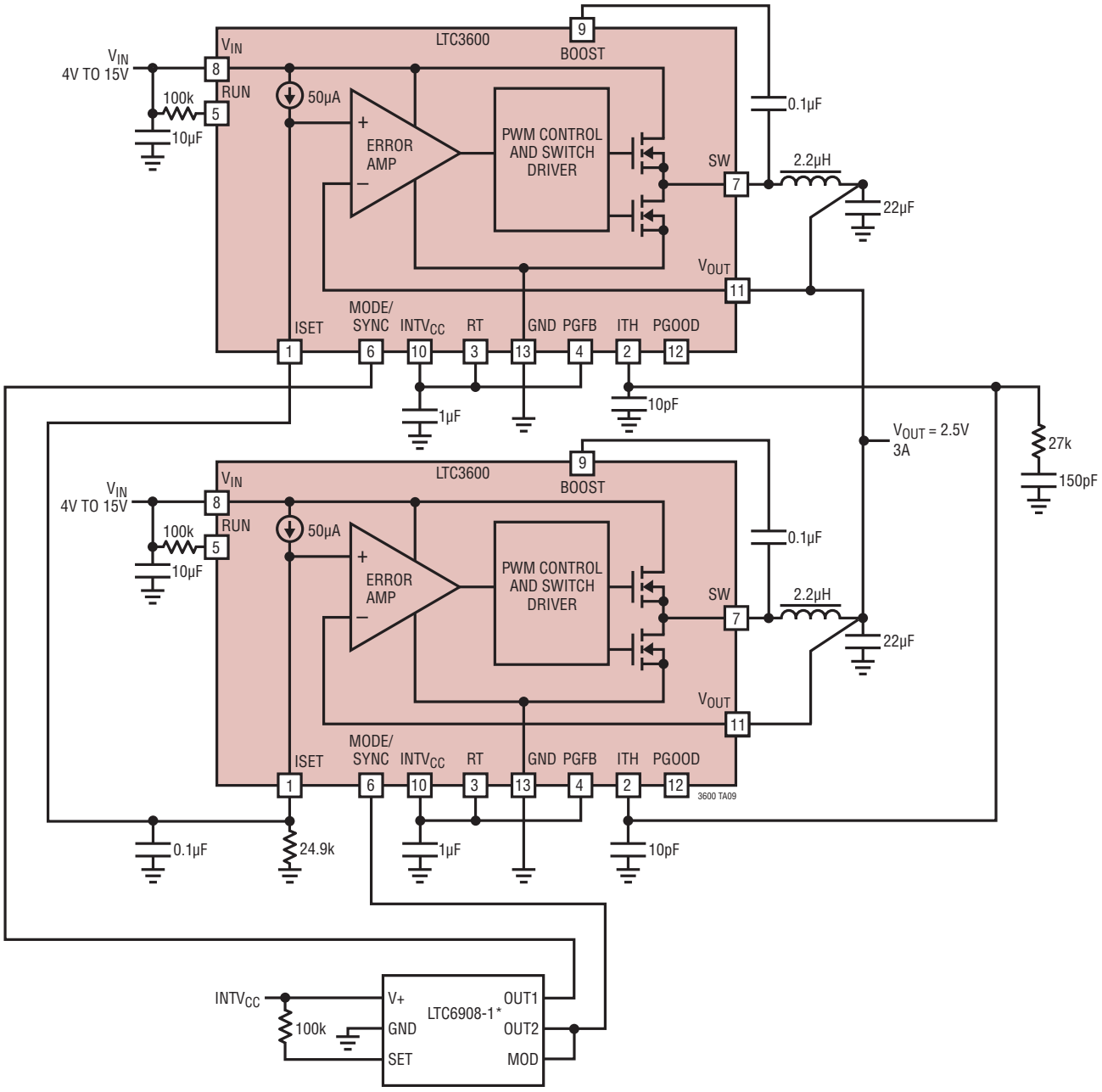


12V Fan Speed Controller



TYPICAL APPLICATIONS

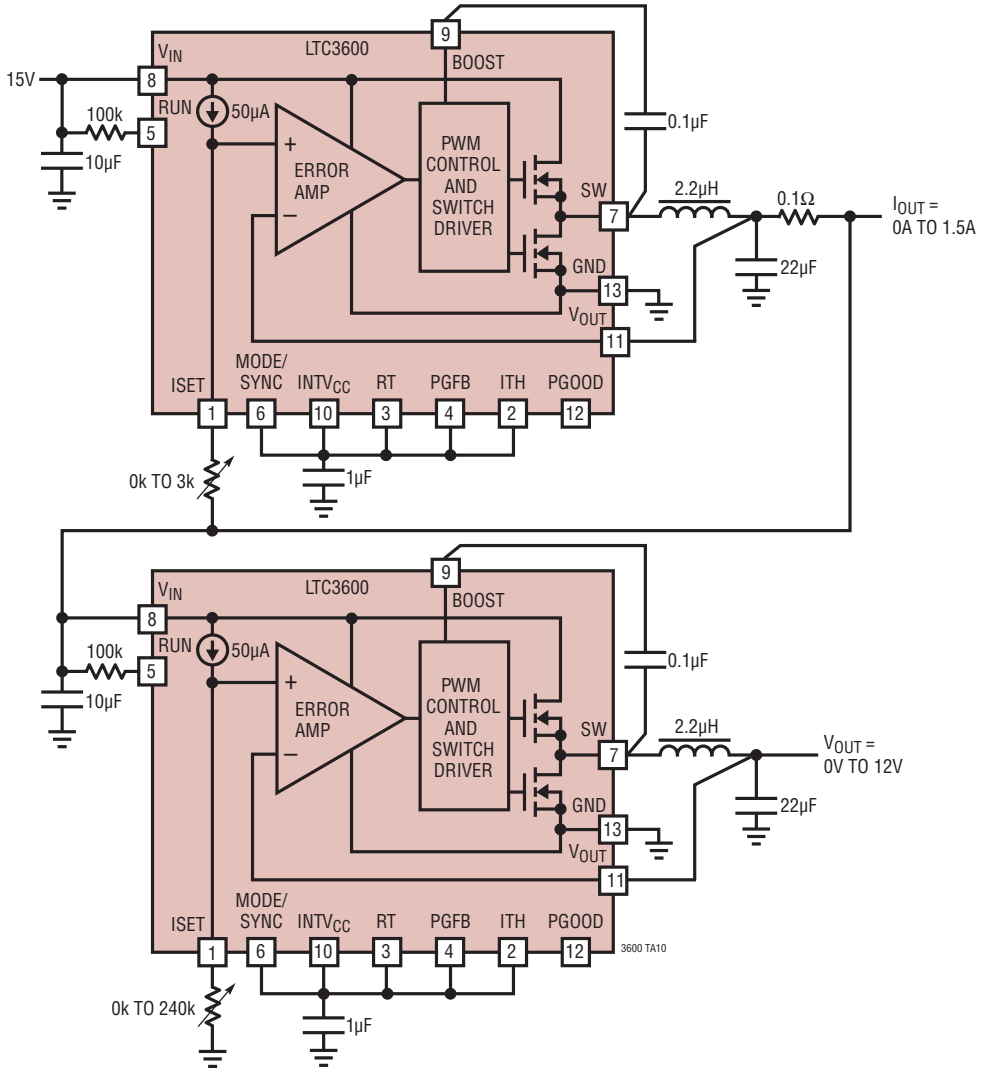
15V, 3A Dual Phase Single-Output Regulator



*EXTERNAL CLOCK FOR FREQUENCY SYNCHRONIZATION IS RECOMMENDED

TYPICAL APPLICATIONS

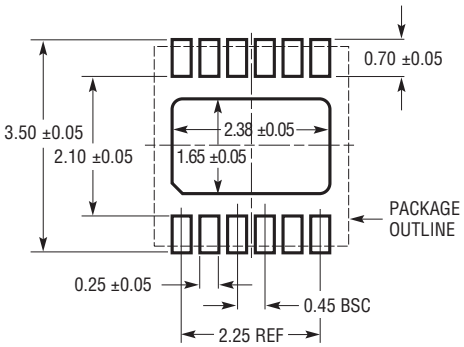
1.5A Lab Supply with Programmable Current Limit



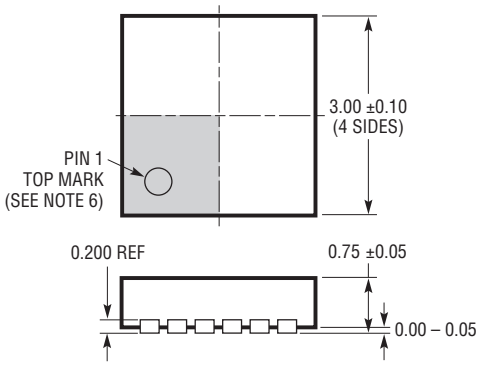
PACKAGE DESCRIPTION

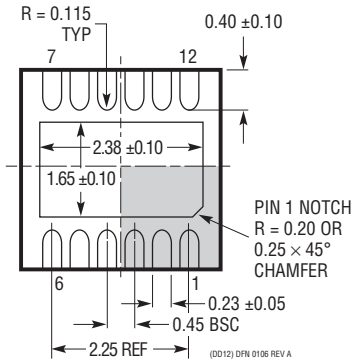
Please refer to http://www.linear.com/product/LTC3600#packaging for the most recent package drawings.

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





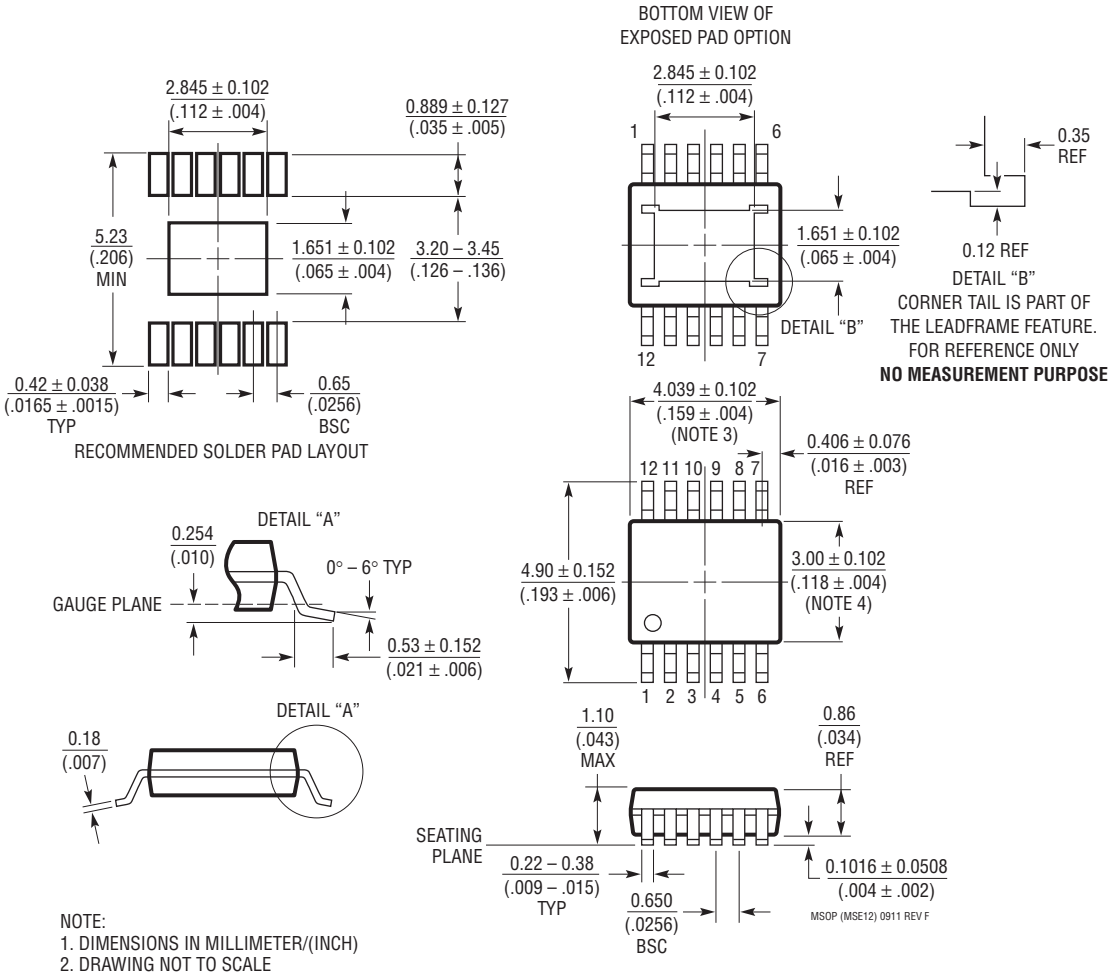
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3600#packaging for the most recent package drawings.

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev F)



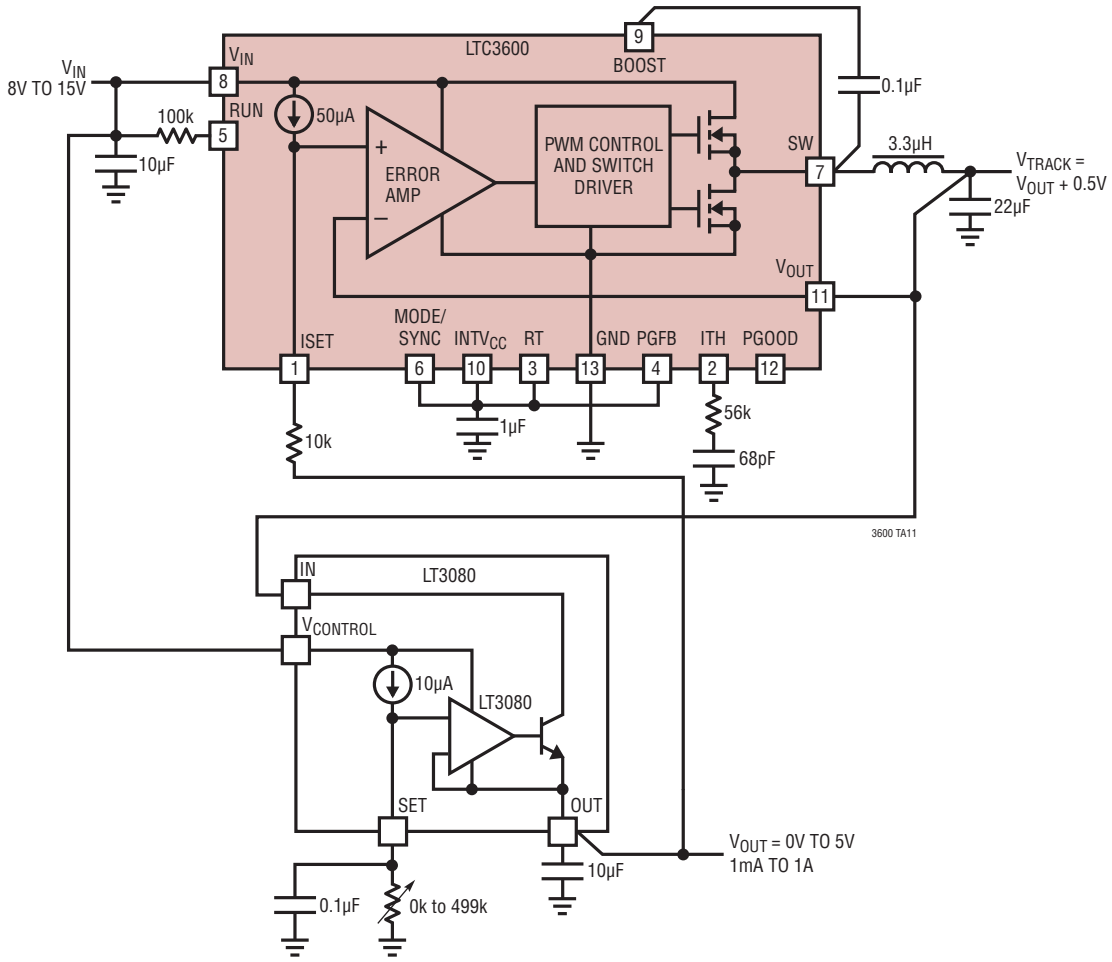
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/12	Clarified Feature and Description	1
		Clarified Electrical Characteristics	3
		Clarified ISET (Pin 1) Description	8
		Clarified Functional Diagram	9
		Modified Application Circuit	28
B	04/12	Changed MODE/SYNC Threshold SYNC $V_{IH(MIN)}$ from 1V to 2.5V	3
C	07/12	Clarified Supply Shutdown Current to Zero	1
		Clarified Absolute Maximum Ratings to include Note 5	2
		Clarified Conditions on Electrical Table, V_{IN} = 12V	3
		Clarified Pin Functions	8
D	06/16	Revised Minimum Off Time Considerations section	11

TYPICAL APPLICATION

High Efficiency, Low Noise 1A Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3601	15V, 1.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 1µA, 4mm × 4mm QFN-20 and MSOP-16E Packages
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20 and MSOP-16E Packages
LTC3633	15V, Dual 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 15µA, 4mm × 5mm QFN-28 and TSSOP-28E Packages
LTC3605	15V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24 and MSOP-16E Packages
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 14µA, 3mm × 3mm QFN-16 and MSOP-16E Packages
LT3080	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2 Supply Operation), Low Noise = 40µV_{RMS} V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, MSOP-8, 3mm × 3mm DFN Packages
LT3083	Adjustable 3A Single Resistor Low Dropout Regulator	310mV Dropout Voltage, Low Noise 40µV_{RMS} V_{IN}: 1.2V to 23V, V_{OUT}: 0V to 22.7V, 4mm × 4mm DFN, TSSOP-16E Packages