ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Terminal Voltages
- V_{CC} (Note 3) ..... –0.3V to 6V
- $\overline{OV}$, $\overline{UV}$ ..... –0.3V to 16V
- TMR ..... –0.3V to (V_{CC} + 0.3V)
- VLn, VHn, $\overline{LATCH}$, DIS, SEL ..... –0.3V to 7.5V

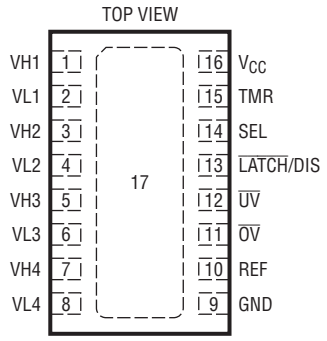
Terminal Currents
- I_{VCC} 10mA
- Reference Load Current (I_{REF}) ..... ±1mA
- $I_{\overline{UV}}$, $I_{\overline{OV}}$ 10mA

Operating Temperature Range
- LTC2914C ..... 0°C to 70°C
- LTC2914I ..... –40°C to 85°C
- LTC2914H ..... –40°C to 125°C

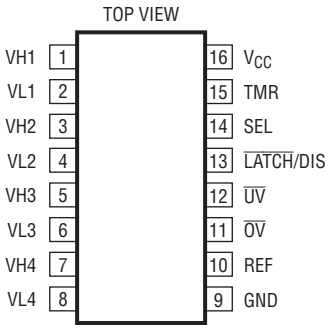
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- SSOP ..... 300°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43.5°C/W
EXPOSED PAD (PIN 17)
PCB GND CONNECTION OPTIONAL



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2914CDHC-1#PBF	LTC2914CDHC-1#TRPBF	29141	16-Lead Plastic (5mm × 3mm) DFN	0°C to 70°C
LTC2914IDHC-1#PBF	LTC2914IDHC-1#TRPBF	29141	16-Lead Plastic (5mm × 3mm) DFN	–40°C to 85°C
LTC2914HDHC-1#PBF	LTC2914HDHC-1#TRPBF	29141	16-Lead Plastic (5mm × 3mm) DFN	–40°C to 125°C
LTC2914CDHC-2#PBF	LTC2914CDHC-2#TRPBF	29142	16-Lead Plastic (5mm × 3mm) DFN	0°C to 70°C
LTC2914IDHC-2#PBF	LTC2914IDHC-2#TRPBF	29142	16-Lead Plastic (5mm × 3mm) DFN	–40°C to 85°C
LTC2914HDHC-2#PBF	LTC2914HDHC-2#TRPBF	29142	16-Lead Plastic (5mm × 3mm) DFN	–40°C to 125°C
LTC2914CGN-1#PBF	LTC2914CGN-1#TRPBF	29141	16-Lead Plastic SSOP	0°C to 70°C
LTC2914IGN-1#PBF	LTC2914IGN-1#TRPBF	2914I1	16-Lead Plastic SSOP	–40°C to 85°C
LTC2914HGN-1#PBF	LTC2914HGN-1#TRPBF	2914H1	16-Lead Plastic SSOP	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2914CGN-2#PBF	LTC2914CGN-2#TRPBF	29142	16-Lead Plastic SSOP	0°C to 70°C
LTC2914IGN-2#PBF	LTC2914IGN-2#TRPBF	2914I2	16-Lead Plastic SSOP	–40°C to 85°C
LTC2914HGN-2#PBF	LTC2914HGN-2#TRPBF	2914H2	16-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.*The temperature grade is identified by a label on the shipping container
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, VLn = 0.45V, VHn = 0.55V, $\overline{LATCH}$ = V_{CC}, SEL = V_{CC}, DIS = Open unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SHUNT}	V_{CC} Shunt Regulator Voltage	I_{CC} = 5mA	●	6.2	6.6	6.9	V
		–40°C < T_A < 125°C	●	6.2	6.6	7.0	V
ΔV_{SHUNT}	V_{CC} Shunt Regulator Load Regulation	I_{CC} = 2mA to 10mA	●		200	300	mV
V_{CC}	Supply Voltage (Note 3)		●	2.3		V_{SHUNT}	V
$V_{CCR(MIN)}$	Minimum V_{CC} Output Valid	DIS = 0V	●			1	V
$V_{CC(UVLO)}$	Supply Undervoltage Lockout	V_{CC} Rising, DIS = 0V	●	1.9	2	2.1	V
$\Delta V_{CC(UVHYST)}$	Supply Undervoltage Lockout Hysteresis	DIS = 0V	●	5	25	50	mV
I_{CC}	Supply Current	V_{CC} = 2.3V to 6V	●		62	100	µA
V_{REF}	Reference Output Voltage	I_{VREF} = ±1mA	●	0.985	1	1.015	V
		–40°C < T_A < 125°C	●	0.985	1	1.020	V
V_{UOT}	Undervoltage/Overvoltage Voltage Threshold		●	492	500	508	mV
t_{UOD}	Undervoltage/Overvoltage Voltage Threshold to Output Delay	VHn = V_{UOT} – 5mV or VLn = V_{UOT} + 5mV	●	50	125	500	µs
I_{VHL}	VHn, VLn Input Current		●			±15	nA
		–40°C < T_A < 125°C	●			±30	nA
t_{UOTO}	$\overline{UV}/\overline{OV}$ Time-Out Period	C_{TMR} = 1nF	●	6	8.5	12.5	ms
		–40°C < T_A < 125°C	●	6	8.5	14	ms
$V_{\overline{LATCH}(IH)}$	$\overline{OV}$ Latch Clear Input High		●	1.2			V
$V_{\overline{LATCH}(IL)}$	$\overline{OV}$ Latch Clear Threshold Input Low		●			0.8	V
I_{LATCH}	$\overline{LATCH}$ Input Current	$V_{\overline{LATCH}}$ > 0.5V	●			±1	µA
$V_{DIS(IH)}$	DIS Input High		●	1.2			V
$V_{DIS(IL)}$	DIS Input Low		●			0.8	V
I_{DIS}	DIS Input Current	V_{DIS} > 0.5V	●	1	2	3	µA
$I_{TMR(UP)}$	TMR Pull-Up Current	V_{TMR} = 0V	●	–1.3	–2.1	–2.8	µA
		–40°C < T_A < 125°C	●	–1.2	–2.1	–2.8	µA
$I_{TMR(DOWN)}$	TMR Pull-Down Current	V_{TMR} = 1.6V	●	1.3	2.1	2.8	µA
		–40°C < T_A < 125°C	●	1.2	2.1	2.8	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, VLn = 0.45V, VHn = 0.55V, $\overline{LATCH}$ = V_{CC}, SEL = V_{CC}, DIS = Open unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{TMR(DIS)}$	Timer Disable Voltage	Referenced to V_{CC}	●	–180	–270		mV
V_{OH}	Output Voltage High $\overline{UV}/\overline{OV}$	V_{CC} = 2.3V, $I_{\overline{UV}/\overline{OV}}$ = –1µA	●	1			V
V_{OL}	Output Voltage Low $\overline{UV}/\overline{OV}$	V_{CC} = 2.3V, $I_{\overline{UV}/\overline{OV}}$ = 2.5mA V_{CC} = 1V, $I_{\overline{UV}}$ = 100µA	● ●		0.1 0.01	0.3 0.15	V V
Three-State Input SEL							
V_{IL}	Low Level Input Voltage		●			0.4	V
V_{IH}	High Level Input Voltage		●	1.4			V
V_Z	Pin Voltage when Left in Hi-Z State	I_{SEL} = ±10µA	●	0.7	0.9	1.1	V
		–40°C < T_A < 125°C	●	0.6	0.9	1.2	V
I_{SEL}	SEL High, Low Input Current		●			±25	µA
$I_{SEL(MAX)}$	Maximum SEL Input Current	SEL Tied to Either V_{CC} or GND	●			±30	µA
t_{PW}	Latch Clear Pulse Width	(Note 4)	●	2			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

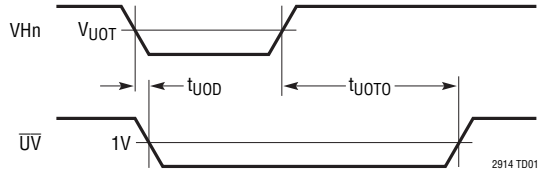
Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3: V_{CC} maximum pin voltage is limited by input current. Since the V_{CC} pin has an internal 6.5V shunt regulator, a low impedance supply that exceeds 6V may exceed the rated terminal current. Operation from higher voltage supplies requires a series dropping resistor. See Applications Information.

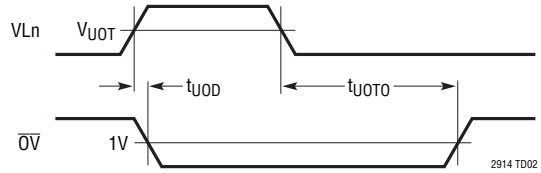
Note 4: Guaranteed by design, not subject to test.

TIMING DIAGRAMS

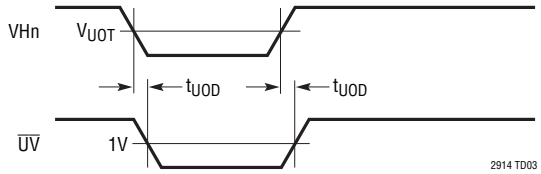
VHn Monitor Timing



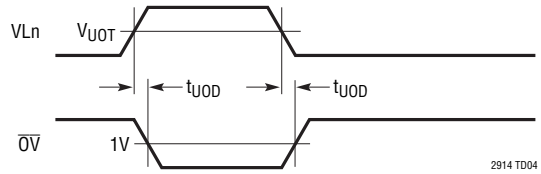
VLn Monitor Timing



VHn Monitor Timing (TMR Pin Strapped to V_{CC})



VLn Monitor Timing (TMR Pin Strapped to V_{CC})

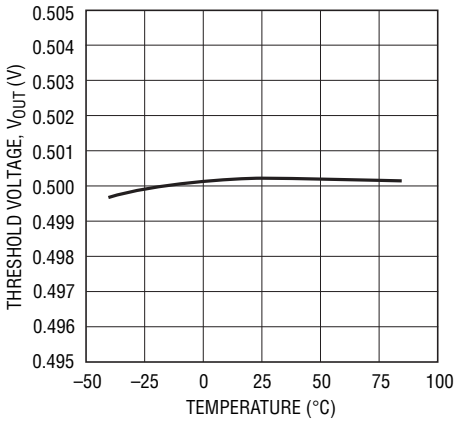


NOTE: WHEN AN INPUT IS CONFIGURED AS A NEGATIVE SUPPLY MONITOR, VHn WILL TRIGGER AN OV CONDITION AND VLn WILL TRIGGER A UV CONDITION

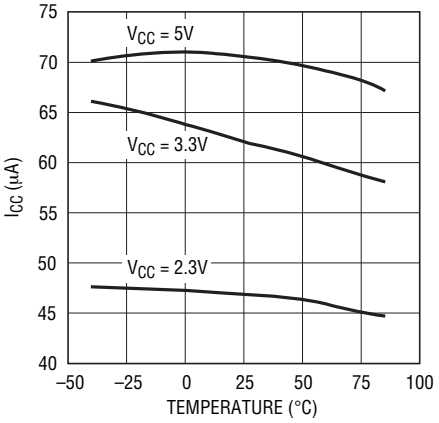
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

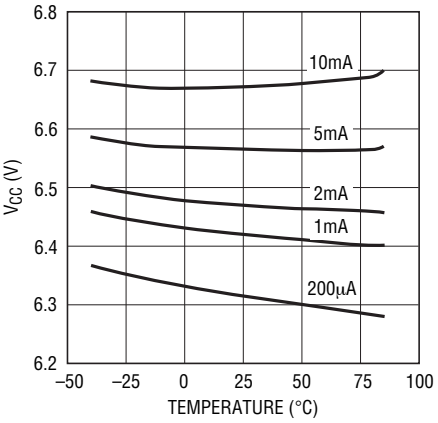
Input Threshold Voltage vs Temperature



Supply Current vs Temperature



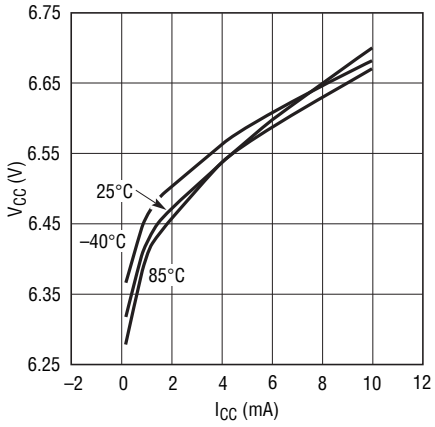
V_{CC} Shunt Voltage vs Temperature



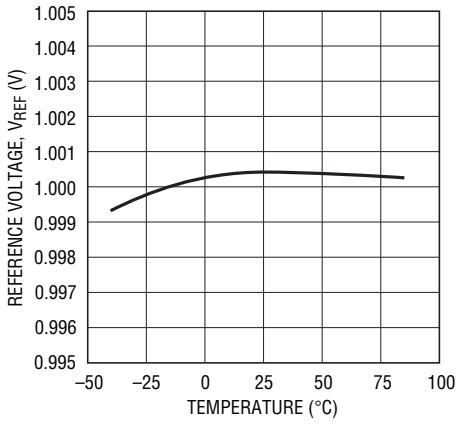
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

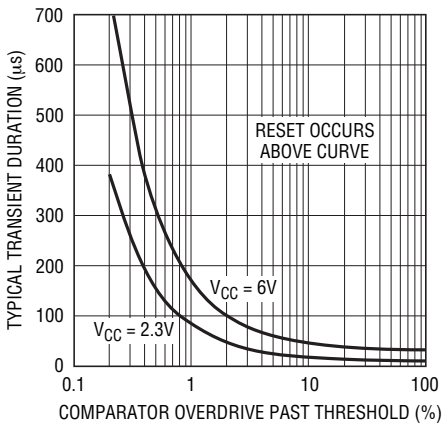
V_{CC} Shunt Voltage vs I_{CC}



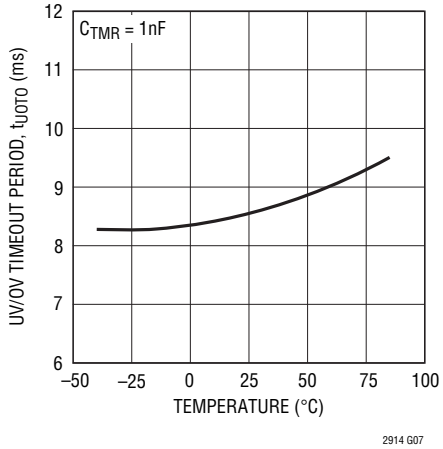
Buffered Reference Voltage vs Temperature



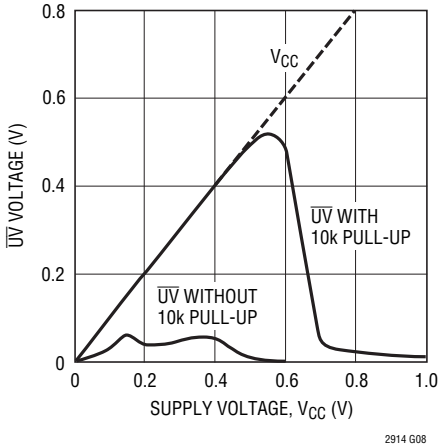
Transient Duration vs Comparator Overdrive



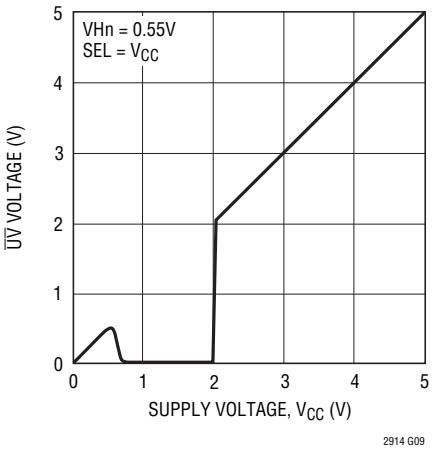
Reset Timeout Period vs Temperature



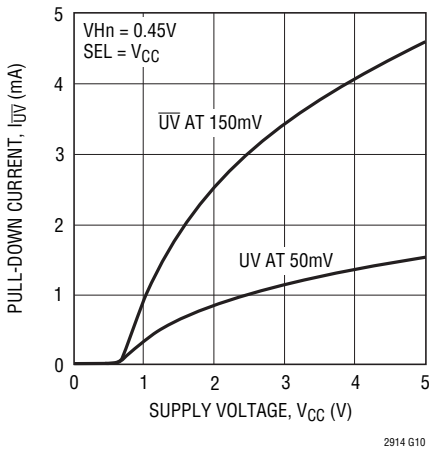
$\overline{UV}$ Output Voltage vs V_{CC}



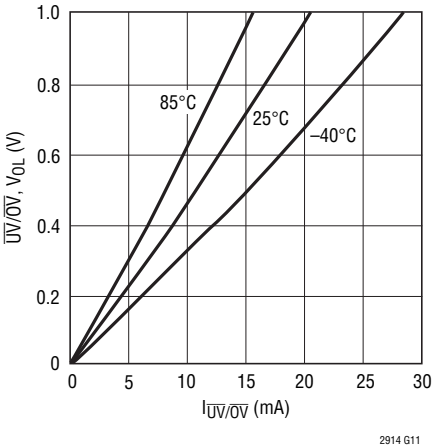
$\overline{UV}$ Output Voltage vs V_{CC}



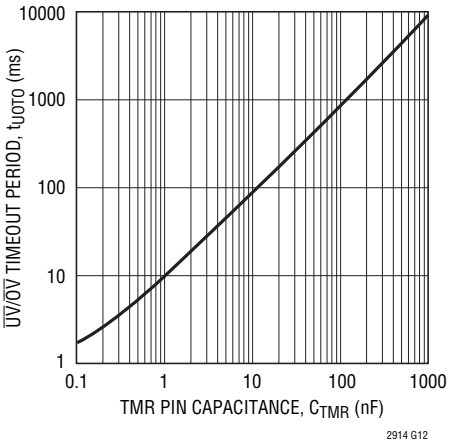
$\overline{UV}$, I_{SINK} vs V_{CC}



$\overline{UV}/\overline{OV}$ Voltage Output Low vs Output Sink Current



Reset Timeout Period vs Capacitance



PIN FUNCTIONS

DIS (Pin 13, LTC2914-2): Output Disable Input. Disables the $\overline{OV}$ and $\overline{UV}$ output pins. When DIS is pulled high, the $\overline{OV}$ and $\overline{UV}$ pins are not asserted except during a UVLO condition. Pin has a weak (2µA) internal pull-down to GND. Leave pin open if unused.

Exposed Pad (Pin 17, DFN Package): Exposed Pad may be left open or connected to device ground.

GND (Pin 9): Device Ground

$\overline{LATCH}$ (Pin 13, LTC2914-1): $\overline{OV}$ Latch Clear/Bypass Input. When pulled low, $\overline{OV}$ is latched when asserted. When pulled high, $\overline{OV}$ latch is cleared. While held high, $\overline{OV}$ has the same delay and output characteristics as $\overline{UV}$.

$\overline{OV}$ (Pin 11): Overvoltage Logic Output. Asserts low when any positive polarity input voltage is above threshold or any negative polarity input voltage is below threshold. Latched low (LTC2914-1). Held low for an adjustable delay time after all inputs are valid (LTC2914-2). Pin has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. Leave pin open if unused.

REF (Pin 10): Buffered Reference Output. 1V reference used for the offset of negative-monitoring applications. The buffered reference sources and sinks up to 1mA. The reference drives capacitive loads up to 1nF. Larger capacitive loads may cause instability. Leave pin open if unused.

SEL (Pin 14): Input Polarity Select Three-State Input. Connect to V_{CC}, GND or leave unconnected in open state to select one of three possible input polarity combinations (refer to Table 1).

TMR (Pin 15): Reset Delay Timer. Attach an external capacitor (C_{TMR}) of at least 10pF to GND to set a reset delay time of 9ms/nF. A 1nF capacitor will generate an 8.5ms reset delay time. Tie pin to V_{CC} to bypass timer.

$\overline{UV}$ (Pin 12): Undervoltage Logic Output. Asserts low when any positive polarity input voltage is below threshold or any negative polarity input voltage is above threshold. Held low for an adjustable delay time after all voltage inputs are valid. Pin has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. Leave pin open if unused.

V_{CC} (Pin 16): Supply Voltage. Bypass this pin to GND with a 0.1µF (or greater) capacitor. Operates as a direct supply input for voltages up to 6V. Operates as a shunt regulator for supply voltages greater than 6V and must have a resistance between the pin and the supply to limit input current to no greater than 10mA. When used without a current-limiting resistance, pin voltage must not exceed 6V.

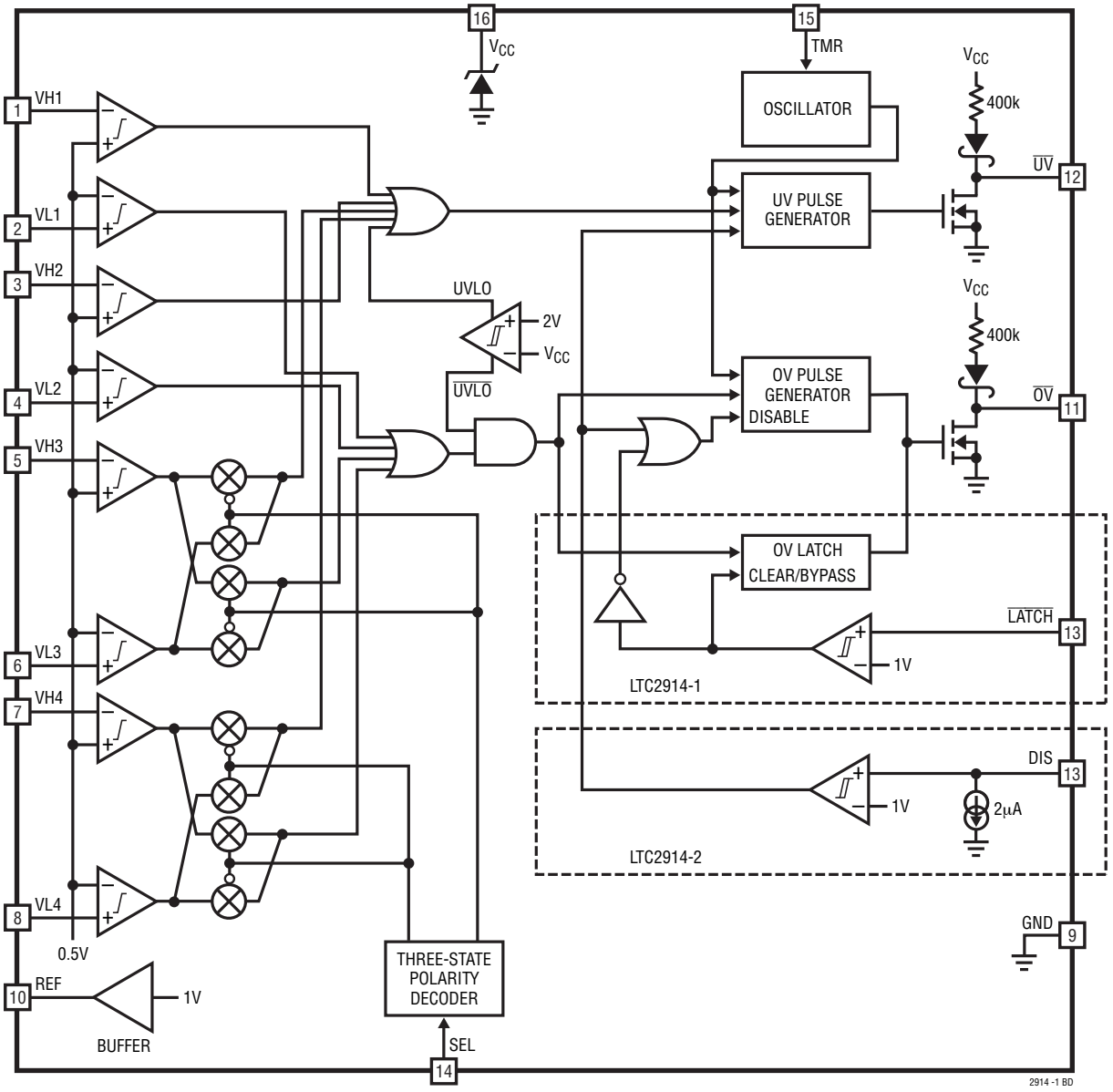
VH1/VH2 (Pin 1/Pin 3): Voltage High Inputs 1 and 2. When the voltage on this pin is below 0.5V, an undervoltage condition is triggered. Tie pin to V_{CC} if unused.

VH3/VH4 (Pin 5/Pin 7): Voltage High Inputs 3 and 4. The polarity of the input is selected by the state of the SEL pin (refer to Table 1). When the monitored input is configured as a positive voltage, an undervoltage condition is triggered when the pin is below 0.5V. When the monitored input is configured as a negative voltage, an overvoltage condition is triggered when the pin is below 0.5V. Tie pin to V_{CC} if unused.

VL1/VL2 (Pin 2/Pin 4): Voltage Low Inputs 1 and 2. When the voltage on this pin is above 0.5V, an overvoltage condition is triggered. Tie pin to GND if unused.

VL3/VL4 (Pin 6/Pin 8): Voltage Low Inputs 3 and 4. The polarity of the input is selected by the state of the SEL pin (refer to Table 1). When the monitored input is configured as a positive voltage, an overvoltage condition is triggered when the pin is above 0.5V. When the monitored input is configured as a negative voltage, an undervoltage condition is triggered when the pin is above 0.5V. Tie pin to GND if unused.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Voltage Monitoring

The LTC2914 is a low power quad voltage monitoring circuit with four undervoltage and four overvoltage inputs. A timeout period that holds $\overline{OV}$ or $\overline{UV}$ asserted after all faults have cleared is adjustable using an external capacitor and is externally disabled.

Each voltage monitor has two inputs (VHn and VLn) for detecting undervoltage and overvoltage conditions. When configured to monitor a positive voltage V_n using the 3-resistor circuit configuration shown in Figure 1, VHn is connected to the high-side tap of the resistive divider and VLn is connected to the low-side tap of the resistive divider. If an input is configured as a negative voltage monitor, the outputs UV_n and OV_n in Figure 1 are swapped internally. V_n is then connected as shown in Figure 2. Note, VHn is still connected to the high-side tap and VLn is still connected to the low-side tap.

Polarity Selection

The three-state polarity-select pin (SEL) selects one of three possible polarity combinations for the input thresholds, as described in Table 1. When an input is configured for negative supply monitoring, VHn is configured to trigger an overvoltage condition and VLn is configured to trigger an undervoltage condition. With this configuration, an OV condition occurs when the supply voltage is more negative than the configured threshold and a UV condition occurs when the voltage is less negative than the configured threshold.

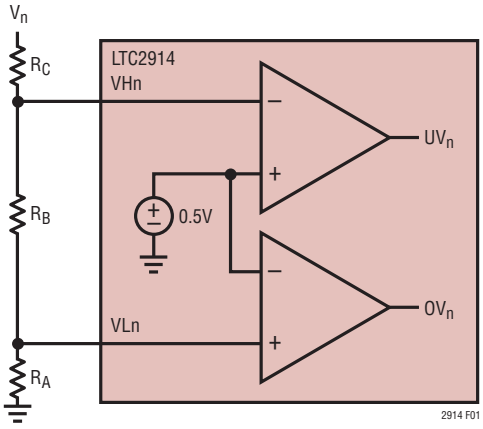


Figure 1. 3-Resistor Positive UV/OV Monitoring Configuration

The three-state input pin SEL is connected to GND, V_{CC} or left unconnected during normal operation. When the pin is left unconnected, the maximum leakage allowed from the pin is ±10µA to ensure it remains in the open state. Table 1 shows the three possible selections of polarity based on the SEL pin connection.

Table 1. Voltage Polarity Programming (V_{UOT} = 0.5V Typical)

SEL	V3 INPUT	V4 INPUT
V_{CC}	Positive VH3 < V_{UOT} → UV VL3 > V_{UOT} → OV	Positive VH4 < V_{UOT} → UV VL4 > V_{UOT} → OV
Open	Positive VH3 < V_{UOT} → UV VL3 > V_{UOT} → OV	Negative VH4 < V_{UOT} → OV VL4 > V_{UOT} → UV
GND	Negative VH3 < V_{UOT} → OV VL3 > V_{UOT} → UV	Negative VH4 < V_{UOT} → OV VL4 > V_{UOT} → UV

3-Step Design Procedure

The following 3-step design procedure allows selecting appropriate resistances to obtain the desired UV and OV trip points for the positive voltage monitor circuit in Figure 1 and the negative voltage monitor circuit in Figure 2. 1% resistor tolerances are suggested to maintain the ±1.5% threshold accuracy.

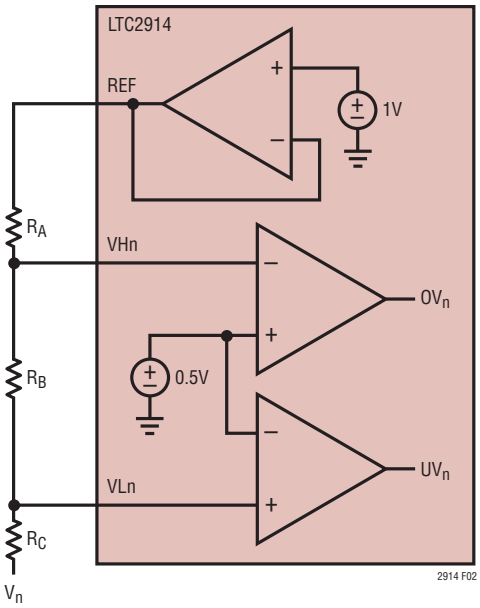


Figure 2. 3-Resistor Negative UV/OV Monitoring Configuration

APPLICATIONS INFORMATION

For positive supply monitoring, V_n is the desired nominal operating voltage, I_{nd} is the desired nominal current through the resistive divider, I_{na} is the resistive divider current calculated using the 1% resistor R_A. V_{OV} is the desired overvoltage trip point and V_{UV} is the desired undervoltage trip point.

For negative supply monitoring, to compensate for the 1V reference, 1V must be subtracted from V_n, V_{OV} and V_{UV} before using each in the following equations.

1A. Choose R_A to obtain the desired OV trip point

R_A is chosen to set the desired trip point for the overvoltage monitor.

$$R_A = \left| \frac{0.5V}{I_n} \bullet \frac{V_n}{V_{OV}} \right| \quad (1)$$

1B. Calculate I_{na}

$$I_{na} = \left| \frac{0.5V}{R_A} \bullet \frac{V_n}{V_{OV}} \right|$$

2. Choose R_B to obtain the desired UV trip point

Once R_A is known, R_B is chosen to set the desired trip point for the undervoltage monitor.

$$R_B = \left| \frac{0.5V}{I_{na}} \bullet \frac{V_n}{V_{UV}} \right| - R_A \quad (2)$$

3. Choose R_C to Complete the Design

Once R_A and R_B are known, R_C is determined by:

$$R_C = \left| \frac{V_n}{I_{na}} \right| - R_A - R_B \quad (3)$$

If any of the variables V_n, I_{na}, I_{nd}, V_{UV} or V_{OV} change, then each step must be recalculated.

Positive Voltage Monitor Example

A positive voltage monitor application is shown in Figure 3. The monitored voltage is a 5V ±10% supply. Nominal current in the resistive divider is 10µA.

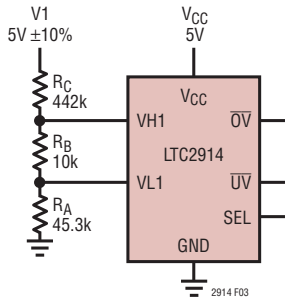


Figure 3. Positive Supply Monitor

1A. Find R_A to set the OV trip point of the monitor.

$$R_A = \left| \frac{0.5V}{10\mu A} \bullet \frac{5V}{5.5V} \right| \approx 45.3k$$

1B. Calculate I_{na}

$$I_{na} = \left| \frac{0.5V}{45.3k} \bullet \frac{5V}{5.5V} \right| = 10.034\mu A$$

2. Find R_B to set the UV trip point of the monitor.

$$R_B = \left| \frac{0.5V}{10.034\mu A} \bullet \frac{5V}{4.5V} \right| - 45.3k \cong 10k$$

3. Determine R_C to complete the design.

$$R_C = \left| \frac{5V}{10.034\mu A} \right| - 45.3k - 10k \approx 442k$$

Negative Voltage Monitor Example 1

A negative voltage monitor application is shown in Figure 4. The monitored voltage is a –5V ±10% supply. Nominal current in the resistive divider is 10µA. For the negative case, 1V is subtracted from V_n, V_{OV} and V_{UV}.

1A. Find R_A to set the OV trip point of the monitor.

$$R_A = \left| \frac{0.5V}{10\mu A} \bullet \frac{-5V-1V}{-5.5V-1V} \right| \approx 46.4k$$

1B. Calculate I_{na}

$$I_{no} \bullet \left| \frac{0.5V}{46.4k} \bullet \frac{-5V-1V}{-5.5V-1V} \right| = 9.947\mu A$$

2. Find R_B to set the UV trip point of the monitor.

$$R_B = \left| \frac{0.5V}{9.947\mu A} \bullet \frac{-5V-1V}{-4.5V-1V} \right| - 46.4k \cong 8.45k$$

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3. *Determine R_C to complete the design.*

$$R_C = \left|\frac{-5V-1V}{9.947\mu A}\right| - 46.4k - 8.45k \approx 549k$$

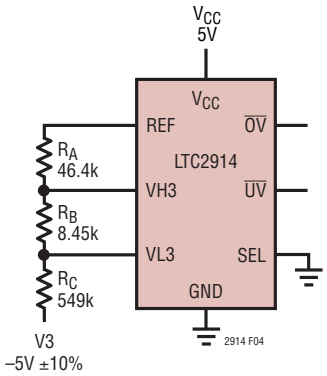

Figure 4. Negative Supply Monitor

Negative Voltage Monitoring Example 2

Negative voltage monitoring applications with wide operating voltage ranges such that:

$$|2 \bullet V_{UV}| < |V_{OV}|$$

create situations where the VH or VL pins exceeds the –0.3V absolute maximum voltage ratings. To ensure that the LTC2914 operates within its design specifications, utilize the equations shown below to determine proper resistor sizing for the circuit in Figure 5. In the following example, the undervoltage trip point is –6V. The overvoltage trip point is –30V.

1A. Find R_{AUV} and R_{BUV} and let node A be a virtual ground, which ensures that the diode current will not affect the voltage monitor threshold accuracy. Let the resistive divider current I_{nd} = 10µA.

$$R_{AUV} = \left|\frac{V_{REF}-0.5V}{I_{nd}}\right| = \left|\frac{1V-0.5V}{10\mu A}\right| \approx 49.9k$$

$$R_{AUV} = R_{BUV}$$

1B. Calculate I_{na} using the resistor values chosen above.

$$I_{na} = \left|\frac{V_{REF}-0.5V}{R_{AUV}}\right| = \left|\frac{1V-0.5V}{R_{AUV}}\right| \approx 10.020\mu A$$

2. Calculate R_{CUV} based on the desired undervoltage trip point of –6V.

$$R_{CUV} = (R_{AUV} + R_{BUV}) \bullet \left|\frac{V_{UV}}{V_{REF}}\right| =$$

$$(49.9k + 49.9k) \bullet \left|\frac{-6V-1V}{1V}\right| \approx 698k$$

3. Calculate R_{AOV} and I_{na}

$$R_{AOV} = \left|\frac{V_{REF}-0.5V}{I_{nd}}\right| = \left|\frac{1V-0.5V}{10\mu A}\right| \approx 49.9k$$

$$I_{na} \approx 10.020\mu A$$

4. Calculate R_{BOV} for a desired overvoltage trip point of –30V.

$$R_{BOV} = \left|\frac{0.5V-V_{OV}}{I_{na}}\right| = \left|\frac{0.5V-30-1}{10.020\mu A}\right| \approx 3.01M$$

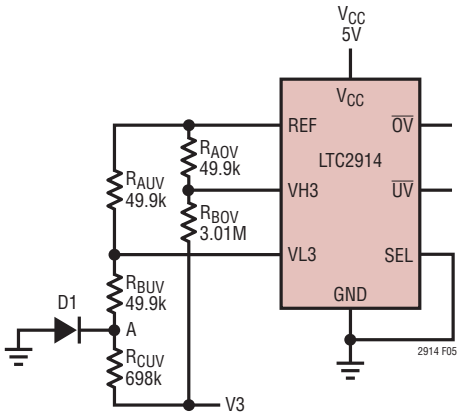

Figure 5. Negative Supply Monitor for Wide Operating Range

Power-Up/Power-Down

As soon as V_{CC} reaches 1V during power-up, the $\overline{UV}$ output asserts low and the $\overline{OV}$ output weakly pulls to V_{CC}.

The LTC2914 is guaranteed to assert $\overline{UV}$ low and $\overline{OV}$ high under conditions of low V_{CC}, down to V_{CC} = 1V. Above V_{CC} = 2V (2.1V maximum) the VH and VL inputs take control.

Once all VH inputs and V_{CC} become valid an internal timer is started. After an adjustable delay time, $\overline{UV}$ weakly pulls high.

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Threshold Accuracy

Reset threshold accuracy is important in a supply-sensitive system. Ideally, such a system resets only if supply voltages fall outside the exact thresholds for a specified margin. All LTC2914 inputs have a relative threshold accuracy of ±1.5% over the full operating temperature range.

For example, when the LTC2914 is programmed to monitor a 5V input with a 10% tolerance, the desired UV trip point is 4.5V. Because of the ±1.5% relative accuracy of the LTC2914, the UV trip point is between 4.433V and 4.567V which is 4.5V ±1.5%.

Likewise, the accuracy of the resistances chosen for R_A, R_B and R_C affect the UV and OV trip points as well. Using the example just given, if the resistances used to set the UV trip point have 1% accuracy, the UV trip range is between 4.354V and 4.650V. This is illustrated in the following calculations.

The UV trip point is given as:

$$V_{UV} = 0.5V\left(1+\frac{R_C}{R_A+R_B}\right)$$

The two extreme conditions, with a relative accuracy of 1.5% and resistance accuracy of 1%, result in:

$$V_{UV(MIN)} = 0.5V \bullet 0.985 \bullet \left(1+\frac{R_C \bullet 0.99}{(R_A+R_B)\bullet 1.01}\right)$$

and

$$V_{UV(MAX)} = 0.5V \bullet 1.015 \bullet \left(1+\frac{R_C \bullet 1.01}{(R_A+R_B)\bullet 0.99}\right)$$

For a desired trip point of 4.5V, $\frac{R_C}{R_A+R_B} = 8$

Therefore,

$$V_{UV(MIN)} = 0.5V \bullet 0.985 \bullet \left(1+8\bullet\frac{0.99}{1.01}\right) = 4.354V$$

and

$$V_{UV(MAX)} = 0.5V \bullet 1.015 \bullet \left(1+8\bullet\frac{1.01}{0.99}\right) = 4.650V$$

Glitch Immunity

In any supervisory application, noise riding on the monitored DC voltage causes spurious resets. To solve this problem without adding hysteresis, which causes a new error term in the trip voltage, the LTC2914 lowpass filters the output of the first stage comparator at each input. This filter integrates the output of the comparator before asserting the UV or OV logic. A transient at the input of the comparator of sufficient magnitude and duration triggers the output logic. The Typical Performance Characteristics section shows a graph of the Transient Duration vs Comparator Overdrive.

UV/OV Timing

The LTC2914 has an adjustable timeout period (t_{UOTO}) that holds $\overline{OV}$ or $\overline{UV}$ asserted after all faults have cleared. This assures a minimum reset pulse width allowing a settling time delay for the monitored voltage after it has entered the valid region of operation.

When any VH input drops below its designed threshold, the $\overline{UV}$ pin asserts low. When all inputs recover above their designed thresholds, the UV output timer starts. If all inputs remain above their designed thresholds when the timer finishes, the $\overline{UV}$ pin weakly pulls high. However, if any input falls below its designed threshold during this time-out period, the timer resets and restarts when all inputs are above the designed thresholds. The $\overline{OV}$ output behaves as the $\overline{UV}$ output when $\overline{LATCH}$ is high (LTC2914-1).

Selecting the UV/OV Timing Capacitor

The UV and OV timeout period (t_{UOTO}) for the LTC2914 is adjustable to accommodate a variety of applications. Connecting a capacitor, C_{TMR}, between the TMR pin and ground sets the timeout period. The value of capacitor needed for a particular timeout period is:

$$C_{TMR} = t_{UOTO} \bullet 115 \bullet 10^{-9}\ (F/s)$$

The Reset Timeout Period vs Capacitance graph found in the Typical Performance Characteristics shows the desired delay time as a function of the value of the timer capacitor that must be used. The TMR pin must have a minimum of 10pF or be tied to V_{CC}. For long timeout periods, the only limitation is the availability of a large value capacitor with

APPLICATIONS INFORMATION

low leakage. Capacitor leakage current must not exceed the minimum TMR charging current of 1.3µA. Tying the TMR pin to V_{CC} bypasses the timeout period.

Undervoltage Lockout

When V_{CC} falls below 2V, the LTC2914 asserts an undervoltage lockout (UVLO) condition. During UVLO, $\overline{UV}$ is asserted and pulled low while $\overline{OV}$ is cleared and blocked from asserting. When V_{CC} rises above 2V, $\overline{UV}$ follows the same timing procedure as an undervoltage condition on any input.

Shunt Regulator

The LTC2914 has an internal shunt regulator. The V_{CC} pin operates as a direct supply input for voltages up to 6V. Under this condition, the quiescent current of the device remains below a maximum of 100µA. For V_{CC} voltages higher than 6V, the device operates as a shunt regulator and must have a resistance R_Z between the supply and the V_{CC} pin to limit the current to no greater than 10mA.

When choosing this resistance value, choose an appropriate location on the I-V curve shown in the Typical Performance Characteristics section to accommodate variations in V_{CC} due to changes in current through R_Z.

$\overline{UV}$ and $\overline{OV}$ Output Characteristics

The DC characteristics of the $\overline{UV}$ and $\overline{OV}$ pull-up and pull-down strength are shown in the Typical Performance Characteristics section. Each pin has a weak internal pull-up to V_{CC} and a strong pull-down to ground. This arrangement allows these pins to have open-drain behavior while possessing several other beneficial characteristics. The weak pull-up eliminates the need for an external pull-up resistor when the rise time on the pin is not critical. On the other hand, the open-drain configuration allows for wired-OR connections and is useful when more than one signal needs to pull down on the output. V_{CC} of 1V guarantees a maximum V_{OL} = 0.15V at $\overline{UV}$.

At V_{CC} = 1V, the weak pull-up current on $\overline{OV}$ is barely turned on. Therefore, an external pull-up resistor of no more than 100k is recommended on the $\overline{OV}$ pin if the state and pull-up strength of the $\overline{OV}$ pin is crucial at very low V_{CC}.

Note however, by adding an external pull-up resistor, the pull-up strength on the $\overline{OV}$ pin is increased. Therefore, if it is connected in a wired-OR connection, the pull-down strength of any single device must accommodate this additional pull-up strength.

Output Rise and Fall Time Estimation

The $\overline{UV}$ and $\overline{OV}$ outputs have strong pull-down capability. The following formula estimates the output fall time (90% to 10%) for a particular external load capacitance (C_{LOAD}):

$$t_{FALL} \approx 2.2 \bullet R_{PD} \bullet C_{LOAD}$$

where R_{PD} is the on-resistance of the internal pull-down transistor, typically 50Ω at V_{CC} > 1V and at room temperature (25°C). C_{LOAD} is the external load capacitance on the pin. Assuming a 150pF load capacitance, the fall time is 16.5ns.

The rise time on the $\overline{UV}$ and $\overline{OV}$ pins is limited by a 400k pull-up resistance to V_{CC}. A similar formula estimates the output rise time (10% to 90%) at the $\overline{UV}$ and $\overline{OV}$ pins:

$$t_{RISE} \approx 2.2 \bullet R_{PU} \bullet C_{LOAD}$$

where R_{PU} is the pull-up resistance.

$\overline{OV}$ Latch (LTC2914-1)

With the $\overline{LATCH}$ pin held low, the $\overline{OV}$ pin latches low when an OV condition is detected. The latch is cleared by raising the $\overline{LATCH}$ pin high. If an $\overline{OV}$ condition changes while $\overline{LATCH}$ is held high, the latch is bypassed and the $\overline{OV}$ pin behaves the same as the UV pin with a similar timeout period at the output. If $\overline{LATCH}$ is pulled low while the timeout period is active, the $\overline{OV}$ pin latches as before.

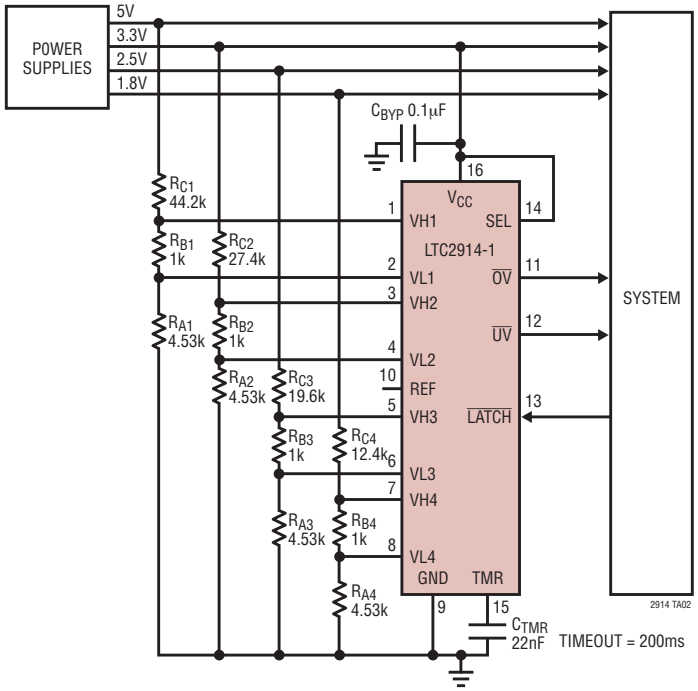
Disable (LTC2914-2)

The LTC2914-2 allows disabling the $\overline{UV}$ and $\overline{OV}$ outputs via the DIS pin. Pulling DIS high forces both outputs to remain weakly pulled high, regardless of any faults that occur on the inputs. However, if a UVLO condition occurs, $\overline{UV}$ asserts and pulls low, but the timeout function is bypassed. $\overline{UV}$ pulls high as soon as the UVLO condition is cleared.

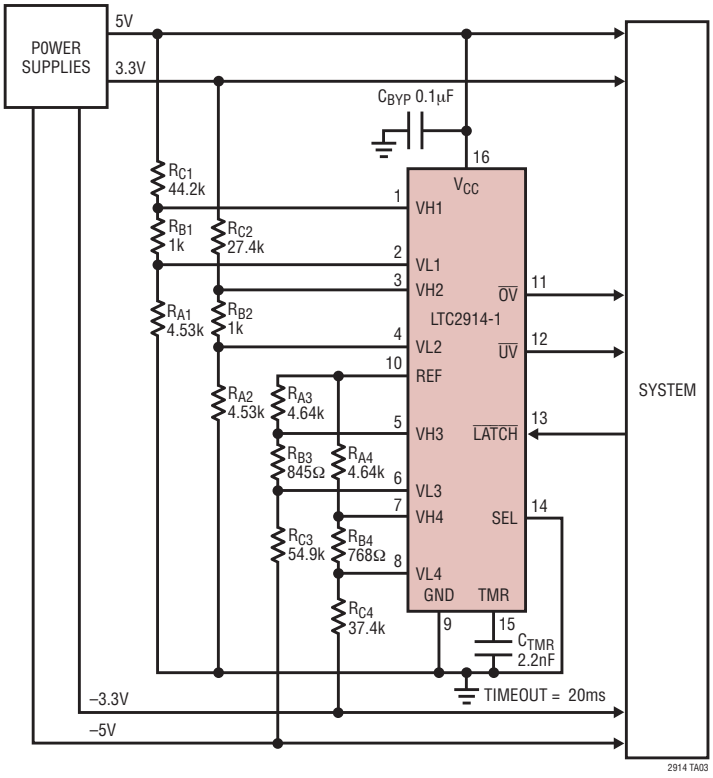
DIS has a weak 2µA (typical) internal pull-down current guaranteeing normal operation with the pin left open.

TYPICAL APPLICATIONS

Quad UV/OV Supply Monitor, 10% Tolerance, 5V, 3.3V, 2.5V, 1.8V

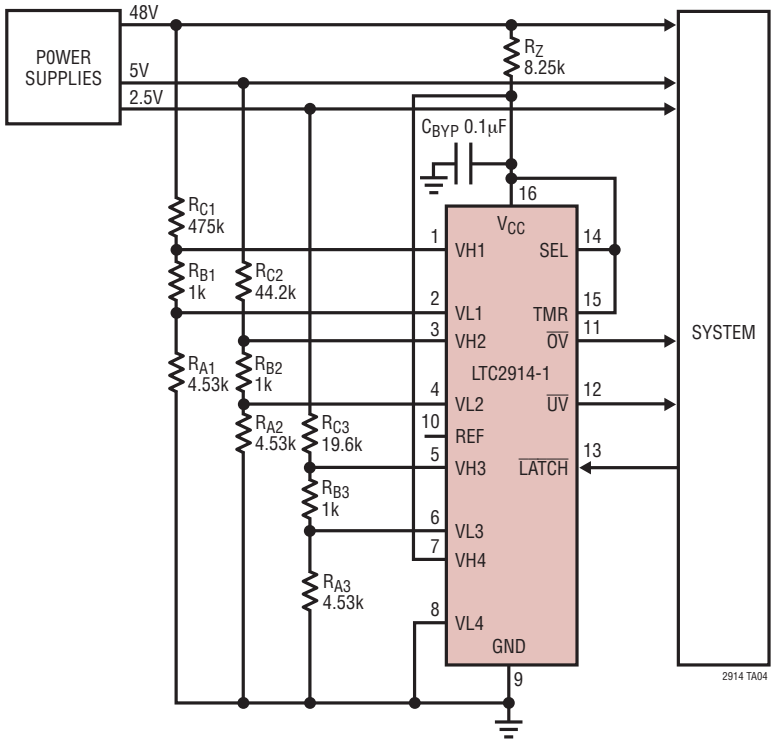


Dual Positive and Dual Negative UV/OV Supply Monitor, 10% Tolerance, 5V, 3.3V, –5V, –3.3V



TYPICAL APPLICATIONS

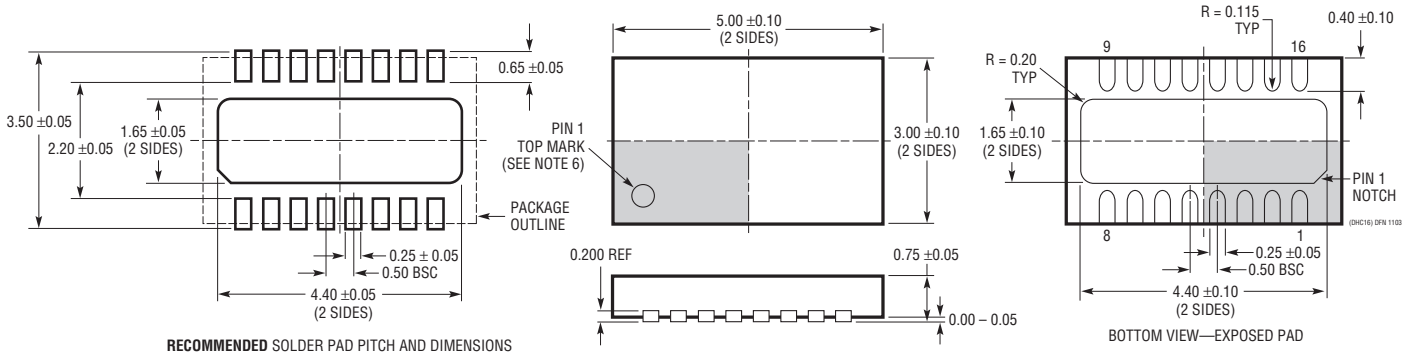
Triple UV/OV Supply Monitor Powered from 48V, 10% Tolerance, 48V, 5V, 2.5V



PACKAGE DESCRIPTION

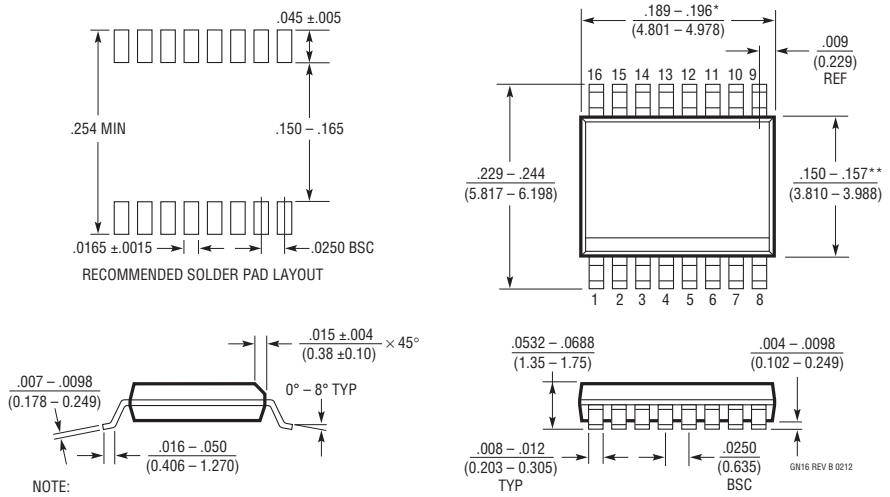
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev Ø)



NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

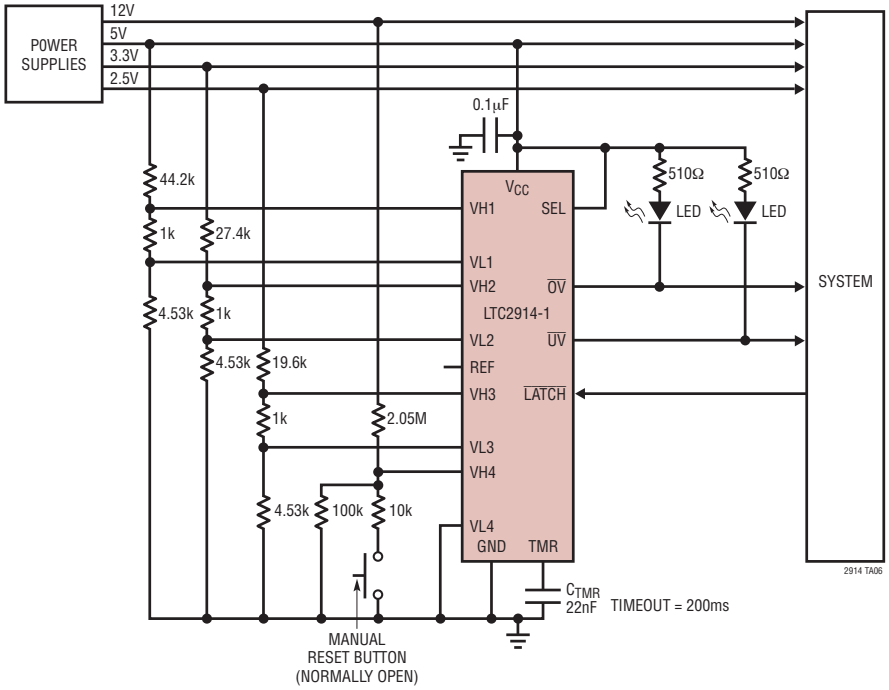
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	10/10	Added t_{PW} and Note 4 to Electrical Characteristics section	4
		Updated equations and added Negative Voltage Monitoring Example 2 to Applications Information section	9-13
C	12/13	Corrected LATCH/DIS label in Pin Configuration section	2

TYPICAL APPLICATION

Quad UV/OV Supply Monitor with LED Undervoltage and Overvoltage Indicator and Manual Undervoltage Reset Button, 10% Tolerance, 12V, 5V, 3.3V, 2.5V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1326/ LTC1326-2.5	Micropower Precision Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%)
LTC1726-2.5/ LTC1726-5	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable $\overline{\text{RESET}}$ and Watchdog Time-Outs
LTC1727-2.5/ LTC1727-5	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728-1.8/ LTC1728-3.3	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1728-2.5/ LTC1728-5	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1985-1.8	Micropower Triple Supply Monitor with Push-Pull Reset	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable RESET, 10-Lead MSOP and 3mm × 3mm 10-Lead DFN Package
LTC2901	Programmable Quad Supply Monitor	Adjustable RESET and Watchdog Timer, 16-Lead SSOP Package
LTC2902	Programmable Quad Supply Monitor	Adjustable RESET and Tolerance, 16-Lead SSOP Package, Margining Functions
LTC2903	Precision Quad Supply Monitor	6-Lead SOT-23 Package, Ultralow Voltage Reset
LTC2904	Three-State Programmable Precision Dual Supply Monitor	Adjustable Tolerance, 8-Lead SOT-23 Package
LTC2905	Three-State Programmable Precision Dual Supply Monitor	Adjustable RESET and Tolerance, 8-Lead SOT-23 Package
LTC2906	Precision Dual Supply Monitor 1 Selectable and 1 Adjustable	Separate V_{CC} Pin, RST/$\overline{\text{RST}}$ Outputs
LTC2907	Precision Dual Supply Monitor 1 Selectable and 1 Adjustable	Separate V_{CC}, Adjustable Reset Timer
LTC2908	Precision Six Supply Monitor	8-Lead TSOT-23 and 3mm × 2mm DFN Packages
LTC2909	Precision Dual Input UV, OV and Negative Voltage Monitor	Separate V_{CC} Pin, Adjustable Reset Timer, 8-Lead TSOT-23 and 3mm × 2mm DFN Packages

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