ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to AGNDF, AGNDS .... −0.3V to 7V
V_{CC} to DGND .... −0.3V to 7V
Total Supply Voltage (V$^+$ to V$^−$) 36V
AGNDF, AGNDS to DGND .... V_{CC} + 0.3V
DGND to AGNDF, AGNDS .... V_{CC} + 0.3V
REF, R_{COM} to AGNDF, AGNDS, DGND .... ±15V
R_{OFS}, R_{FB}, R1, to AGNDF, AGNDS, DGND .... ±15V
Digital Inputs to DGND .... −0.3V to (V_{CC} + 0.3V)
I_{OUT} to AGNDF, AGNDS.............. −0.3V to (V_{CC} + 0.3V)
Maximum Junction Temperature .... 150°C
Operating Temperature Range
    LTC1821C/LTC1821-1C .... 0°C to 70°C
    LTC1821I/LTC1821-1I .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)................. 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

DGND	1		36	D4
V_{CC}	2		35	D5
D3	3		34	D6
D2	4		33	D7
D1	5		32	D8
D0	6		31	D9
$\overline{CLR}$	7		30	D10
REF	8		29	D11
R_{COM}	9		28	D12
R1	10		27	D13
R_{OFS}	11		26	D14
R_{FB}	12		25	D15
V_{OUT}	13		24	WR
I_{OUT}	14		23	LD
V$^+$	15		22	NC
AGNDS	16		21	DNC*
AGNDF	17		20	V$^−$
DNC*	18		19	DNC*

GW PACKAGE
36-LEAD PLASTIC SSOP WIDE
T_{JMAX} = 125°C, θ_{JA} = 80°C/W
*DO NOT CONNECT

ORDER PART NUMBER

LTC1821ACGW
LTC1821BCGW
LTC1821-1ACGW
LTC1821-1BCGW
LTC1821AIGW
LTC1821BIGW
LTC1821-1AIGW
LTC1821-1BIGW

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = T_{MIN} to T_{MAX}, V$^+$ = 15V, V$^−$ = −15V, V_{CC} = 5V, V_{REF} = 10V, AGNDF = AGNDS = DGND = 0V.

SYMBOL	PARAMETER	CONDITIONS		LTC1821B/-1B MIN	TYP	MAX	LTC1821A/-1A MIN	TYP	MAX	UNITS
Accuracy										
	Resolution		●	16			16			Bits
	Monotonicity		●	16			16			Bits
INL	Integral Nonlinearity	T_A = 25°C (Note 2)				±2		±0.25	±1	LSB
		T_{MIN} to T_{MAX}	●			±2		±0.35	±1	LSB
DNL	Differential Nonlinearity	T_A = 25°C				±1		±0.2	±1	LSB
		T_{MIN} to T_{MAX}	●			±1		±0.2	±1	LSB
GE	Gain Error	Unipolar Mode T_A = 25°C (Note 3)				±16		±5	±16	LSB
		T_{MIN} to T_{MAX}	●			±24		±8	±16	LSB
		Bipolar Mode T_A = 25°C (Note 3)				±16		±2	±16	LSB
		T_{MIN} to T_{MAX}	●			±24		±5	±16	LSB
	Gain Temperature Coefficient	ΔGain/ΔTemperature (Note 4)	●		1	3		1	3	ppm/°C
	Unipolar Zero-Scale Error	T_A = 25°C				±3		±0.25	±2	LSB
		T_{MIN} to T_{MAX}	●			±6		±0.50	±4	LSB
	Bipolar Zero Error	T_A = 25°C				±12		±2	±8	LSB
		T_{MIN} to T_{MAX}	●			±16		±3	±10	LSB
PSRR	Power Supply Rejection Ratio	V_{CC} = 5V ±10%	●			2		0.7	2	LSB/V
		V$^+$, V$^−$ = ±4.5V to ±16.5V				±2		±0.1	±2	LSB/V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = T_{MIN}$ to T_{MAX}, $V^+ = 15V$, $V^- = -15V$, $V_{CC} = 5V$, $V_{REF} = 10V$, AGNDF = AGNDS = DGND = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
R_{REF}	DAC Input Resistance (Unipolar)	(Note 6)	●	4.5	6	10	kΩ
R1/R2	R1/R2 Resistance (Bipolar)	(Notes 6, 11)	●	9	12	20	kΩ
R_{OFS}, R_{FB}	Feedback and Offset Resistances	(Note 6)	●	9	12	20	kΩ
AC Performance (Note 4)							
	Output Voltage Settling Time	$\Delta V_{OUT} = 10V$ (Notes 7, 8)			2		µs
	Midscale Glitch Impulse	(Note 10)			2		nV•s
	Digital-Feedthrough	(Note 9)			2		nV•s
	Multiplying Feedthrough Error	$V_{REF} = \pm10V$, 10kHz Sine Wave (Note 7)			1		mV$_{P-P}$
	Multiplying Bandwidth	Code = Full Scale (Note 7)			600		kHz
	Output Noise Voltage Density	1kHz to 100kHz (Note 7) Code = Zero Scale Code = Full Scale			13 20		nV/√Hz nV/√Hz
	Output Noise Voltage	0.1Hz to 10Hz (Note 7) Code = Zero Scale Code = Full Scale			0.45 1		µV$_{RMS}$ µV$_{RMS}$
	1/f Noise Corner	(Note 7)			30		Hz
Analog Outputs (Note 4)							
V_{OUT}	DAC Output Swing	$R_L = 2k$, $V^+ = 15V$, $V^- = -15V$ $R_L = 2k$, $V^+ = 5V$, $V^- = -5V$	● ●	±12.6 ±2.6			V V
	DAC Output Load Regulation	$V^+ = 15V$, $V^- = -15V$, ±5mA Load	●		0.02	0.2	LSB/mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V^+ = 15V$, $V^- = -15V$	●	12	40		mA
SR	Slew Rate	$R_L = 2k$, $V^+ = 15V$, $V^- = -15V$ $R_L = 2k$, $V^+ = 5V$, $V^- = -5V$			20 14		V/µs V/µs
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 4) $V_{IN} = 0V$	●			8	pF
Timing Characteristics							
t_{DS}	Data to $\overline{WR}$ Setup Time		●	60	20		ns
t_{DH}	Data to $\overline{WR}$ Hold Time		●	0	−12		ns
$t_{\overline{WR}}$	$\overline{WR}$ Pulse Width		●	60	25		ns
t_{LD}	LD Pulse Width		●	110	55		ns
$t_{\overline{CLR}}$	Clear Pulse Width		●	60	40		ns
t_{LWD}	$\overline{WR}$ to LD Delay Time		●	0			ns
Power Supply							
I_{CC}	Supply Current, V_{CC}	Digital Inputs = 0V or V_{CC}	●		1.5	10	µA
I_S	Supply Current, V^+, V^-	±15V ±5V	● ●		4.5 4.0	7.0 6.8	mA mA
V_{CC}	Supply Voltage		●	4.5	5	5.5	V
V^+	Supply Voltage		●	4.5		16.5	V
V^-	Supply Voltage		●	−16.5		−4.5	V

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: ± 1LSB = $\pm 0.0015\%$ of full scale = ± 15.3ppm of full scale.

Note 3: Using internal feedback resistor.

Note 4: Guaranteed by design, not subject to test.

Note 5: I_{OUT} with DAC register loaded to all 0s.

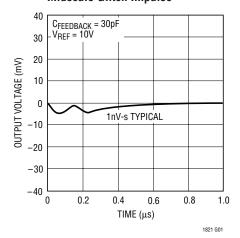**Note 6:** Typical temperature coefficient is 100ppm/°C.

Note 7: Measured in unipolar mode.

Note 8: To 0.0015% for a full-scale change, measured from the rising edge of LD.

Note 9: REF = 0V. DAC register contents changed from all 0s to all 1s or all 1s to all 0s. LD low and $\overline{WR}$ high.

Note 10: Midscale transition code: 0111 1111 1111 1111 to 1000 0000 0000 0000. Unipolar mode, $C_{FEEDBACK}$ = 33pF.
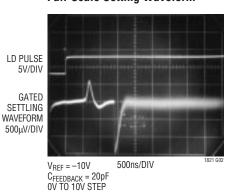
Note 11: R1 and R2 are measured between R1 and R_{COM}, REF and R_{COM}.

TYPICAL PERFORMANCE CHARACTERISTICS

Midscale Glitch Impulse

1821 G01
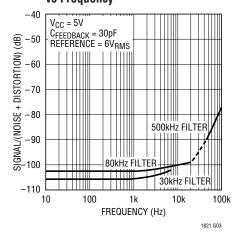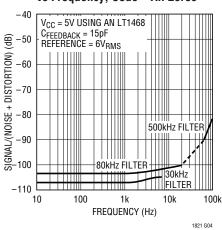
Full-Scale Setting Waveform
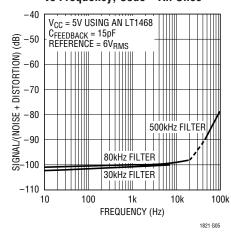
V_{REF} = –10V
$C_{FEEDBACK}$ = 20pF
0V TO 10V STEP

Unipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency
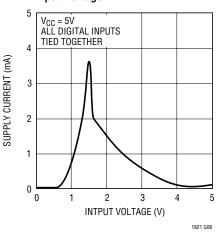

1821 G03

Bipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency, Code = All Zeros

1821 G04

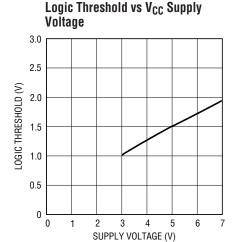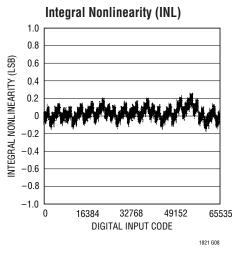**Bipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency, Code = All Ones**

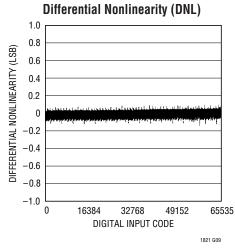1821 G05

V_{CC} Supply Current vs Digital Input Voltage

1821 G06

4

TYPICAL PERFORMANCE CHARACTERISTICS

Logic Threshold vs V_CC Supply Voltage

1821 G07

Integral Nonlinearity (INL)
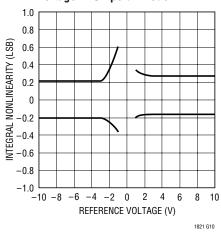

1821 G08

Differential Nonlinearity (DNL)

1821 G09

Integral Nonlinearity vs Reference Voltage in Unipolar Mode
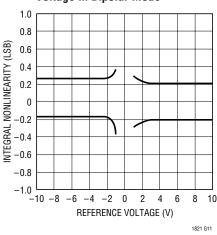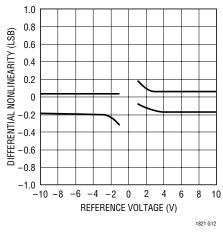

1821 G10

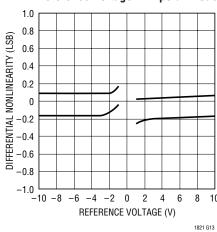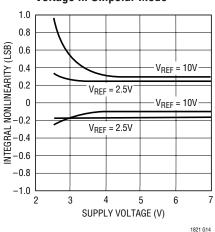**Integral Nonlinearity vs Reference Voltage in Bipolar Mode**

1821 G11

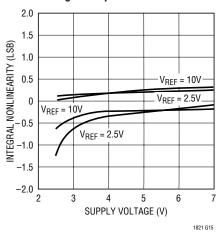**Differential Nonlinearity vs Reference Voltage in Unipolar Mode**

1821 G12

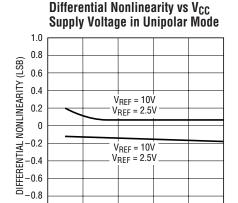**Differential Nonlinearity vs Reference Voltage in Bipolar Mode**

1821 G13

Integral Nonlinearity vs V_CC Supply Voltage in Unipolar Mode

1821 G14

Integral Nonlinearity vs V_CC Supply Voltage in Bipolar Mode

1821 G15

5

TYPICAL PERFORMANCE CHARACTERISTICS

Differential Nonlinearity vs V_{CC} Supply Voltage in Unipolar Mode

Differential Nonlinearity vs V_{CC} Supply Voltage in Unipolar Mode

Differential Nonlinearity vs V_{CC} Supply Voltage in Bipolar Mode

$V_{REF} = 10V$
$V_{REF} = 2.5V$
$V_{REF} = 10V$
$V_{REF} = 2.5V$

DIFFERENTIAL NONLINEARITY (LSB)
SUPPLY VOLTAGE (V)

1821 G16

$V_{REF} = 10V$
$V_{REF} = 2.5V$
$V_{REF} = 10V$
$V_{REF} = 2.5V$

DIFFERENTIAL NONLINEARITY (LSB)
SUPPLY VOLTAGE (V)

1821 G17

Unipolar Multiplying Mode Frequency Response vs Digital Code

ALL BITS ON
D15 ON
D14 ON
D13 ON
D12 ON
D11 ON
D10 ON
D9 ON
D8 ON
D7 ON
D6 ON
D5 ON
D4 ON
D3 ON
D2 ON
D1 ON
D0 ON
ALL BITS OFF

ATTENUATION (dB)
FREQUENCY (Hz)

1821 G18

Bipolar Multiplying Mode Frequency Response vs Digital Code

ALL BITS ON
D15 AND D14 ON
D15 AND D13 ON
D15 AND D12 ON
D15 AND D11 ON
D15 AND D10 ON
D15 AND D9 ON
D15 AND D8 ON
D15 AND D7 ON
D15 AND D6 ON
D15 AND D5 ON
D15 AND D4 ON
D15 AND D3 ON
D15 AND D2 ON
D15 AND D1 ON
D15 AND D0 ON
D15 ON*

CODES FROM MIDSCALE TO FULL SCALE

ATTENUATION (dB)
FREQUENCY (Hz)

1821 G19

*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO −96dB TYPICAL (−78dB MAX, A GRADE)

Bipolar Multiplying Mode Frequency Response vs Digital Code

ALL BITS OFF
D14 ON
D14 AND D13 ON
D14 TO D12 ON
D14 TO D11 ON
D14 TO D10 ON
D14 TO D9 ON
D14 TO D8 ON
D14 TO D7 ON
D14 TO D6 ON
D14 TO D5 ON
D14 TO D4 ON
D14 TO D3 ON
D14 TO D2 ON
D14 TO D1 ON
D14 TO D0 ON
D15 ON*

CODES FROM MIDSCALE TO ZERO SCALE

ATTENUATION (dB)
FREQUENCY (Hz)

1821 G20

*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO −96dB TYPICAL (−78dB MAX, A GRADE)

V_{REF}
30pF
8 9 10 11 12
14
13
LTC1821
1 16 17
V_{OUT}

V_{REF}
3
LT1468
6
2
12pF
12pF
15pF
10
9
8 11 12
14
13
LTC1821
1 16 17
V_{OUT}

V_{REF}
3
LT1468
6
2
12pF
12pF
15pF
10
9
8 11 12
14
13
LTC1821
1 16 17
V_{OUT}

PIN FUNCTIONS

DGND (Pin 1): Digital Ground. Connect to analog ground.

V_{CC} (Pin 2): Positive Supply Input. $4.5V \leq V_{CC} \geq 5.5V$. Requires a bypass capacitor to ground.

D3 (Pin 3): Digital Input Data Bit 3.

D2 (Pin 4): Digital Input Data Bit 2.

D1 (Pin 5): Digital Input Data Bit 1.

D0 (Pin 6): LSB or Digital Input Data Bit 0.

$\overline{CLR}$ (Pin 7): Digital Clear Control Function for the DAC. When $\overline{CLR}$ is taken to a logic low, it sets the DAC output and all internal registers to: zero code for the LTC1821 and midscale code for the LTC1821-1.

REF (Pin 8): Reference Input and 4-Quadrant Resistor R2. Typically ±10V, accepts up to ±15V. In 2-quadrant mode, tie this pin to the external reference signal. In 4-quadrant mode, this pin is driven by external inverting reference amplifier.

R_{COM} (Pin 9): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation. Otherwise this pin is shorted to the REF pin. See Figures 1 and 2.

R1 (Pin 10): 4-Quadrant Resistor R1. In 2-quadrant operation, short this pin to the REF pin. In 4-quadrant mode, tie this pin to the external reference signal.

R_{OFS} (Pin 11): Bipolar Offset Resistor. Typically swings ±10V, accepts up to ±15V. For 2-quadrant operation, tie this pin to R_{FB} and for 4-quadrant operation, tie this pin to R1.

R_{FB} (Pin12): Feedback Resistor. Normally connected to V_{OUT}. Typically swings ±10V. The voltage at this pin swings 0 to V_{REF} in unipolar mode and ±V_{REF} in bipolar mode.

V_{OUT} (Pin 13): DAC Voltage Output. Normally connected to R_{FB} and to I_{OUT} through a 22pF feedback capacitor in unipolar mode (15pF in bipolar mode). Typically swings ±10V.

I_{OUT} (Pin 14): DAC Current Output. Normally tied through a 22pF feedback capacitor in unipolar mode (15pF in bipolar mode) to V_{OUT}.

V^+ (Pin 15): Amplifier Positive Supply. Range is 4.5V to 16.5V.

AGNDS (Pin 16): Analog Ground Sense. Connect to analog ground.

AGNDF (Pin 17): Analog Ground Force. Connect to analog ground.

DNC (Pin 18, 19, 21): Connected internally. Do not connect external circuitry to these pins.

V^- (Pin 20): Amplifier Negative Supply. Range is −4.5V to −16.5V.

NC (Pin 22): No Connection.

LD (Pin 23): DAC Digital Input Load Control Input. When LD is taken to a logic high, data is loaded from the input register into the DAC register, updating the DAC output.

$\overline{WR}$ (Pin 24): DAC Digital Write Control Input. When $\overline{WR}$ is taken to a logic low, data is written from the digital input pins into the 16-bit wide input reigster.

D15 (Pins 25): MSB or Digital Input Data Bit 15.

D14 (Pin 26): Digital Input Data Bit 14.

D13 (Pin 27): Digital Input Data Bit 13.

D12 (Pin 28): Digital Input Data Bit 12.

D11 (Pin 29): Digital Input Data Bit 11.

D10 (Pin 30): Digital Input Data Bit 10.

D9 (Pin 31): Digital Input Data Bit 9.

D8 (Pin 32): Digital Input Data Bit 8.

D7 (Pin 33): Digital Input Data Bit 7.

D6 (Pin 34): Digital Input Data Bit 6.

D5 (Pin 35): Digital Input Data Bit 5.
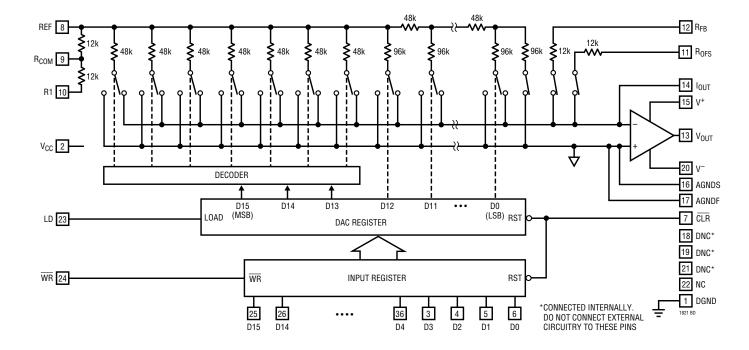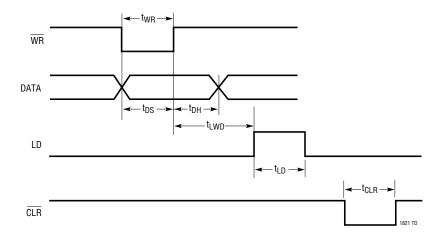
D4 (Pin 36): Digital Input Data Bit 4.

LTC1821

TRUTH TABLE

Table 1

CONTROL INPUTS			
CLR	$\overline{\text{WR}}$	LD	REGISTER OPERATION
0	X	X	Reset Input and DAC Register to All 0s for LTC1821 and Midscale for LTC1821-1 (Asynchronous Operation)
1	0	0	Write Input Register with All 16 Data Bits
1	1	1	Load DAC Register with the Contents of the Input Register
1	0	1	Input and DAC Register Are Transparent
1	⎍⎍	⎍⎍	CLK = LD and $\overline{\text{WR}}$ Tied Together. The 16 Data Bits Are Written Into the Input Register on the Falling Edge of the CLK and Then Loaded Into the DAC Register on the Rising Edge of the CLK
1	1	0	No Register Operation

BLOCK DIAGRAM

TIMING DIAGRAM

APPLICATIONS INFORMATION

Description

The LTC1821 is a 16-bit voltage output DAC with a full parallel 16-bit digital interface. The device can operate from 5V and ±15 supplies and provides both unipolar 0V to –10V or 0V to 10V and bipolar ±10V output ranges from a 10V or –10V reference input. Additionally, the power supplies for the LTC1821 can go as low as 4.5V and ±4.5V. In this case for a 2.5V or –2.5V reference, the output range is 0V to –2.5V, 0V to 2.5V and ±2.5V. The LTC1821 has three additional precision resistors on chip for bipolar operation. Refer to the block diagram regarding the following description.

The 16-bit DAC consists of a precision R-2R ladder for the 13 LSBs. The three MSBs are decoded into seven segments of resistor value R. Each of these segments and the R-2R ladder carries an equally weighted current of one eighth of full scale. The feedback resistor R_{FB} and 4-quadrant resistor R_{OFS} have a value of R/4. 4-quadrant resistors R1 and R2 have a magnitude of R/4. R1 and R2 together with an external op amp (see Figure 2) inverts the reference input voltage and applies it to the 16-bit DAC input REF, in 4-quadrant operation. The REF pin presents a constant input impedance of R/8 in unipolar mode and R/12 in bipolar mode.

The LTC1821 contains an onboard precision high speed amplifier. This amplifier together with the feedback resistor (R_{FB}) form a precision current-to-voltage converter for the DAC's current output. The amplifier has very low noise, offset, input bias current and settles in less than 2μs to 0.0015% for a 10V step. It can sink and source 22mA (±15V) typically and can drive a 300pF capacitive load. An added feature of these devices, especially for waveform generation, is a proprietary deglitcher that reduces glitch impulse to below 2nV-s over the DAC output voltage range.
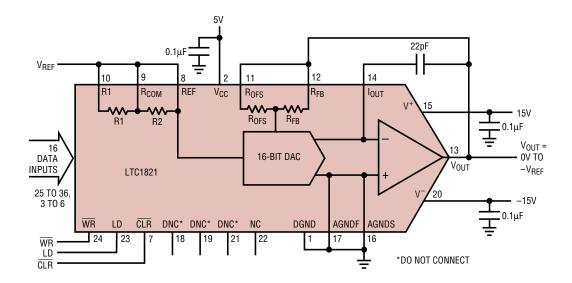
Digital Section

The LTC1821 has a 16-bit wide full parallel data bus input. The device is double-buffered with two 16-bit registers. The double-buffered feature permits the update of several DACs simultaneously. The input register is loaded directly from a 16-bit microprocessor bus when the $\overline{WR}$ pin is brought to a logic low level. The second register (DAC register) is updated with the data from the input register when the LD signal is brought to a logic high. Updating the DAC register updates the DAC output with the new data. To make both registers transparent in flowthrough mode, tie $\overline{WR}$ low and LD high. However, this defeats the deglitcher operation and output glitch impulse may increase. The deglitcher is activated on the rising edge of the LD pin. The

APPLICATIONS INFORMATION

versatility of the interface also allows the use of the input and DAC registers in a master slave or edge-triggered configuration. This mode of operation occurs when $\overline{WR}$ and LD are tied together. The asynchronous clear pin resets the LTC1821 to zero scale and the LTC1821-1 to midscale. $\overline{CLR}$ resets both the input and DAC registers. These devices also have a power-on reset. Table 1 shows the truth table for the LTC1821.

Unipolar Mode
(2-Quadrant Multiplying, V_{OUT} = 0V to $-V_{REF}$)

The LTC1821 can be used to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed $-10V$ reference, the circuit shown gives a precision unipolar 0V to 10V output swing.

Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	$-V_{REF}$ (65,535/65,536)
1000	0000	0000	0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000	0000	0000	0001	$-V_{REF}$ (1/65,536)
0000	0000	0000	0000	0V

1821 F01

Figure 1. Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$
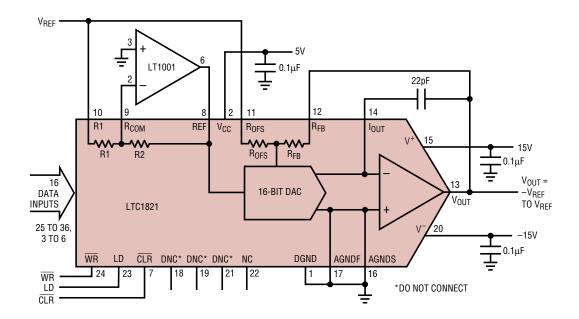
APPLICATIONS INFORMATION

Bipolar Mode
(4-Quadrant Multiplying, $V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1821 contains on chip all the 4-quadrant resistors necessary for bipolar operation. 4-quadrant multiplying operation can be achieved with a minimum of external components—a capacitor and a single op amp, as shown in Figure 2. With a fixed 10V reference, the circuit shown gives a precision bipolar –10V to 10V output swing.

Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	V_{REF} (32,767/32,768)
1000	0000	0000	0001	V_{REF} (1/32,768)
1000	0000	0000	0000	0V
0111	1111	1111	1111	$-V_{REF}$ (1/32,768)
0000	0000	0000	0000	$-V_{REF}$

1821 F02

Figure 2. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

APPLICATIONS INFORMATION

Precision Voltage Reference Considerations

Because of the extremely high accuracy of the 16-bit LTC1821, careful thought should be given to the selection of a precision voltage reference. As shown in the section describing the basic operation of the LTC1821, the output voltage of the DAC circuit is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 16-bit applications: output voltage initial tolerance, output voltage temperature coefficient (TC), and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error due to the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

As precision DAC applications move to 16-bit and higher performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references, like the LT1236, produce low output noise in the 0.1Hz to 10Hz region, well below the 16-bit LSB level in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.
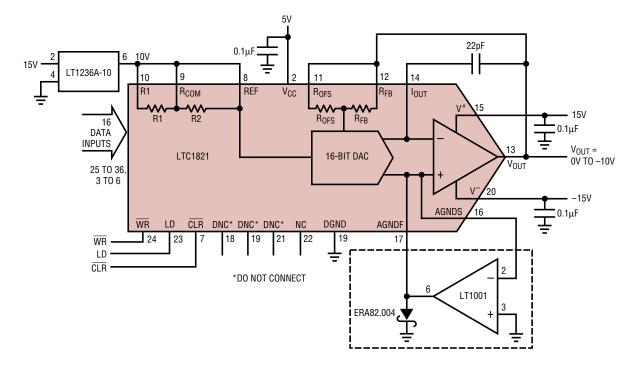
Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. AGNDF and AGNDS must be tied to the star ground with as low a resistance as possible. When it is not possible to locate star ground close to AGNDF and AGNDS, separate traces should be used to route these pins to the star ground. This minimizes the voltage drop from these pins to ground due to the code dependent current flowing into the ground plane. If the resistance of these separate circuit board traces exceeds 1Ω, the circuit of Figure 3 eliminates this code dependent voltage drop error for high resistance traces.

To calculate PC track resistance in squares, divide the length of the PC track by the width and multiply this result by the sheet resistance of copper foil. For 1 oz copper (≈1.4 mils thick), the sheet resistance is 0.045Ω per square.

Table 2. Partial List of LTC Precision References Recommended for Use with the LTC1821, with Relevant Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz to 10Hz NOISE
LT1019A-5, LT1019A-10	±0.05%	5ppm/°C	12μV$_{P-P}$
LT1236A-5, LT1236A-10	±0.05%	5ppm/°C	3μV$_{P-P}$
LT1460A-5, LT1460A-10	±0.075%	10ppm/°C	20μV$_{P-P}$
LT1790A-2.5	±0.05%	10ppm/°C	12μV$_{P-P}$

12

LINEAR TECHNOLOGY
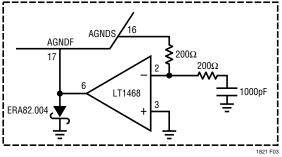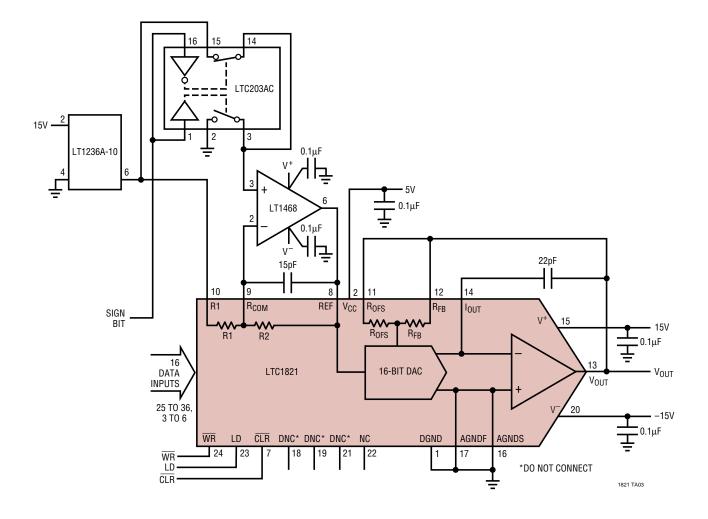
APPLICATIONS INFORMATION

Figure 3. Driving AGNDF and AGNDS with a Force/Sense Amplifier

TYPICAL APPLICATION

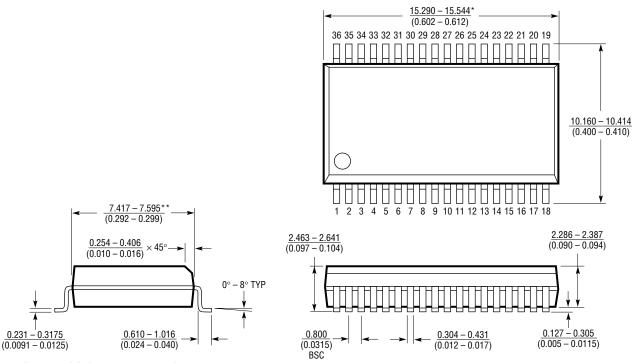**17-Bit Sign Magnitude Output Voltage DAC with Bipolar Zero Error of 140µV (0.92LSB at 17 Bits)**

1821 TA03

*DO NOT CONNECT

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GW Package
36-Lead Plastic SSOP (Wide 0.300)
(LTC DWG # 05-08-1642)

15.290 – 15.544*
(0.602 – 0.612)

36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

10.160 – 10.414
(0.400 – 0.410)

7.417 – 7.595**
(0.292 – 0.299)

0.254 – 0.406
(0.010 – 0.016) × 45°

0° – 8° TYP

0.231 – 0.3175
(0.0091 – 0.0125)

0.610 – 1.016
(0.024 – 0.040)

2.463 – 2.641
(0.097 – 0.104)

2.286 – 2.387
(0.090 – 0.094)

0.800
(0.0315)
BSC

0.304 – 0.431
(0.012 – 0.017)

0.127 – 0.305
(0.005 – 0.0115)

NOTE: DIMENSIONS ARE IN MILLIMETERS
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

GW36 SSOP 1098

15

RELATED PARTS

PART NUMBER		DESCRIPTION	COMMENTS
ADCs	LTC1417	Low Power 400ksps, 14-Bit ADC	20mW, Single or ±5V, Serial I/O
	LTC1418	14-Bit, 200ksps, Single 5V ADC	15mW, Serial/Parallel ±10V
	LTC1604/LTC1608	16-Bit, 333ksps/500ksps, ±5V ADC	90dB SINAD, 100dB THD, ±2.5V Inputs
	LTC1605/LTC1606	16-Bit, 100ksps/250ksps, Single 5V ADC	±10V Inputs, 55mW/75mW, Byte or Parallel I/O
	LTC1609	16-Bit, 200ksps, Single 5V ADC	±10V Inputs, 65mW, Serial I/O
	LTC2400	24-Bit, Micropower $\Delta\Sigma$ ADC in SO-8	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
	LTC2410	24-Bit, Fully Differential, No Latency $\Delta\Sigma$ ADC	0.16ppm Noise, 2ppm INL, 10ppm Total Unadjusted Error, 200µA
DACs	LTC1591/LTC1597	Parallel 14-/16-Bit Current Output DACs	On-Chip 4-Quadrant Resistors
	LTC1595/LTC1596	Serial 16-Bit Current Output DACs in SO-8/S16	Low Glitch, ±1LSB Maximum INL, DNL
	LTC1599	Parallel 2 Byte 16-Bit Current Output DAC	On-Chip 4-Quadrant Resistors
	LTC1650	Serial 16-Bit ±5V Voltage Output DAC	Low Noise and Low Glitch Rail-to-Rail V_{OUT}
	LTC1654	Dual 14-Bit Rail-to-Rail V_{OUT} DAC	Programmable Speed/Power, 3.5µs/750µA, 8µs/450µA
	LTC1655/LTC1655L	Serial 5V/3V 16-Bit Voltage Output DAC in SO-8	Low Power, Deglitched, Rail-to-Rail V_{OUT}
	LTC1657/LTC1657L	Parallel 5V/3V 16-Bit Voltage Output DAC	Low Power, Deglitched, Rail-to-Rail V_{OUT}
	LTC1658	Serial 14-Bit Voltage Output DAC	Low Power, 8-Lead MSOP Rail-to-Rail V_{OUT}
Op Amps	LT1001	Precision Operational Amplifier	Low Offset, Low Drift
	LT1468	90MHz, 22V/µs, 16-Bit Accurate Op Amp	Precise, 1µs Settling to 0.0015%
References	LT1019	Bandgap Reference	±0.05% Initial Tolerance, 5ppm/°C
	LT1236	Precision Buried Zener Reference	±0.05% Initial Tolerance, Low Noise 3µV$_{P-P}$
	LT1460	Micropower Bandgap Reference	±0.075% Initial Tolerance, 10ppm/°C
	LT1790	SOT-23 Micropower, Low Dropout Reference	±0.05% Initial Tolerance, 10ppm/°C

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