

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages: $5V_{IN}$, $3V_{IN}$ 10V

Input Voltages: (Pins 15, 16) -0.3V to 10V

Output Voltages: (Pins 1, 3, 4) -0.3V to 10V

Analog Voltages and Currents:

(Pin 9) -0.3V to $(3V_{IN} + 0.3V)$ (Pins 2, 5, 7, 11, 13, 14) -0.3V to $(5V_{IN} + 0.3V)$ (Pin 10) $\pm 20mA$

Operating Temperature Range:

LTC1646C $0^{\circ}C$ to $70^{\circ}C$ LTC1646I $-40^{\circ}C$ to $85^{\circ}C$ Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$ Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

TOP VIEW	
RESETOUT [1]	[16] RESETIN
TIMER [2]	[15] OFF/ON
FAULT [3]	[14] DRIVE
PWRGD [4]	[13] PRECHARGE
$5V_{OUT}$ [5]	[12] $5V_{IN}$
GND [6]	[11] $5V_{SENSE}$
$3V_{OUT}$ [7]	[10] GATE
$3V_{IN}$ [8]	[9] $3V_{SENSE}$
GN PACKAGE 16-LEAD PLASTIC SSOP $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 135^{\circ}C/W$	
ORDER PART NUMBER	GN PART MARKING
LTC1646CGN	1646
LTC1646IGN	1646I
Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/	

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS The \bullet denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. $V_{5VIN} = 5V$ and $V_{3VIN} = 3.3V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD}	V_{5VIN} Supply Current	OFF/ON = 0V	\bullet		1.5	4	mA
V_{LKO}	Undervoltage Lockout	$5V_{IN}$ $3V_{IN}$	\bullet \bullet	2.3 2.3	2.50 2.55	2.7 2.7	V V
V_{FB}	Foldback Current Limit Voltage	$V_{FB} = (V_{5VIN} - V_{5VSENSE})$, $V_{5VOUT} = 0V$, TIMER = 0V $V_{FB} = (V_{5VIN} - V_{5VSENSE})$, $V_{5VOUT} = 4V$, TIMER = 0V $V_{FB} = (V_{3VIN} - V_{3VSENSE})$, $V_{3VOUT} = 0V$, TIMER = 0V $V_{FB} = (V_{3VIN} - V_{3VSENSE})$, $V_{3VOUT} = 2V$, TIMER = 0V	\bullet \bullet \bullet \bullet	15 50 15 50	20 55 20 55	30 65 30 65	mV mV mV mV
V_{CB}	Circuit Breaker Trip Voltage	$V_{CB} = (V_{5VIN} - V_{5VSENSE})$, $V_{5VOUT} = 5V$, TIMER Open $V_{CB} = (V_{3VIN} - V_{3VSENSE})$, $V_{3VOUT} = 3.3V$, TIMER Open	\bullet \bullet	50 50	56 56	65 65	mV mV
t_{OC}	Overcurrent Fault Response Time	$(V_{5VIN} - V_{5VSENSE}) = 100mV$, TIMER Open $(V_{3VIN} - V_{3VSENSE}) = 100mV$, TIMER Open	\bullet \bullet	10 10	21 21	30 30	μs μs
t_{SS}	Short-Circuit Fault Response Time	$(V_{5VIN} - V_{5VSENSE}) = 200mV$, TIMER Open $(V_{3VIN} - V_{3VSENSE}) = 200mV$, TIMER Open	\bullet \bullet		0.145 0.145	1 1	μs μs
I_{CP}	GATE Pin Output Current	OFF/ON = 0V, $V_{GATE} = 0V$, TIMER = 0V OFF/ON = 5V, $V_{GATE} = 5V$, TIMER = 0V OFF/ON = 0V, $V_{GATE} = 5V$, FAULT = 0V, TIMER Open	\bullet \bullet \bullet	-18 80 4	-13 200 7	-8 300 12	μA μA mA
V_{GATE}	External Gate Voltage (GATE to GND)	OFF/ON = 0V, $I_{GATE} = -1\mu A$ OFF/ON = 0V, $V_{5VIN} = 3.3V$, $I_{GATE} = -1\mu A$	\bullet \bullet	12 11	15 13	16 15	V V
V_{TH}	Power Good Threshold Voltage	$3V_{OUT}$ $5V_{OUT}$	\bullet \bullet	2.8 4.5	2.9 4.65	3.0 4.75	V V
V_{3VONLY}	No 5V Input Mode Window Voltage	$V_{3VONLY} = V_{5VIN} - V_{3VIN} $, $V_{5VOUT} = V_{3VOUT} = 3.3V$	\bullet	50	120	200	mV
V_{IL}	Input Low Voltage	OFF/ON, RESETIN, FAULT	\bullet			0.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{5VIN} = 5\text{V}$ and $V_{3VIN} = 3.3\text{V}$ unless otherwise noted.

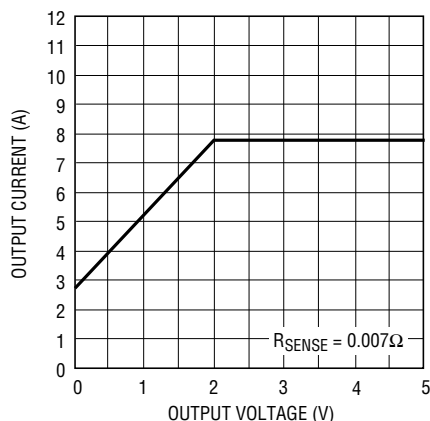
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input High Voltage	OFF/ $\overline{\text{ON}}$, $\overline{\text{RESETIN}}$, $\overline{\text{FAULT}}$	●	2			V
V_{TIMER}	TIMER Threshold Voltage	V_{TIMER} , $\overline{\text{FAULT}} = 0\text{V}$	●	1.15	1.25	1.35	V
I_{IN}	OFF/ $\overline{\text{ON}}$ Input Current	OFF/ $\overline{\text{ON}} = 5\text{V}$	●		± 0.08	± 10	μA
		OFF/ $\overline{\text{ON}} = 0\text{V}$	●		± 0.08	± 10	μA
	$\overline{\text{RESETIN}}$ Input Current	$\overline{\text{RESETIN}} = 5\text{V}$	●		± 0.08	± 10	μA
		$\overline{\text{RESETIN}} = 0\text{V}$	●		± 0.08	± 10	μA
	$5V_{\text{SENSE}}$ Input Current	$5V_{\text{SENSE}} = 5\text{V}$, $5V_{\text{OUT}} = 0\text{V}$	●		66	100	μA
	$3V_{\text{SENSE}}$ Input Current	$3V_{\text{SENSE}} = 3.3\text{V}$, $3V_{\text{OUT}} = 0\text{V}$	●		66	100	μA
	$3V_{\text{IN}}$ Input Current	$3V_{\text{IN}} = 3.3\text{V}$	●		460	1000	μA
	$5V_{\text{OUT}}$ Input Current	$5V_{\text{OUT}} = 5\text{V}$, OFF/ $\overline{\text{ON}} = 0\text{V}$	●		0.9	1.5	mA
	$3V_{\text{OUT}}$ Input Current	$3V_{\text{OUT}} = 3.3\text{V}$, OFF/ $\overline{\text{ON}} = 0\text{V}$	●		0.9	1.5	mA
I_{TIMER}	TIMER Pin Current	OFF/ $\overline{\text{ON}} = 0\text{V}$, $V_{\text{TIMER}} = 0\text{V}$	●	-7	-5	-3	μA
		OFF/ $\overline{\text{ON}} = 5\text{V}$, $V_{\text{TIMER}} = 5\text{V}$			6.6		mA
R_{DIS}	$5V_{\text{OUT}}$ Discharge Impedance	OFF/ $\overline{\text{ON}} = 5\text{V}$	●		120	220	Ω
	$3V_{\text{OUT}}$ Discharge Impedance	OFF/ $\overline{\text{ON}} = 5\text{V}$	●		120	220	Ω
V_{OL}	Output Low Voltage	$\overline{\text{FAULT}}$, $\overline{\text{PWRGD}}$, $\overline{\text{RESETOUT}}$, $I = 2\text{mA}$	●		0.25	0.4	V
V_{PXG}	PRECHARGE Reference Voltage	$V_{\text{PRECHARGE}}$, $V_{5VIN} = 5\text{V}$ and 3.3V	●	0.90	1.00	1.10	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

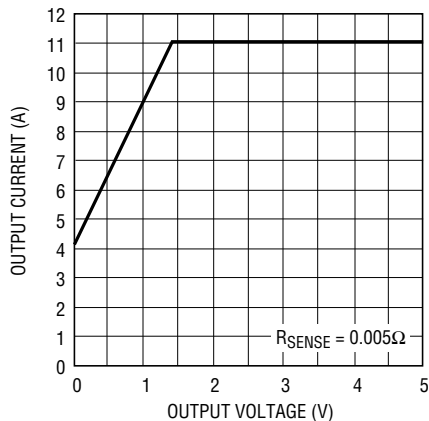
TYPICAL PERFORMANCE CHARACTERISTICS

5V Current Foldback Profile



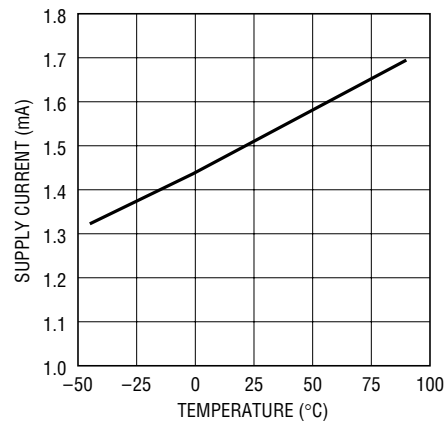
1646 G01

3.3V Current Foldback Profile



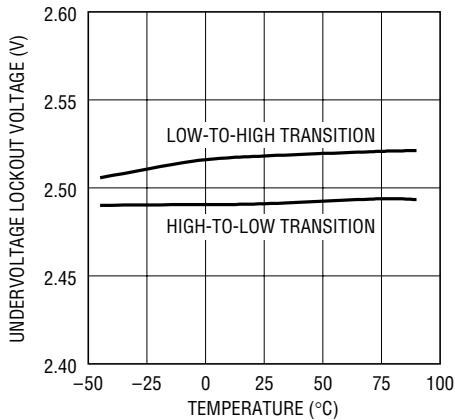
1646 G02

5V_{IN} Supply Current vs Temperature

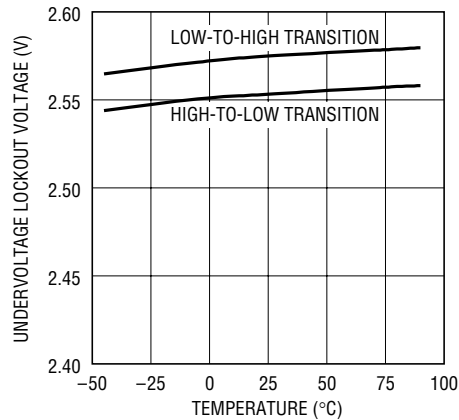


1646 G03

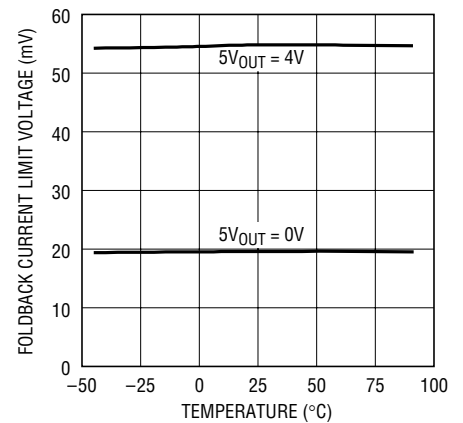
TYPICAL PERFORMANCE CHARACTERISTICS

**5V_{IN} Undervoltage Lockout
Voltage vs Temperature**

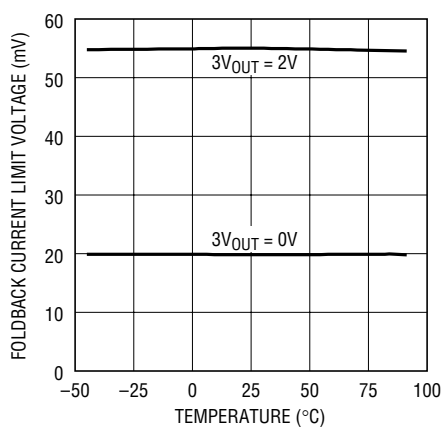
1646 G04

**3V_{IN} Undervoltage Lockout
Voltage vs Temperature**

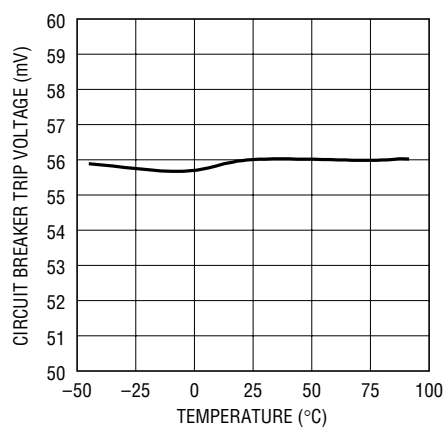
1646 G05

**5V_{IN} Foldback Current Limit
Voltage vs Temperature**

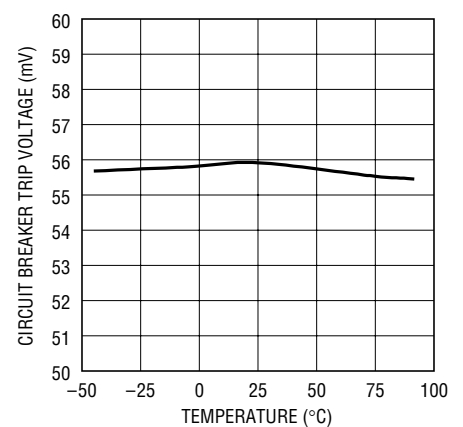
1646 G06

**3V_{IN} Foldback Current Limit
Voltage vs Temperature**

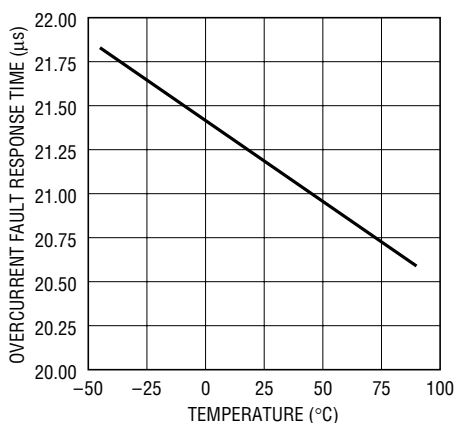
1646 G07

**5V_{IN} Circuit Breaker Trip Voltage
vs Temperature**

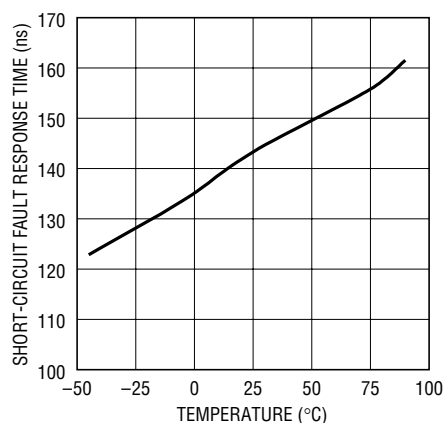
1646 G08

**3V_{IN} Circuit Breaker Trip Voltage
vs Temperature**

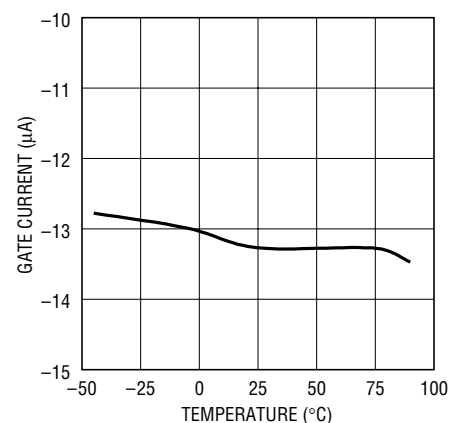
1646 G09

**5V_{IN}/3V_{IN} Overcurrent Fault
Response Time vs Temperature**

1646 G10

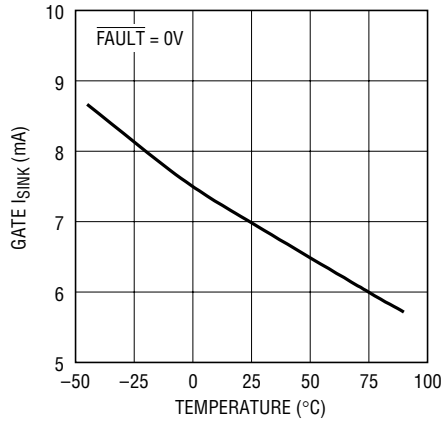
**5V_{IN}/3V_{IN} Short-Circuit Fault
Response Time vs Temperature**

1646 G11

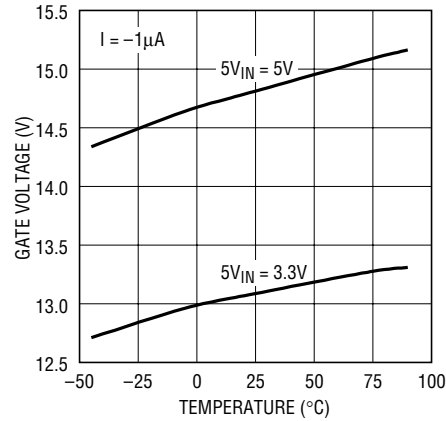
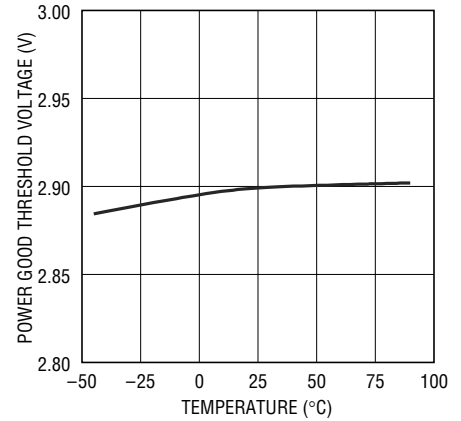
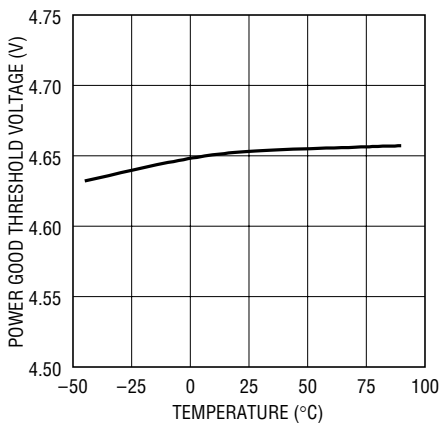
Gate Current vs Temperature

1646 G12

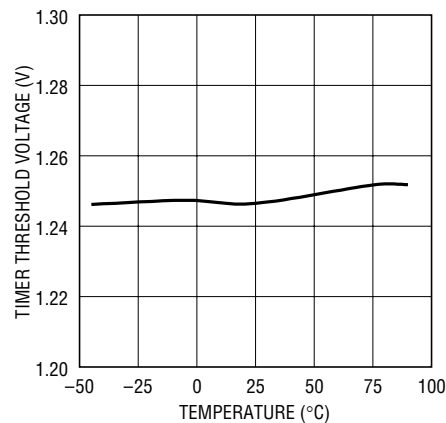
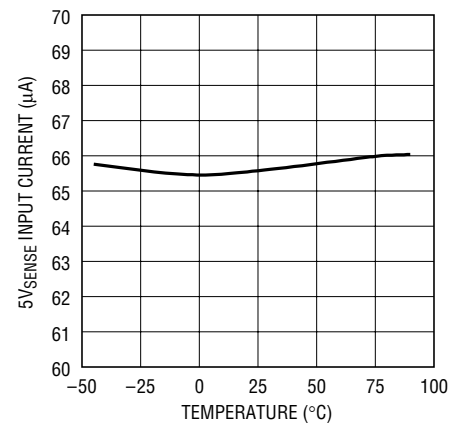
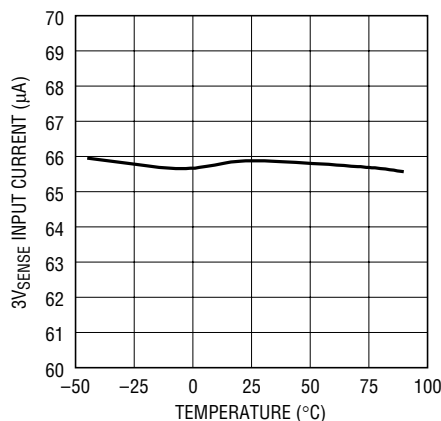
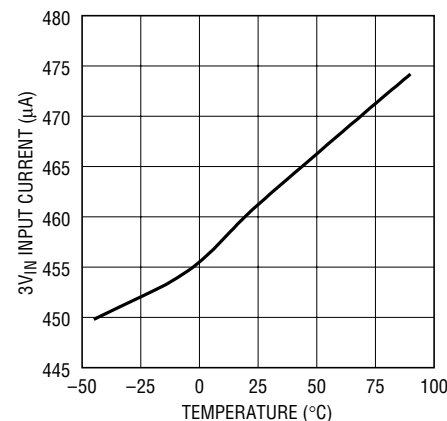
TYPICAL PERFORMANCE CHARACTERISTICS

Gate I_{SINK} vs Temperature

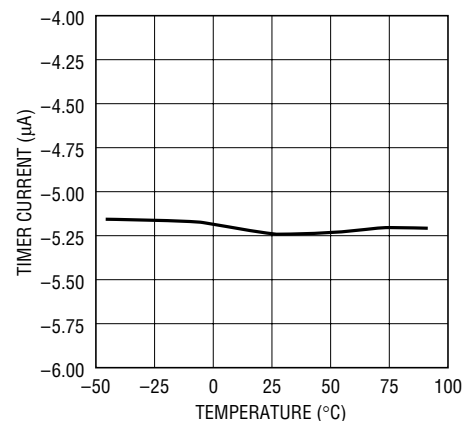
Gate Voltage vs Temperature

Power Good Threshold Voltage vs Temperature (3V_{OUT})Power Good Threshold Voltage vs Temperature (5V_{OUT})

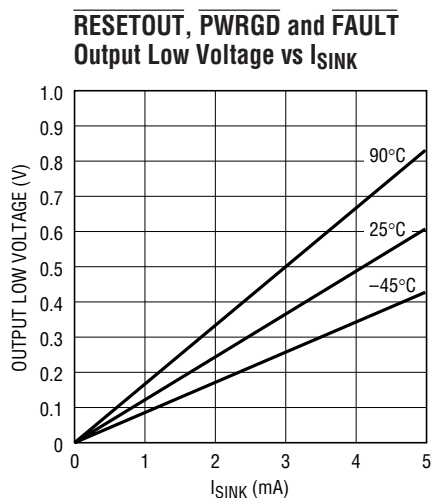
Timer Threshold Voltage vs Temperature

5V_{SENSE} Input Current vs Temperature3V_{SENSE} Input Current vs Temperature3V_{IN} Input Current vs Temperature

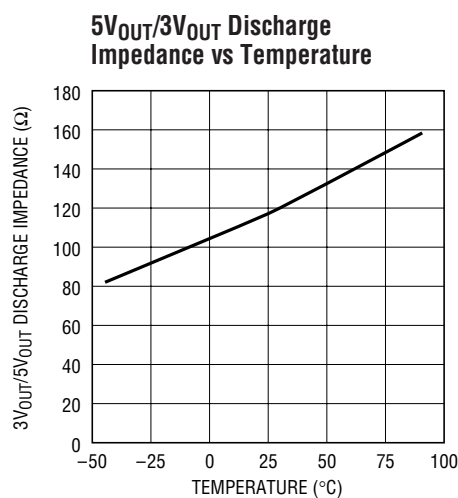
Timer Current vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS



1646 G22



1646 G23

PIN FUNCTIONS

RESETOUT (Pin 1): Open Drain Digital Output. Connect the CPCI LOCAL_PCI_RST# signal to the RESETOUT pin. RESETOUT is the logical combination of RESETIN and PWRGD (see Table 4).

TIMER (Pin 2): Current Fault Inhibit Timing Input. Connect a capacitor from TIMER to GND. With the chip turned off, the TIMER pin is internally held at GND. When the chip is turned on, a 5μA pull-up current source is connected to TIMER. Current limit and voltage compliance faults will be ignored until the voltage at the TIMER pin is greater than 1.25V.

FAULT (Pin 3): Open Drain Digital I/O. FAULT is pulled low when a current limit fault is detected. Faults are ignored while the voltage at the TIMER pin is less than 1.25V. Once the TIMER cycle is complete, FAULT will pull low and the chip will latch off in the event of an overcurrent fault. The chip will remain latched in the off state until the OFF/ON pin is cycled high then low or the power is cycled.

Forcing the FAULT pin low with an external pull-down will cause the chip to be latched into the off state after a 21μs deglitching time.

PWRGD (Pin 4): Open Drain Power Good Digital Output. Connect the CPCI HEALTHY# signal to the PWRGD pin. PWRGD remains low while $V_{3V_{OUT}} \geq 2.9V$ and $V_{5V_{OUT}} \geq 4.65V$. When either of the supplies falls below its power good threshold voltage, PWRGD will go high after a 50μs deglitching time.

5V_{OUT} (Pin 5): 5V Output Sense. The PWRGD pin will not pull low until the 5V_{OUT} pin voltage exceeds 4.65V. If no 5V input supply is available, tie the 5V_{OUT} pin to the 3V_{OUT} pin in order to disable the 5V_{OUT} power good function.

GND (Pin 6): Chip Ground

3V_{OUT} (Pin 7): 3.3V Output Sense. The PWRGD pin will not pull low until the 3V_{OUT} pin voltage exceeds 2.90V. If no 3.3V input supply is available, tie the 3V_{OUT} pin to the 5V_{OUT} pin.

3V_{IN} (Pin 8): 3.3V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the 3V_{IN} pin is less than 2.5V. If no 3.3V input supply is available, connect a diode between 5V_{IN} and 3V_{IN} (tie anode to 5V_{IN} and cathode to 3V_{IN}). See Figure 11.

PIN FUNCTIONS

3V_{SENSE} (Pin 9): 3.3V Current Limit Set. With a sense resistor placed in the supply path between 3V_{IN} and 3V_{SENSE}, the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor and a constant current through the switch while the TIMER pin voltage is less than 1.25V. A foldback feature makes the current limit decrease as the voltage at the 3V_{OUT} pin approaches GND.

When the TIMER pin voltage exceeds 1.25V, the circuit breaker function is enabled. If the voltage across the sense resistor exceeds 56mV, the circuit breaker is tripped after a 21μs time delay. In the event the sense resistor voltage exceeds 150mV, the circuit breaker trips immediately and the chip latches off. To disable the 3.3V current limit, 3V_{SENSE} and 3V_{IN} can be shorted together.

GATE (Pin 10): High Side Gate Drive for the External 3.3V and 5V N-Channel pass transistors. Requires an external series RC network for the current limit loop compensation and setting the minimum ramp-up rate. During power-up, the slope of the voltage rise at the GATE is set by the 13μA current source connected to the internal charge pump and the external capacitor connected to GND or by the 3.3V or 5V current limit and the bulk capacitance on the 3V_{OUT} or 5V_{OUT} supply lines. During power-down, the slope of the ramp down voltage is set by the 200μA current source connected to GND and the external GATE capacitor.

The voltage at the GATE pin will be modulated to maintain a constant current when either the 3V or 5V supplies go into current limit while the TIMER pin voltage is less than 1.25V. If a current fault occurs after the TIMER pin voltage exceeds 1.25V, the GATE pin is immediately pulled to GND.

5V_{SENSE} (Pin 11): 5V Current Limit Set. With a sense resistor placed in the supply path between 5V_{IN} and 5V_{SENSE}, the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor and a constant current through the switch while the TIMER pin voltage is less than 1.25V. A foldback feature makes the current limit decrease as the voltage at the 5V_{OUT} pin approaches GND.

When the TIMER pin voltage is greater than 1.25V, the circuit breaker function is enabled. If the voltage across the sense resistor exceeds 56mV but is less than 150mV, the circuit breaker is tripped after a 21μs time delay. In the event the sense resistor voltage exceeds 150mV, the circuit breaker trips immediately and the chip latches off. To disable the 5V current limit, short 5V_{SENSE} and 5V_{IN} together.

5V_{IN} (Pin 12): 5V Supply Sense Input. An undervoltage lockout circuit prevents the GATE pin voltage from ramping up when the voltage at the 5V_{IN} pin is less than 2.5V. If no 5V input supply is available, tie the 5V_{IN} pin to the 3V_{IN} pin.

PRECHARGE (Pin 13): Precharge Monitor Input. An on-chip error amplifier with a 1V reference servos the DRIVE pin voltage to keep the precharge node at 1V. If the precharge function is not being used, tie the PRECHARGE pin to GND.

DRIVE (Pin 14): Precharge Base Drive Output. Provides base drive for an external NPN emitter-follower which in turn biases the PRECHARGE node. If the precharge function is not being used, allow the DRIVE pin to float.

OFF/ $\overline{\text{ON}}$ (Pin 15): Digital Input. Connect the CPCI BD_SEL# signal to the OFF/ $\overline{\text{ON}}$ pin. When the OFF/ $\overline{\text{ON}}$ pin is pulled low, the GATE pin is pulled high by a 13μA current source. When the OFF/ $\overline{\text{ON}}$ pin is pulled high the GATE pin will be pulled to ground by a 200μA current source.

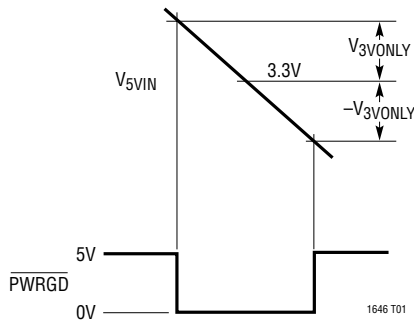
The OFF/ $\overline{\text{ON}}$ pin is also used to reset the electronic circuit breaker. If the OFF/ $\overline{\text{ON}}$ pin is cycled high and low following the trip of the circuit breaker, the circuit breaker is reset, and a normal power-up sequence will occur.

RESETIN (Pin 16): Digital Input. Connect the CPCI PCI_RST# signal to the RESETIN pin. Pulling RESETIN low will cause the RESETOUT pin to pull low.

TEST DIAGRAM

V_{3VONLY} No 5V Input Mode Window Voltage

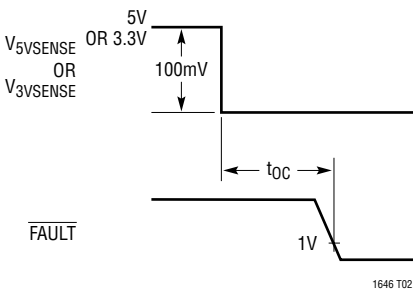
$V_{3VONLY} = |5V_{IN} - 3V_{IN}|$ $5V_{OUT} = 3V_{OUT} = 3.3V$, $3V_{IN} = 3.3V$



TIMING DIAGRAMS

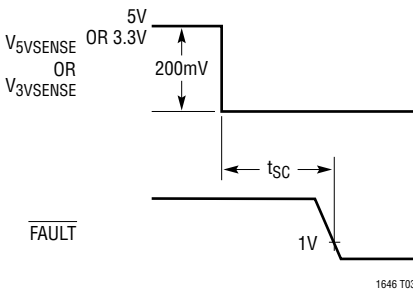
t_{OC} Overcurrent Fault Detect

FALL TIME ≤ 1μs, 5V_{IN} = 5V, 3V_{IN} = 3.3V

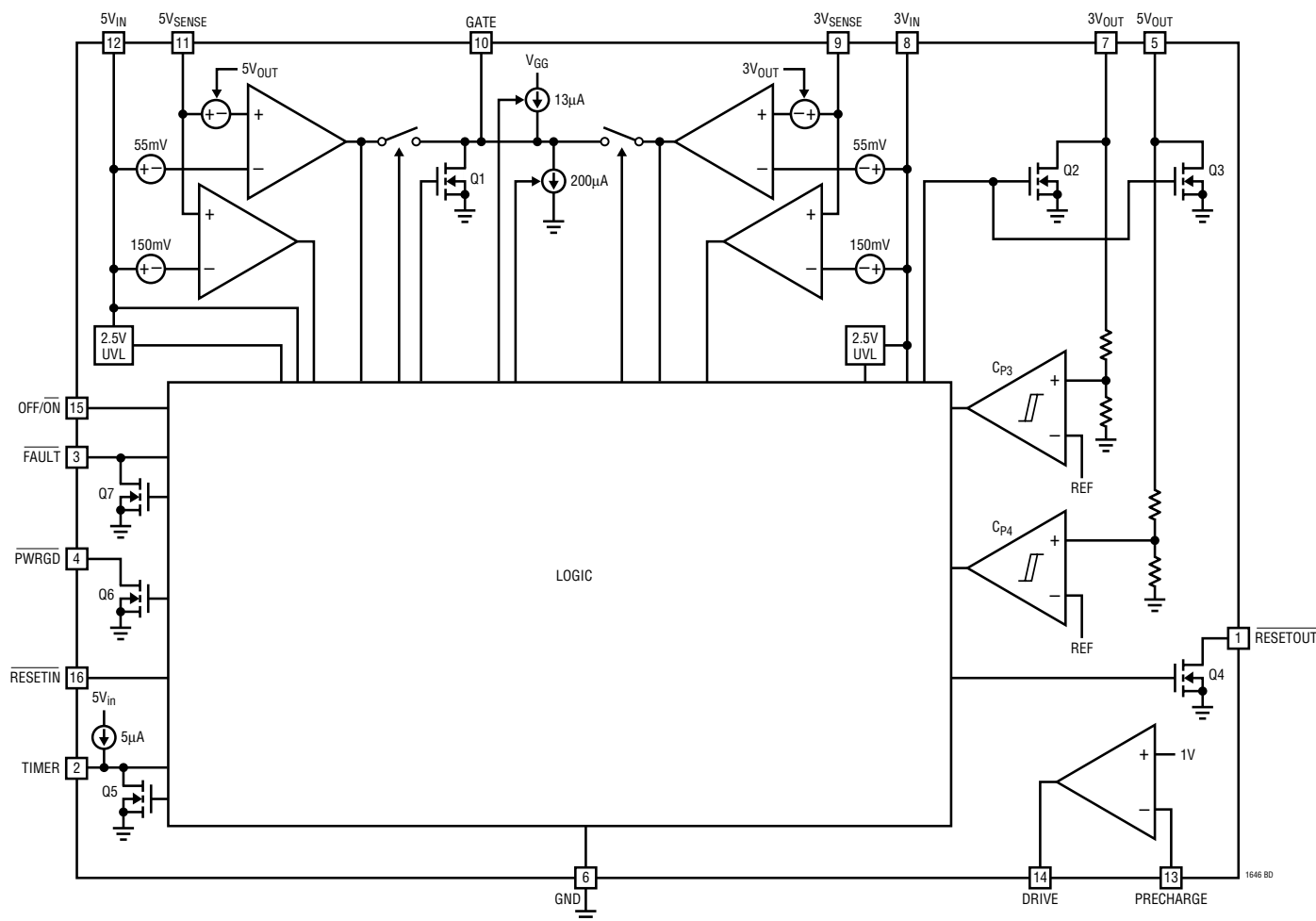


t_{SC} Short-Circuit Fault Detect

FALL TIME ≤ 30ns, 5V_{IN} = 5V, 3V_{IN} = 3.3V



BLOCK DIAGRAM



APPLICATIONS INFORMATION

Hot Circuit Insertion

When a circuit board is inserted into a live CompactPCI (CPCI) slot, the supply bypass capacitors on the board can draw huge supply transient currents from the CPCI power bus as they charge up. The transient currents can cause glitches on the power bus, causing other boards in the system to reset.

The LTC1646 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live CPCI slot without glitching the system power supplies. The chip also protects the supplies from shorts, precharges the bus I/O pins during insertion and extraction and monitors the supply voltages.

The LTC1646 is specifically designed for CPCI applications where the chip resides on the plug-in board.

LTC1646 Feature Summary

1. Allows safe board insertion and removal from a CPCI backplane.
2. Controls 5V and 3.3V CPCI supplies.
3. Current limit during power-up: the supplies are allowed to power up in current limit. This allows the chip to power up boards with widely varying capacitive loads without tripping the circuit breaker. The maximum allowable power-up time is programmable using the TIMER pin and an external capacitor.

APPLICATIONS INFORMATION

4. Programmable foldback current limit: a programmable analog current limit with a value that depends on the output voltage. If the output is shorted to ground, the current limit drops to keep power dissipation and supply glitches to a minimum.
5. Dual-level, programmable 5V and 3.3V circuit breakers: this feature is enabled when the **TIMER** pin voltage exceeds 1.25V. If either supply exceeds current limit for more than 21μs, the circuit breaker will trip, the supplies will be turned off, and the **FAULT** pin is pulled low. In the event that either supply exceeds three times the set current limit, all supplies will be turned off and the **FAULT** pin is pulled low without delay.
6. 15V high side drive for external 3.3V and 5V N-channel MOSFETs.
7. **PWRGD** output: monitors the voltage status of the supply voltages.
8. **PCI_RST#** combined on-chip with **HEALTHY#** to create **LOCAL_PCI_RST#** output. If **HEALTHY#** deasserts, **LOCAL_PCI_RST#** is asserted independent of **PCI_RST#**.
9. Precharge output: on-chip reference and amplifier provide 1V for biasing bus I/O connector pins during CPCI card insertion and extraction.
10. Space saving 16-pin SSOP package.

PCI Power Requirements

CPCI systems may require up to four power rails: 5V, 3.3V, 12V and -12V. The LTC1646 is designed for CPCI applications which only use the 5V and/or 3.3V supplies. The tolerance of the supplies as measured at the components on the plug-in card is summarized in Table 1.

Table 1. PCI Power Supply Requirements

SUPPLY	TOLERANCE	CAPACITIVE LOAD
5V	5V ±5%	<3000μF
3.3V	3.3V ±0.3V	<3000μF

Power-Up Sequence

The LTC1646 is specifically designed for hot swapping CPCI boards. The typical application is shown in Figure 1.

The main 3.3V and 5V inputs to the LTC1646 come from the medium length power pins. The long 3.3V, 5V connector pins are shorted to the medium length 5V and 3.3V connector pins on the CPCI plug-in card and provide early power for the LTC1646's precharge circuitry, the V(I/O) pull-up resistors and the PCI bridge chip. The **BD_SEL#** signal is connected to the **OFF/ON** pin while the **PWRGD** pin is connected to the **HEALTHY#** signal. The **HEALTHY#** signal is combined with the **PCI_RST#** signal on-chip to generate the **LOCAL_PCI_RST#** signal which is available at the **RESETOUT** pin.

The power supplies are controlled by placing external N-channel pass transistors in the 3.3V and 5V power paths.

Resistors R1 and R2 provide current fault detection and R5 and C1 provide current control loop compensation. Resistors R3 and R4 prevent high frequency oscillations in Q1 and Q2.

When the CPCI card is inserted, the long 5V and 3.3V connector pins and GND pins make contact first. The LTC1646's precharge circuit biases the bus I/O pins to 1V during this stage of the insertion (Figure 2). The 5V and 3.3V medium length pins make contact during the next stage of insertion, but the slot power is disabled as long as the **OFF/ON** pin is pulled high by the 1.2k pull-up resistor to V(I/O). During the final stage of board insertion, the **BD_SEL#** short connector pin makes contact and the **OFF/ON** pin can be pulled low. This enables the pass transistors to turn on and a 5μA current source is connected to the **TIMER** pin.

The current in each pass transistor increases until it reaches the current limit for each supply. The 5V and 3.3V supplies are then allowed to power up based on one of the following power-up rates:

$$\frac{dV}{dt} = \frac{13\mu A}{C1}, \text{ or } = \frac{I_{LIMIT(5V)}}{C_{LOAD(5VOUT)}}, \text{ or } = \frac{I_{LIMIT(3V)}}{C_{LOAD(3VOUT)}} \quad (1)$$

whichever is slower.

Current limit faults are ignored while the **TIMER** pin voltage is ramping up and is less than 1.25V. Once both supply voltages are within tolerance, **HEALTHY#** will pull low and **LOCAL_PCI_RST#** is free to follow **PCI_RST#**.

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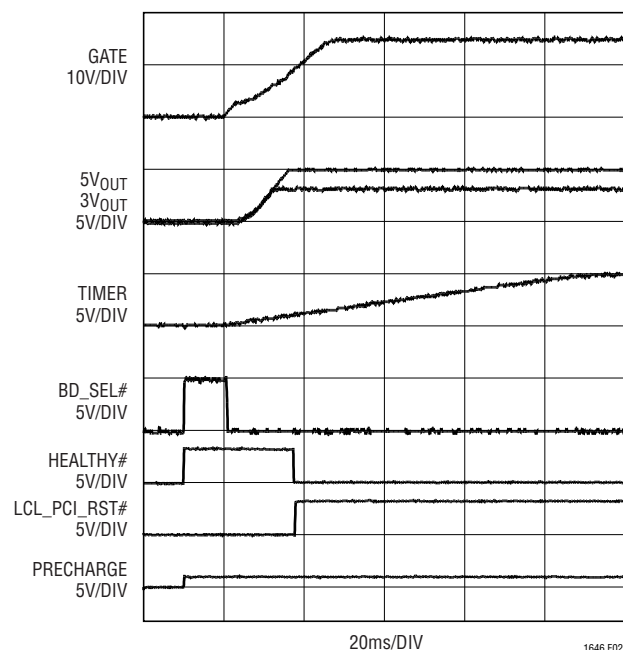


Figure 2. Normal Power-Up Sequence

Power-Down Sequence

When BD_SEL# is pulled high, a power-down sequence begins (Figure 3).

Internal switches are connected to each of the output supply voltage pins to discharge the bypass capacitors to ground. The TIMER pin (Pin 2) is immediately pulled low. The GATE pin (Pin 10) is pulled down by a 200μA current source to prevent the load currents on the 3.3V and 5V supplies from going to zero instantaneously in order to prevent glitching the power supply voltages. When either of the output voltages dips below its threshold, HEALTHY# pulls high and LOCAL_PCI_RST# will be asserted low.

Once the power-down sequence is complete, the CPCI card may be removed from the slot. During extraction, the precharge circuit will continue to bias the bus I/O pins at 1V until the 5V and 3.3V long connector pin connections are separated.

Timer

During a power-up sequence, a 5μA current source is connected to the TIMER pin and current limit faults are ignored until the voltage exceeds 1.25V. This feature

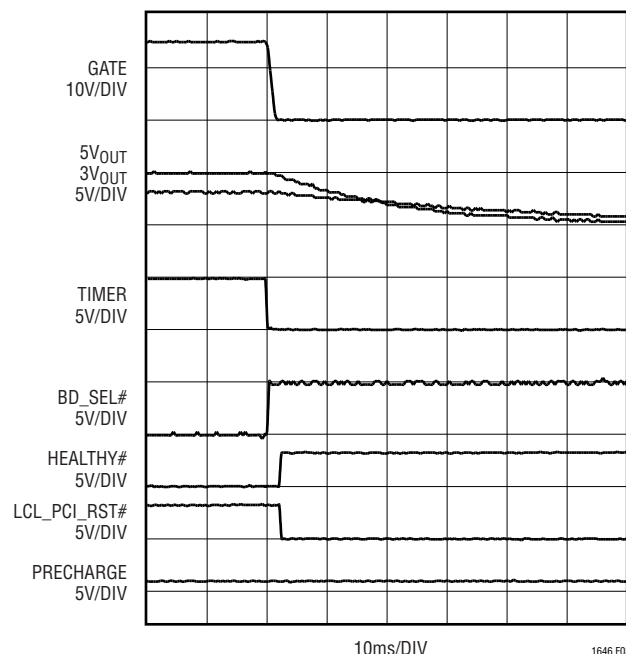


Figure 3. Normal Power-Down Sequence

allows the chip to power up CPCI boards with widely varying capacitive loads on the supplies. The power-up time for either of the two outputs is given by:

$$t_{ON}(XV_{OUT}) = 2 \cdot \frac{C_{LOAD}(XV_{OUT}) \cdot XV_{OUT}}{I_{LIMIT}(XV_{OUT}) - I_{LOAD}(XV_{OUT})} \quad (2)$$

Where $XV_{OUT} = 5V_{OUT}$ or $3V_{OUT}$. For example, for $C_{LOAD}(5V_{OUT}) = 2000\mu F$, $I_{LIMIT} = 7A$, and $I_{LOAD} = 5A$, the $5V_{OUT}$ turn-on time will be ~10ms. By substituting the variables in Equation 2 with the appropriate values, the turn-on time for the $3V_{OUT}$ output can also be calculated. The timer period should be set longer than the maximum supply turn-on time but short enough to not exceed the maximum safe operating area of the pass transistor during a short-circuit. The timer period for the LTC1646 is given by:

$$t_{TIMER} = \frac{C_{TIMER} \cdot 1.25V}{5\mu A} \quad (3)$$

As a design aid, the timer period as a function of the timing capacitor using standard values from 0.01μF to 1μF is shown in Table 2.

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Table 2. t_{TIMER} vs C_{TIMER}

C_{TIMER}	t_{TIMER}	C_{TIMER}	t_{TIMER}
0.01 μF	2.5ms	0.22 μF	55ms
0.022 μF	5.5ms	0.33 μF	82.5ms
0.033 μF	8.25ms	0.47 μF	118ms
0.047 μF	11.8ms	0.68 μF	170ms
0.068 μF	17ms	0.82 μF	205ms
0.082 μF	20.5ms	1 μF	250ms
0.1 μF	25ms		

The TIMER pin is immediately pulled low when BD_SEL\# goes high.

Short-Circuit Protection

During a normal power-up sequence, if the TIMER pin is done ramping and a supply is still in current limit, all of the pass transistors will be immediately turned off and $\overline{\text{FAULT}}$ (Pin 3) will be pulled low as shown in Figure 4.

In order to prevent excessive power dissipation in the pass transistors and to prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases.

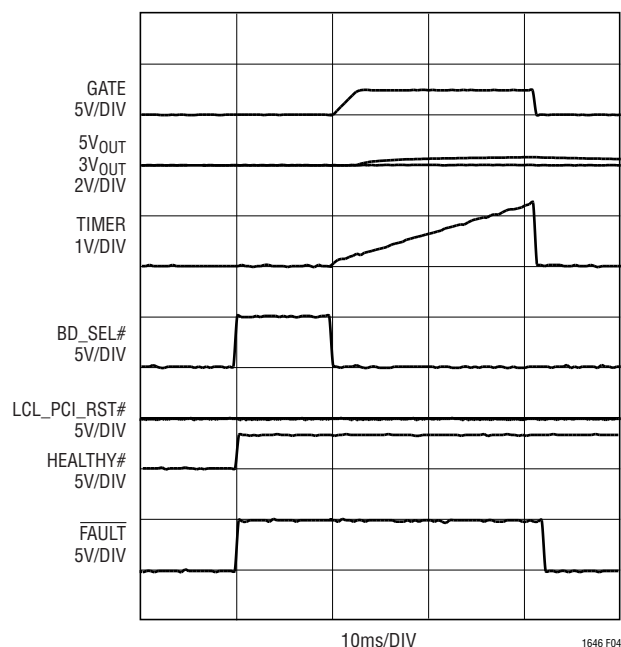


Figure 4. Power-Up into a Short on 3.3V Output

Unlike a traditional circuit breaker function where huge currents can flow before the breaker trips, the current foldback feature assures that the supply current will be kept at a safe level and prevents voltage glitches at the input supply when powering up into a short circuit.

After power-up (TIMER pin voltage $>1.25\text{V}$), the 5V and 3.3V supplies are protected from overcurrent and short-circuit conditions by dual-level circuit breakers. If the sense resistor voltage of either supply current exceeds 56mV but is less than 150mV, an internal timer is started. If the supply is still overcurrent after 21 μs , the circuit breaker trips and both supplies are turned off (Figure 5).

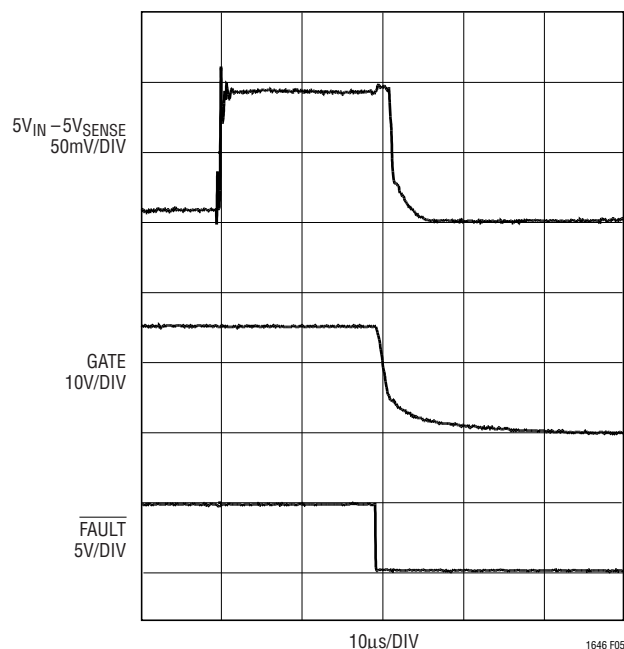


Figure 5. Overcurrent Fault on 5V

If a short-circuit occurs and the sense resistor voltage of either supply current exceeds 150mV, the circuit breakers trip without delay and the chip latches off (Figure 6). The chip will stay in the latched-off state until OFF/ON (Pin 15) is cycled high then low, or the 5V_{IN} (Pin 12) power supply is cycled.

The current limit and the foldback current level for the 5V and 3.3V outputs are both a function of the external sense resistor (R_1 for 3V_{OUT} and R_2 for 5V_{OUT} , see Figure 1). As shown in Figure 1, a sense resistor is connected between


$$I_{LIMIT(XVOUT)} = \frac{55mV}{R_{SENSE(XVOUT)}} \quad (4)$$

$$I_{\text{FOLDBACK}(XVOUT)} = \frac{20\text{mV}}{R_{\text{SENSE}(XVOUT)}} \quad (5)$$

Table 3. I_{LIMIT(XVOUT)} and I_{FOLDBACK(XVOUT)} vs R_{SENSE}

where $XV_{OUT} = 3V_{OUT}$ or $5V_{OUT}$.

Figure 7. Circuit Breaker Equivalent Circuit for Calculating R_{SENSE}

$$R_{\text{SENSE(MAX)}} = \frac{V_{\text{CB(MIN)}}}{I_{\text{TRIP(MAX)}}} \quad (6)$$

The second step is to determine the nominal value of the sense resistor which is dependent on its tolerance

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(RTOL = $\pm 1\%$, $\pm 2\%$ or $\pm 5\%$) and standard sense resistor values. Equation 7 can be used to calculate the nominal value from the maximum value found by Equation 6:

$$R_{\text{SENSE(NOM)}} = \frac{R_{\text{SENSE(MAX)}}}{1 + \left(\frac{\text{RTOL}}{100}\right)} \quad (7)$$

Often, the result of Equation 7 may not yield a standard sense resistor value. In this case, two sense resistors with the same RTOL can be connected in parallel to yield $R_{\text{SENSE(NOM)}}$.

The last step requires calculating a new value for $I_{\text{TRIP(MAX, NEW)}}$ based on a minimum value for R_{SENSE} ($R_{\text{SENSE(MIN)}}$) and the upper limit for the circuit breaker threshold, $V_{\text{CB(MAX)}}$. Should the calculated value for $I_{\text{TRIP(MAX, NEW)}}$ be much greater than the design value for $I_{\text{TRIP(MAX)}}$, a larger sense resistor value should be selected and the process repeated. The new value for $I_{\text{TRIP(MAX, NEW)}}$ is given by Equation 8:

$$I_{\text{TRIP(MAX, NEW)}} = \frac{V_{\text{CB(MAX)}}}{R_{\text{SENSE(MIN)}}} \quad (8)$$

$$\text{where } R_{\text{SENSE(MIN)}} = R_{\text{SENSE(NOM)}} \cdot \left[1 - \left(\frac{\text{RTOL}}{100}\right)\right]$$

Example: A 5V supply exhibits a nominal 5A load with a maximum load current of 6.8A ($I_{\text{LOAD(MAX)}} = 6.8\text{A}$), and sense resistors with $\pm 5\%$ RTOL will be used. According to Equation 6, $V_{\text{CB(MIN)}} = 50\text{mV}$ and $R_{\text{SENSE(MAX)}}$ is given by:

$$R_{\text{SENSE(MAX)}} = \frac{V_{\text{CB(MIN)}}}{I_{\text{TRIP(MAX)}}} = \frac{50\text{mV}}{6.8\text{A}} = 0.0074\Omega$$

The nominal sense resistor value is (Equation 7):

$$R_{\text{SENSE(NOM)}} = \frac{R_{\text{SENSE(MAX)}}}{1 + \left(\frac{\text{RTOL}}{100}\right)} = \frac{0.0074\Omega}{1 + \left(\frac{5}{100}\right)} = 0.007\Omega$$

And the new current-limit trip point is Equation 8:

$$I_{\text{TRIP(MAX, NEW)}} = \frac{V_{\text{CB(MAX)}}}{R_{\text{SENSE(MIN)}}} = \frac{V_{\text{CB(MAX)}}}{R_{\text{SENSE(NOM)}} \cdot \left[1 - \left(\frac{\text{RTOL}}{100}\right)\right]} = \frac{65\text{mV}}{0.0065} = 9.8\text{A}$$

Since $I_{\text{TRIP(MAX, NEW)}} > I_{\text{LOAD(MAX)}}$, a larger value for R_{SENSE} should be selected and the process repeated again to lower $I_{\text{TRIP(MAX, NEW)}}$ without substantially affecting $I_{\text{LOAD(MAX)}}$.

Output Voltage Monitor

The status of both 5V and 3.3V output voltages is monitored by the power good function. In addition, the PCI_RST# signal is logically combined on-chip with the HEALTHY# signal to create LOCAL_PCI_RST# (see Table 4).

Table 4. LOCAL_PCI_RST# Truth Table

PCI_RST#	HEALTHY#	LOCAL_PCI_RST#
LO	LO	LO
LO	HI	LO
HI	LO	HI
HI	HI	LO

If either of the output voltages drop below the power good threshold for more than 50 μs , the HEALTHY# signal will be pulled high and the LOCAL_PCI_RST# signal will be pulled low.

Precharge

The PRECHARGE input and DRIVE output pins are intended for use in generating the 1V precharge voltage that is used to bias the bus I/O connector pins during board insertion. The LTC1646 is also capable of generating precharge voltages other than 1V. Figure 8 shows a circuit that can be used in applications requiring a precharge voltage less than 1V. The circuit in Figure 9 can be used for applications that need precharge voltages greater than 1V. Table 5 lists suggested resistor values for R1 and R2 vs precharge voltage for the application circuits shown in Figures 8 and 9.

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Since there is no bulk capacitance to damp the parasitic trace inductance, supply voltage transients excite parasitic resonant circuits formed by the power MOSFET capacitance and the combined parasitic inductance from the wiring harness, the backplane and the circuit board traces. These ringing transients appear as a fast edge on the 3.3V or 5V supply, exhibiting a peak overshoot to 2.5 times the steady-state value followed by a damped sinusoidal response whose duration and period is dependent on the resonant circuit parameters. Since the absolute maximum supply voltage of the LTC1646 is 10V, transient protection against 3.3V and 5V supply voltage spikes and ringing is highly recommended.

In these applications, there are two methods for eliminating these supply voltage transients: using Zener diodes to clip the transient to a safe level and snubber networks. Snubbers are RC networks whose time constants are large enough to safely damp the inductance of the board's parasitic resonant circuits. As a starting point, the shunt capacitors in these networks are chosen to be $10\times$ to $100\times$ the power MOSFET's C_{OSS} under bias. The value of the series resistor (R6 and R7 in Figure 13) is then chosen to be large enough to damp the resulting series R-L-C circuit and typically ranges from 1Ω to 10Ω . Note that in all

LTC1646 circuit schematics, Zener diodes and snubber networks have been added to each 3.3V and 5V supply rail and should be used always. These protection networks should be mounted very close to the LTC1646's supply voltage using short lead lengths to minimize lead inductance. This is shown schematically in Figure 13 and a recommended layout of the transient protection devices around the LTC1646 is shown in Figure 14.

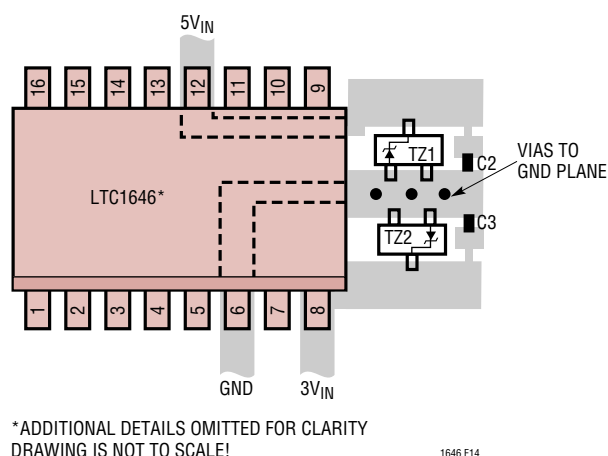


Figure 14. Recommended Layout for Transient Protection Components

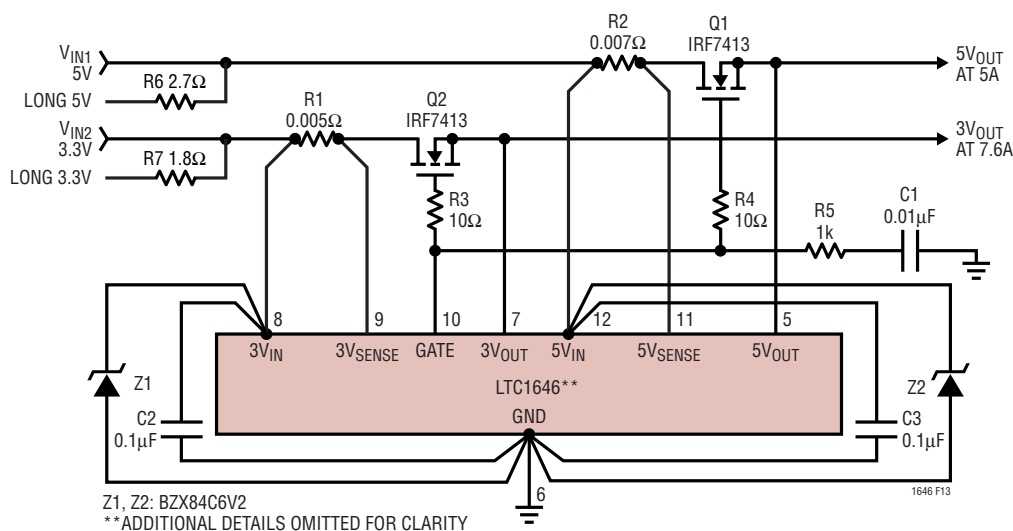


Figure 13. Place Transient Protection Device Close to the LTC1646

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PCB Layout Considerations

For proper operation of the LTC1646's circuit breaker function, a 4-wire Kelvin connection to the sense resistors is highly recommended. A recommended PCB layout for the sense resistor, the power MOSFET, and the GATE drive components around the LTC1646 is illustrated in Figure 15. In Hot Swap applications where load currents can reach 10A, narrow PCB tracks exhibit more resistance than wider tracks and operate at more elevated temperatures. Since the sheet resistance of 1 ounce copper foil is approximately $0.5\text{m}\Omega/\square$, track resistances add up quickly in high current applications. Thus, to keep PCB track resistance and temperature rise to a minimum, the suggested trace width in these applications for 1 ounce copper foil is 0.03" for each ampere of DC current.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PC board. For 1 ounce copper foil plating, a general rule is 1A of DC current per via, making sure the via is properly dimensioned so that solder completely fills any void. For other plating thicknesses, check with your PCB fabrication facility.

Power MOSFET and Sense Resistor Selection

Table 6 lists some current MOSFET transistors that are available and Table 7 lists some current sense resistors that can be used with the LTC1646's circuit breakers. Table 8 lists supplier web site addresses for discrete component mentioned throughout the LTC1646 data sheet.

Table 6. N-Channel Power MOSFET Selection Guide

CURRENT LEVEL (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	MMDF3N02HD	Dual N-Channel SO-8 $R_{DS(ON)} = 0.1\Omega$	ON Semiconductor
2 to 5	MMSF5N02HD	Single N-Channel SO-8 $R_{DS(ON)} = 0.025\Omega$	ON Semiconductor
5 to 10	MTB50N06V	Single N-Channel DD Pak $R_{DS(ON)} = 0.028\Omega$	ON Semiconductor
5 to 10	IRF7413	Single N-Channel SO-8 $R_{DS(ON)} = 0.01\Omega$	International Rectifier
5 to 10	Si4410DY	Single N-Channel SO-8 $R_{DS(ON)} = 0.01\Omega$	Vishay-Siliconix

Table 7. Sense Resistor Selection Guide

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LR120601R055F WSL1206R055	0.055 Ω , 0.5W, 1% Resistor	IRC-TT Vishay-Dale
2A	LR120601R028F WSL1206R028	0.028 Ω , 0.5W, 1% Resistor	IRC-TT Vishay-Dale
5A	LR120601R011F WSL2010R011	0.011 Ω , 0.5W, 1% Resistor	IRC-TT Vishay-Dale
7.6A	WSL2512R007	0.007 Ω , 1W, 1% Resistor	Vishay-Dale
10A	WSL2512R005	0.005 Ω , 1W, 1% Resistor	Vishay-Dale

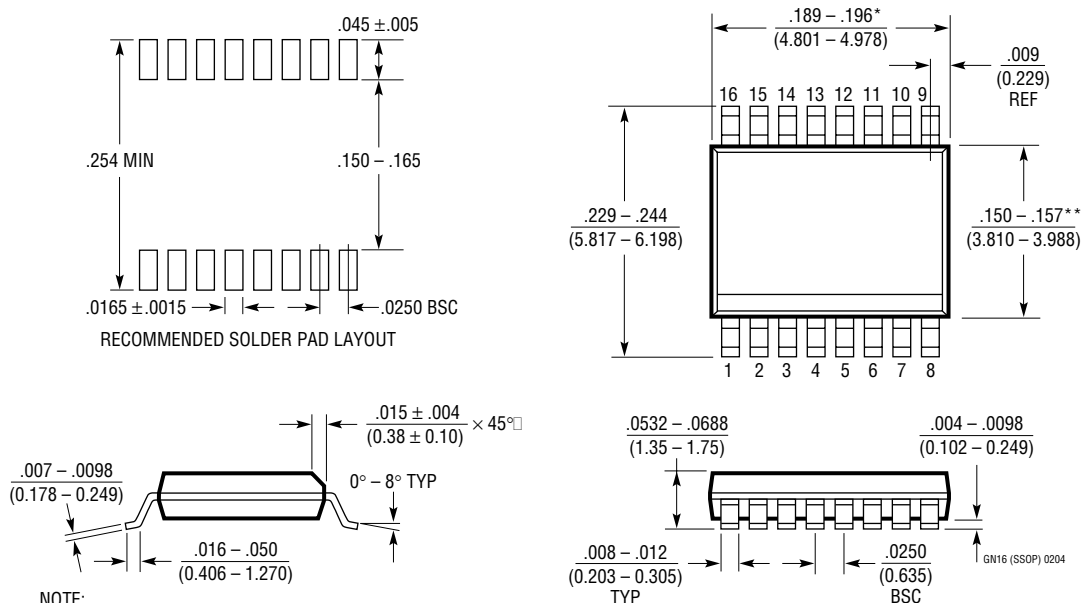
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Table 8. Manufacturers' Web Site

MANUFACTURER	WEB SITE
International Rectifier	www.irf.com
ON Semiconductor	www.onsemi.com
IRC-TT	www.irctt.com
Vishay-Dale	www.vishay.com
Vishay-Siliconix	www.vishay.com
Diodes, Inc.	www.diodes.com

PACKAGE DESCRIPTION

GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



NOTE:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

