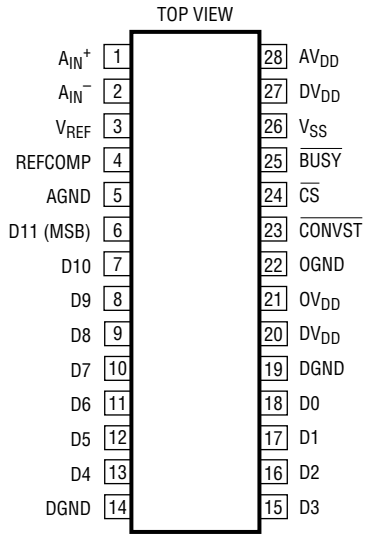
ABSOLUTE MAXIMUM RATINGS

$AV_{DD} = DV_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) ..... (V_{SS} – 0.3V) to 10V
Digital Output Voltage ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC1412C ..... 0°C to 70°C
LTC1412I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP
T_{JMAX} = 110°C, θ_{JA} = 95°C/ W

ORDER PART NUMBER
LTC1412CG
LTC1412IG

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With internal reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●		±0.35	±1	LSB
Differential Linearity Error		●		±0.25	±1	LSB
Offset Error	(Note 8)	 ●		±2	±6 ±8	LSB LSB
Full-Scale Error					±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±15		ppm/°C

ANALOG INPUT

(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.75V	●		±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			10 4		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		20	50	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–0.5		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				1		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	–2.5V < (A_{IN}^- = A_{IN}) < 2.5V			63		dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal 1.465MHz Input Signal		 70	72.5 72		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First 5 Harmonics 1.465MHz Input Signal, First 5 Harmonics			–90 –80		dB dB
SFDR	Spurious Free Dynamic Range	1.465MHz Input Signal			82		dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–84		dB
	Full Power Bandwidth				40		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 68dB			4		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0			±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V			0.01 0.01		LSB/V LSB/V
V_{REF} Output Resistance	0.1mA ≤ $\lvert I_{OUT} \rvert$ ≤ 0.1mA			2		kΩ
COMP Output Voltage	I_{OUT} = 0			4.06		V

DIGITAL INPUTS AND OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				1.4		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_O = –10µA V_{DD} = 4.75V, I_O = –200µA	 ●	 4.0	4.75 4.71		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_O = 160µA V_{DD} = 4.75V, I_O = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)			7		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Note 10)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 10)		–4.75		–5.25	V
I_{DD}	Positive Supply Current	$\overline{CS}$ High	●		12	16	mA
I_{SS}	Negative Supply Current	$\overline{CS}$ High	●		18	28	mA
P_D	Power Dissipation		●		150	220	mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	3			MHz
$t_{THROUGHPUT}$	Throughput Time (Acquisition + Conversion)		●			333	ns
t_{CONV}	Conversion Time		●		240	283	ns
t_{ACQ}	Acquisition Time		●		20	50	ns
t_1	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	5			ns
t_2	$\overline{CONVST}$ Low Time	(Note 10)	●	20			ns
t_3	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF			5		ns
			●			20	ns
t_4	Data Ready Before $\overline{BUSY}\uparrow$			–20	0	20	ns
			●	–25		25	ns
t_5	Delay Between Conversions	(Note 10)	●	50			ns
t_6	Data Access Time After $\overline{CS}\downarrow$	C_L = 25pF			10	35	ns
			●			45	ns
t_7	Bus Relinquish Time				8	30	ns
		LTC1412C	●			35	ns
		LTC1412I	●			40	ns
t_8	$\overline{CONVST}$ High Time		●	20			ns
t_9	Aperture Delay of Sample-and-Hold				–1		ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 3MHz and $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended A_{IN} input with A_{IN}^- grounded.

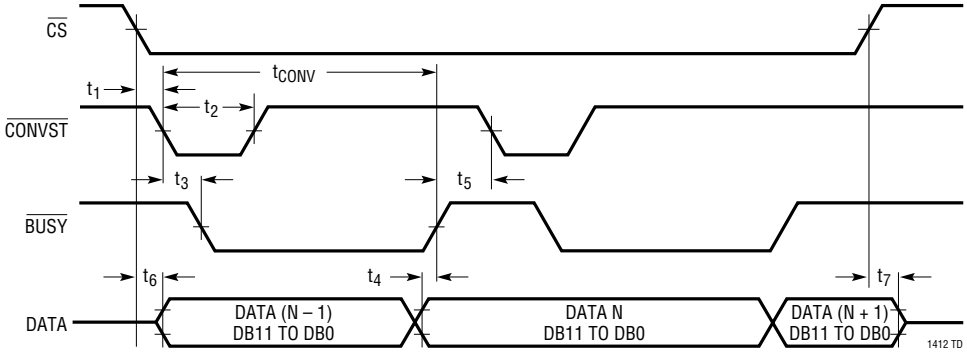
Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

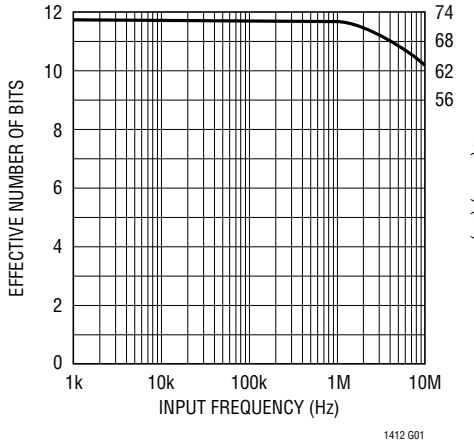
Note 10: Recommended operating conditions.

TIMING DIAGRAM

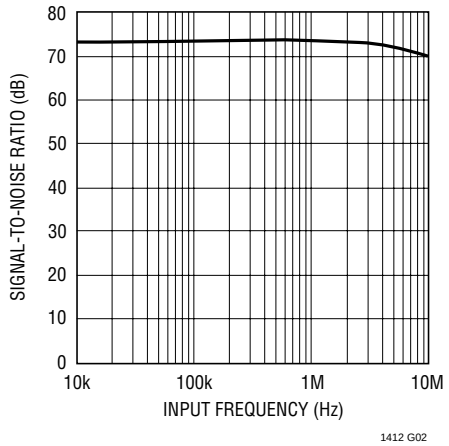


TYPICAL PERFORMANCE CHARACTERISTICS

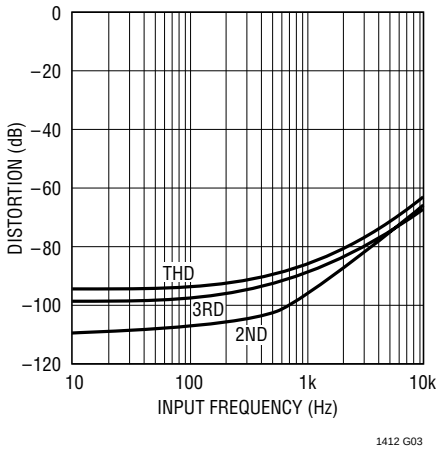
S/(N + D) and Effective Number of Bits vs Input Frequency



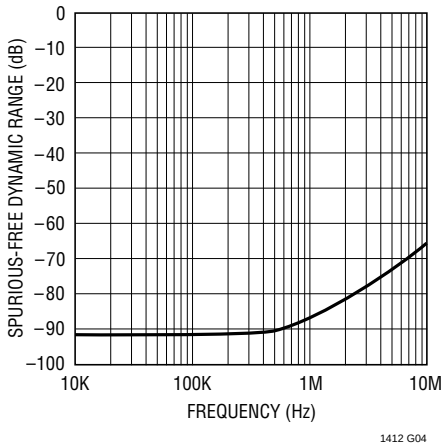
Signal-to-Noise Ratio vs Input Frequency



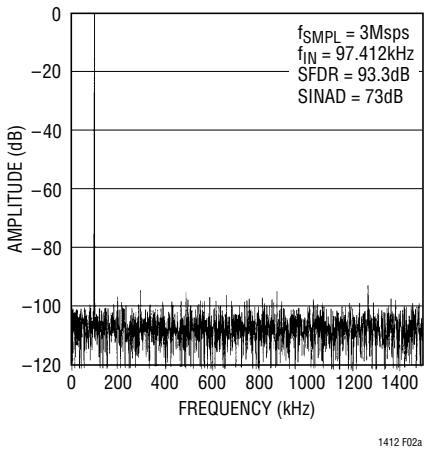
Distortion vs Input Frequency



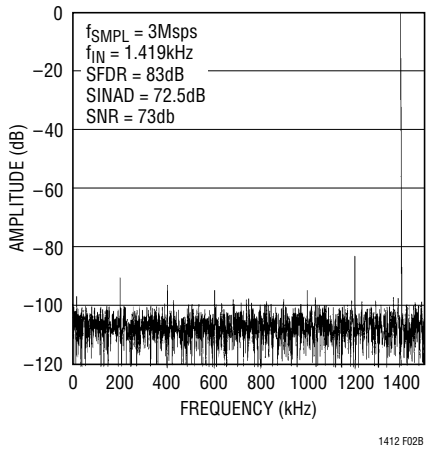
Spurious-Free Dynamic Range vs Input Frequency



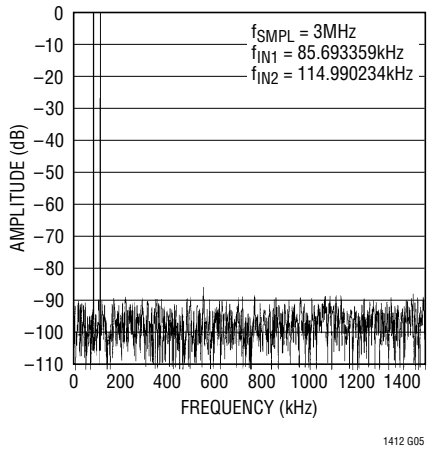
Nonaveraged, 4096 Point FFT, Input Frequency = 100kHz



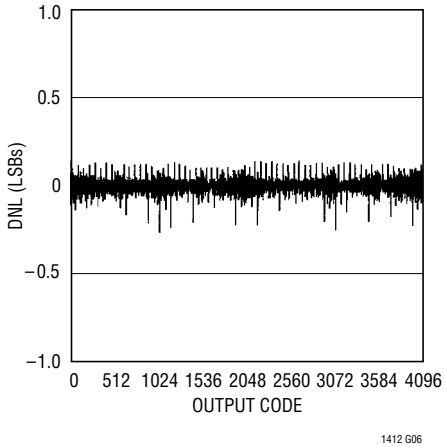
Nonaveraged, 4096 Point FFT, Input Frequency = 1.45kHz



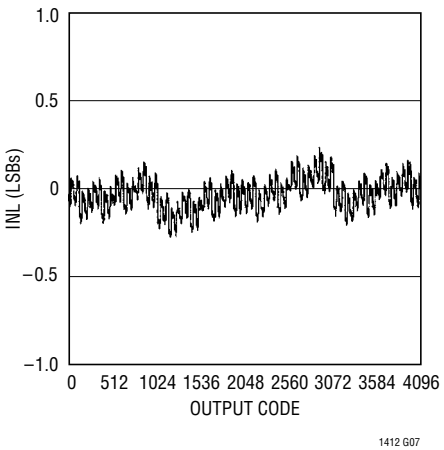
Intermodulation Distortion Plot



Differential Nonlinearity vs Output Code

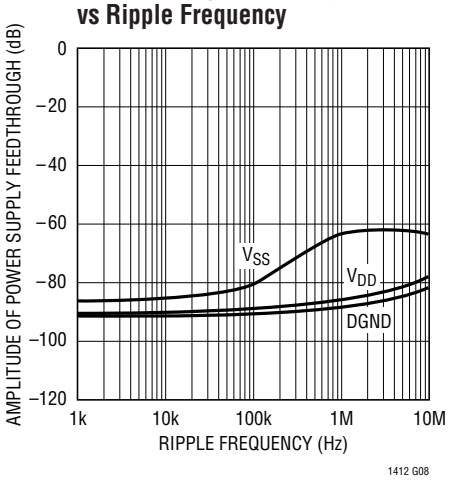


Integral Nonlinearity vs Output Code

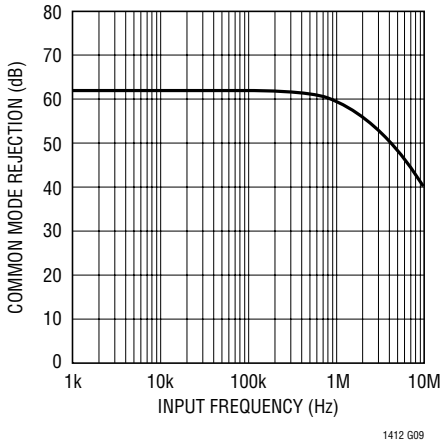


TYPICAL PERFORMANCE CHARACTERISTICS

Power Supply Feedthrough vs Ripple Frequency



Input Common Mode Rejection vs Input Frequency



PIN FUNCTIONS

A_{IN}^+ (Pin 1): Positive Analog Input. ±2.5V input range when A_{IN}^- is grounded. ±2.5V differential if A_{IN}^- is driven.

A_{IN}^- (Pin 2): Negative Analog Input. Can be grounded or driven differentially with A_{IN}^+.

V_{REF} (Pin 3): 2.5V Reference Output.

REFCOMP (Pin 4): 4.06V Reference Bypass Pin. Bypass to AGND with 10µF ceramic (or 10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 5): Analog Ground.

D11 to D4 (Pins 6 to 13): Three-State Data Outputs.

DGND (Pin 14): Digital Ground for Internal Logic.

D3 to D0 (Pins 15 to 18): Three-State Data Outputs.

DGND (Pin 19): Digital Ground for Internal Logic.

DV_{DD} (Pin 20): 5V Positive Supply. Tie to Pin 28. Bypass to AGND with 0.1µF ceramic.

OV_{DD} (Pin 21): Positive Supply for the Output Drivers. Tie to Pin 28 when driving 5V logic. Tie to 3V when driving 3V logic.

OGND (Pin 22): Digital Ground for the Output Drivers.

$\overline{\text{CONVST}}$ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

$\overline{\text{CS}}$ (Pin 24): Chip Select. This input must be low for the ADC to recognize the $\overline{\text{CONVST}}$ inputs.

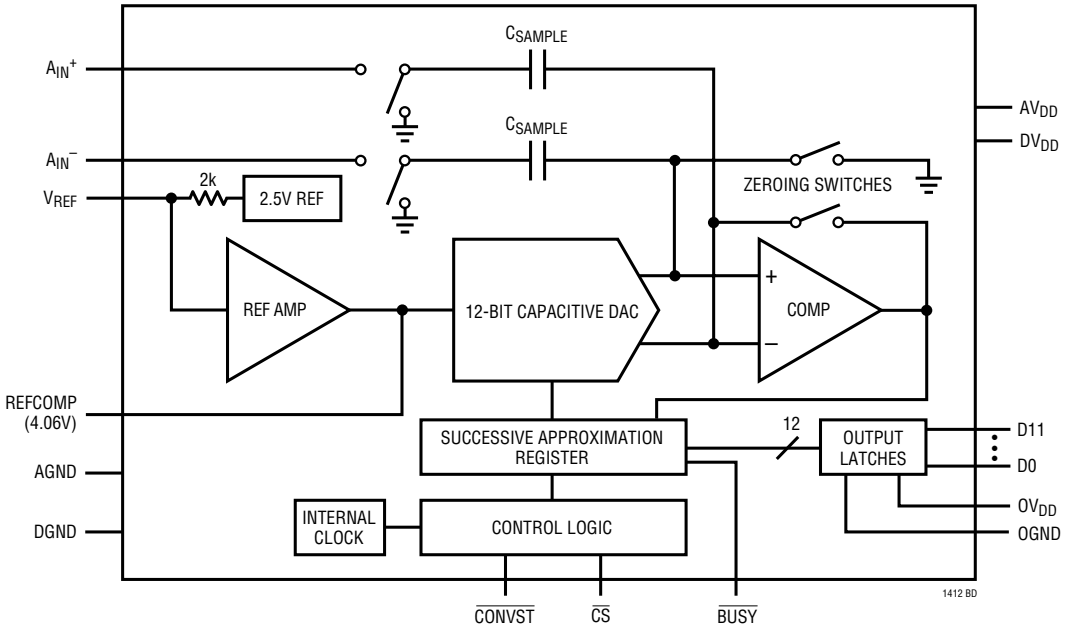
$\overline{\text{BUSY}}$ (Pin 25): The $\overline{\text{BUSY}}$ Output Shows the Converter Status. It is low when a conversion is in progress.

V_{SS} (Pin 26): –5V Negative Supply. Bypass to AGND with 10µF ceramic (or 10µF tantalum in parallel with 0.1µF ceramic).

DV_{DD} (Pin 27): 5V Positive Supply. Tie to Pin 28.

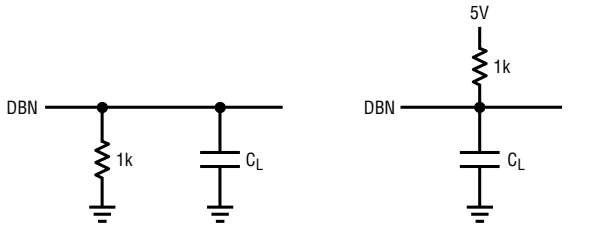
AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF ceramic (or 10µF tantalum in parallel with 0.1µF ceramic).

FUNCTIONAL BLOCK DIAGRAM

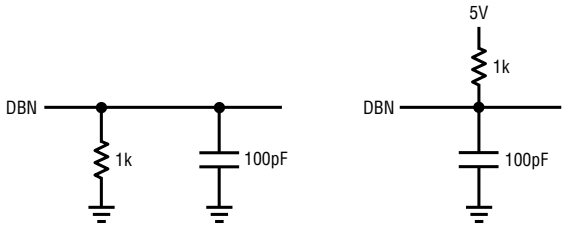


TEST CIRCUITS

Load Circuits for Access Timing



Load Circuits for Output Float Delay



APPLICATIONS INFORMATION

Conversion Details

The LTC1412 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal differential 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN}^+ and A_{IN}^- inputs are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum delay of 50ns will provide enough time for the

APPLICATIONS INFORMATION

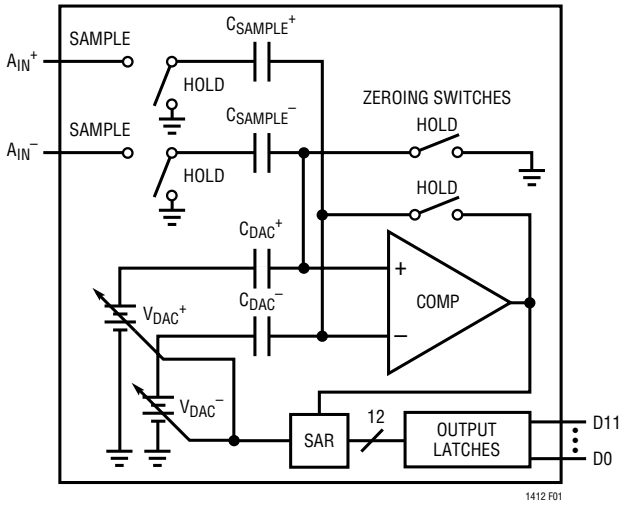


Figure 1. Simplified Block Diagram

sample-and-hold capacitors to acquire the analog signal. During the convert phase the comparator zeroing switches open, putting the comparator into compare mode. The input switches connect the C_{SAMPLE} capacitors to ground, transferring the differential analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the A_{IN}^+ and A_{IN}^- input charges. The SAR contents (a 12-bit data word) which represents the difference of A_{IN}^+ and A_{IN}^- are loaded into the 12-bit output latches.

Dynamic Performance

The LTC1412 has excellent high speed sampling capability. FFT (Fast Four Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1412 FFT plot.

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited

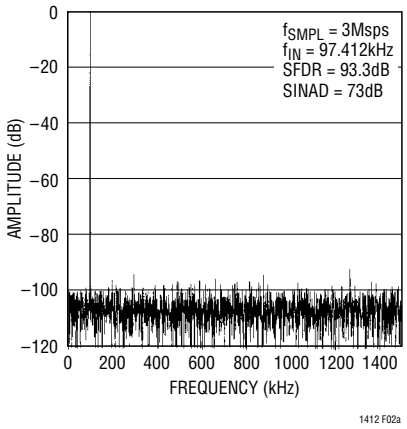


Figure 2a. LTC1412 Nonaveraged, 4096 Point FFT, Input Frequency = 100kHz

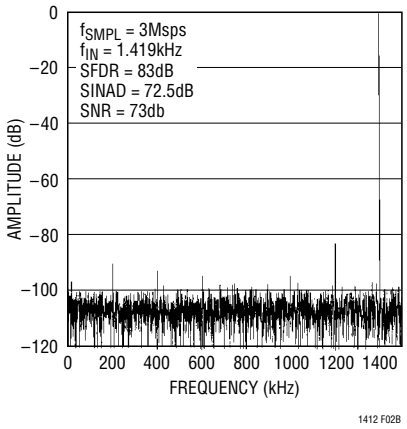


Figure 2b. LTC1412 Nonaveraged, 4096 Point FFT, Input Frequency = 1.45MHz

to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with a 3MHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to and beyond the Nyquist limit of 1.5MHz.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) – 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 3MHz the LTC1412 maintains near ideal ENOBs up to the Nyquist input frequency of 1.5MHz. Refer to Figure 3.

APPLICATIONS INFORMATION

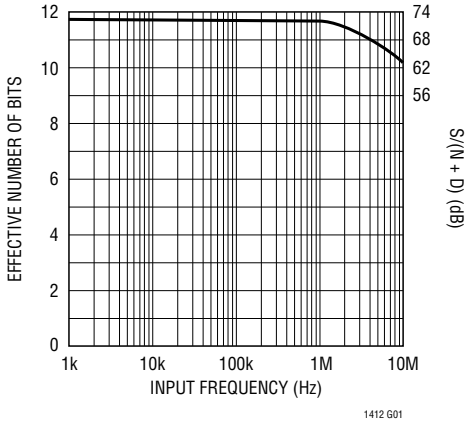


Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_n^2}}{V_1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through Nth harmonics. THD vs input frequency is shown in Figure 4. The LTC1412 has good distortion performance up to the Nyquist frequency and beyond.

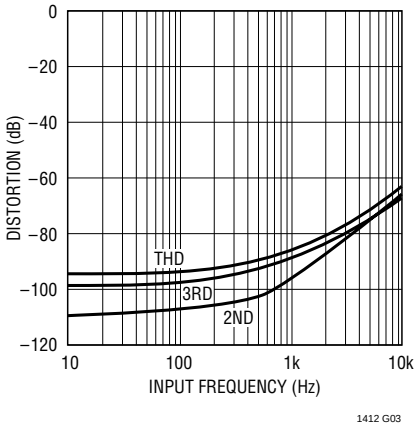


Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ±nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(f_a + f_b\right) = 20 \log \frac{\text{Amplitude at } \left(f_a \pm f_b\right)}{\text{Amplitude at } f_a}$$

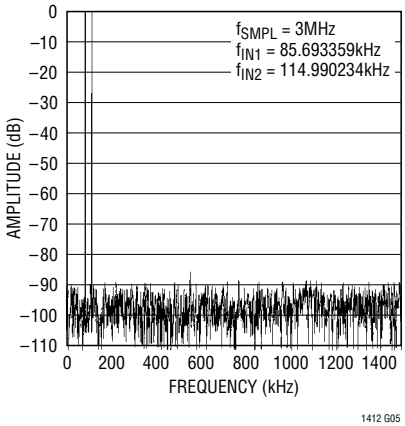


Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1412 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with fre-

APPLICATIONS INFORMATION

quencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The differential analog inputs of the LTC1412 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is grounded). The A_{IN}^+ and A_{IN}^- inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1412 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 6). For minimum acquisition time, with high source impedance, a buffer amplifier must be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 50ns for full throughput rate).

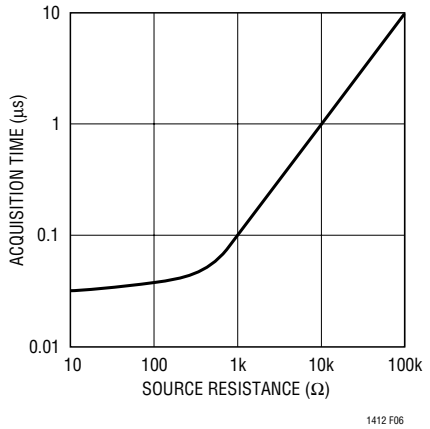


Figure 6. Acquisition Time vs Source Resistance

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz should be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 40MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1412 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1412. More detailed information is available in the Linear Technology Databooks and on the LinearView™ CD-ROM.

LT®1223: 100MHz Video Current Feedback Amplifier. 6mA supply current. ±5V to ±15V supplies. Low Noise. Good for AC applications.

LT1227: 140MHz Video Current Feedback Amplifier. 10mA supply current. ±5V to ±15V supplies. Low Noise. Best for AC applications.

LT1229/LT1230: Dual and Quad 100MHz Current Feedback Amplifiers. ±2V to ±15V supplies. Low Noise. Good AC specifications, 6mA supply current each amplifier.

LT1360: 50MHz Voltage Feedback Amplifier. 3.8mA supply current. ±5V to ±15V supplies. Good AC and DC specifications. 70ns settling to 0.5LSB.

LT1363: 70MHz, 1000V/µs Op Amps. 6.3mA supply current. Good AC and DC specifications. 60ns settling to 0.5LSB.

LT1364/LT1365: Dual and Quad 70MHz, 1000V/µs Op Amps. 6.3mA supply current per amplifier. 60ns settling to 0.5LSB.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1412 noise and distortion. The small-signal band-

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APPLICATIONS INFORMATION

width of the sample-and-hold circuit is 40MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

For example, Figure 7 shows a 500pF capacitor from A_{IN}^+ to ground and a 100Ω source resistor to limit the input bandwidth to 3.2MHz. The 500pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch-sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

When high amplitude unwanted signals are close in frequency to the desired signal frequency, a multiple pole filter is required. Figure 7b shows a simple implementation using an LTC1560-1 fifth-order elliptic continuous time filter.

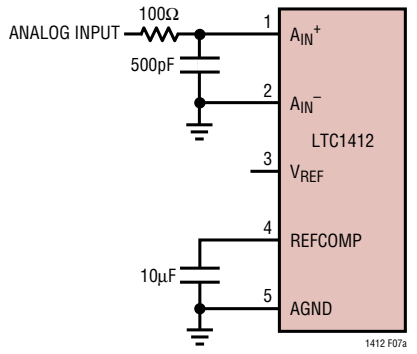


Figure 7a. RC Input Filter

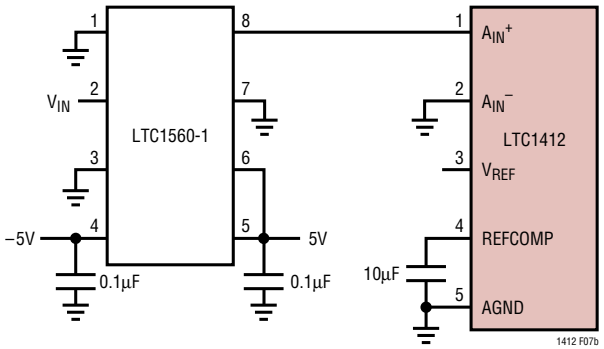


Figure 7b. 1MHz Fifth-Order Elliptic Lowpass Filter

Input Range

The ±2.5V input range of the LTC1412 is optimized for low noise and low distortion. Most op amps also perform best over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The LTC1412 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

Internal Reference

The LTC1412 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3), see Figure 8a. A 2k resistor is in series with the output so that it can be easily overdriven by an external reference or other circuitry, see Figure 8b. The reference amplifier gains the voltage at the V_{REF} pin by 1.625 to create the required internal reference voltage. This provides buffering between the V_{REF} pin and the high speed capacitive DAC. The reference amplifier compensation pin, REFCOMP (Pin 4) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or 10µF tantalum in parallel with a 0.1µF ceramic is recommended.

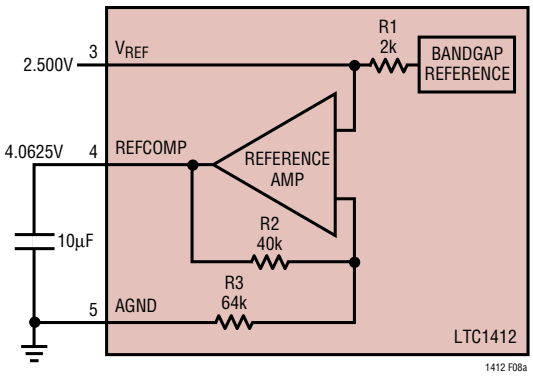


Figure 8a. LTC1412 Reference Circuit

APPLICATIONS INFORMATION

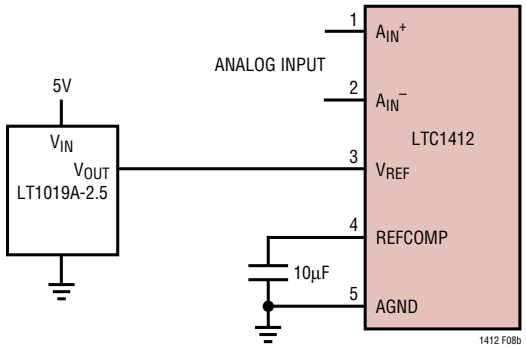


Figure 8b. Using the LT1019-2.5 as an External Reference

The V_{REF} pin can be driven with a DAC or other means shown in Figure 9. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal LTC1412 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 5ms should be allowed for after a reference adjustment.

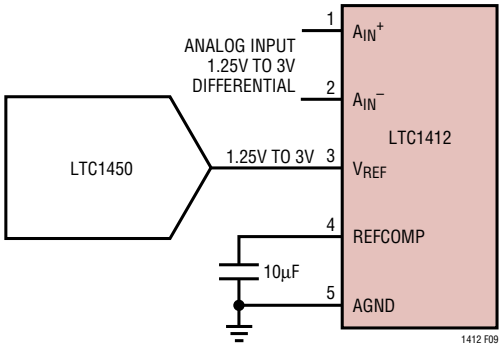


Figure 9. Driving V_{REF} with a DAC

Differential Inputs

The LTC1412 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of $A_{IN}^+ - (A_{IN}^-)$ independent of the common mode voltage. The common mode rejection holds up to extremely high frequencies, see Figure 10. The only requirement is that both inputs cannot exceed the AV_{DD} or AV_{SS} power supply voltages. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage, however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage. Dynamic performance is also affected by the common

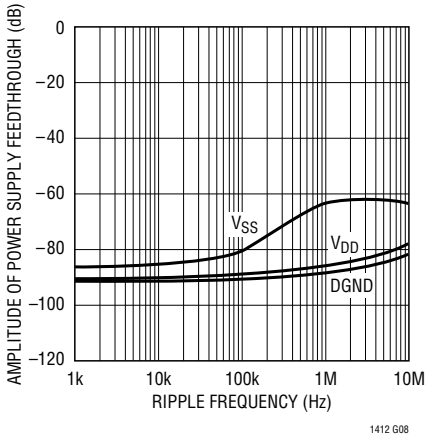


Figure 10. CMRR vs Input Frequency

mode voltage. THD will degrade as the inputs approach either power supply rail, from –86dB with a common mode of 0V to –75dB with a common mode of 2.5V or –2.5V.

Full-Scale and Offset Adjustment

Figure 11a shows the ideal input/output characteristics for the LTC1412. The code transitions occur midway between successive integer LSB values (i.e., –FS/2 + 0.5LSB, –FS/2 + 1.5LSB, –FS/2 + 2.5LSB,...FS/2 – 1.5LSB, FS/2 – 0.5LSB). The output is two's complement binary with 1LSB = FS – (–FS)/4096 = 5V/4096 = 1.22mV.

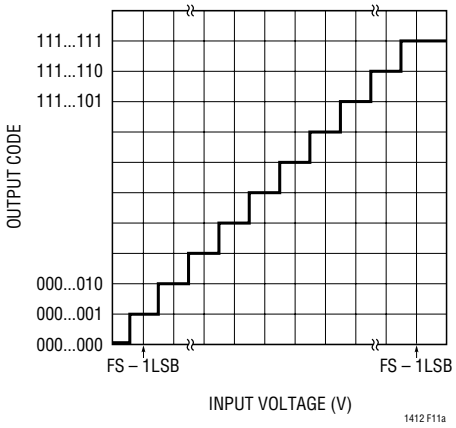


Figure 11a. LTC1412 Transfer Characteristics

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 11b shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error apply

APPLICATIONS INFORMATION

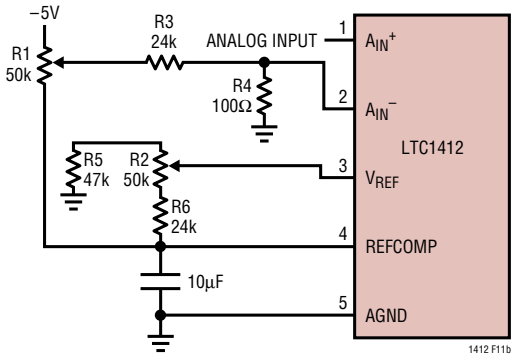


Figure 11b. Offset and Full-Scale Adjust Circuit

–0.61mV (i.e., –0.5LSB) at A_{IN}^+ and adjust the offset at the A_{IN}^- input until the output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.49817V (FS/2 – 1.5LSBs) is applied to A_{IN}^+ and R2 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

Board Layout and Bypassing

To obtain the best performance from the LTC1412, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital line alongside an analog signal line.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 5 (AGND), Pins 19 and 14 (DGND) and Pin 22 (OGND) and all other analog grounds should be connected to this single analog ground point. The REFCOMP bypass capacitor and the DV_{DD} bypass capacitor should also be connected to this analog ground plane, see Figure 12. All analog circuitry grounds should be terminated to this analog ground plane. The ground return from the ground plane to the power supply should be low impedance. Digital circuitry grounds must be connected to the digital supply common. Low impedance analog and digital power supply lines are essential to low noise operation of the ADC. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1412 has differential inputs to minimize noise coupling. Common mode noise on the A_{IN}^+ and A_{IN}^- leads will be rejected by the input CMRR. The A_{IN}^- input can be used as a ground sense for the A_{IN}^+ input; the LTC1412 will hold and convert the difference voltage between A_{IN}^+ and A_{IN}^-. The leads to A_{IN}^+ (Pin 1) and A_{IN}^- (Pin 2) should be kept as short as possible. In applications where this is not possible, the A_{IN}^+ and A_{IN}^- traces should be run side by side to equalize coupling.

Supply Bypassing

High quality, low series resistance ceramic, 10µF bypass capacitors should be used at the V_{DD} and REFCOMP pins. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Example Layout

Figures 13a, 13b, 13c and 13d show the schematic and layout of an evaluation board. The layout demonstrates the proper use of decoupling capacitors and ground plane with a two layer printed circuit board.

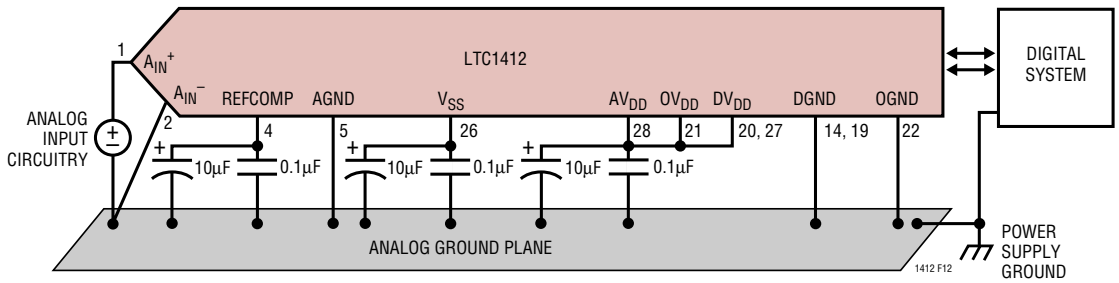


Figure 12. Power Supply Grounding Practice

APPLICATIONS INFORMATION

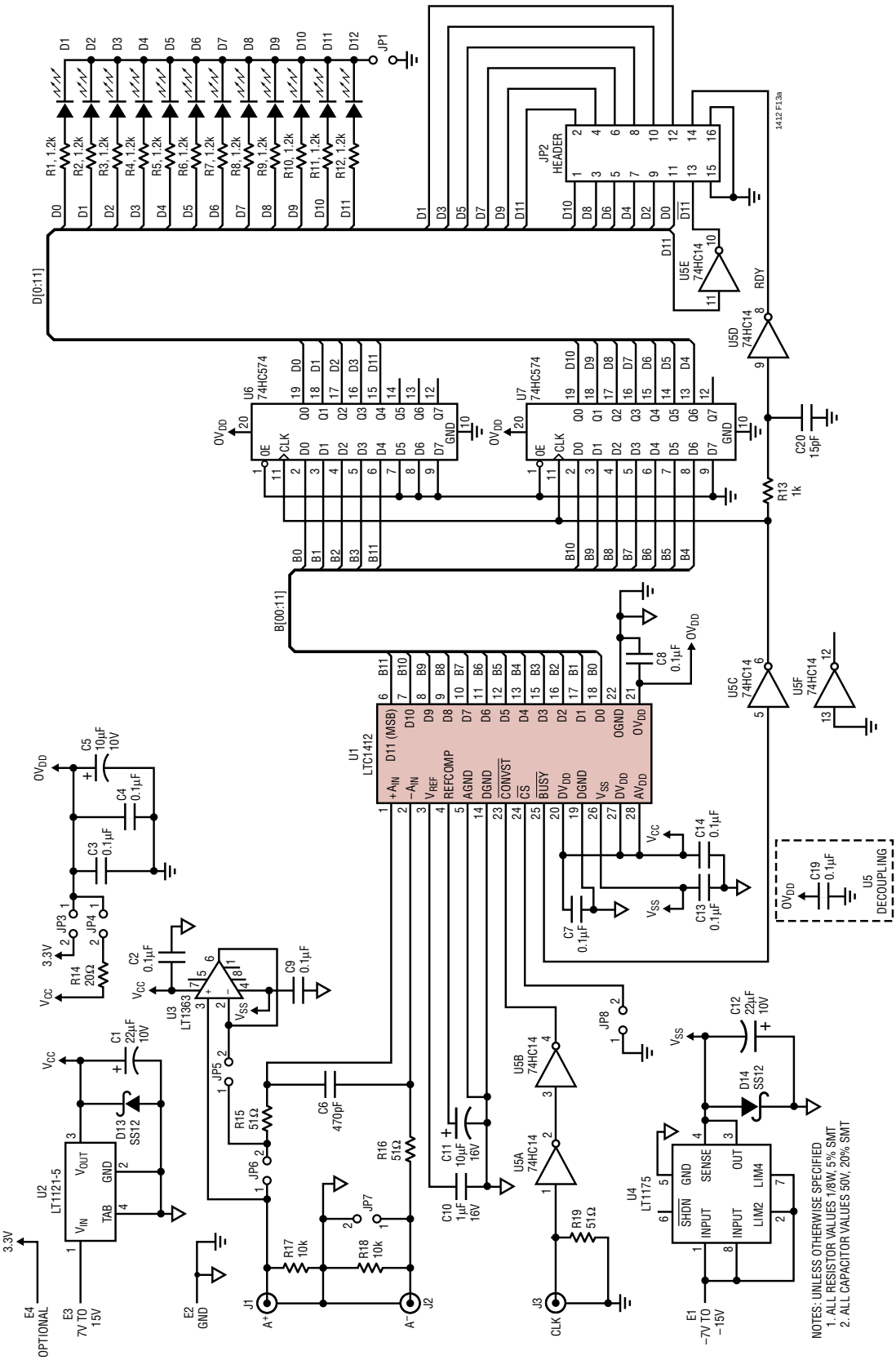


Figure 13a. LTC1412 Demonstration Board Features Analog Input Signal Buffer, 3Msps, Parallel Data Output 12-Bit ADC, Data Latches and LED Binary Data Display. Latched Conversion Data is Available on the 16-Pin Header, P2

APPLICATIONS INFORMATION

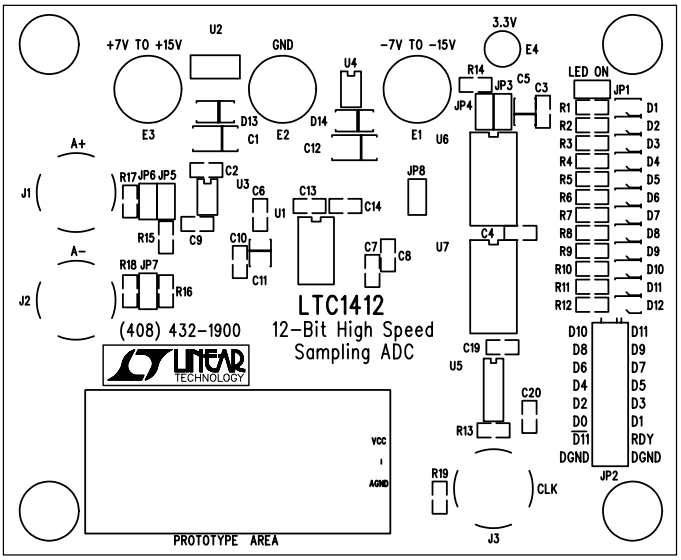


Figure 13b. Component Side Silkscreen

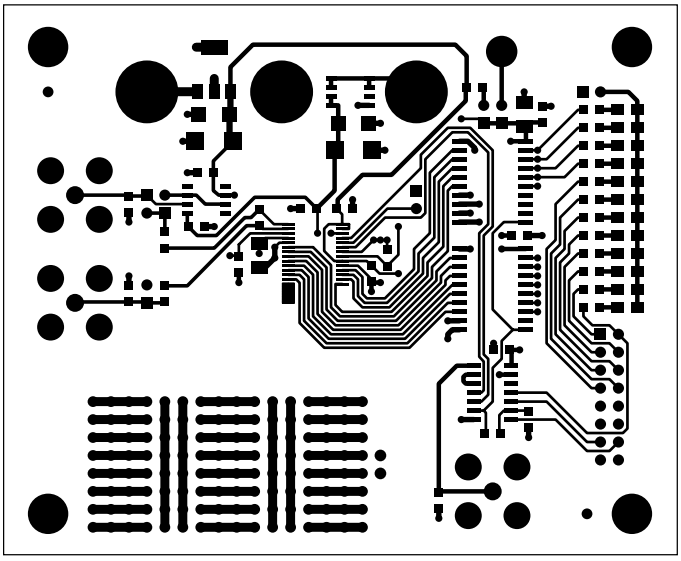


Figure 13c. Component Side

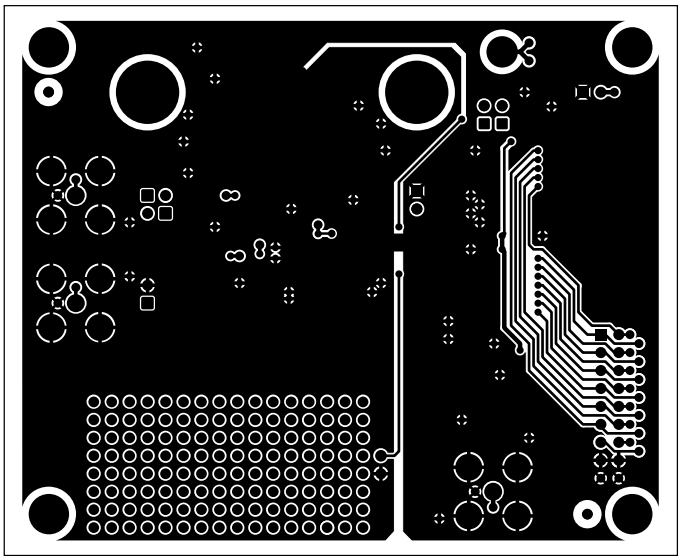
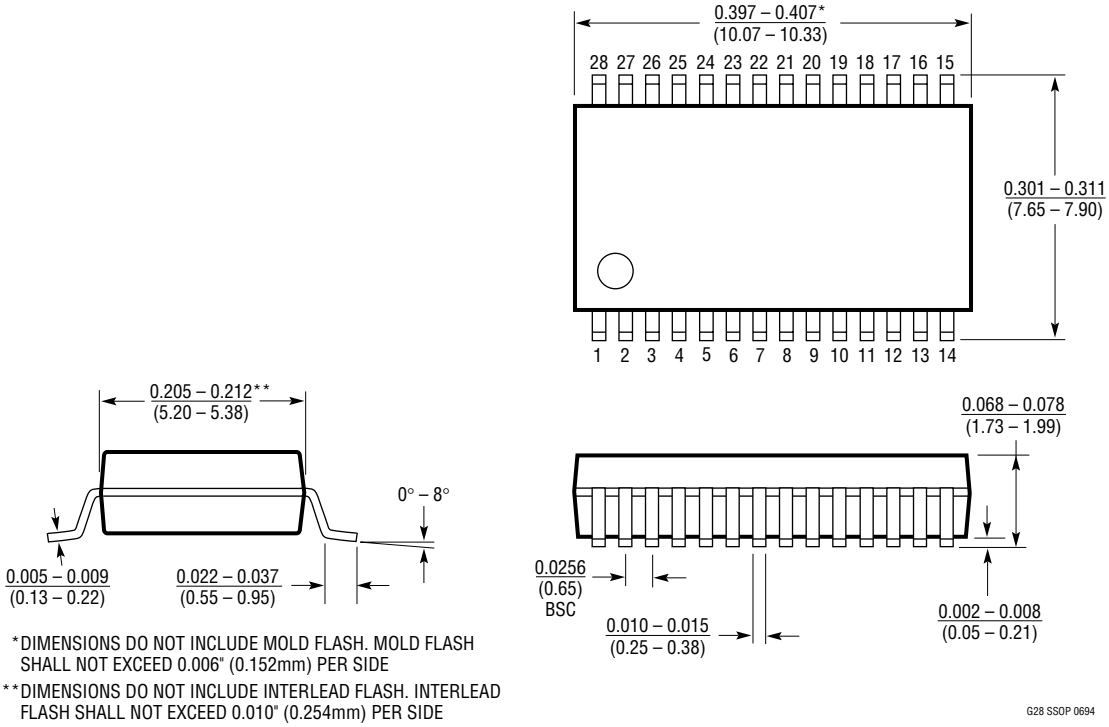


Figure 13d. Solder Side

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	RESOLUTION	SPEED	COMMENTS
16-Bit			
LTC1604	16	333ksps	±2.5V Input Range, ±5V Supply
LTC1605	16	100ksps	±10V Input Range, Single 5V Supply
14-Bit			
LTC1419	14	800ksps	150mW, 81.5dB SINAD and 95dB SFDR
LTC1416	14	400ksps	75mW, Low Power with Excellent AC Specs
LTC1418	14	200ksps	15mW, Single 5V, Serial/Parallel I/O
12-Bit			
LTC1410	12	1.25Msps	150mW, 71.5dB SINAD and 84dB THD
LTC1415	12	1.25Msps	55mW, Single 5V Supply
LTC1409	12	800ksps	80mW, 71.5dB SINAD and 84dB THD
LTC1279	12	600ksps	60mW, Single 5V or ±5V Supply
LTC1404	12	600ksps	High Speed Serial I/O in SO-8 Package
LTC1278-5	12	500ksps	75mW, Single 5V or ±5V Supply
LTC1278-4	12	400ksps	75mW, Single 5V or ±5V Supply
LTC1400	12	400ksps	High Speed Serial I/O in SO-8 Package

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