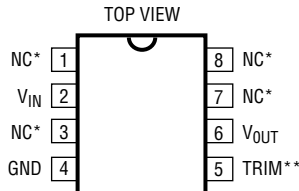
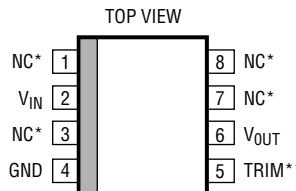


ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V	Output Short-Circuit Duration	
Input/Output Voltage Differential	35V	$V_{IN} = 35V$	10 sec
Output-to-Ground Voltage (Shunt Mode Current Limit)		$V_{IN} \leq 20V$	Indefinite
LT1236-5	10V	Operating Temperature Range	
LT1236-10	16V	LT1236AC, BC, CC	0°C to 70°C
Trim Pin-to-Ground Voltage		LT1236AI, BI, CI	–40°C to 85°C
Positive	Equal to V_{OUT}	Storage Temperature Range	–65°C to 150°C
Negative	–20V	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

 TOP VIEW NC* [1] [8] NC* V_{IN} [2] [7] NC* NC* [3] [6] V_{OUT} GND [4] [5] TRIM** N8 PACKAGE 8-LEAD PDIP *CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS **SEE APPLICATIONS INFORMATION SECTION $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$	ORDER PART NUMBER	 TOP VIEW NC* [1] [8] NC* V_{IN} [2] [7] NC* NC* [3] [6] V_{OUT} GND [4] [5] TRIM** S8 PACKAGE 8-LEAD PLASTIC SO *CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS **SEE APPLICATIONS INFORMATION SECTION $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 190^{\circ}C/W$	ORDER PART NUMBER
	LT1236ACN8-5 LT1236BCN8-5 LT1236CCN8-5 LT1236ACN8-10 LT1236BCN8-10 LT1236CCN8-10 LT1236AIN8-5 LT1236BIN8-5 LT1236CIN8-5 LT1236AIN8-10 LT1236BIN8-10 LT1236CIN8-10		LT1236ACS8-5 LT1236AIS8-5 LT1236BCS8-5 LT1236BIS8-5 LT1236CCS8-5 LT1236CIS8-5 LT1236ACS8-10 LT1236AIS8-10 LT1236BCS8-10 LT1236BIS8-10 LT1236CCS8-10 LT1236CIS8-10
		S8 PART MARKING	
		236AC5 236AI5 236BC5 236BI5 236CC5 236CI5 236AC1 236AI1 236BC1 236BI1 236CC1 236CI1	

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS $V_{IN} = 10V$, $I_{OUT} = 0$, $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	CONDITIONS	LT1236-5			UNITS
		MIN	TYP	MAX	
Output Voltage (Note 1)	LT1236A-5	4.9975	5.000	5.0025	V
	LT1236B-5/LT1236C-5	4.9950	5.000	5.0050	V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$				
	LT1236A-5		2	5	ppm/°C
	LT1236B-5		5	10	ppm/°C
	LT1236C-5		10	15	ppm/°C
Line Regulation (Note 3)	$7.2V \leq V_{IN} \leq 10V$		4	12	ppm/V
		●		20	ppm/V
	$10V \leq V_{IN} \leq 40V$		2	6	ppm/V
		●		10	ppm/V
Load Regulation (Sourcing Current) (Note 3)	$0 \leq I_{OUT} \leq 10mA$		10	20	ppm/mA
		●		35	ppm/mA

ELECTRICAL CHARACTERISTICS $V_{IN} = 10V$, $I_{OUT} = 0$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS		LT1236-5			UNITS
			MIN	TYP	MAX	
Load Regulation (Sinking Current) (Note 3)	$0 \leq I_{OUT} \leq 10mA$	●		60	100 150	ppm/mA ppm/mA
Supply Current		●		0.8	1.2 1.5	mA mA
Output Voltage Noise (Note 5)	$0.1Hz \leq f \leq 10Hz$ $10Hz \leq f \leq 1kHz$			3.0 2.2	3.5	μV_{P-P} μV_{RMS}
Long-Term Stability of Output Voltage (Note 6)	$\Delta t = 1000Hrs$ Non-Cumulative			20		ppm
Temperature Hysteresis of Output (Note 7)	$\Delta T = \pm 25^\circ C$			10		ppm

 $V_{IN} = 15V$, $I_{OUT} = 0$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS		LT1236-10			UNITS
			MIN	TYP	MAX	
Output Voltage (Note 1)	LT1236A-10 LT1236B-10/LT1236C-10		9.995 9.990	10.000	10.005 10.010	V V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$ LT1236A-10 LT1236B-10 LT1236C-10			2 5 10	5 10 15	ppm/ $^\circ C$ ppm/ $^\circ C$ ppm/ $^\circ C$
Line Regulation (Note 3)	$11.5V \leq V_{IN} \leq 14.5V$	●		1.0	4	ppm/V
	$14.5V \leq V_{IN} \leq 40V$	●		0.5	6 2 4	ppm/V ppm/V ppm/V
Load Regulation (Sourcing Current) (Note 3)	$0 \leq I_{OUT} \leq 10mA$	●		12	25 40	ppm/mA ppm/mA
Load Regulation (Shunt Mode) (Notes 3, 4)	$1.7mA \leq I_{SHUNT} \leq 10mA$	●		50	100 150	ppm/mA ppm/mA
Series Mode Supply Current		●		1.2	1.7 2.0	mA mA
Shunt Mode Minimum Current	V_{IN} is Open	●		1.1	1.5 1.7	mA mA
Output Voltage Noise (Note 5)	$0.1Hz \leq f \leq 10Hz$ $10Hz \leq f \leq 1kHz$			6.0 3.5	6	μV_{P-P} μV_{RMS}
Long-Term Stability of Output Voltage (Note 6)	$\Delta t = 1000Hrs$ Non-Cumulative			30		ppm
Temperature Hysteresis of Output (Note 7)	$\Delta T = \pm 25^\circ C$			5		ppm

The ● denotes specifications which apply over the specified temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature. **Incremental slope is also measured at 25°C.**

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

Note 5: RMS noise is measured with a 2-pole highpass filter at 10Hz and a 2-pole lowpass filter at 1kHz. The resulting output is full-wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. Correction factors are used to convert from average to RMS, and 0.88 is used to correct for the non-ideal bandpass of the filters. Peak-to-peak noise is measured with a single highpass filter at 0.1Hz and a 2-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

Note 6: Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours, with a continuing trend toward reduced drift with time. Significant improvement in long-term drift can be

ELECTRICAL CHARACTERISTICS

$V_{IN} = 15V$, $I_{OUT} = 0$, $T_A = 25^\circ C$, unless otherwise noted.

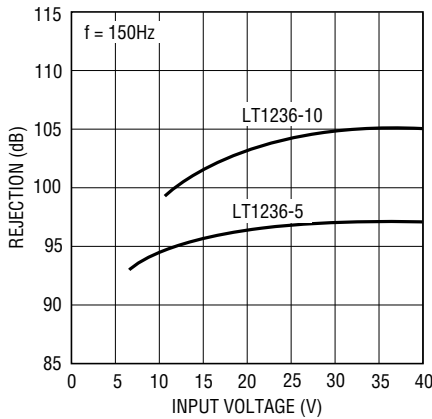
realized by preconditioning the IC with a 100-200 hour, $125^\circ C$ burn in. Long term stability will also be affected by differential stresses between the IC and the board material created during board assembly. Temperature cycling and baking of completed boards is often used to reduce these stresses in critical applications.

Note 7: Hysteresis in output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower

temperature. Output voltage is always measured at $25^\circ C$, but the IC is cycled to $50^\circ C$ or $0^\circ C$ before successive measurements. Hysteresis is roughly proportional to the square of temperature change. Hysteresis is not normally a problem for operational temperature excursions, but can be significant in critical narrow temperature range applications where the instrument might be stored at high or low temperatures.

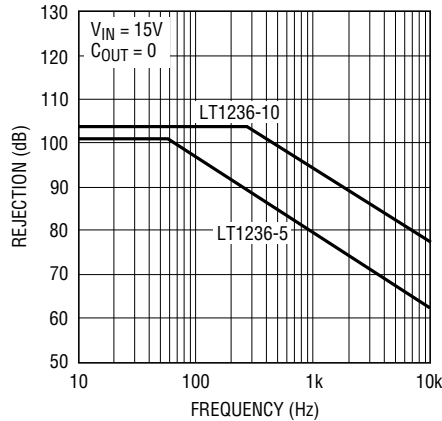
TYPICAL PERFORMANCE CHARACTERISTICS

Ripple Rejection



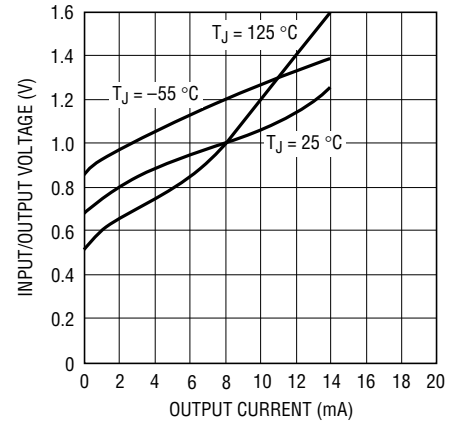
LT1236 G01

Ripple Rejection



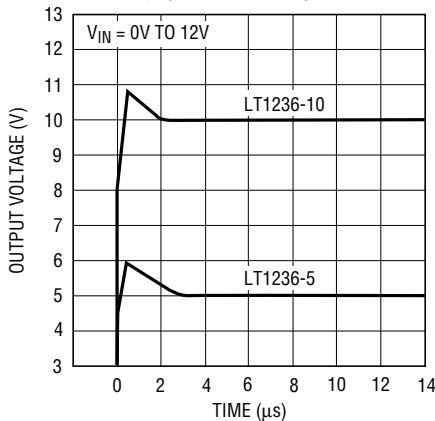
LT1236 G02

Minimum Input/Output Differential, LT1236-10



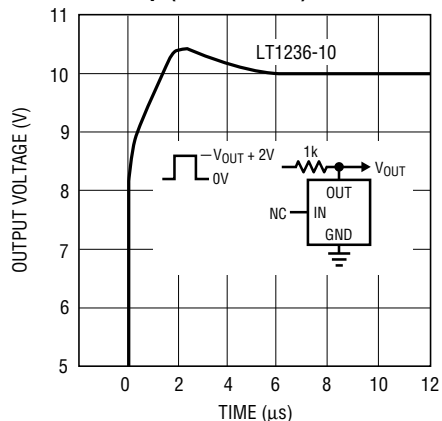
LT1236 G03

Start-Up (Series Mode)



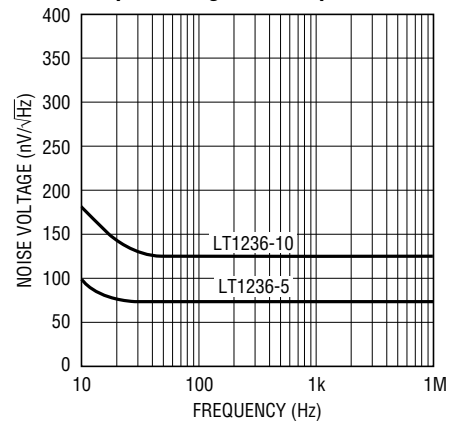
LT1236 G04

Start-Up (Shunt Mode), LT1236-10



LT1236 G05

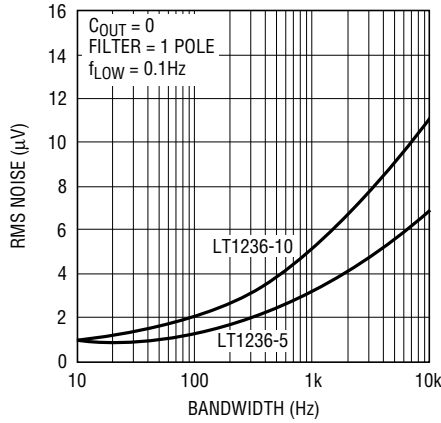
Output Voltage Noise Spectrum



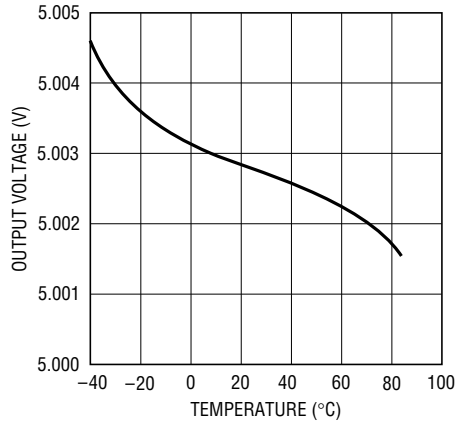
LT1236 G06

TYPICAL PERFORMANCE CHARACTERISTICS

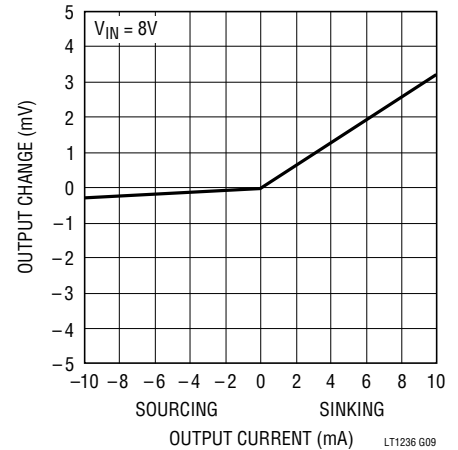
Output Voltage Noise



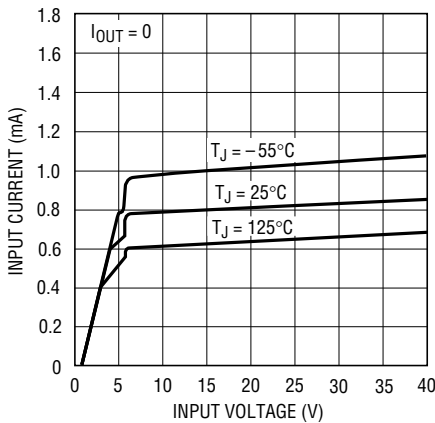
Output Voltage Temperature Drift
LT1236-5



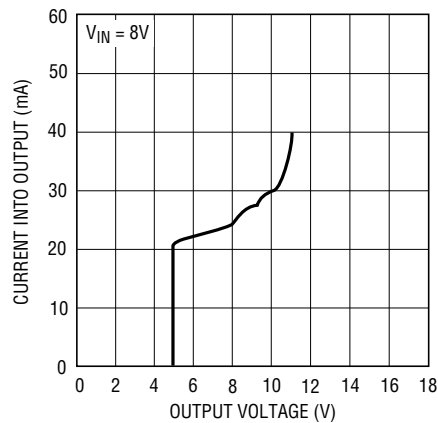
Load Regulation LT1236-5



Quiescent Current, LT1236-5

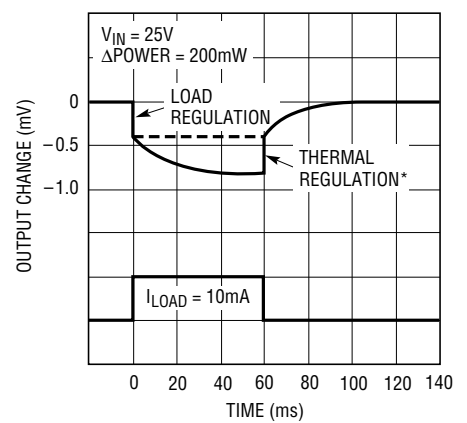


Sink Mode* Current Limit,
LT1236-5



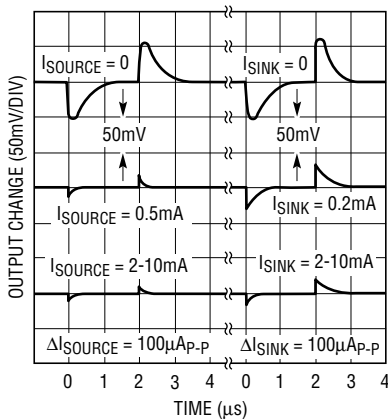
*NOTE THAT AN INPUT VOLTAGE IS REQUIRED FOR 5V UNITS.

Thermal Regulation, LT1236-5

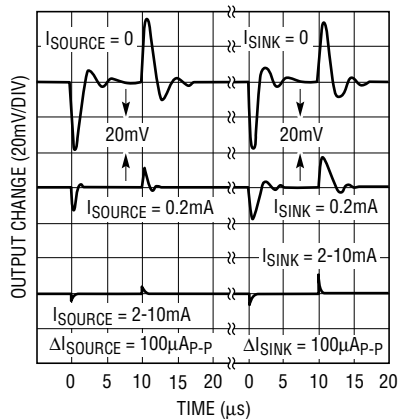


*INDEPENDENT OF TEMPERATURE COEFFICIENT

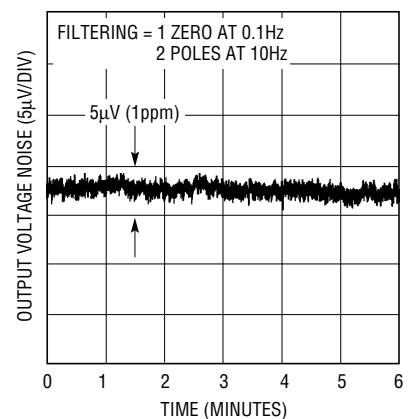
Load Transient Response,
LT1236-5, CLOAD = 0



Load Transient Response,
LT1236-5, CLOAD = 1000pF

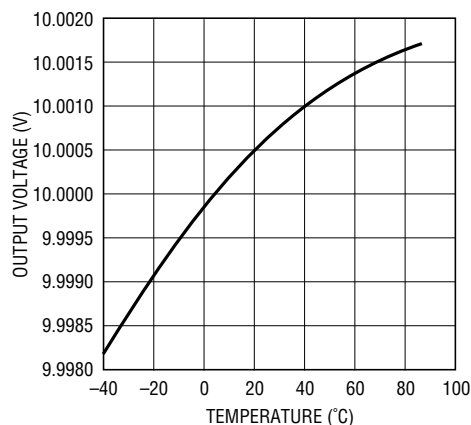


Output Noise 0.1Hz to 10Hz,
LT1236-5



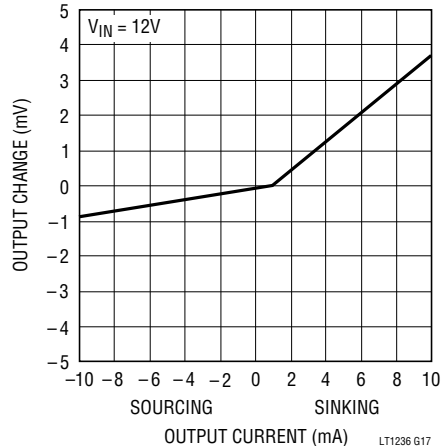
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Temperature Drift, LT1236-10



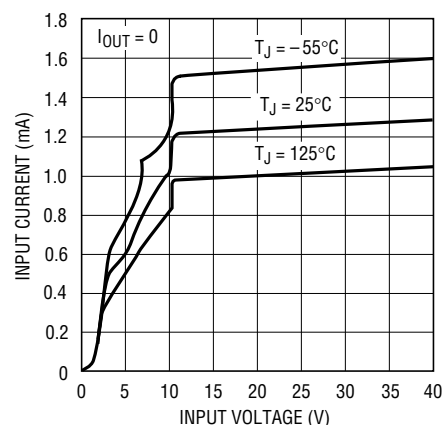
LT1236 G16

Load Regulation, LT1236-10



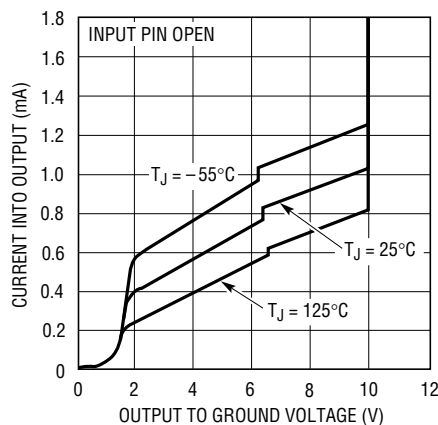
LT1236 G17

Input Supply Current, LT1236-10



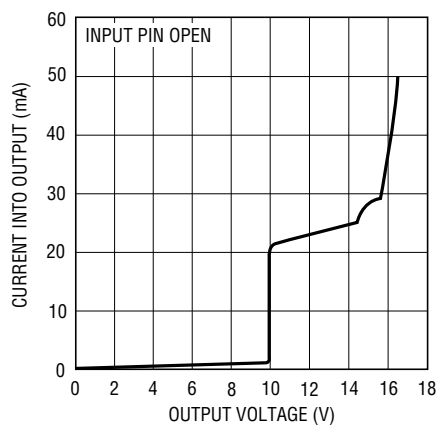
LT1236 G18

Shunt Characteristics, LT1236-10



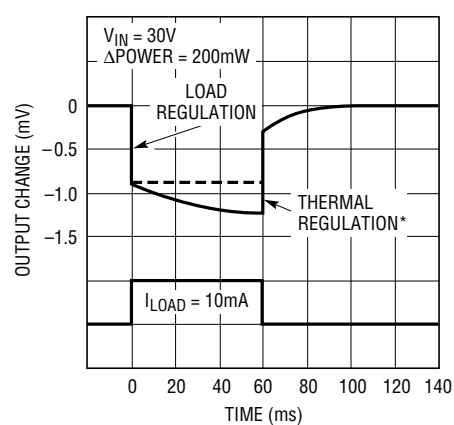
LT1236 G19

Shunt Mode Current Limit, LT1236-10



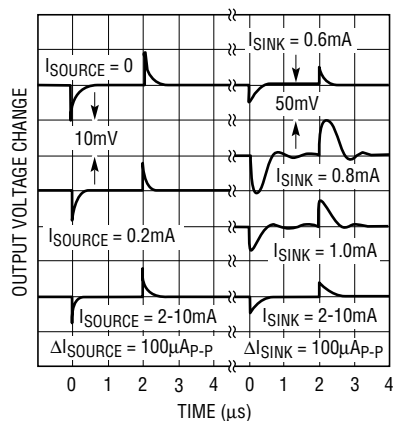
LT1236 G20

Thermal Regulation, LT1236-10



*INDEPENDENT OF TEMPERATURE COEFFICIENT
LT1236 G21

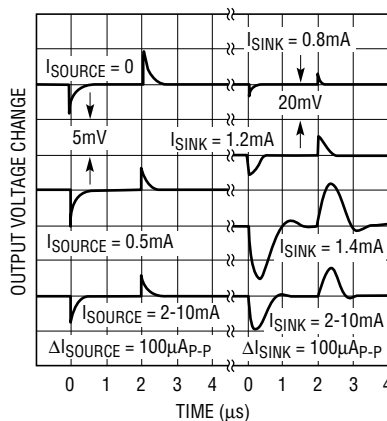
Load Transient Response, LT1236-10, C_{LOAD} = 0



NOTE VERTICAL SCALE CHANGE
BETWEEN SOURCING AND SINKING

LT1236 G22

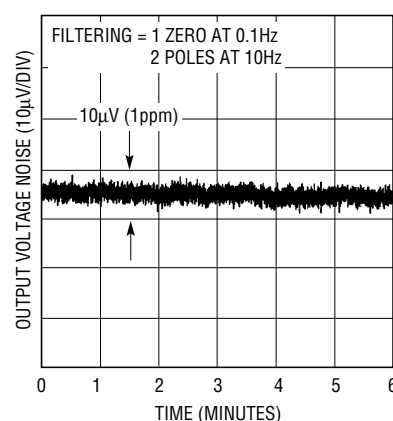
Load Transient Response, LT1236-10, C_{LOAD} = 1000pF



NOTE VERTICAL SCALE CHANGE
BETWEEN SOURCING AND SINKING

LT1236 G23

Output Noise 0.1Hz to 10Hz, LT1236-10

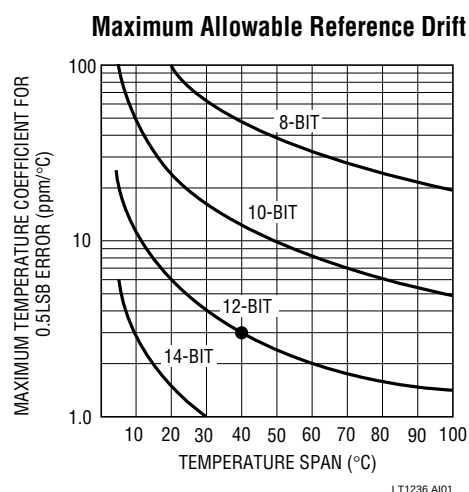


LT1236 G24

APPLICATIONS INFORMATION

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. This graph indicates the maximum temperature coefficient allowable if the reference is to contribute no more than 0.5LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 3ppm/°C if it is to contribute less than 0.5LSB error. For this reason, the LT1236 family has been optimized for low drift.



Trimming Output Voltage

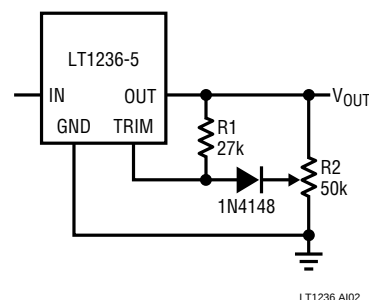
The LT1236-10 has a trim pin for adjusting output voltage. The impedance of the trim pin is about 12kΩ with a nominal open circuit voltage of 5V. It is designed to be driven from a source impedance of 3kΩ or less to minimize changes in the LT1236 TC with output trimming. Attenuation between the trim pin and the output is 70:1. This allows ±70mV trim range when the trim pin is tied to the wiper of a potentiometer connected between the output and ground. A 10kΩ potentiometer is recommended, preferably a 20 turn cermet type with stable characteristics over time and temperature.

The LT1236-10 “A” version is pre-trimmed to ±5mV and therefore can utilize a restricted trim range. A 75k resistor

in series with a 20kΩ potentiometer will give ±10mV trim range. Effect on the output TC will be only 1ppm/°C for the ±5mV trim needed to set the “A” device to 10.000V.

LT1236-5

The LT1236-5 does have an output voltage trim pin, but the TC of the nominal 4V open circuit voltage at pin 5 is about -1.7mV/°C. For the voltage trimming not to affect reference output TC, the external trim voltage must track the voltage on the trim pin. Input impedance of the trim pin is about 100kΩ and attenuation to the output is 13:1. The technique shown below is suggested for trimming the output of the LT1236-5 while maintaining minimum shift in output temperature coefficient. The R1/R2 ratio is chosen to minimize interaction of trimming and TC shifts, so the exact values shown should be used.



Capacitive Loading and Transient Response

The LT1236 is stable with all capacitive loads, but for optimum settling with load transients, output capacitance should be under 1000pF. The output stage of the reference is class AB with a fairly low idling current. This makes transient response worse-case at light load currents. Because of internal current drain on the output, actual worst-case occurs at $I_{LOAD} = 0$ on LT1236-5 and $I_{LOAD} = 1.4\text{mA}$ (sinking) on LT1236-10. Significantly better load transient response is obtained by moving slightly away from these points. See Load Transient Response curves for details. In general, best transient response is obtained when the output is sourcing current. In critical applications, a 10μF solid tantalum capacitor with several ohms in series provides optimum output bypass.

APPLICATIONS INFORMATION

Kelvin Connections

Although the LT1236 does not have true force/sense capability at its outputs, significant improvements in ground loop and line loss problems can be achieved with proper hook-up. In series mode operation, the ground pin of the LT1236 carries only $\approx 1\text{mA}$ and can be used as a sense line, greatly reducing ground loop and loss problems on the low side of the reference. The high side supplies load current so line resistance must be kept low. Twelve feet of #22 gauge hook-up wire or 1 foot of 0.025 inch printed circuit trace will create 2mV loss at 10mA output current. This is equivalent to 1LSB in a 10V, 12-bit system.

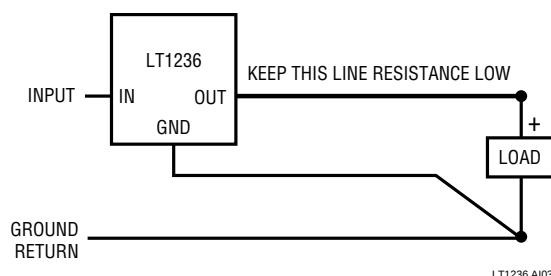
The following circuits show proper hook-up to minimize errors due to ground loops and line losses. Losses in the output lead can be greatly reduced by adding a PNP boost transistor if load currents are 5mA or higher. R2 can be added to further reduce current in the output sense lead.

Effects of Air Movement on Low Frequency Noise

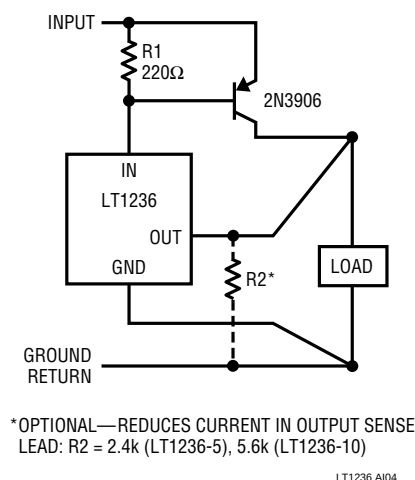
The LT1236 has very low noise because of the buried zener used in its design. In the 0.1Hz to 10Hz band, peak-to-peak noise is about 0.5ppm of the DC output. To achieve this low noise, however, care must be taken to shield the reference from ambient air turbulence. Air movement can create noise because of thermoelectric differences between IC package leads and printed circuit board materials and/or sockets. Power dissipation in the reference, even though it rarely exceeds 20mW, is enough to cause small

temperature gradients in the package leads. Variations in thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference.

Standard Series Mode

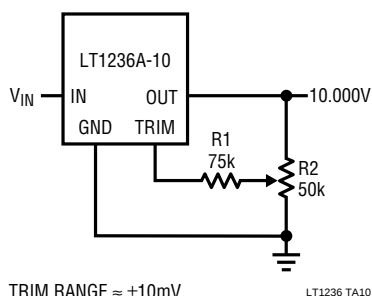


Series Mode with Boost Transistor

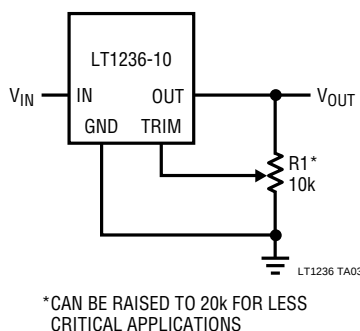


TYPICAL APPLICATIONS

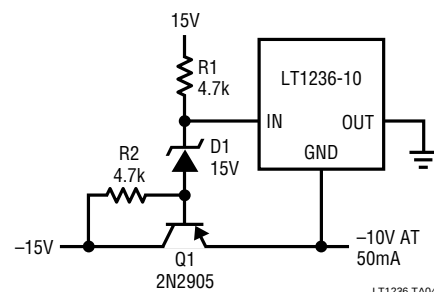
Restricted Trim Range for Improved Resolution, 10V, "A" Version Only



LT1236-10 Full Trim Range ($\pm 0.7\%$)

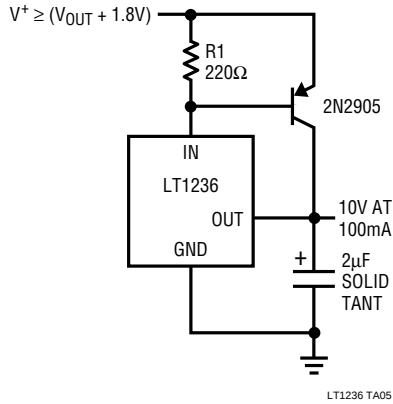


Negative Series Reference

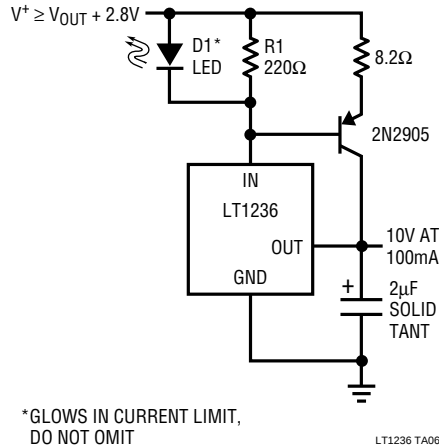


TYPICAL APPLICATIONS

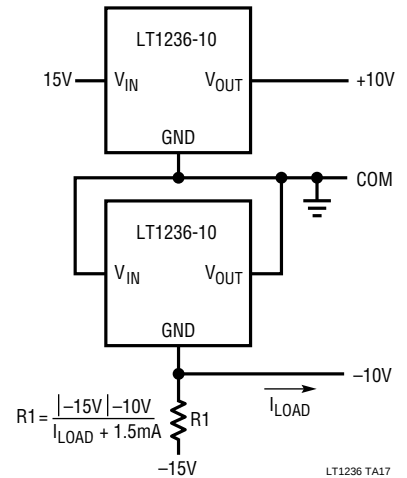
Boosted Output Current with No Current Limit



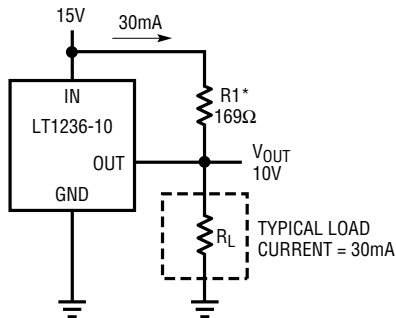
Boosted Output Current with Current Limit



±10V Output Reference

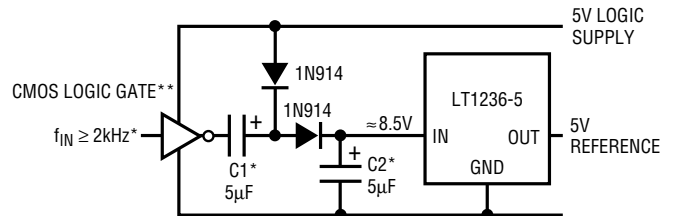


Handling Higher Load Currents



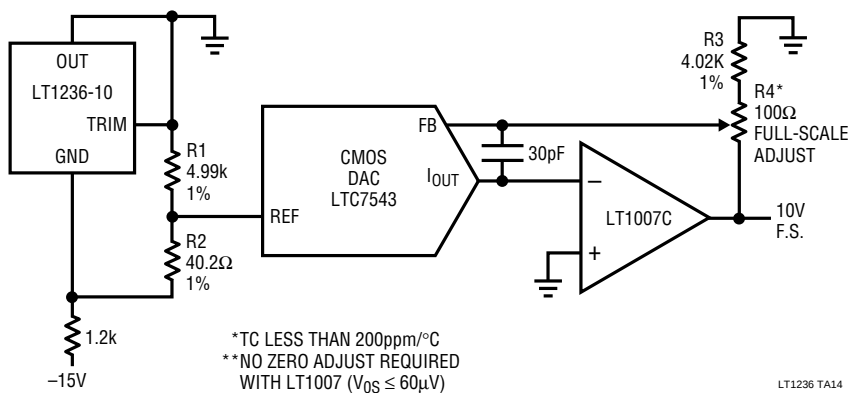
*SELECT R1 TO DELIVER TYPICAL LOAD CURRENT. LT1236 WILL THEN SOURCE OR SINK AS NECESSARY TO MAINTAIN PROPER OUTPUT. DO NOT REMOVE LOAD AS OUTPUT WILL BE DRIVEN UNREGULATED HIGH. LINE REGULATION IS DEGRADED IN THIS APPLICATION

Operating 5V Reference from 5V Supply

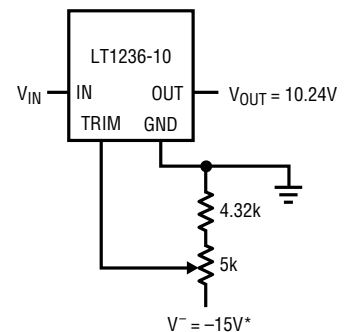


*FOR HIGHER FREQUENCIES C1 AND C2 MAY BE DECREASED
**PARALLEL GATES FOR HIGHER REFERENCE CURRENT LOADING

CMOS DAC with Low Drift Full-Scale Trimming**



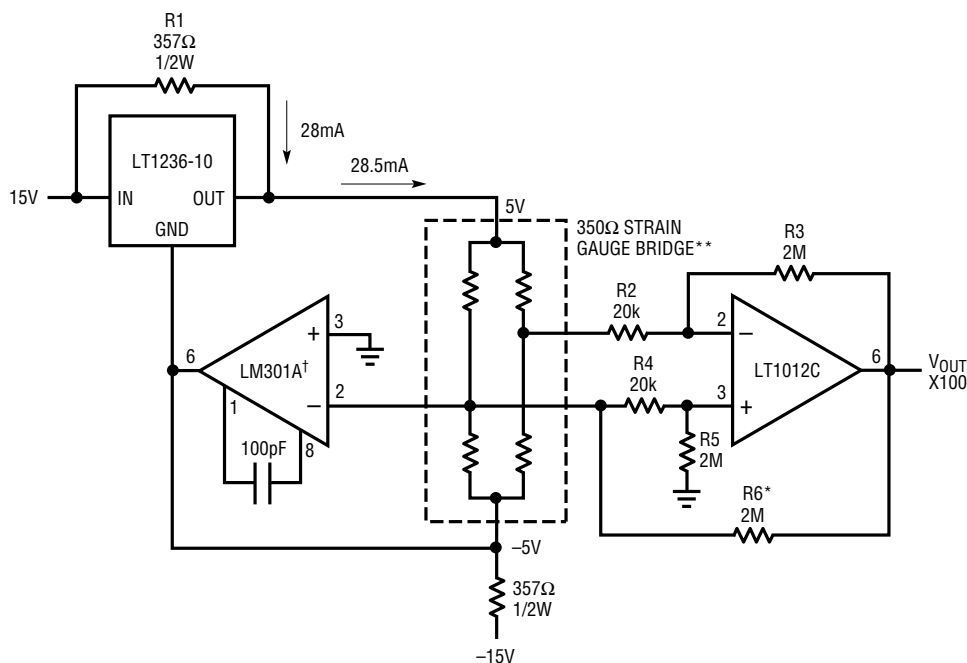
Trimming 10V Units to 10.24V



*MUST BE WELL REGULATED
 $\frac{dV_{OUT}}{dV^-} = \frac{15mV}{V}$

TYPICAL APPLICATIONS

Strain Gauge Conditioner for 350Ω Bridge



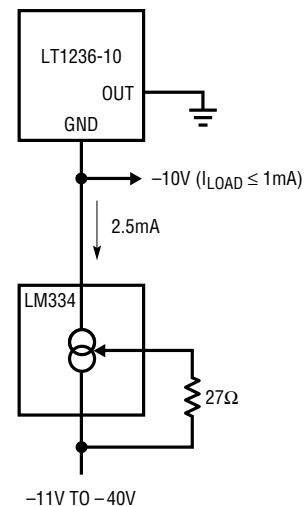
*THIS RESISTOR PROVIDES POSITIVE FEEDBACK TO THE BRIDGE TO ELIMINATE LOADING EFFECT OF THE AMPLIFIER. EFFECTIVE Z_{IN} OF AMPLIFIER STAGE IS $\geq 1M\Omega$. IF R2 TO R5 ARE CHANGED, SET R6 = R3

**BRIDGE IS ULTRA-LINEAR WHEN ALL LEGS ARE ACTIVE, TWO IN COMPRESSION AND TWO IN TENSION, OR WHEN ONE SIDE IS ACTIVE WITH ONE COMPRESSED AND ONE TENSIONED LEG

†OFFSET AND DRIFT OF LM301A ARE VIRTUALLY ELIMINATED BY DIFFERENTIAL CONNECTION OF LT1012C

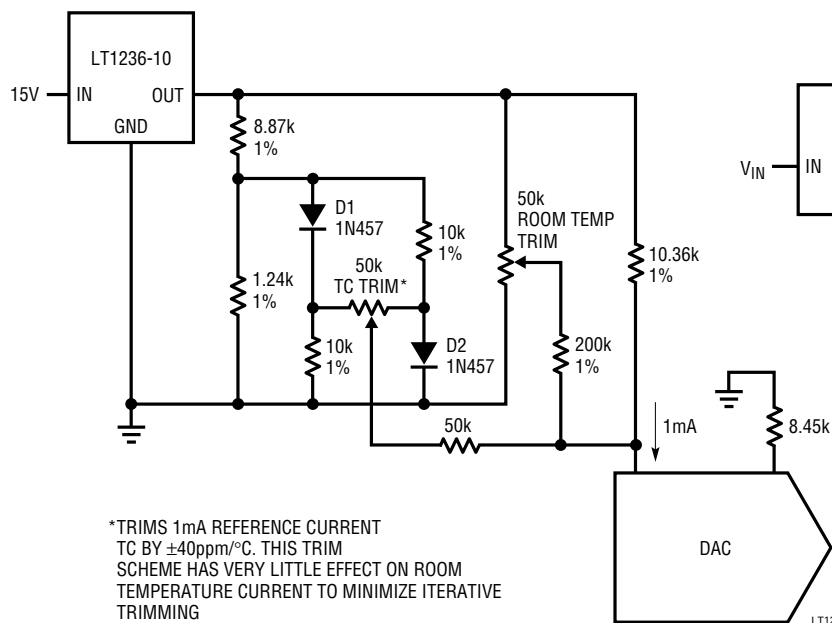
LT1236 TA08

Negative Shunt Reference Driven by Current Source



LT1236 TA13

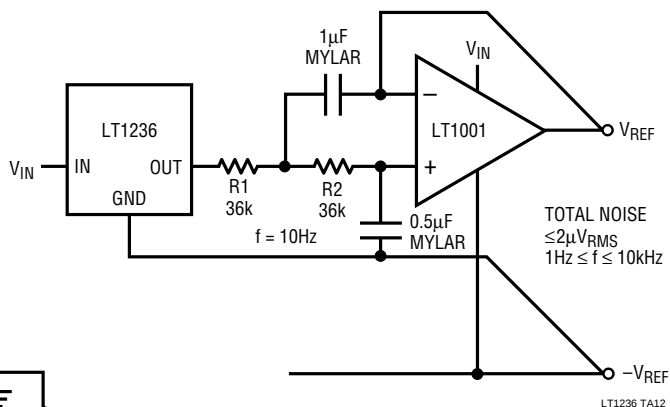
Precision DAC Reference with System TC Trim



*TRIMS 1mA REFERENCE CURRENT TC BY $\pm 40\text{ppm}/^\circ\text{C}$. THIS TRIM SCHEME HAS VERY LITTLE EFFECT ON ROOM TEMPERATURE CURRENT TO MINIMIZE ITERATIVE TRIMMING

LT1236 TA16

2-Pole Lowpass Filtered Reference

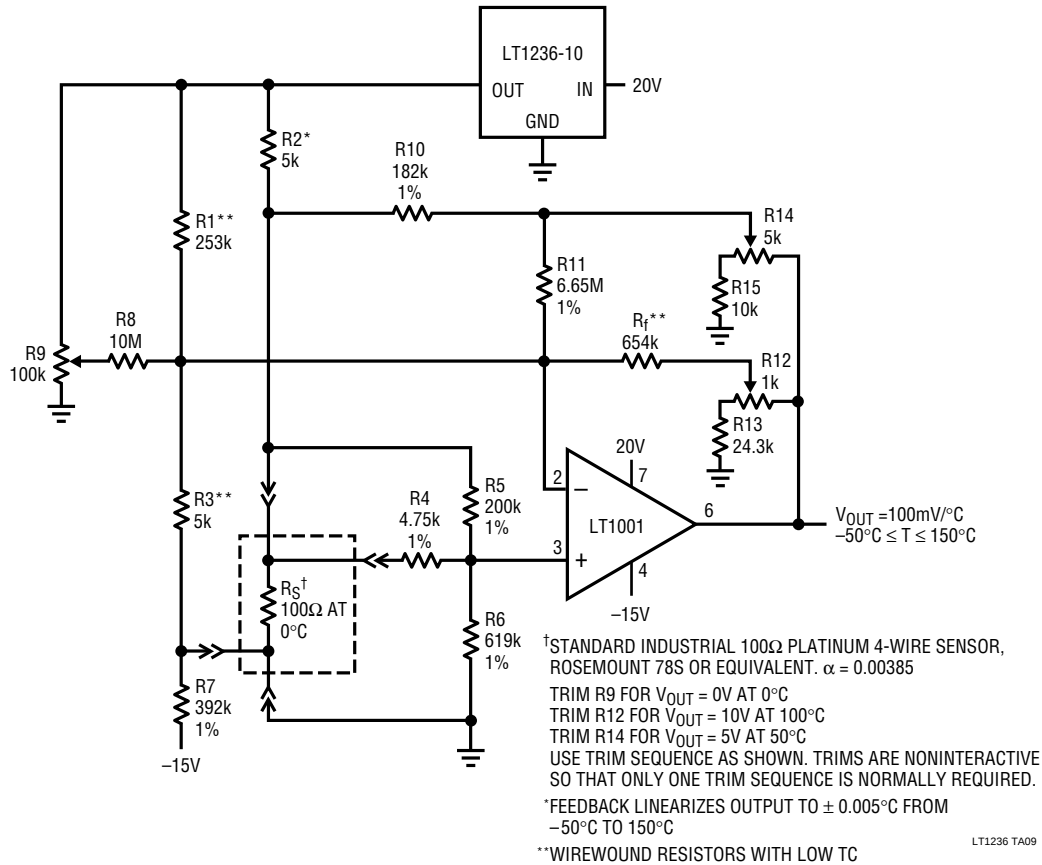


TOTAL NOISE $\leq 2\mu\text{VRMS}$
 $1\text{Hz} \leq f \leq 10\text{kHz}$

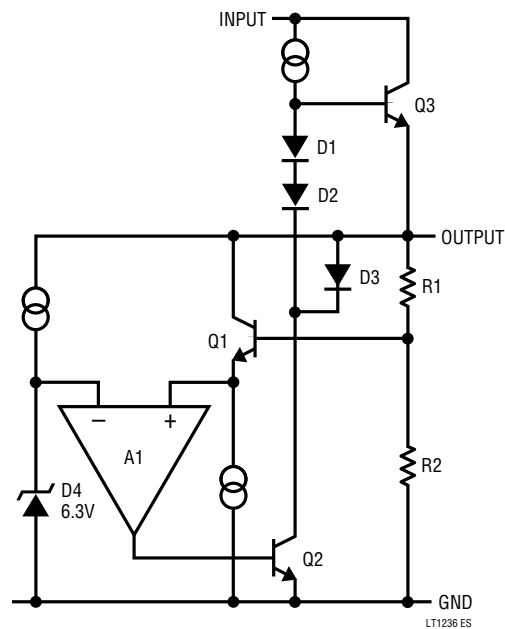
LT1236 TA12

TYPICAL APPLICATIONS

Ultra-Linear Platinum Temperature Sensor*

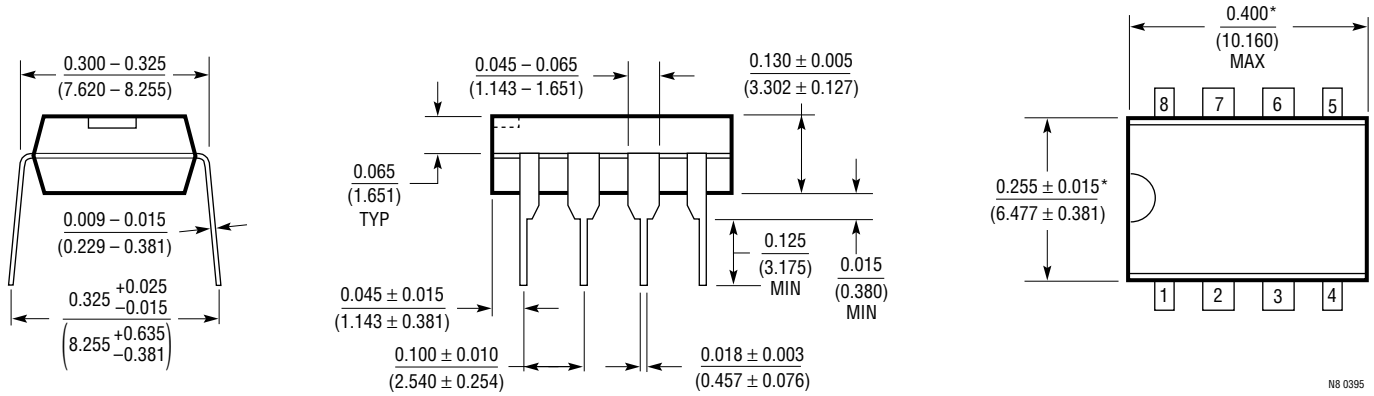


EQUIVALENT SCHEMATIC



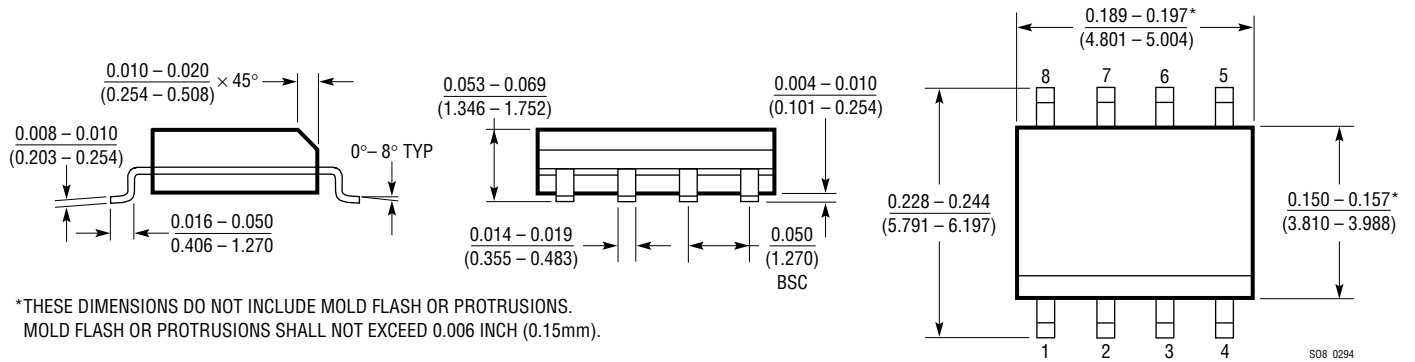
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N8 Package 8-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

S8 Package 8-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Bandgap Reference	0.05%, 5ppm/°C
LT1027	Precision 5V Reference	0.02%, 2ppm/°C