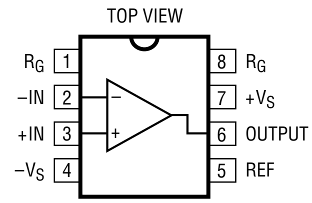
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage .... ±20V
Differential Input Voltage (Within the
Supply Voltage) .... ±40V
Input Voltage (Equal to Supply Voltage) .... ±20V
Input Current (Note 2) .... ±20mA
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range
  LT1168AC/LT1168C (Note 5) .... –40°C to 85°C
  LT1168AI/LT1168I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX} = 150°C, \theta_{JA} = 150°C/W$ (N8)
$T_{JMAX} = 150°C, \theta_{JA} = 190°C/W$ (S8)

ORDER PART NUMBER
LT1168ACN8
LT1168ACS8
LT1168AIN8
LT1168AIS8
LT1168CN8
LT1168CS8
LT1168IN8
LT1168IS8

S8 PART MARKING	
1168A	1168
1168AI	1168I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$. $V_S = ±15V$, $V_{CM} = 0V$, $R_L = 10k$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	LT1168AC/LT1168AI MIN	TYP	MAX	LT1168C/LT1168I MIN	TYP	MAX	UNITS
G	Gain Range	$G = 1 + (49.4k/R_G)$	1		10k	1		10k	
	Gain Error	G = 1		0.008	0.02		0.015	0.03	%
		G = 10 (Note 7)		0.04	0.4		0.05	0.5	%
		G = 100 (Note 7)		0.04	0.5		0.05	0.6	%
		G = 1000 (Note 7)		0.08	0.5		0.08	0.6	%
	Gain Nonlinearity (Notes 7, 8)	$V_O = ±10V$, G = 1		2	6		3	10	ppm
		$V_O = ±10V$,G = 10 and 100		10	20		15	25	ppm
		$V_O = ±10V$, G = 1000		20	40		25	60	ppm
		$V_O = ±10V$, G = 1, $R_L = 2k$		4	15		5	20	ppm
		$V_O = ±10V$,G = 10 and 100, $R_L = 2k$		20	40		30	60	ppm
		$V_O = ±10V$, G = 1000, $R_L = 2k$		40	75		50	90	ppm
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$							
V_{OSI}	Input Offset Voltage	G = 1000, $V_S = ±5V$ to ±15V		15	40		20	60	µV
V_{OSO}	Output Offset Voltage	G = 1, $V_S = ±5V$ to ±15V		40	200		50	300	µV
I_{OS}	Input Offset Current			50	300		60	450	pA
I_B	Input Bias Current			40	250		80	500	pA
e_n	Input Noise Voltage, RTI	0.1Hz to 10Hz, G = 1		2.00			2.00		$µV_{P-P}$
		0.1Hz to 10Hz, G = 1000		0.28			0.28		$µV_{P-P}$
	Input Noise Voltage Density, RTI	$f_O = 1kHz$		10	15		10	15	$nV/\sqrt{Hz}$
	Output Noise Voltage Density, RTI	$f_O = 1kHz$ (Note 9)		165	220		165	220	$nV/\sqrt{Hz}$
i_n	Input Noise Current	$f_O = 0.1Hz$ to 10Hz		5			5		pA_{P-P}
	Input Noise Current Density	$f_O = 10Hz$		74			74		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{IN} = ±10V$	300	1250		200	1250		GΩ

ELECTRICAL CHARACTERISTICS $T_A = 25°C$. $V_S = ±15V$, $V_{CM} = 0V$, $R_L = 10k$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	LT1168AC/LT1168AI MIN	TYP	MAX	LT1168C/LT1168I MIN	TYP	MAX	UNITS
$C_{IN(DIFF)}$	Differential Input Capacitance	f_O = 100kHz		1.6			1.6		pF
$C_{IN(CM)}$	Common Mode Input Capacitance	f_O = 100kHz		1.6			1.6		pF
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded V_S = ±2.3V to ±5V V_S = ±5V to ±18V	 $-V_S + 1.9$ $-V_S + 1.9$		 $+V_S - 1.2$ $+V_S - 1.4$	 $-V_S + 1.9$ $-V_S + 1.9$		 $+V_S - 1.2$ $+V_S - 1.4$	 V V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0V to ±10V G = 1 G = 10 G = 100 G = 1000	 90 106 120 126	 95 115 135 140		 85 100 110 120	 95 115 135 140		 dB dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±18V G = 1 G = 10 G = 100 G = 1000	 103 122 131 135	 108 128 145 150		 100 118 126 130	 108 128 145 150		 dB dB dB dB
I_S	Supply Current	V_S = ±2.3V to ±18V		350	530		350	530	μA
V_{OUT}	Output Voltage Swing	R_L = 10k V_S = ±2.3V to ±5V V_S = ±5V to ±18V	 $-V_S + 1.1$ $-V_S + 1.2$		 $+V_S - 1.2$ $+V_S - 1.3$	 $-V_S + 1.1$ $-V_S + 1.2$		 $+V_S - 1.2$ $+V_S - 1.3$	 V V
I_{OUT}	Output Current		20	32		20	32		mA
BW	Bandwidth	G = 1 G = 10 G = 100 G = 1000		400 200 13 1			400 200 13 1		kHz kHz kHz kHz
SR	Slew Rate	G = 1, V_{OUT} = ±10V	0.3	0.5		0.3	0.5		V/μs
	Settling Time to 0.01%	10V Step G = 1 to 100 G = 1000		 30 200			 30 200		 μs μs
REFIN	Reference Input Resistance			60			60		kΩ
I_{REFIN}	Reference Input Current	V_{REF} = 0V		18			18		μA
V_{REF}	Reference Voltage Range		$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V
A_{VREF}	Reference Gain to Output			1 ± 0.0001			1 ± 0.0001		

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. $V_S = ±15V$, $V_{CM} = 0V$, $R_L = 10k$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)		LT1168AC MIN	TYP	MAX	LT1168C MIN	TYP	MAX	UNITS
	Gain Error	G = 1 G = 10 (Note 7) G = 100 (Note 7) G = 1000 (Note 7)	● ● ● ●		0.01 0.40 0.45 0.50	0.03 1.5 1.6 1.7		0.012 0.500 0.550 0.600	0.04 1.6 1.7 1.8	% % % %
	Gain Nonlinearity (Notes 7, 8)	V_{OUT} = ±10V, G = 1 V_{OUT} = ±10V, G = 10 and 100 V_{OUT} = ±10V, G = 1000	● ● ●		2 7 25	15 30 60		3 10 30	20 35 80	ppm ppm ppm
ΔG/ΔT	Gain vs Temperature	G < 1000 (Note 7)	●		100	200		100	200	ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)		LT1168AC MIN	LT1168AC TYP	LT1168AC MAX	LT1168C MIN	LT1168C TYP	LT1168C MAX	UNITS
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$								
V_{OSI}	Input Offset Voltage	V_S = ±5V to ±15V	●		18	60		23	80	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 7, 10)	●		3.0			3.0		µV
V_{OSO}	Output Offset Voltage	V_S = ±5V to ±15V	●		60	380		70	500	µV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 7, 10)	●		30			30		µV
V_{OSI}/T	Input Offset Drift (RTI)	(Note 9)	●		0.05	0.3		0.06	0.4	µV/°C
V_{OSO}/T	Output Offset Drift	(Note 9)	●		0.7	3		0.8	4	µV/°C
I_{OS}	Input Offset Current		●		100	400		120	550	pA
I_{OS}/T	Input Offset Current Drift		●		0.3			0.4		pA/°C
I_B	Input Bias Current		●		65	350		105	600	pA
I_B/T	Input Bias Current Drift		●		1.4			1.4		pA/°C
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded								
		V_S = ±2.3V to ±5V	●	$–V_S + 2.1$		$+V_S – 1.3$	$–V_S + 2.1$		$+V_S – 1.3$	V
		V_S = ±5V to ±18V	●	$–V_S + 2.1$		$+V_S – 1.4$	$–V_S + 2.1$		$+V_S – 1.4$	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0V to ±10V								
		G = 1	●	88	92		83	92		dB
		G = 10	●	100	110		97	110		dB
		G = 100	●	115	120		113	120		dB
		G = 1000	●	117	135		114	135		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±18V								
		G = 1	●	102	115		98	115		dB
		G = 10	●	123	130		118	130		dB
		G = 100	●	127	135		124	135		dB
		G = 1000	●	129	145		126	145		dB
I_S	Supply Current	V_S = ±2.3V to ±18V	●		390	615		390	615	µA
V_{OUT}	Output Voltage Swing	R_L = 10k								
		V_S = ±2.3V to ±5V	●	$–V_S + 1.4$		$+V_S – 1.3$	$–V_S + 1.4$		$+V_S – 1.3$	V
		V_S = ±5V to ±18V	●	$–V_S + 1.6$		$+V_S – 1.5$	$–V_S + 1.6$		$+V_S – 1.5$	V
I_{OUT}	Output Current		●	16	25		16	25		mA
SR	Slew Rate	G = 1, V_{OUT} = ±10V	●	0.25	0.48		0.25	0.48		V/µs
V_{REF}	Voltage Range	(Note 9)	●	$–V_S + 1.6$		$+V_S – 1.6$	$–V_S + 1.6$		$+V_S – 1.6$	V

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS (Note 6)		LT1168AI MIN	LT1168AI TYP	LT1168AI MAX	LT1168I MIN	LT1168I TYP	LT1168I MAX	UNITS
	Gain Error	G = 1	●		0.014	0.04		0.015	0.05	%
		G = 10 (Note 7)	●		0.600	1.9		0.700	2.0	%
		G = 100 (Note 7)	●		0.600	2.0		0.700	2.1	%
		G = 1000 (Note 7)	●		0.600	2.1		0.700	2.2	%
G_N	Gain Nonlinearity (Notes 7, 8)	V_O = ±10V, G = 1	●		3	20		5	25	ppm
		V_O = ±10V, G = 10 and 100	●		10	35		15	40	ppm
		VO = ±10V, G = 1000	●		30	70		35	100	ppm
ΔG/ΔT	Gain vs Temperature	G < 1000 (Note 7)	●		100	200		100	200	ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the −40°C ≤ T_A ≤ 85°C temperature range. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS (Note 6)		LT1168AI MIN	LT1168AI TYP	LT1168AI MAX	LT1168I MIN	LT1168I TYP	LT1168I MAX	UNITS
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$								
V_{OSI}	Input Offset Voltage		●		20	75		25	100	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 7, 10)	●		3.0			3.0		µV
V_{OSO}	Output Offset Voltage		●		180	500		200	600	µV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 7, 10)	●		30			30		µV
V_{OSI}/T	Input Offset Drift (RTI)	(Note 9)	●		0.05	0.3		0.06	0.4	µV/°C
V_{OSO}/T	Output Offset Drift	(Note 9)	●		0.8	5		1	6	µV/°C
I_{OS}	Input Offset Current		●		110	550		120	700	pA
I_{OS}/T	Input Offset Current Drift		●		0.3			0.3		pA/°C
I_B	Input Bias Current		●		120	500		220	800	pA
I_B/T	Input Bias Current Drift		●		1.4			1.4		pA/°C
V_{CM}	Input Voltage Range	V_S = ±2.3V to ±5V V_S = ±5V to ±18V	● ●	$-V_S + 2.1$ $-V_S + 2.1$		$+V_S - 1.3$ $+V_S - 1.4$	$-V_S + 2.1$ $-V_S + 2.1$		$+V_S - 1.3$ $+V_S - 1.4$	V V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0V to ±10V G = 1 G = 10 G = 100 G = 1000	 ● ● ● ●	 86 98 114 116	 90 105 118 133		 81 95 112 112	 90 105 118 133		 dB dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±18V G = 1 G = 10 G = 100 G = 1000	 ● ● ● ●	 100 120 125 128	 112 125 132 140		 95 115 120 125	 112 125 132 140		 dB dB dB dB
I_S	Supply Current		●		420	650		420	650	µA
V_{OUT}	Output Voltage Swing	V_S = ±2.3V to ±5V V_S = ±5V to ±18V	● ●	$-V_S + 1.4$ $-V_S + 1.6$		$+V_S - 1.3$ $+V_S - 1.5$	$-V_S + 1.4$ $-V_S + 1.6$		$+V_S - 1.3$ $+V_S - 1.5$	V V
I_{OUT}	Output Current		●	15	22		15	22		mA
SR	Slew Rate		●	0.22	0.41		0.22	0.42		V/µs
V_{REF}	Voltage Range	(Note 9)	●	$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: If the input voltage exceeds the supplies, the input current should be limited to less than 20mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1168AC/LT1168C are guaranteed functional over the operating temperature range of −40°C and 85°C.

Note 5: The LT1168AC/LT1168C are guaranteed to meet specified performance from 0°C to 70°C. The LT1168AC/LT1168C are designed, characterized and expected to meet specified performance from −40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1168AI/LT1168I are guaranteed to meet specified performance from −40°C to 85°C.

Note 6: Typical parameters are defined as the 60% of the yield parameter distribution.

Note 7: Does not include the tolerance of the external gain resistor R_G.

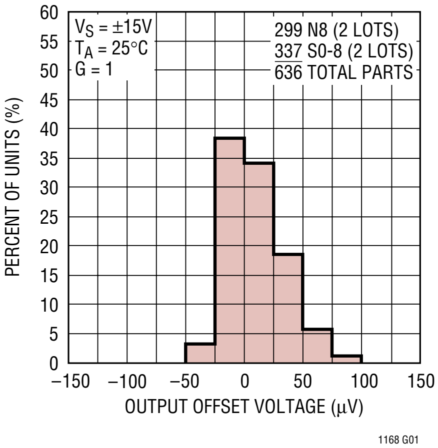
Note 8: This parameter is measured in a high speed automatic tester that does not measure the thermal effects with longer time constants. The magnitude of these thermal effects are dependent on the package used, heat sinking and air flow conditions.

Note 9: This parameter is not 100% tested.

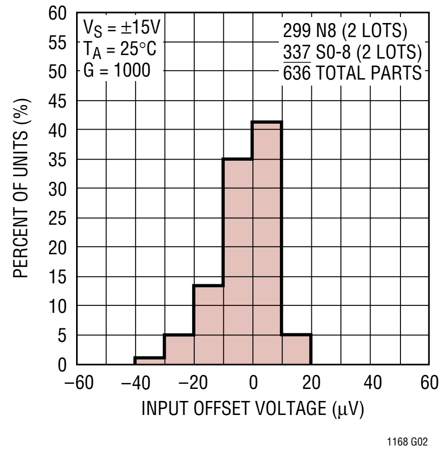
Note 10: Hysteresis in offset voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Offset voltage hysteresis is always measured at 25°C, but the IC is cycled to 85°C I-grade (or 70°C C-grade) or −40°C I-grade (0°C C-grade) before successive measurement. 60% of the parts will pass the typical limit on the data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

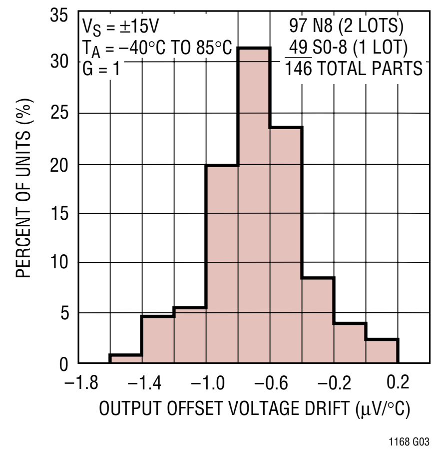
Distribution of Output Offset Voltage



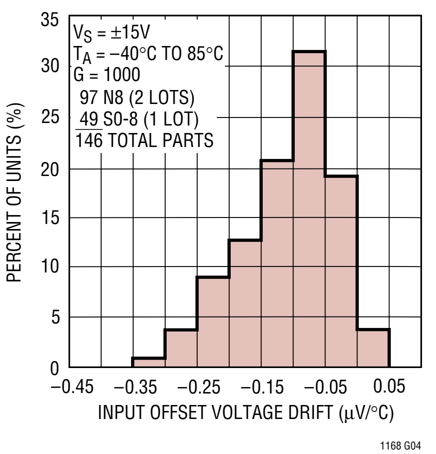
Distribution of Input Offset Voltage



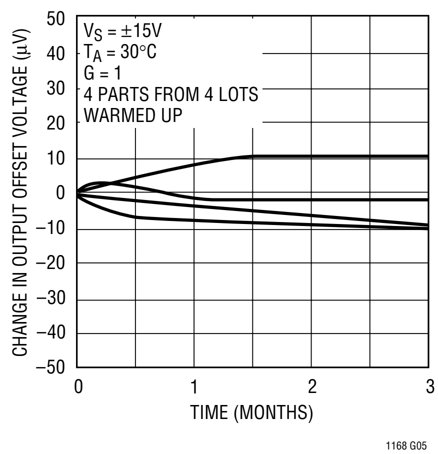
Distribution of Output Offset Voltage Drift



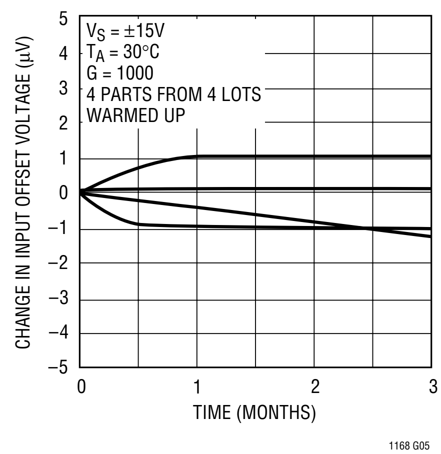
Distribution of Input Offset Voltage Drift



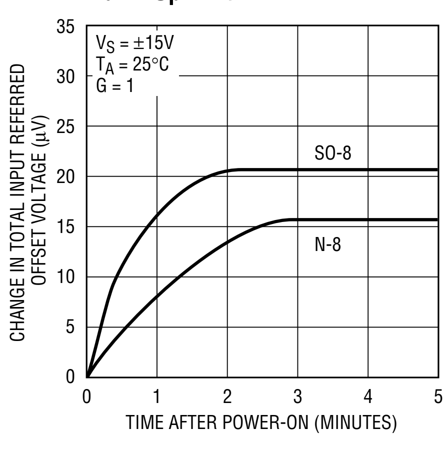
Output Offset Voltage Long-Term Drift



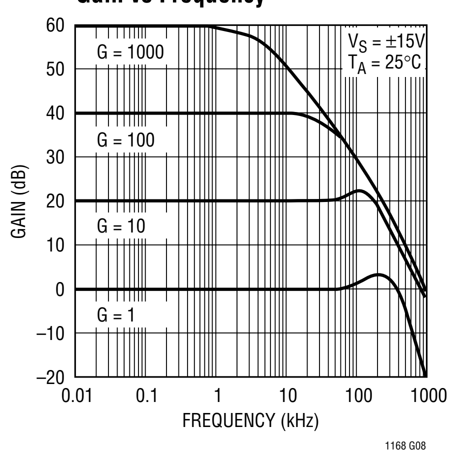
Input Offset Voltage Long-Term Drift



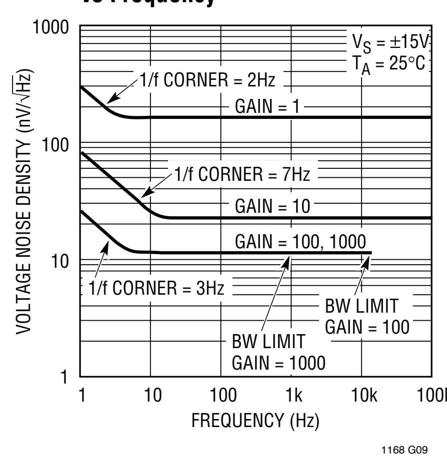
Warm-Up Drift



Gain vs Frequency

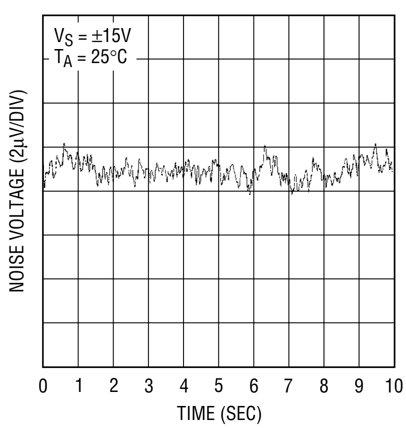


Voltage Noise Density vs Frequency

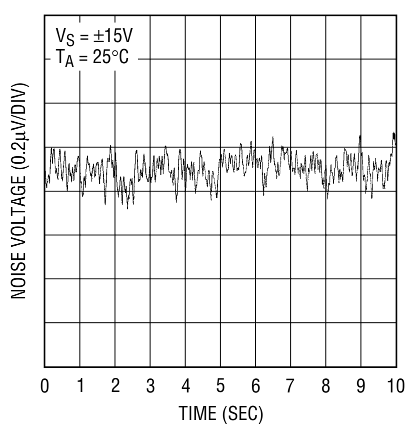


TYPICAL PERFORMANCE CHARACTERISTICS

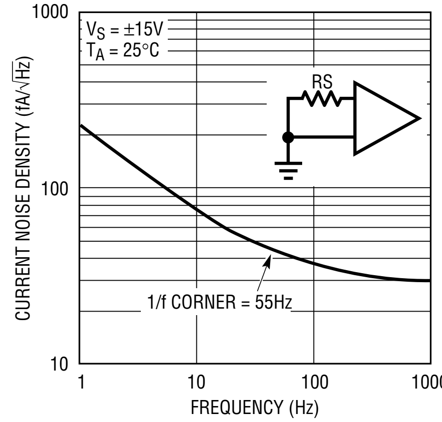
0.1Hz to 10Hz Noise Voltage, G = 1



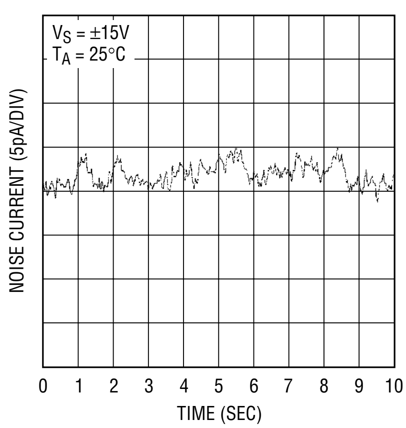
0.1Hz to 10Hz Noise Voltage, RTI G = 1000



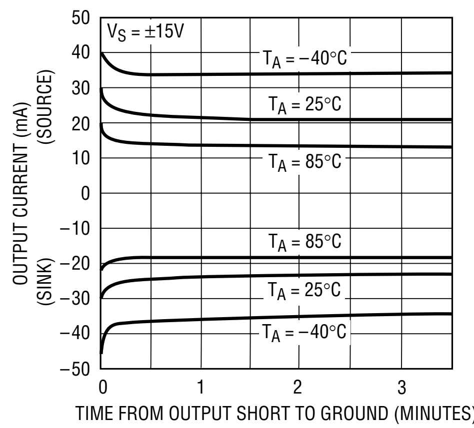
Current Noise Density vs Frequency



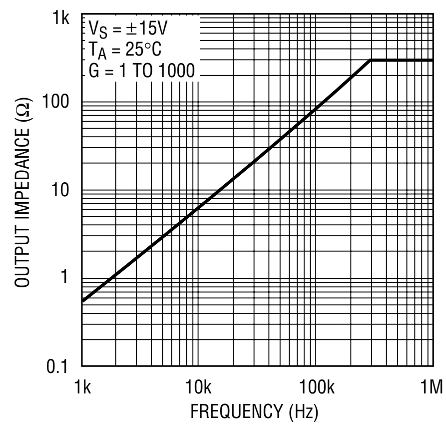
0.1Hz to 10Hz Current Noise



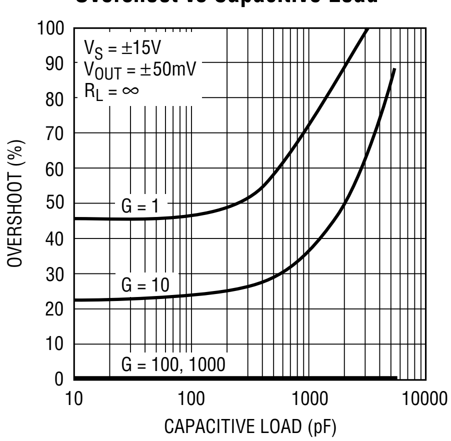
Short-Circuit Current vs Time



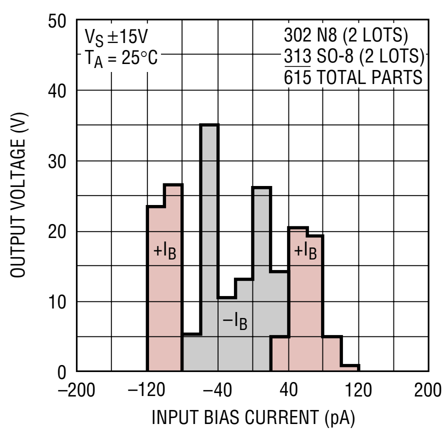
Output Impedance vs Frequency



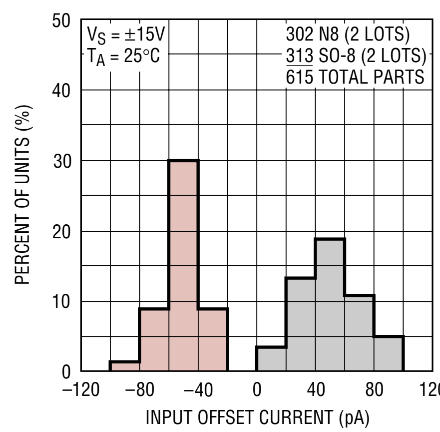
Overshoot vs Capacitive Load



Input Bias Current

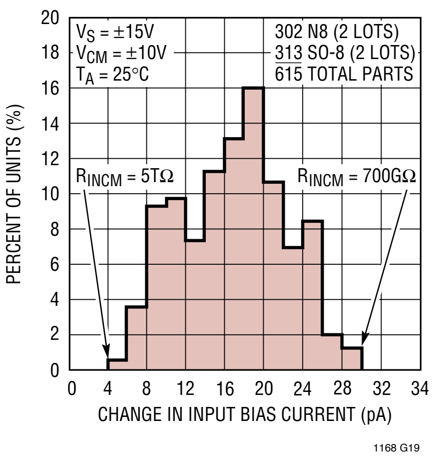


Input Offset Current

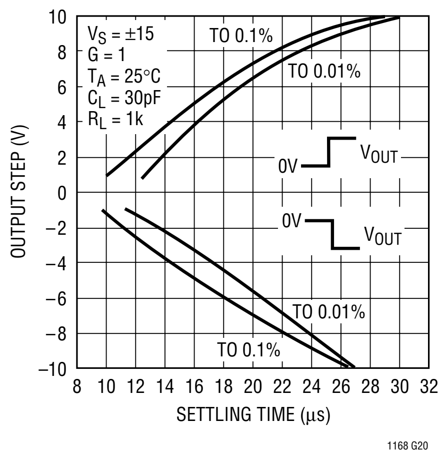


TYPICAL PERFORMANCE CHARACTERISTICS

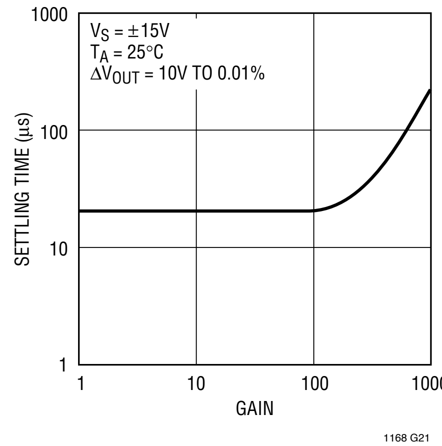
Change in Input Bias Current for V_{CM} = 20V



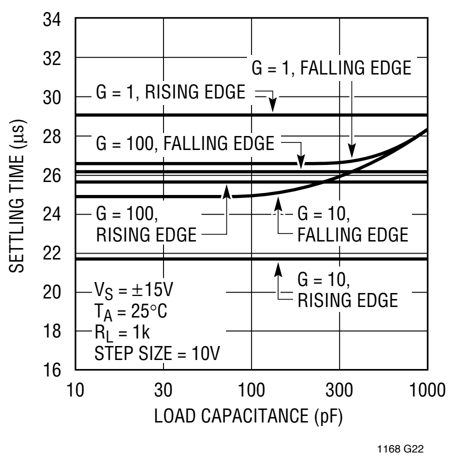
Settling Time vs Step Size



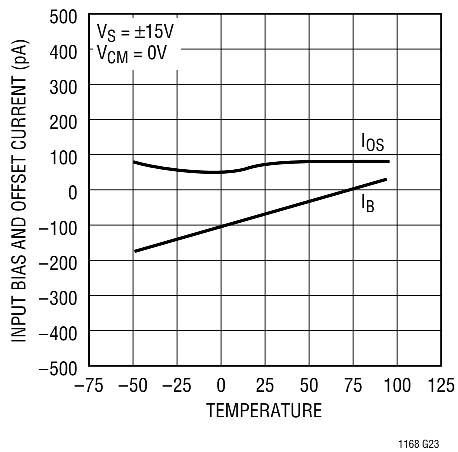
Settling Time vs Gain



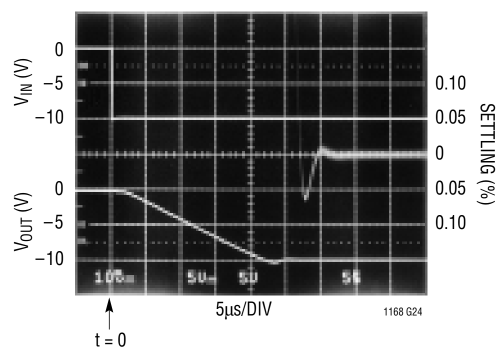
Settling Time (0.1%) vs Load Capacitance



Input Bias and Offset Current vs Temperature

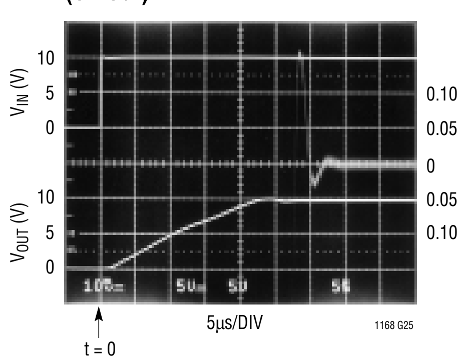


Falling Edge Settling Time (0.10%)



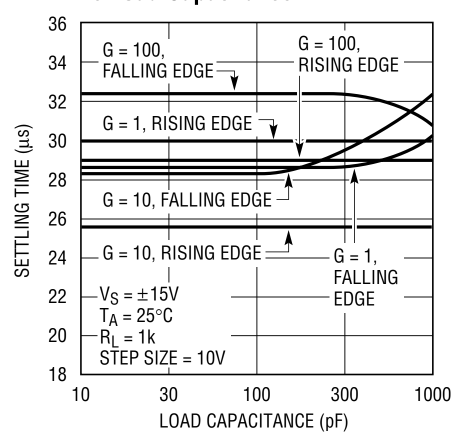
T_A = 25°C
V_S = ±15V
R_L = 2k
C_L = 15pF

Rising Edge Settling Time (0.10%)

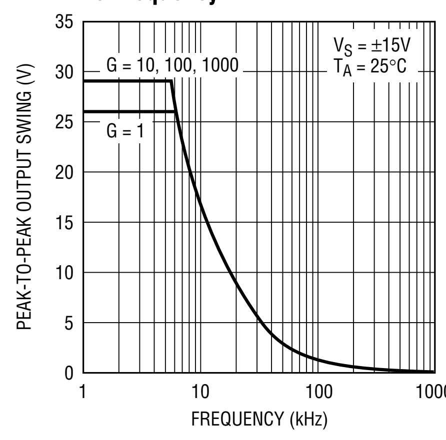


T_A = 25°C
V_S = ±15V
R_L = 2k
C_L = 15pF

Settling Time (0.01%) vs Load Capacitance

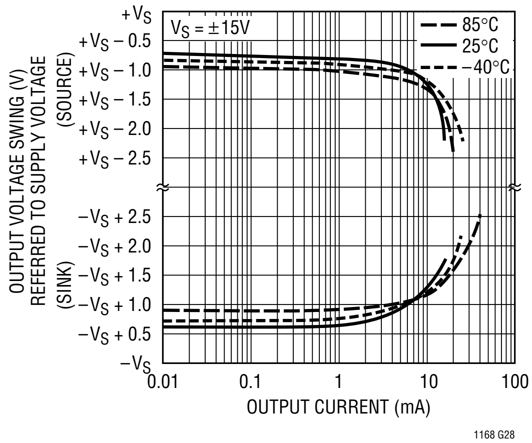


Undistorted Output Swing vs Frequency

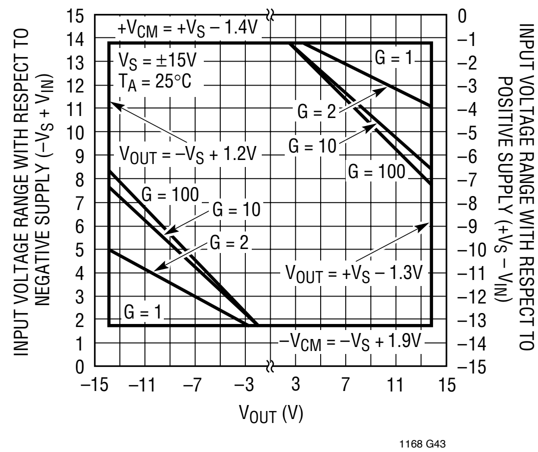


TYPICAL PERFORMANCE CHARACTERISTICS

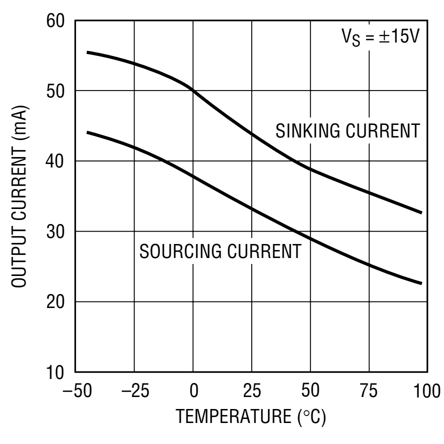
Output Voltage Swing vs Load Current



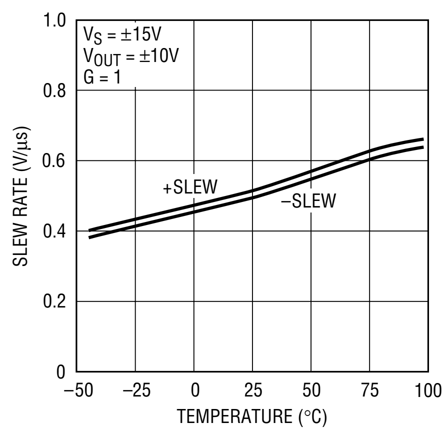
Input Voltage Range vs Output Voltage for Various Gains



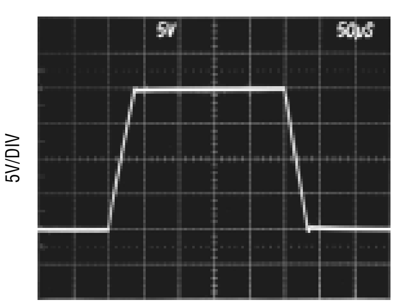
Output Short-Circuit Current vs Temperature



Slew Rate vs Temperature

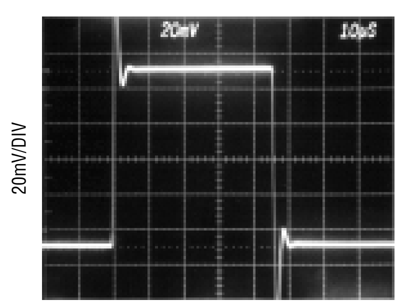


Large-Signal Transient Response



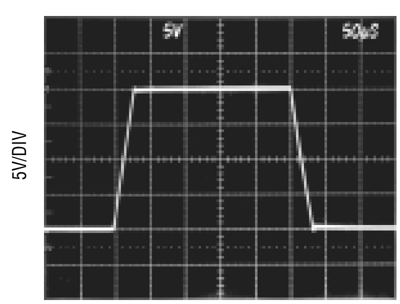
G = 1 50µs/DIV
$V_S = \pm15V$
$R_L = 2k$
$C_L = 60pF$

Small-Signal Transient Response



G = 1 10µs/DIV
$V_S = \pm15V$
$R_L = 2k$
$C_L = 60pF$

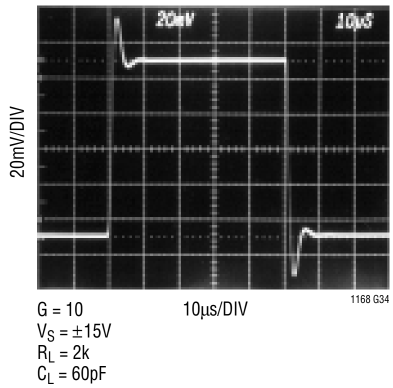
Large-Signal Transient Response



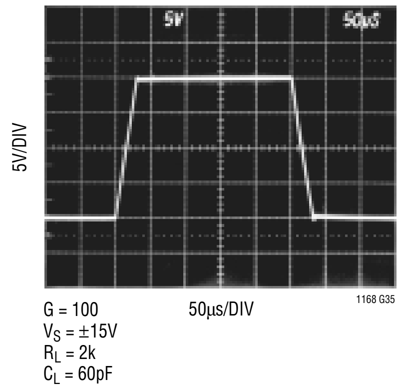
G = 10 50µs/DIV
$V_S = \pm15V$
$R_L = 2k$
$C_L = 60pF$

TYPICAL PERFORMANCE CHARACTERISTICS

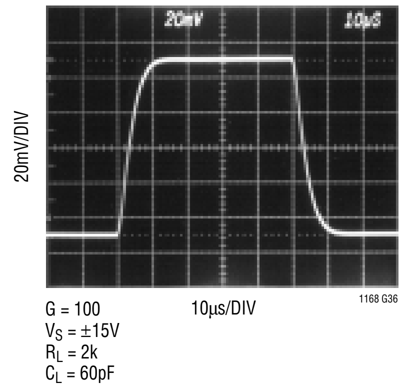
Small-Signal Transient Response



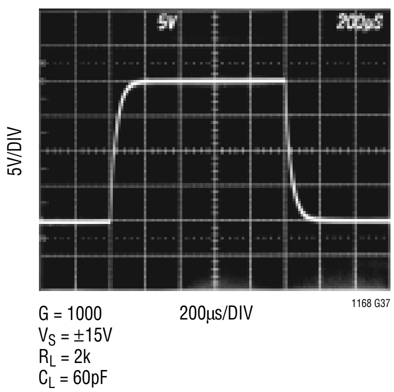
Large-Signal Transient Response



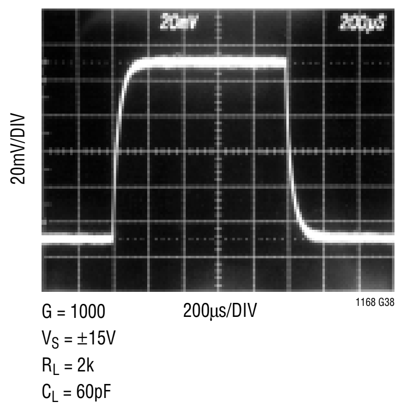
Small-Signal Transient Response



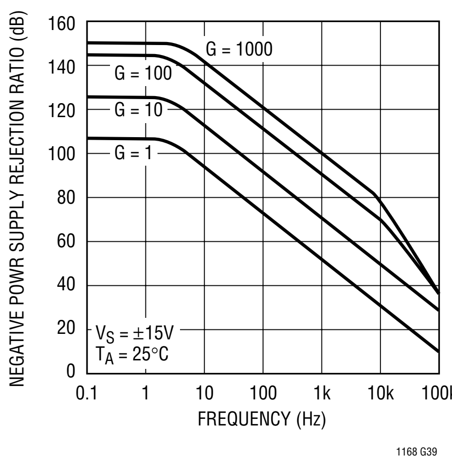
Large-Signal Transient Response



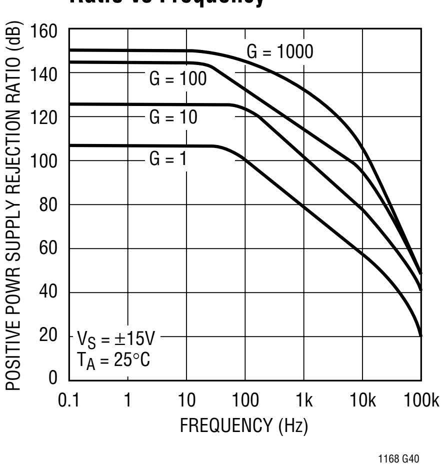
Small-Signal Transient Response



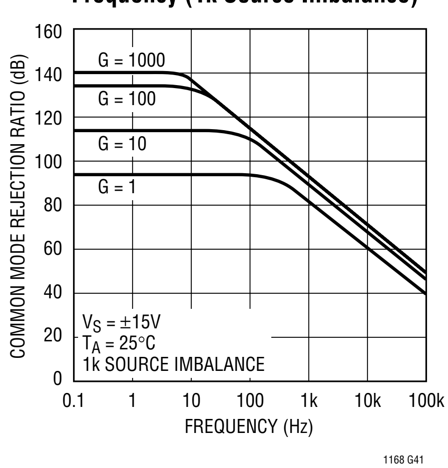
Negative Power Supply Rejection Ratio vs Frequency



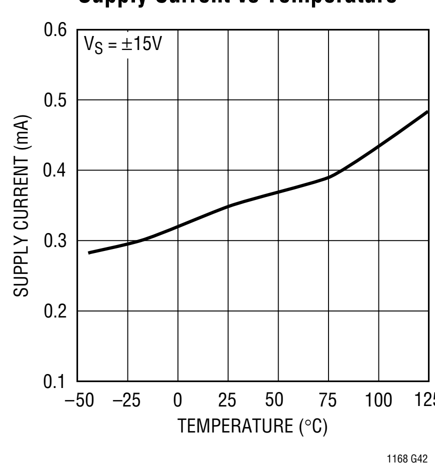
Positive Power Supply Rejection Ratio vs Frequency



Common Mode Rejection Ratio vs Frequency (1k Source Imbalance)



Supply Current vs Temperature



BLOCK DIAGRAM

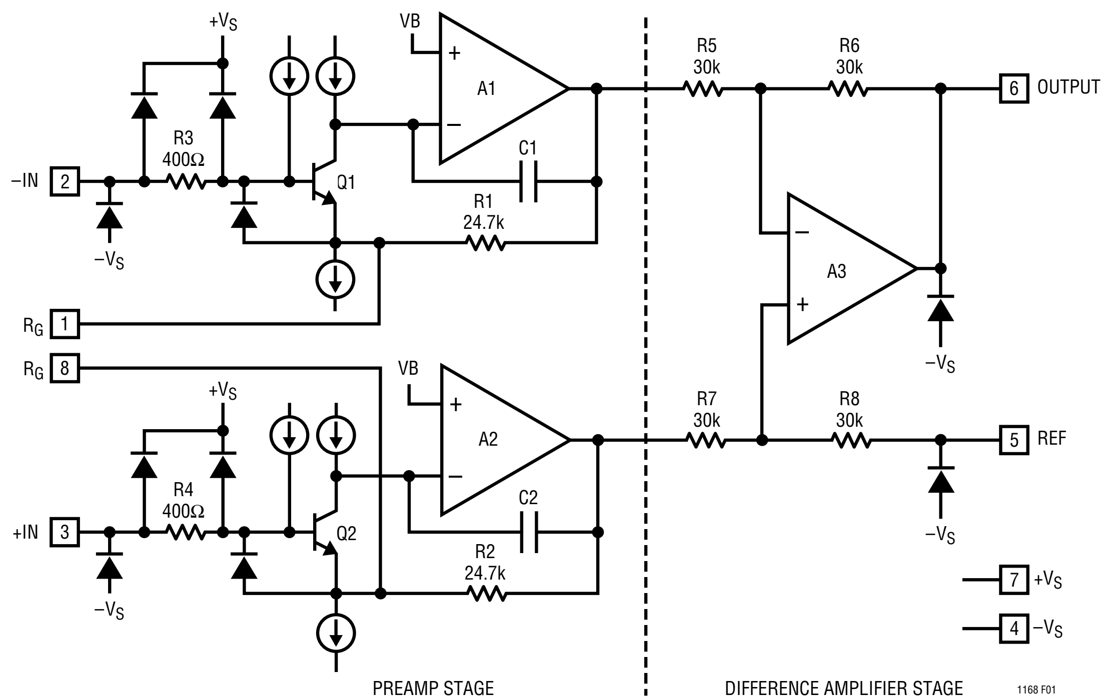


Figure 1. Block Diagram

THEORY OF OPERATION

The LT1168 is a modified version of the three op amp instrumentation amplifier. Laser trimming and monolithic construction allow tight matching and tracking of circuit parameters over the specified temperature range. Refer to the block diagram (Figure 1) to understand the following circuit description. The collector currents in Q1 and Q2 are trimmed to minimize offset voltage drift, thus assuring a high level of performance. R1 and R2 are trimmed to an absolute value of 24.7k to assure that the gain can be set accurately (0.6% at G = 100) with only one external resistor R_G. The value of R_G in parallel with R1 (R2) determines the transconductance of the preamp stage. As R_G is reduced for larger programmed gains, the transconductance of the input preamp stage increases to that of the input transistors Q1 and Q2. This increases the open-loop gain when the programmed gain is increased, reducing the input referred gain related errors and noise. The input voltage noise at gains greater than 50 is determined only by Q1 and Q2. At lower gains the noise of the difference amplifier and preamp gain setting resistors increase the noise. The gain bandwidth product is determined by C1, C2 and the preamp transconductance which increases with programmed gain. Therefore, the bandwidth does not drop proportionally with gain.

The input transistors Q1 and Q2 offer excellent matching, which is inherent in NPN bipolar transistors, as well as picoampere input bias current due to superbeta processing. The collector currents in Q1 and Q2 are held constant due to the feedback through the Q1-A1-R1 loop and Q2-A2-R2 loop which in turn impresses the differential input voltage across the external gain set resistor R_G. Since the current that flows through R_G also flows through R1 and R2, the ratios provide a gained-up differential

THEORY OF OPERATION

voltage, $G = (R1 + R2)/R_G$, to the unity-gain difference amplifier A3. The common mode voltage is removed by A3, resulting in a single-ended output voltage referenced to the voltage on the REF pin. The resulting gain equation is:

$$G = (49.4k\Omega/R_G) + 1$$

solving for the gain set resistor gives:

$$R_G = 49.4k\Omega/(G - 1)$$

Table 1 shows appropriate 1% resistor values for a variety of gains.

Table 1

DESIRED GAIN	R_G	CLOSEST 1% VALUE	RESULTANT GAIN
1	Open	Open	1
2	49400Ω	49900Ω	1.99
5	12350Ω	12400Ω	4.984
10	5488.89Ω	5490Ω	9.998
20	2600Ω	2610Ω	19.93
50	1008.16Ω	1000Ω	50.4
100	498.99Ω	499Ω	99.998
200	248.24Ω	249Ω	199.4
500	99Ω	100Ω	495
1000	49.95Ω	49.4Ω	1001

Input and Output Offset Voltage

The offset voltage of the LT1168 has two components: the output offset and the input offset. The total offset voltage referred to the input (RTI) is found by dividing the output offset by the programmed gain (G) and adding it to the input offset. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is:

Total input offset voltage (RTI)
= input offset + (output offset/G)

Total output offset voltage (RTO)
= (input offset • G) + output offset

Reference Terminal

The reference terminal is one end of one of the four 30k resistors around the difference amplifier. The output voltage of the LT1168 (Pin 6) is referenced to the voltage on the reference terminal (Pin 5). Resistance in series with the REF pin must be minimized for best common mode rejection. For example, a 6Ω resistance from the REF pin to ground will not only increase the gain error by 0.02% but will lower the CMRR to 80dB.

Input Voltage Range

The input voltage range for the LT1168 is specified in the data sheet at 1.4V below the positive supply to 1.9V above the negative supply for a gain of one. As the gain increases the input voltage range decreases. This is due to the IR drop across the internal gain resistors R1 and R2 in Figure 1. For the unity gain condition there is no IR drop across the gain resistors R1 and R2, the output of the GM amplifiers is just the differential input voltage at Pin 2 and Pin 3 (level shifted by one V_{BE} from Q1 and Q2). When a gain resistor is connected across Pins 1 and 8, the output swing of the GM cells is now the differential input voltage (level shifted by V_{BE}) plus the differential voltage times the gain (ratio of the internal gain resistors to the external gain resistor across Pins 1 and 8). To calculate how close to the positive rail the input (V_{IN}) can swing for a gain of 2 and a maximum expected output swing of 10V, use the following equation:

$$+V_S - V_{IN} = -0.5 - (V_{OUT}/G) \bullet (G - 1)/2$$

Substituting yields:

$$-0.5 - (10/2) \bullet (1/2) = -3V$$

below the positive supply or 12V for a 15V supply. To calculate how far above the negative supply the input can swing for a gain of 10 with a maximum expected output swing of –10V, the equation for the negative case is:

$$-V_S + V_{IN} = 1.5 - (V_{OUT}/G) \bullet (G - 1)/2$$

Substituting yields:

$$1.5 - (-10/10) \bullet 9/2 = 6V$$

above the negative supply or –9V for a negative supply voltage of –15V. Figures 2 and 3 are for the positive common mode and negative common mode cases respectively.

THEORY OF OPERATION

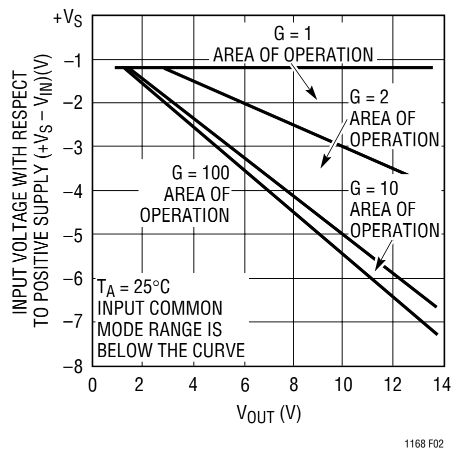


Figure 2. Positive Input Range vs Output Voltage for Different Gains

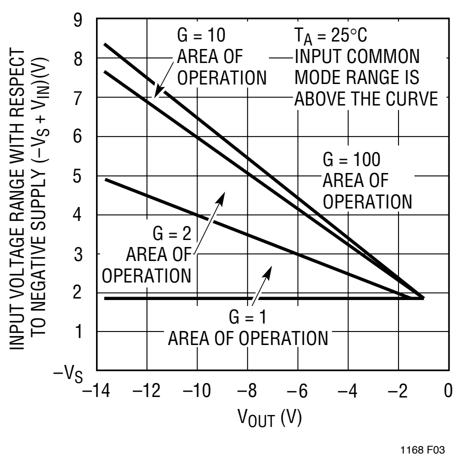


Figure 3. Negative Input Voltage Range vs Output Voltage for Various Gains

Single Supply Operation

For best results under single supply operation, the REF pin should be raised above the negative supply (Pin 4) and one of the inputs should be at least 2.5V above ground. The barometer application later in this data sheet is an example that satisfies these conditions. The resistance R_{SET} from the bridge transducer to ground sets the operating current for the bridge, and with R6, also has the effect of raising the input common mode voltage. The output of the LT1168 is always inside the specified range since the barometric pressure rarely goes low enough to cause the output to clip (30.00 inches of Hg corresponds to 3.000V). For applications that require the output to swing at or below the REF potential, the voltage on the REF pin can be further level shifted. The application in the front of this data sheet, Single Supply Pressure Monitor, is an example. An op amp is used to buffer the voltage on the REF pin since a parasitic series resistance will degrade the CMRR.

Output Offset Trimming

The LT1168 is laser trimmed for low offset voltage so that no external offset trimming is required for most applications. In the event that the offset needs to be adjusted, the circuit in Figure 4 is an example of an optional offset adjust circuit. The op amp buffer provides a low impedance to the REF pin where resistance must be kept to minimum for best CMRR and lowest gain error.

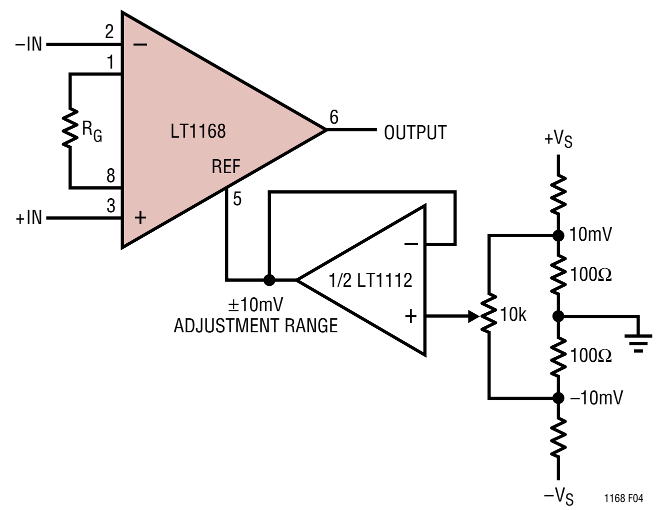


Figure 4. Optional Trimming of Output Offset Voltage

Input Bias Current Return Path

The low input bias current of the LT1168 (250pA) and the high input impedance (200GΩ) allow the use of high impedance sources without introducing additional offset voltage errors, even when the full common mode range is required. However, a path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path the inputs will float to either rail and exceed the input common mode range of the LT1168, resulting in a saturated input stage. Figure 5 shows three examples of an input bias current

THEORY OF OPERATION

path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both common mode rejection and DC offset.

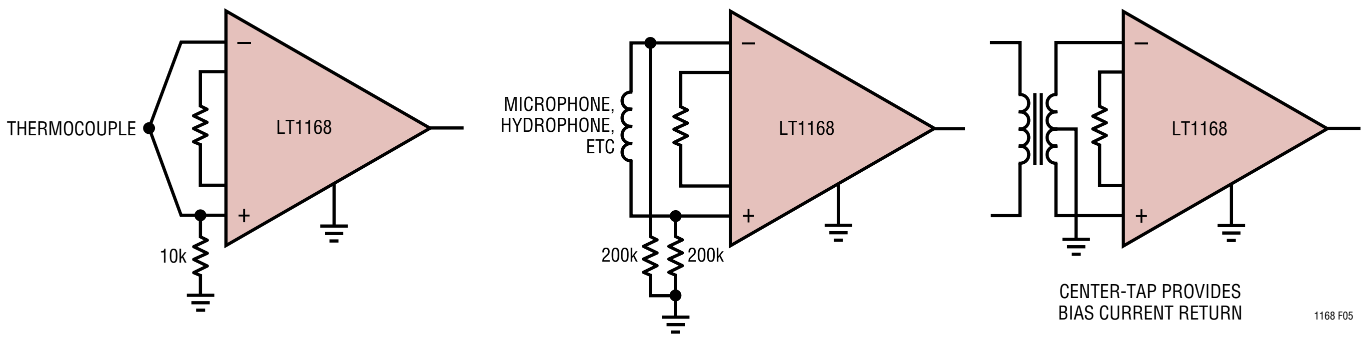


Figure 5. Providing an Input Common Mode Current Path

APPLICATIONS INFORMATION

The LT1168 is a low power precision instrumentation amplifier that requires only one external resistor to accurately set the gain anywhere from 1 to 1000. The LT1168 is trimmed for critical DC parameters such as gain error (0.04%, G = 10), input offset voltage (40μV, RTI), CMRR (90dB min, G = 1) and PSRR (103dB min, G = 1). These trims allow the amplifier to achieve very high DC accuracy. The LT1168 achieves low input bias current of just 250pA (max) through the use of superbeta processing. The output can handle capacitive loads up to 1000pF in any gain configuration and the inputs are protected against ESD strikes up to ±13kV (human body).

Input Protection

The LT1168 can safely handle up to ±20mA of input current in an overload condition. Adding an external 5k input resistor in series with each input allows DC input fault voltage up to ±100V and improves the ESD immunity to ±8kV (contact) and ±15kV (air discharge), which is the IEC 1000-4-2 level 4 specification. If lower value input resistors must be used, a clamp diode from the positive supply to each input will maintain the IEC 1000-4-2 specification to level 4 for both air and contact discharge. A 2N4393 drain/source to gate is a good low leakage diode for use with resistors between 1k and 20k, see Figure 6. The input resistors should be carbon and not metal film or carbon film in order to withstand the fault conditions.

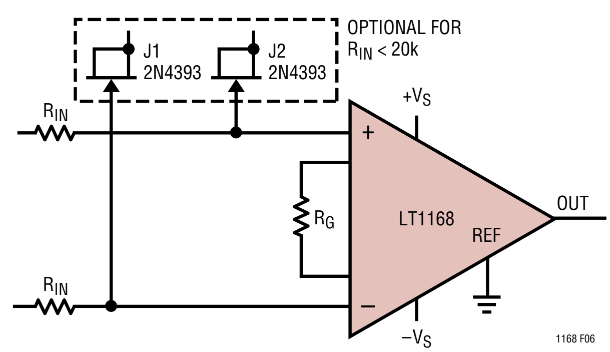


Figure 6. Input Protection

RFI Reduction

In many industrial and data acquisition applications, instrumentation amplifiers are used to accurately amplify small signals in the presence of large common mode

APPLICATIONS INFORMATION

voltages or high levels of noise. Typically, the sources of these very small signals (on the order of microvolts or millivolts) are sensors that can be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry, using shielded or unshielded twisted-pair cabling, the cabling may act as antennae, conveying very high frequency interference directly into the input stage of the LT1168.

The amplitude and frequency of the interference can have an adverse effect on an instrumentation amplifier's input stage by causing an unwanted DC shift in the amplifier's input offset voltage. This well known effect is called RFI rectification and is produced when out-of-band interference is coupled (inductively, capacitively or via radiation) and rectified by the instrumentation amplifier's input transistors. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled into the circuit, an out-of-band error signal appears in series with the instrumentation amplifier's inputs.

To significantly reduce the effect of these out-of-band signals on the input offset voltage of instrumentation amplifiers, simple lowpass filters can be used at the inputs. This filter should be located very close to the input pins of the circuit. An effective filter configuration is illustrated in Figure 7, where three capacitors have been added to the inputs of the LT1168. Capacitors C_{XCM1} and C_{XCM2} form lowpass filters with the external series resistors $R_{S1,\,2}$ to any out-of-band signal appearing on each of the input traces. Capacitor C_{XD} forms a filter to reduce any unwanted signal that would appear across the input traces. An added benefit to using C_{XD} is that the circuit's AC common mode rejection is not degraded due to common mode capacitive imbalance. The differential mode and common mode time constants associated with the capacitors are:

$$t_{DM(LPF)} = (R_{S1} + R_{S2})(C_{XD} + C_{XCM1} + C_{XCM2})$$

$$t_{CM(LPF)} = (R_{S1} \| R_{S2})(C_{XCM1} + C_{XCM2})$$

Setting the time constants requires a knowledge of the frequency, or frequencies of the interference. Once this frequency is known, the common mode time constants can be set followed by the differential mode time constant. To avoid any possibility of inadvertently affecting the signal to be processed, set the common mode time constant an order of magnitude (or more) smaller than the differential mode time constant. Set the common mode time constants such that they do not degrade the LT1168 inherent AC CMR. Then the differential mode time constant can be set for the bandwidth required for the application. Setting the differential mode time constant close to the sensor's BW also minimizes any noise pickup along the leads. To avoid any possibility of common mode to differential mode signal conversion, match the common mode time constants to 1% or better. If the sensor is an RTD or a resistive strain gauge and is in proximity to the instrumentation amplifier, then the series resistors $R_{S1,\,2}$ can be omitted.

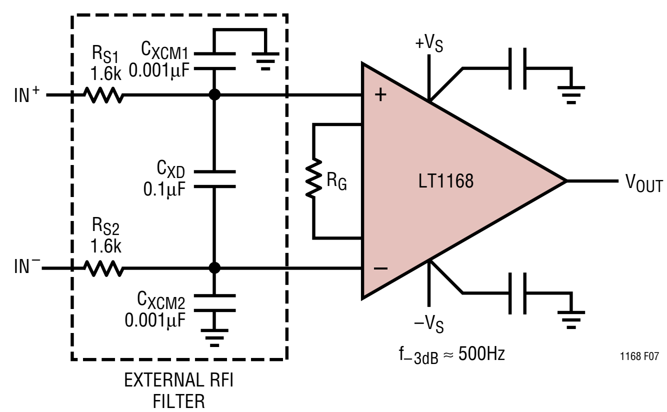


Figure 7. Adding a Simple RC Filter at the Inputs to an Instrumentation Amplifier is Effective in Reducing Rectification of High Frequency Out-of-Band Signals

Nerve Impulse Amplifier

The LT1168's low current noise makes it ideal for EMG monitors that have high source impedances. Demonstrating the LT1168's ability to amplify low level signals, the circuit in Figure 8 takes advantage of the amplifier's high gain and low noise operation. This circuit amplifies the low level nerve impulse signals received from a patient at Pins 2 and 3. R_G and the parallel combination of R3 and R4 set a gain of ten. The potential on LT1112's Pin 1 creates

APPLICATIONS INFORMATION

a ground for the common mode signal. C1 was chosen to maintain the stability of the patient ground. The LT1168's high CMRR ensures that the desired differential signal is amplified and unwanted common mode signals are attenuated. Since the DC portion of the signal is not important, R6 and C2 make up a 0.3Hz highpass filter. The AC signal at LT1112's Pin 5 is amplified by a gain of 101 set by R7/R8 +1. The parallel combination of C3 and R7 form a lowpass filter that decreases this gain at frequencies above 1kHz. The ability to operate at ±3V on 350μA of supply current makes the LT1168 ideal for battery-powered applications. Total supply current for this application is 1.05mA. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

Low I_B Favors High Impedance Bridges, Lowers Dissipation

The LT1168's low supply current, low supply voltage operation and low input bias currents allow it to fit nicely into battery-powered applications. Low overall power dissipation necessitates using higher impedance bridges. The single supply pressure monitor application on the front of this data sheet, shows the LT1168 connected to the differential output of a 3.5k bridge. The picoampere input bias currents keep the error caused by offset current to a negligible level. The LT1112 level shifts the LT1168's reference pin and the ADC's analog ground pins above ground. The LT1168's and LT1112's combined power dissipation is still less than the bridge's. This circuit's total supply current is just 2.2mA.

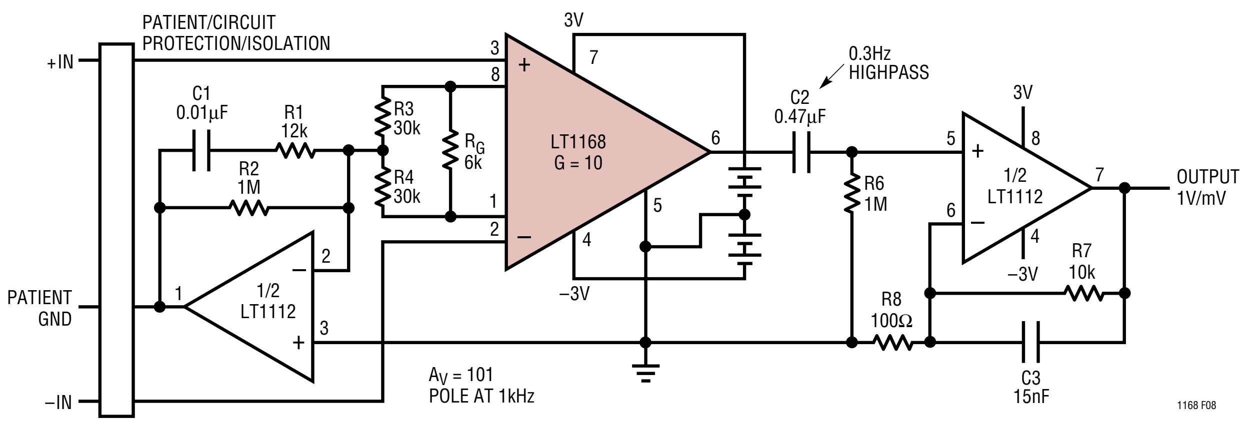


Figure 8. Nerve Impulse Amplifier

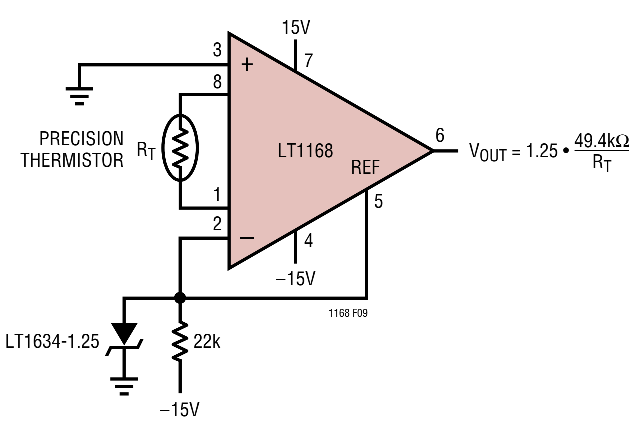


Figure 9. Precision Temperature Without Precision Resistors

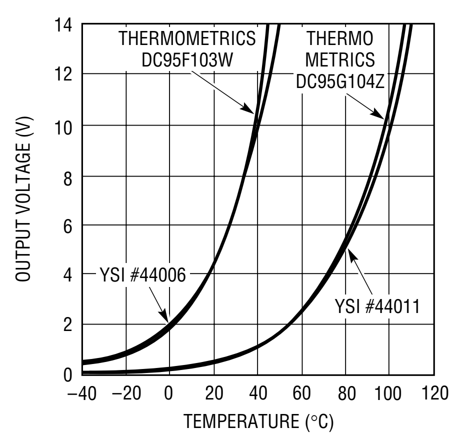
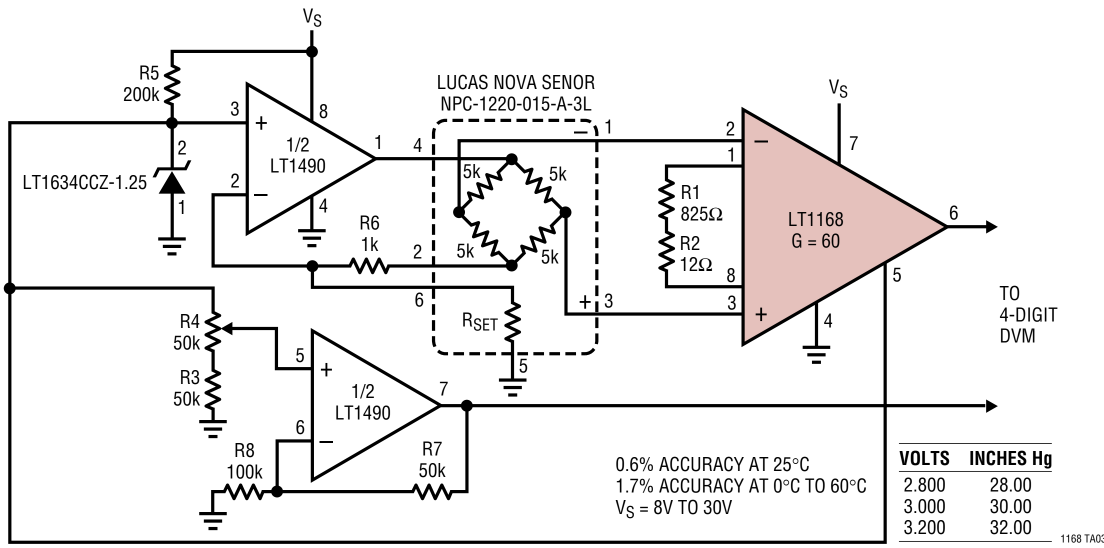


Figure 10. Response of Figure 9 for Various Thermistors

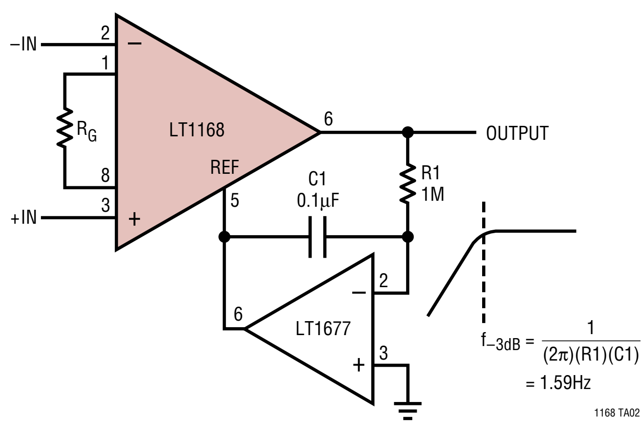
TYPICAL APPLICATIONS

Single Supply Barometer



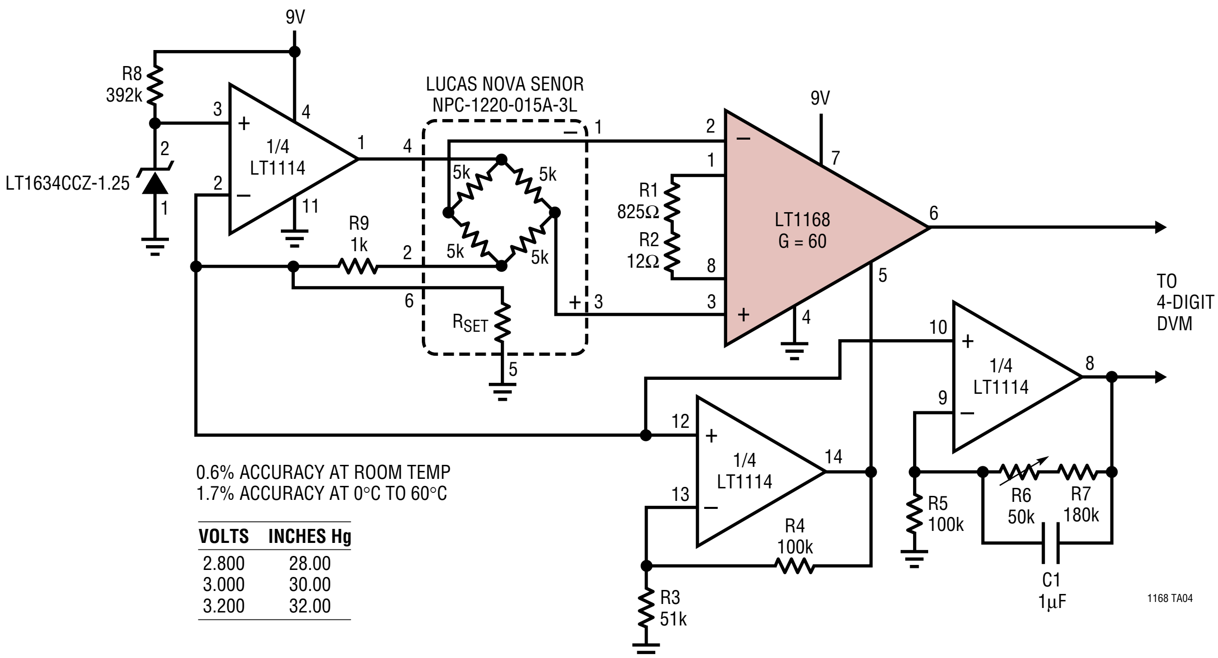
VOLTS	INCHES Hg
2.800	28.00
3.000	30.00
3.200	32.00

AC Coupled Instrumentation Amplifier



TYPICAL APPLICATIONS

4-Digit Pressure Sensor



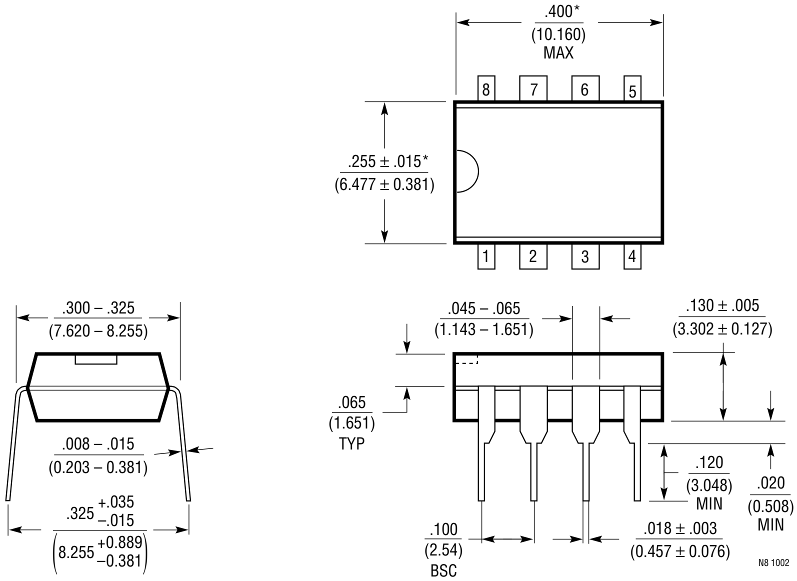
0.6% ACCURACY AT ROOM TEMP
1.7% ACCURACY AT 0°C TO 60°C

VOLTS	INCHES Hg
2.800	28.00
3.000	30.00
3.200	32.00

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

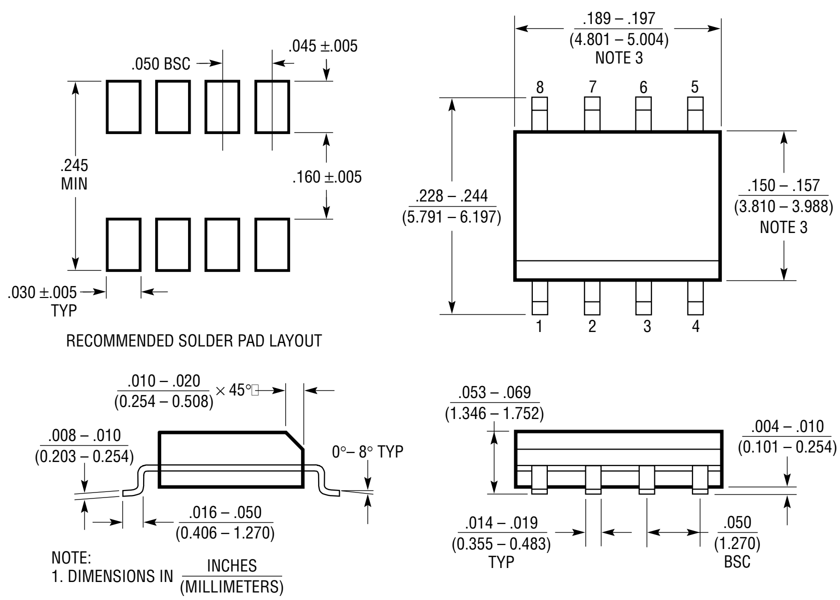
N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

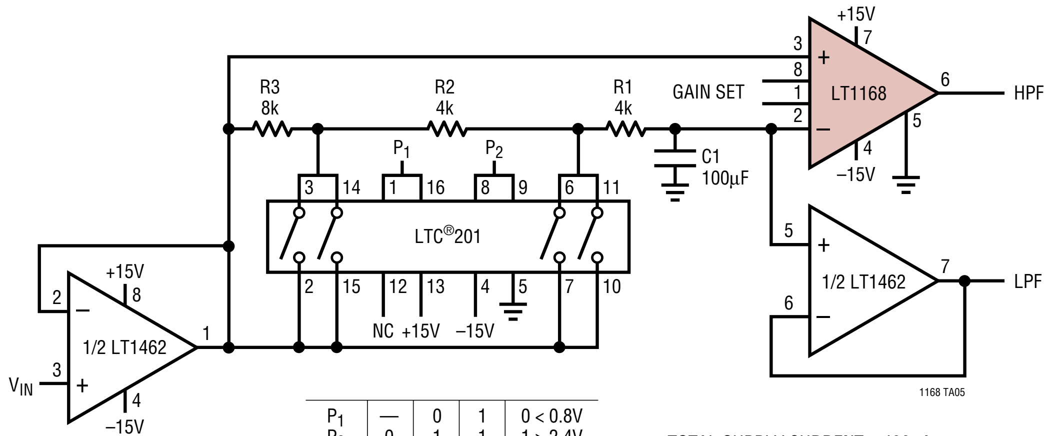


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

TYPICAL APPLICATION

Low Power Programmable Audio HPF/LPF with "Pop-Less" Switching



P_1 / P_2	— / 0	0 / 1	1 / 1	0 < 0.8V / 1 > 2.4V
POLE	100	200	400	Hz

TOTAL SUPPLY CURRENT < 400µA

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1043	Dual Precision Instrumentation Building Block	Switched Capacitor, Rail-to-Rail Input, 120dB CMRR
LTC1100	Precision Chopper-Stabilized Instrumentation Amplifier	G = 10 or 100, V_{OS} = 10µV, I_B = 50pA
LT1101	Precision, Micropower, Single Supply Instrumentation Amplifier	G = 10 or 100, I_S = 105µA
LT1102	High Speed, JFET Instrumentation Amplifier	G = 10 or 100, Slew Rate = 30V/µs
LT1167	Single Resistor Programmable Precision Instrumentation Amplifier	Lower Noise than LT1168, $e_N = 7.5nV/\sqrt{Hz}$

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

LT/LWI 0906 REV A • PRINTED IN USA