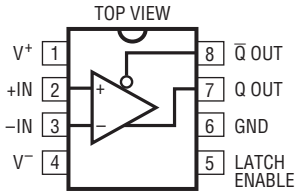
ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage (Note 5) 7V
Negative Supply Voltage 7V
Differential Input Voltage (Note 7) ..... ±5V
+IN, –IN and LATCH ENABLE Current (Note 7) .... ±10mA
Output Current (Continuous) (Note 7)..... ±20mA

Operating Temperature Range
LT1016I.....–40°C to 85°C
LT1016C..... 0°C to 70°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

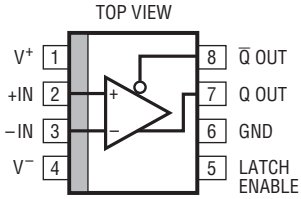
PIN CONFIGURATION



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER
LT1016CN8 LT1016IN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 120°C/W

ORDER PART NUMBER	S8 PART MARKING
LT1016CS8 LT1016IS8	1016 1016I

Consult LTC marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 5V, V_{OUT} (Q) = 1.4V, V_{LATCH} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			LT1016C/I MIN	LT1016C/I TYP	LT1016C/I MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 2)		 ●		1.0	±3 3.5	mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift			●		4		µV/°C
I_{OS}	Input Offset Current	(Note 2)		 ●		0.3 0.3	1.0 1.3	µA µA
I_B	Input Bias Current	(Note 3)		 ●		5	10 13	µA µA
	Input Voltage Range	(Note 6) Single 5V Supply		● ●	–3.75 1.25		3.5 3.5	V V
CMRR	Common Mode Rejection	$-3.75V \le V_{CM} \le 3.5V$		●	80	96		dB
PSRR	Supply Voltage Rejection	Positive Supply 4.6V ≤ V^+ ≤ 5.4V LT1016C		●	60	75		dB
		Positive Supply 4.6V ≤ V^+ ≤ 5.4V LT1016I		●	54	75		dB
		Negative Supply 2V ≤ V^- ≤ 7V		●	80	100		dB
A_V	Small-Signal Voltage Gain	1V ≤ V_{OUT} ≤ 2V			1400	3000		V/V
V_{OH}	Output High Voltage	$V^+ \ge 4.6V$	I_{OUT} =1mA I_{OUT} = 10mA	● ●	2.7 2.4	3.4 3.0		V V
V_{OL}	Output Low Voltage		I_{SINK} = 4mA I_{SINK} = 10mA	●		0.3 0.4	0.5	V V
I^+	Positive Supply Current			●		25	35	mA
I^-	Negative Supply Current			●		3	5	mA
V_{IH}	LATCH Pin Hi Input Voltage			●	2.0			V
V_{IL}	LATCH Pin Lo Input Voltage			●			0.8	V
I_{IL}	LATCH Pin Current	V_{LATCH} = 0V		●			500	µA
t_{PD}	Propagation Delay (Note 4)	ΔV_{IN} = 100mV, OD = 5mV		 ●		10	14 16	ns ns
		ΔV_{IN} = 100mV, OD = 20mV		 ●		9	12 15	ns ns
Δt_{PD}	Differential Propagation Delay	(Note 4) ΔV_{IN} = 100mV, OD = 5mV					3	ns
	Latch Setup Time					2		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 3: Input bias current (I_B) is defined as the average of the two input currents.

Note 4: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1016 is sample tested with a 1V step and 500mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} limits shown can be guaranteed with this test if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions V_{OS} is added to overdrive. Differential propogation delay is defined as: $\Delta t_{PD} = t_{PDLH} - t_{PDHL}$

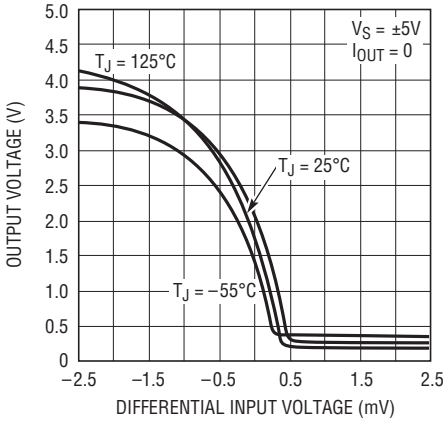
Note 5: Electrical specifications apply only up to 5.4V.

Note 6: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization. See text for discussion of input voltage range for supplies other than ±5V or 5V.

Note 7: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

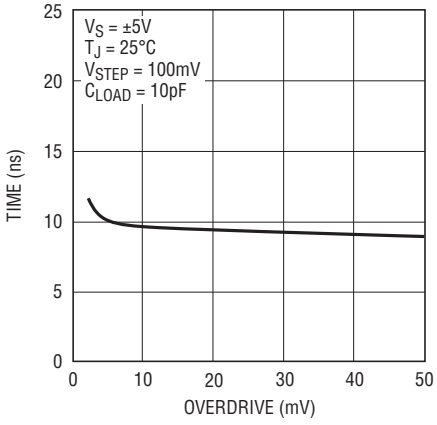
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Characteristics



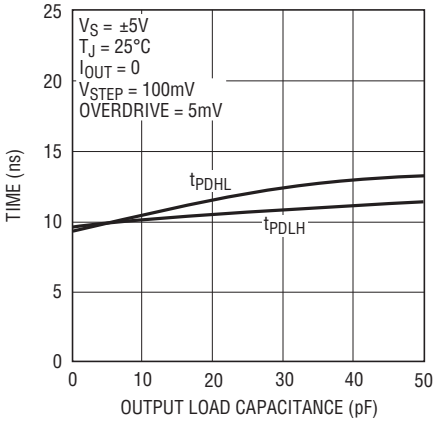
1016 G01

Propagation Delay vs Input Overdrive



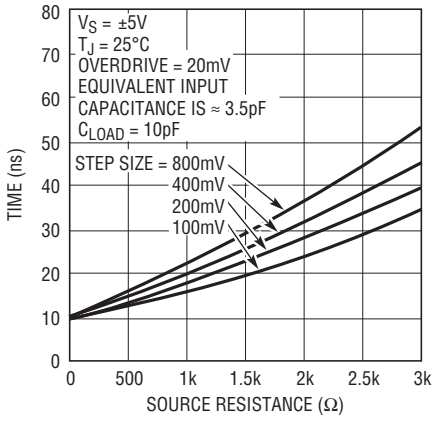
1016 G02

Propagation Delay vs Load Capacitance



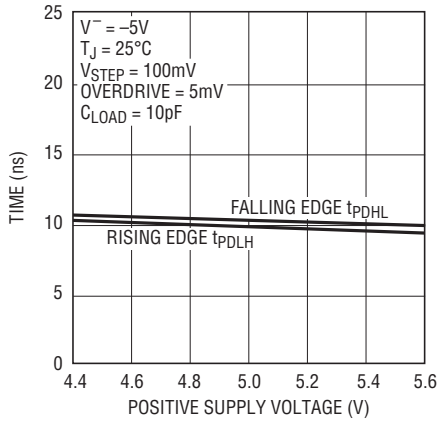
1016 G03

Propagation Delay vs Source Resistance



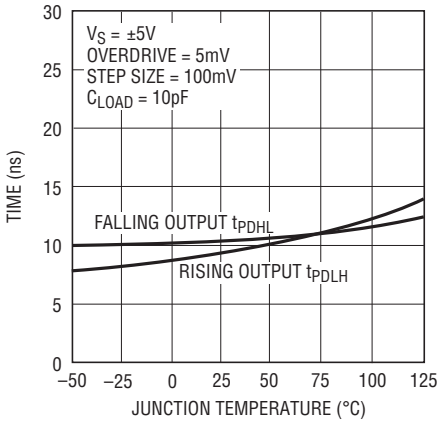
1016 G04

Propagation Delay vs Supply Voltage



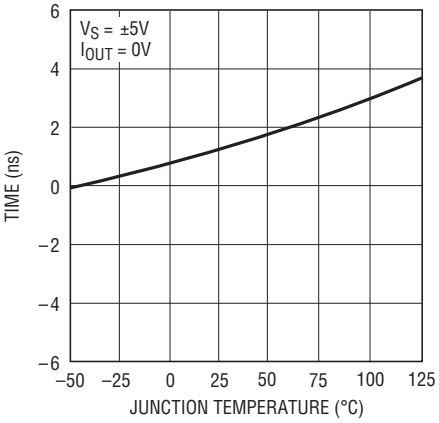
1016 G05

Propagation Delay vs Temperature



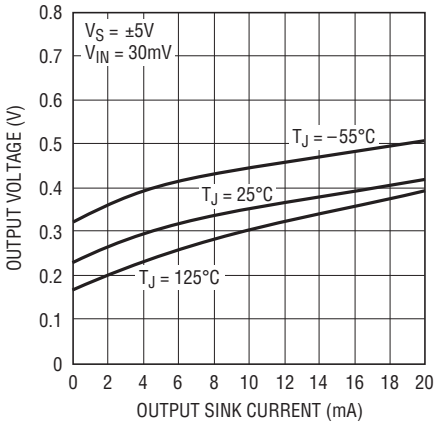
1016 G06

Latch Set-Up Time vs Temperature



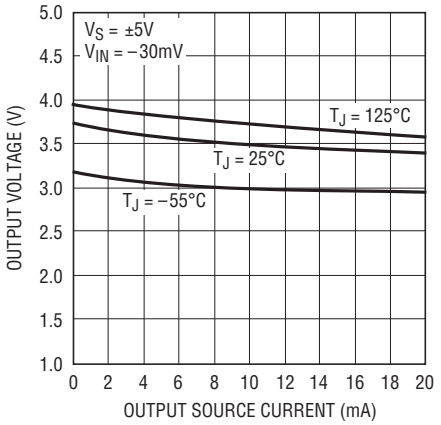
1016 G07

Output Low Voltage (V_{OL}) vs Output Sink Current



1016 G08

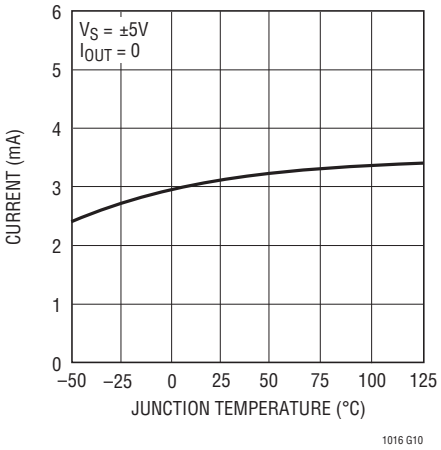
Output High Voltage (V_{OH}) vs Output Source Current



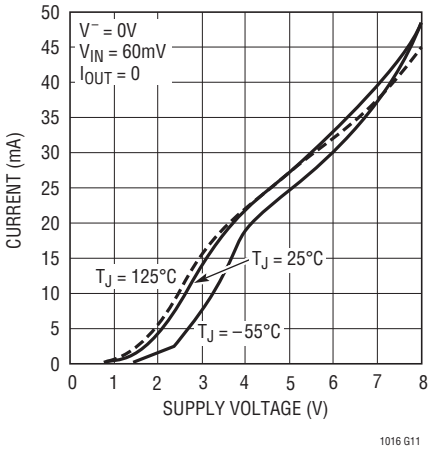
1016 G09

TYPICAL PERFORMANCE CHARACTERISTICS

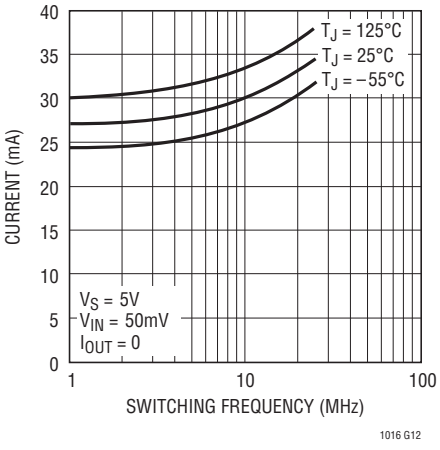
Negative Supply Current vs Temperature



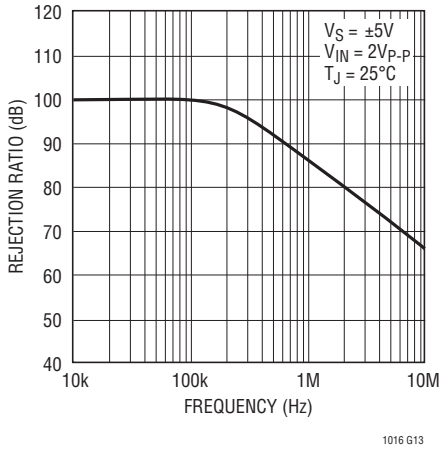
Positive Supply Current vs Positive Supply Voltage



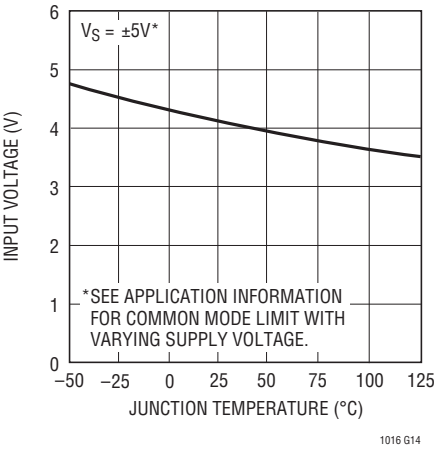
Positive Supply Current vs Switching Frequency



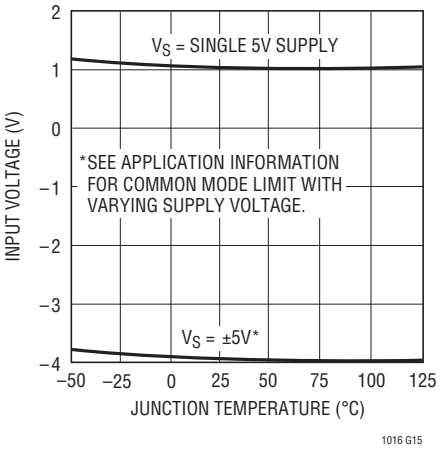
Common Mode Rejection vs Frequency



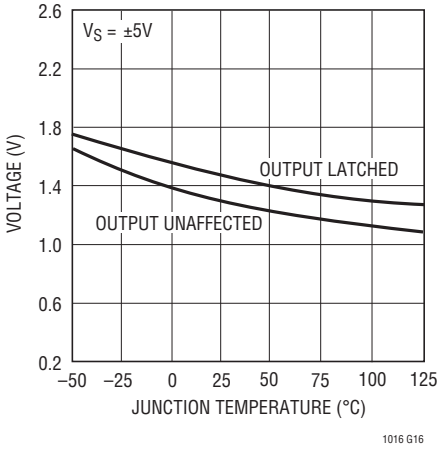
Positive Common Mode Limit vs Temperature



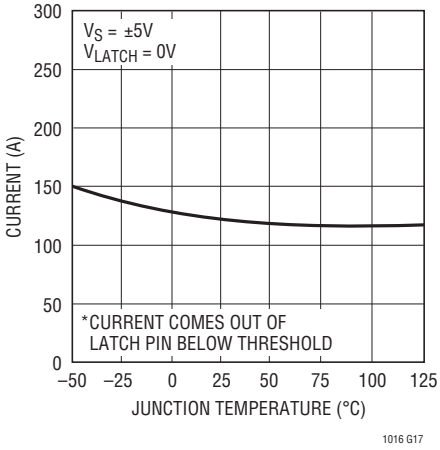
Negative Common Mode Limit vs Temperature



LATCH Pin Threshold vs Temperature



LATCH Pin Current* vs Temperature



APPLICATIONS INFORMATION

Common Mode Considerations

The LT1016 is specified for a common mode range of –3.75V to 3.5V with supply voltages of ±5V. A more general consideration is that the common mode range is 1.25V above the negative supply and 1.5V below the positive supply, independent of the actual supply voltage. The criteria for common mode limit is that the output still responds correctly to a small differential input signal. Either input may be outside the common mode limit (up to the supply voltage) as long as the remaining input is within the specified limit, and the output will still respond correctly. There is one consideration, however, for inputs that exceed the positive common mode limit. Propagation delay will be increased by up to 10ns if the signal input is more positive than the upper common mode limit and then switches back to within the common mode range. This effect is not seen for signals more negative than the lower common mode limit.

Input Impedance and Bias Current

Input bias current is measured with the output held at 1.4V. As with any simple NPN differential input stage, the LT1016 bias current will go to zero on an input that is low and double on an input that is high. If both inputs are less than 0.8V above V^-, both input bias currents will go to zero. If either input exceeds the positive common mode limit, input bias current will increase rapidly, approaching several milliamperes at $V_{IN} = V^+$.

Differential input resistance at zero differential input voltage is about 10kΩ, rapidly increasing as larger DC differential input signals are applied. Common mode input resistance is about 4MΩ with zero differential input voltage. With large differential input signals, the high input will have an input resistance of about 2MΩ and the low input greater than 20MΩ.

Input capacitance is typically 3.5pF. This is measured by inserting a 1k resistor in series with the input and measuring the resultant change in propagation delay.

LATCH Pin Dynamics

The LATCH pin is intended to retain input data (output latched) when the LATCH pin goes high. This pin will float to a high state when disconnected, so a flowthrough condition requires that the LATCH pin be grounded. To guarantee data retention, the input signal must be valid at least 5ns before the latch goes high (setup time) and must remain valid at least 3ns after the latch goes high (hold time). When the latch goes low, new data will appear at the output in approximately 8ns to 10ns. The LATCH pin is designed to be driven with TTL or CMOS gates. It has no built-in hysteresis.

Measuring Response Time

The LT1016 is able to respond quickly to fast low level signals because it has a very high gain-bandwidth product (≈50GHz), even at very high frequencies. To properly measure the response of the LT1016 requires an input signal source with very fast rise times and exceptionally clean settling characteristics. This last requirement comes about because the standard comparator test calls for an input step size that is large compared to the overdrive amplitude. Typical test conditions are 100mV step size with only 5mV overdrive. This requires an input signal that settles to within 1% (1mV) of final value in only a few nanoseconds with no ringing or “long tailing.” Ordinary high speed pulse generators are not capable of generating such a signal, and in any case, no ordinary oscilloscope is capable of displaying the waveform to check its fidelity. Some means must be used to inherently generate a fast, clean edge with known final value.

APPLICATIONS INFORMATION

The circuit shown in Figure 1 is the best *electronic* means of generating a known fast, clean step to test comparators. It uses a very fast transistor in a common base configuration. The transistor is switched "off" with a fast edge from the generator and the collector voltage settles to exactly 0V in just a few nanoseconds. The most important feature of this circuit is the lack of feedthrough from the generator to the comparator input. This prevents overshoot on the comparator input that would give a false fast reading on comparator response time.

To adjust this circuit for exactly 5mV overdrive, V1 is adjusted so that the LT1016 output under test settles to 1.4V (in the linear region). Then V1 is *changed* –5V to set overdrive at 5mV.

The test circuit shown measures low to high transition on the "+" input. For opposite polarity transitions on the output, simply reverse the inputs of the LT1016.

High Speed Design Techniques

A substantial amount of design effort has made the LT1016 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1016 is stable in its linear region, a feature no other high speed comparator has. Additionally, output stage switching does not appreciably change power supply current, further enhancing stability. These features make the application of the 50GHz gain-bandwidth LT1016 considerably easier than other fast comparators. Unfortunately, laws of physics dictate that the circuit *environment* the LT1016 works in must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns and memory access times in terms of nanoseconds. The LT1016 can be used in such fast digital systems and Figure 2 shows just how fast the device is. The simple test circuit allows us to see that the LT1016's (Trace B) response to the pulse generator (Trace A) is as fast as a TTL inverter (Trace C) even when the LT1016 has only millivolts of input signal! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

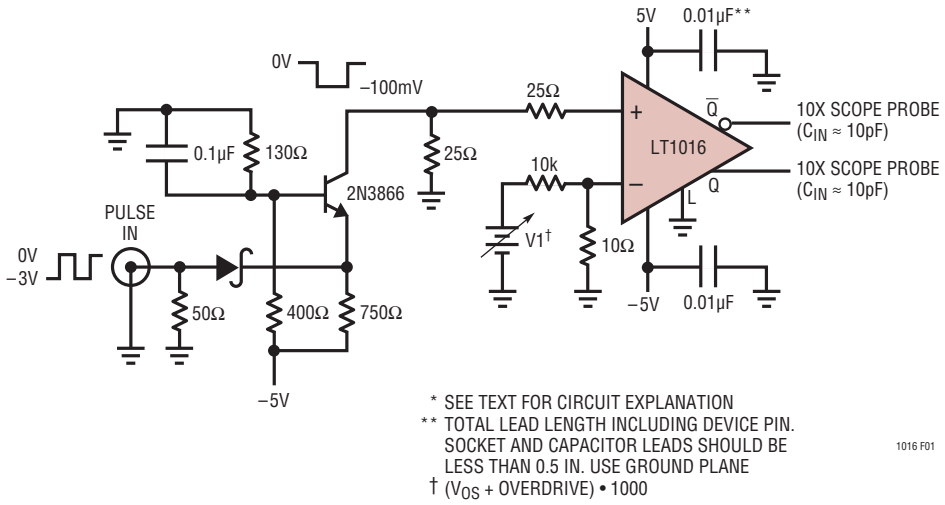


Figure 1. Response Time Test Circuit

APPLICATIONS INFORMATION

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully. An unbypassed LT1016 is shown responding to a pulse input in Figure 3. The power supply the LT1016 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1016, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors.*

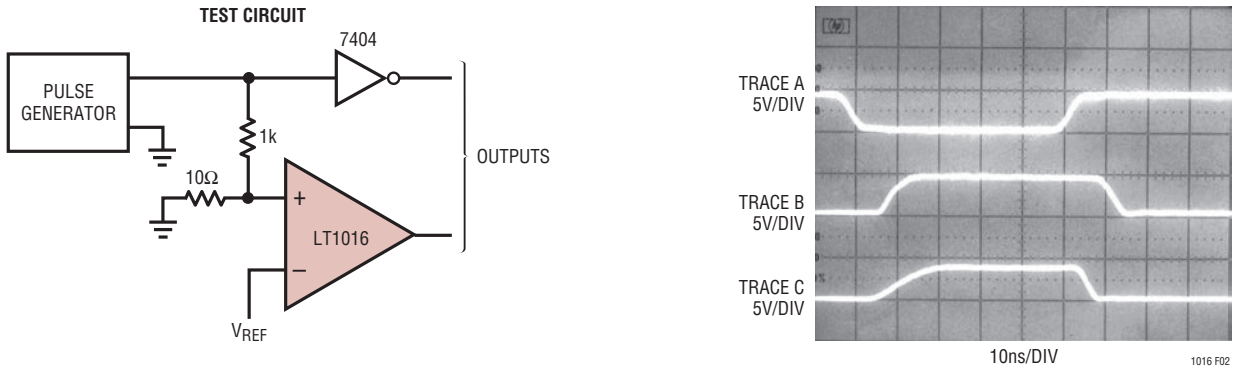


Figure 2. LT1016 vs a TTL Gate

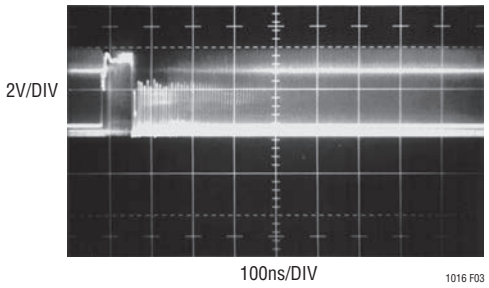


Figure 3. Unbypassed LT1016 Response

APPLICATIONS INFORMATION

In Figure 4 the LT1016's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount them as close as possible to the LT1016. An inch of wire between the capacitor and the LT1016 can cause problems. If operation in the linear region is desired, the LT1016 must be over a ground plate with good RF bypass capacitors (≥0.01µF) having lead lengths less than 0.2 inches. Do not use sockets.*

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V—quite a trick for a device running from a 5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes that match your oscilloscope's input characteristics and compensate them properly.* Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 10ns response time LT1016 appears to have 50ns edges! In this case, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1× or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

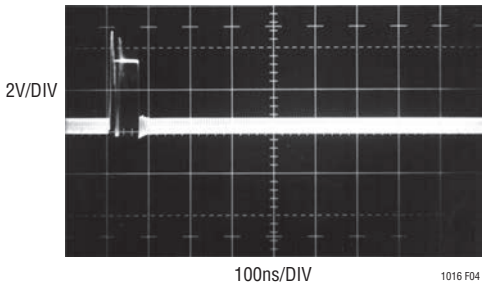


Figure 4. LT1016 Response with Poor Bypassing

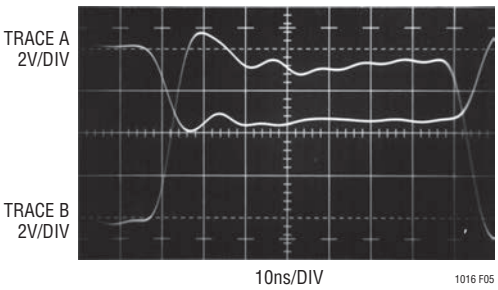


Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error

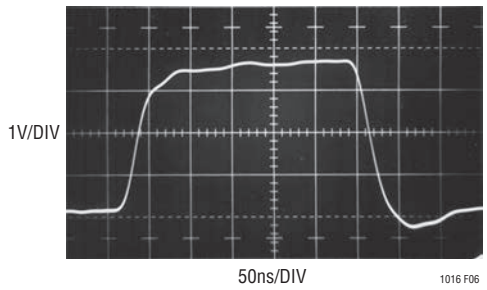


Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow

APPLICATIONS INFORMATION

In Figure 7 the probes are properly selected and applied but the LT1016's output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about six inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed one inch in length. *Keep the probe ground connection as short as possible.*

Figure 8 shows the LT1016's output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1016's GND pin connection is one inch long. The ground lead of the LT1016 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1016's ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1016's ground pin connection as short (typically 1/4 inch) as possible and run it directly to a low impedance ground. Do not use sockets.*

Figure 9 addresses the issue of the "low impedance ground," referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1016 without a "ground plane." A ground plane is formed by using a continuous conductive plane over the surface of the circuit board. The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1016 when input signal levels are low or slow moving.*

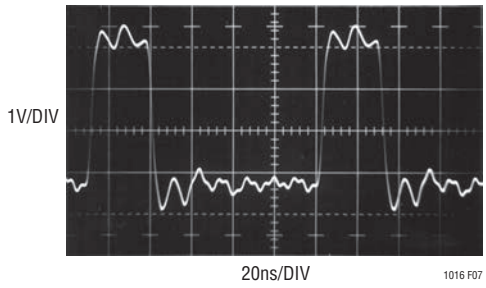


Figure 7. Typical Results Due to Poor Probe Grounding

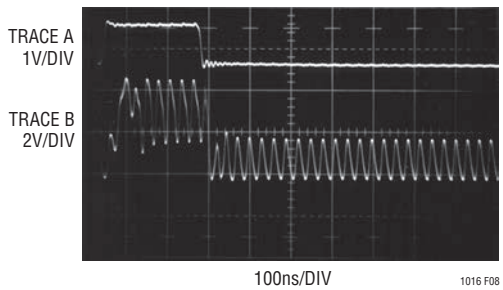


Figure 8. Excessive LT1016 Ground Path Resistance Causes Oscillation

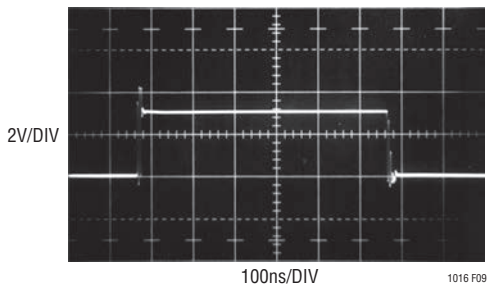


Figure 9. Transition Instabilities Due to No Ground Plane

APPLICATIONS INFORMATION

"Fuzz" on the edges is the difficulty in Figure 10. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A 3kΩ input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedances as low as possible, preferably 1k or less. Route output and input pins and components away from each other.*

The opposite of stray-caused oscillations appears in Figure 11. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input and output delay occurs. An RC combination of 2k source resistance and 10pF to ground gives a 20ns time constant—significantly longer than the LT1016's response time. *Keep source impedances low and minimize stray input capacitance to ground.*

Figure 12 shows another capacitance related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be caused by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few circumstances it may not affect overall circuit operation and is tolerable. *Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load.*

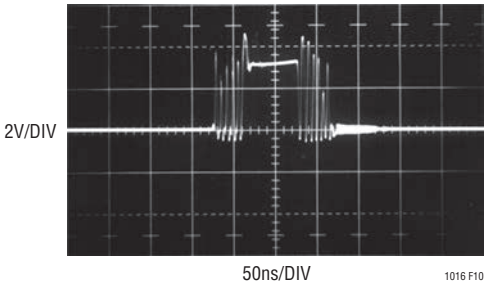


Figure 10. 3pF Stray Capacitive Feedback with 3kΩ Source Can Cause Oscillation

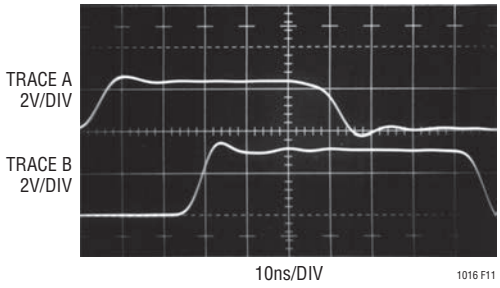


Figure 11. Stray 5pF Capacitance from Input to Ground Causes Delay

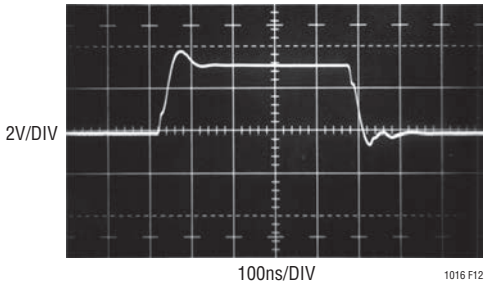


Figure 12. Excessive Load Capacitance Forces Edge Distortion

APPLICATIONS INFORMATION

Another output-caused fault is shown in Figure 13. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead that is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. *Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typically 250Ω to 400Ω).*

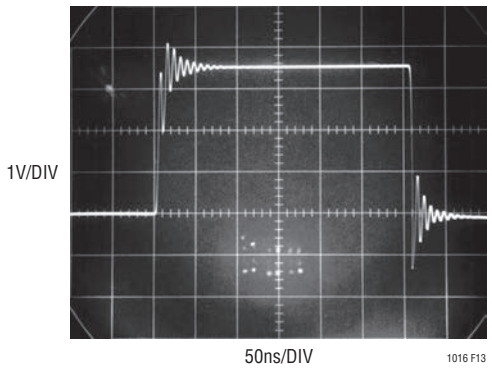


Figure 13. Lengthy, Unterminated Output Lines Ring from Reflections

200ns-0.01% Sample-and-Hold Circuit

Figure 14's circuit uses the LT1016's high speed to improve upon a standard circuit function. The 200ns acquisition time is well beyond monolithic sample-and-hold capabilities. Other specifications exceed the best commercial unit's performance. This circuit also gets around many of the problems associated with standard sample-and-hold approaches, including FET switch errors and amplifier settling time. To achieve this, the LT1016's high speed is used in a circuit which completely abandons traditional sample-and-hold methods.

Important specifications for this circuit include:

Acquisition Time	<200ns
Common Mode Input Range	±3V
Droop	1μV/μs
Hold Step	2mV
Hold Settling Time	15ns
Feedthrough Rejection	>>100dB

When the sample-and-hold line goes low, a linear ramp starts just below the input level and ramps upward. When the ramp voltage reaches the input voltage, A1 shuts off the ramp, latches itself off and sends out a signal indicating sampling is complete.

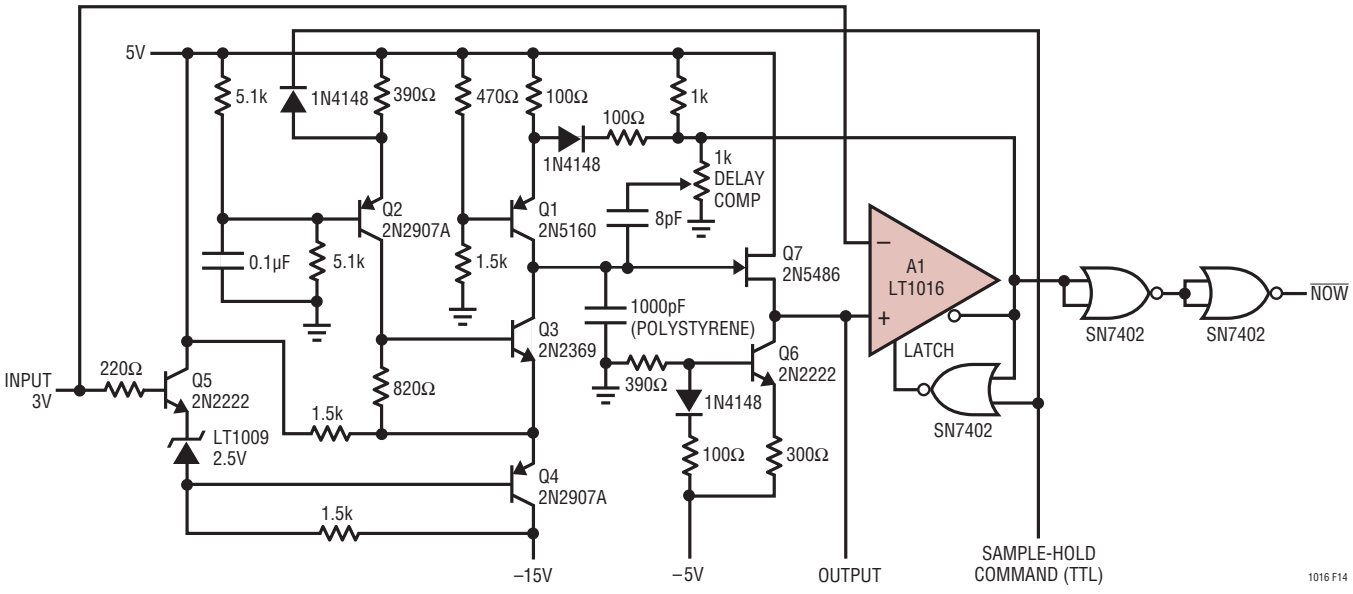


Figure 14. 200ns Sample-and-Hold

APPLICATIONS INFORMATION

1.8µs, 12-Bit A/D Converter

The LT1016's high speed is used to implement a very fast 12-bit A/D converter in Figure 15. The circuit is a modified form of the standard successive approximation approach and is faster than most commercial SAR 12-bit units. In this arrangement the 2504 successive approximation register (SAR), A1 and C1 test each bit, beginning with the MSB, and produce a digital word representing V_{IN}'s value.

To get faster conversion time, the clock is controlled by the window comparator monitoring the DAC input summing junction. Additionally, the DMOS FET clamps the DAC output to ground at the beginning of each clock cycle, shortening DAC settling time. After the fifth bit is converted, the clock runs at maximum speed.

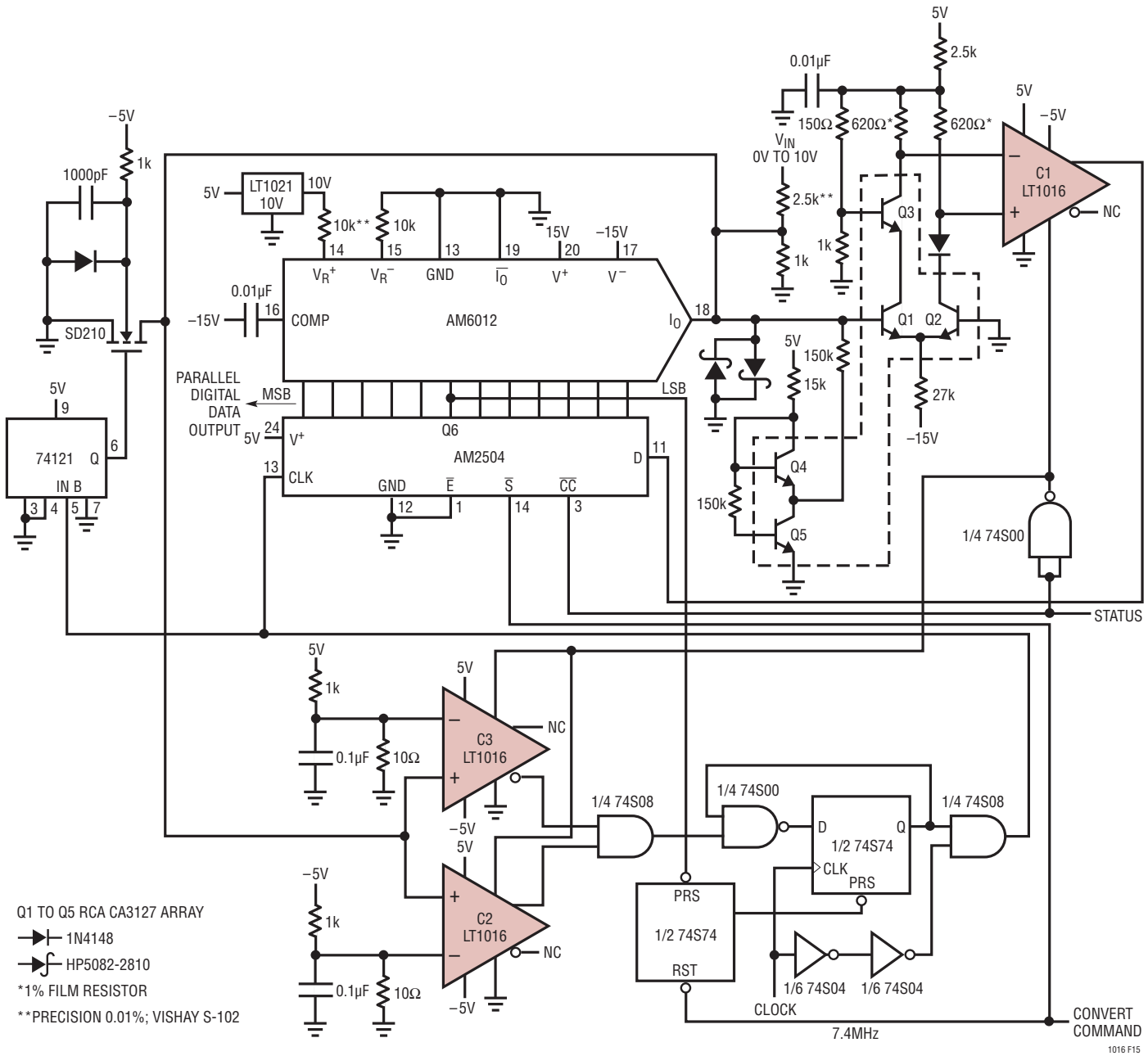
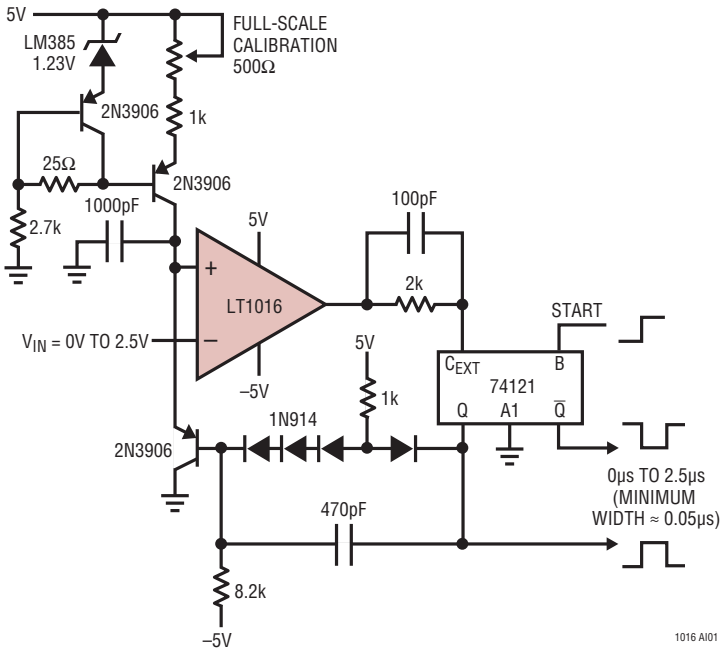


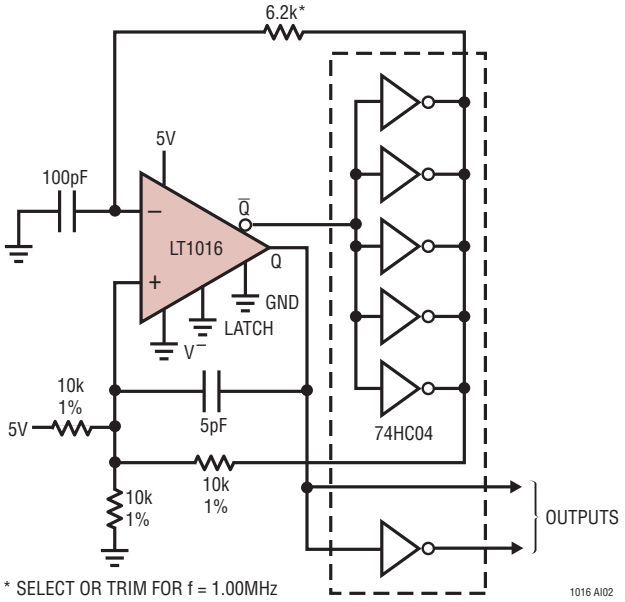
Figure 15. 12-Bit 1.8µs SAR A-to-D

TYPICAL APPLICATIONS

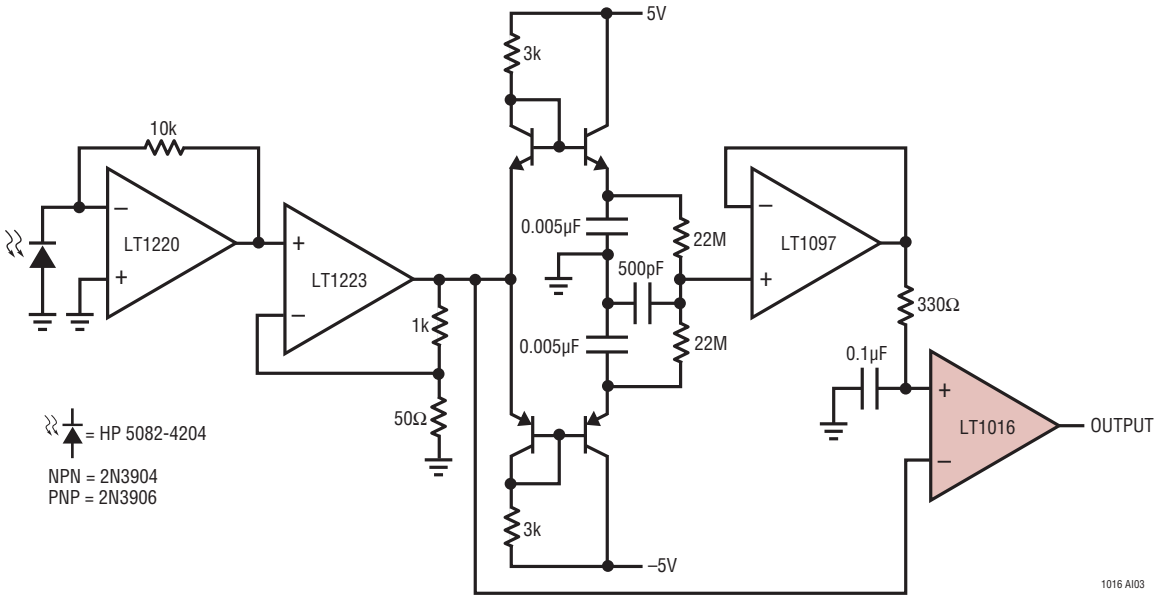
Voltage Controlled Pulse Width Generator



Single Supply Precision RC 1MHz Oscillator

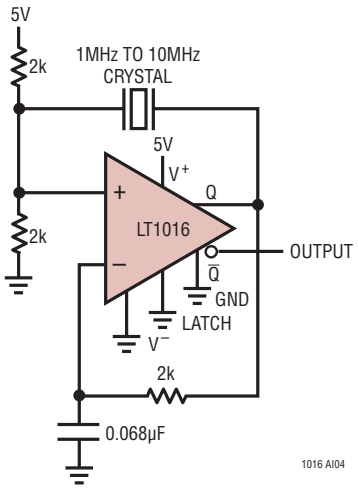


50MHz Fiber Optic Receiver with Adaptive Trigger

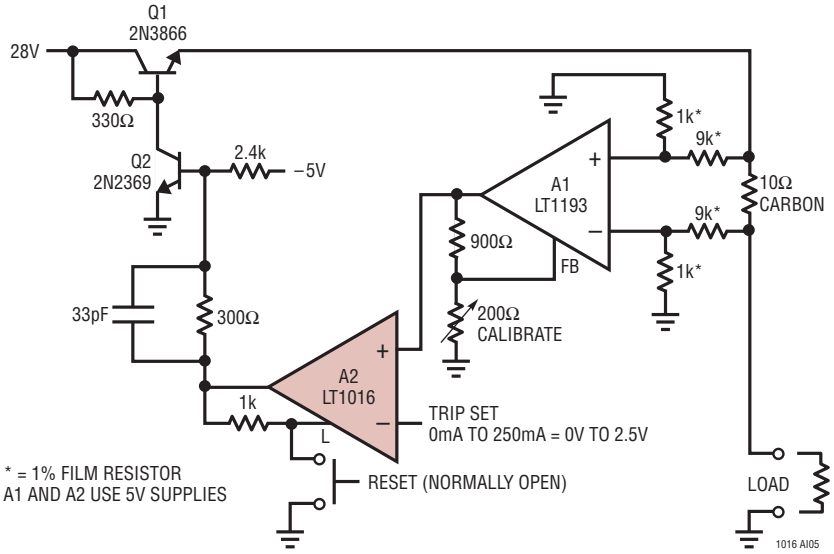


TYPICAL APPLICATIONS

1MHz to 10MHz Crystal Oscillator



18ns Fuse with Voltage Programmable Trip Point



APPENDIX A

About Level Shifts

The TTL output of the LT1016 will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1016 based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1016 is a sink-source pair (Figure A1) with good ability to drive capacitance (such as feedforward capacitors).

Figure A2 shows a noninverting voltage gain stage with a 15V output. When the LT1016 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

Figure A3 is a very versatile stage. It features a bipolar swing that may be programmed by varying the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1016 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1016's output transition (Trace A, Figure A4), but Q2's switching is clean (Trace B, Figure A4) with 3ns delay on the rise and fall of the pulse.

Figure A5 is similar to Figure A2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET which switches 1A at 15V. Most of the 7ns to 9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_Ts. To get the kind of results shown, switching times in the ns range and f_Ts approaching 1GHz are required.

APPENDIX A

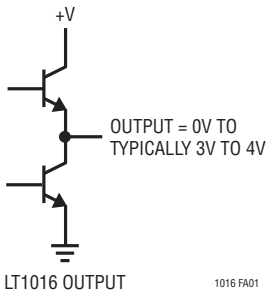


Figure A1

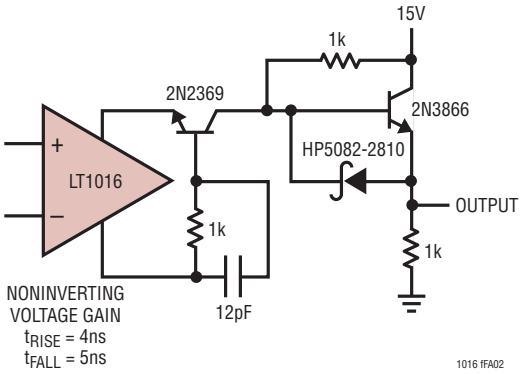


Figure A2

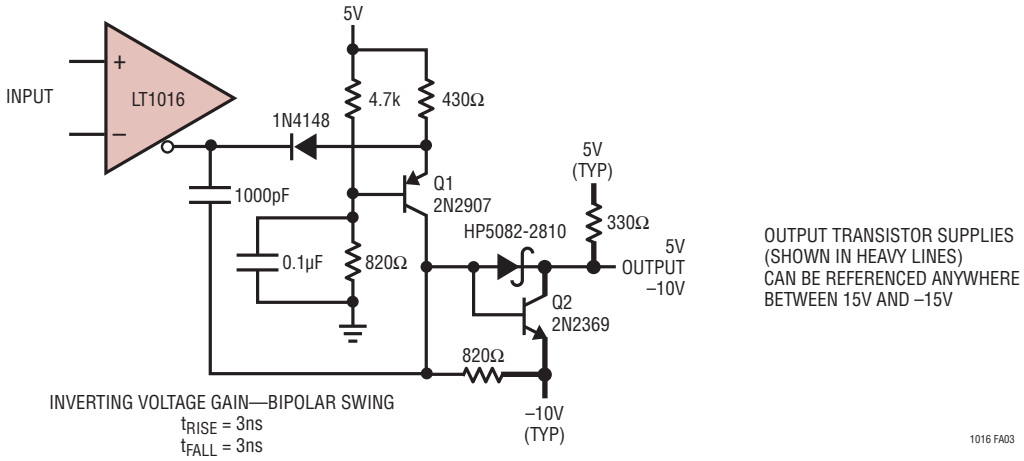


Figure A3

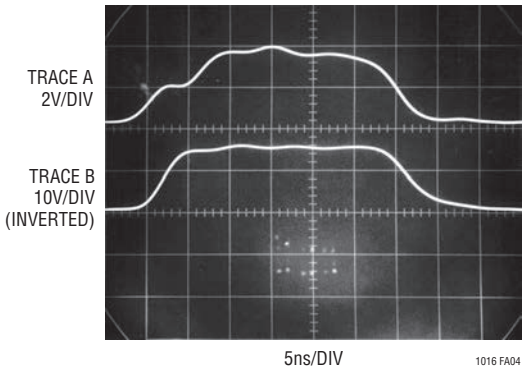


Figure A4. Figure A3's Waveforms

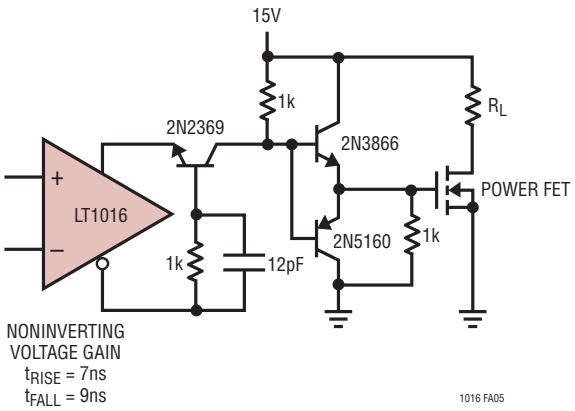
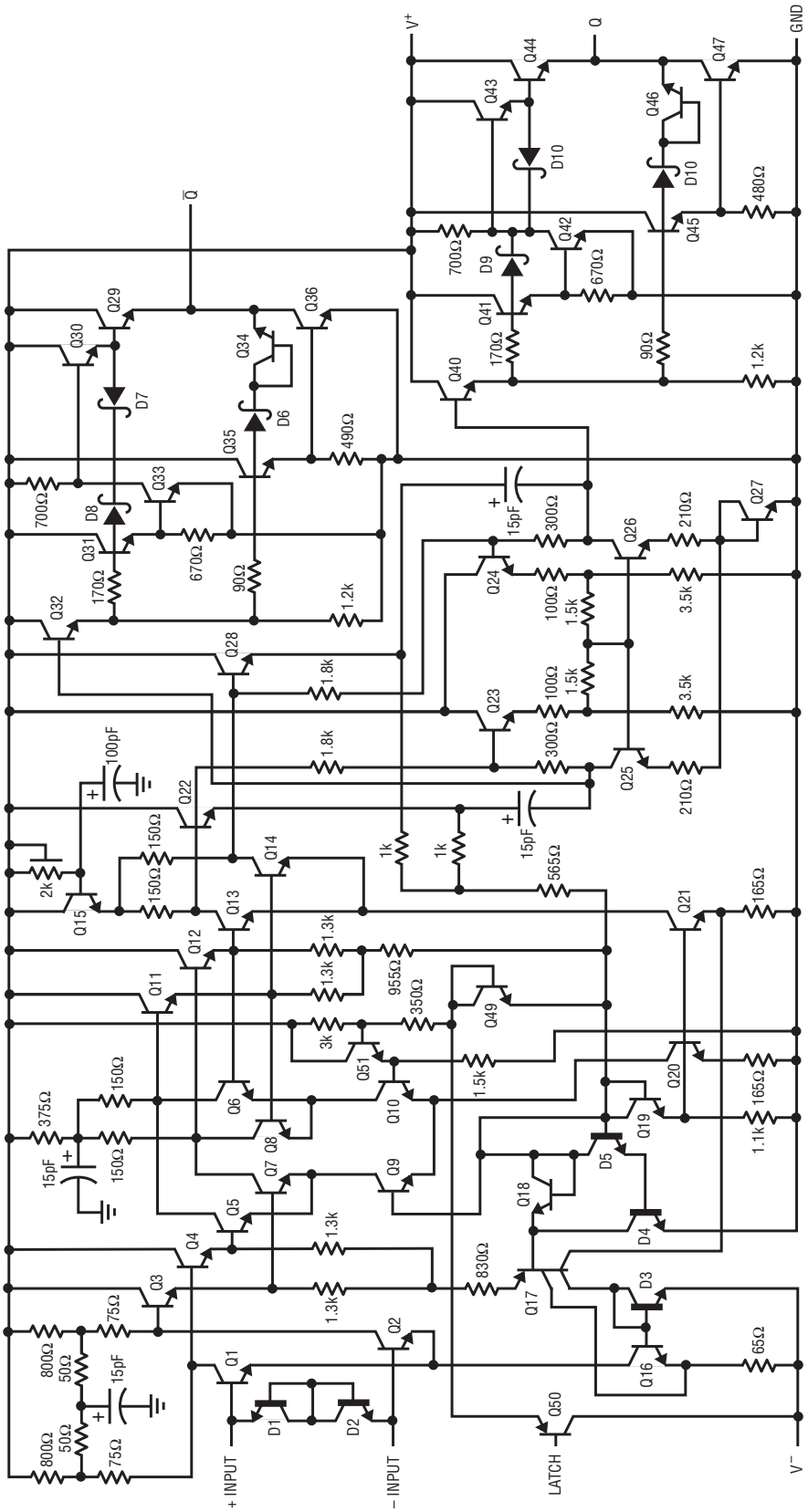


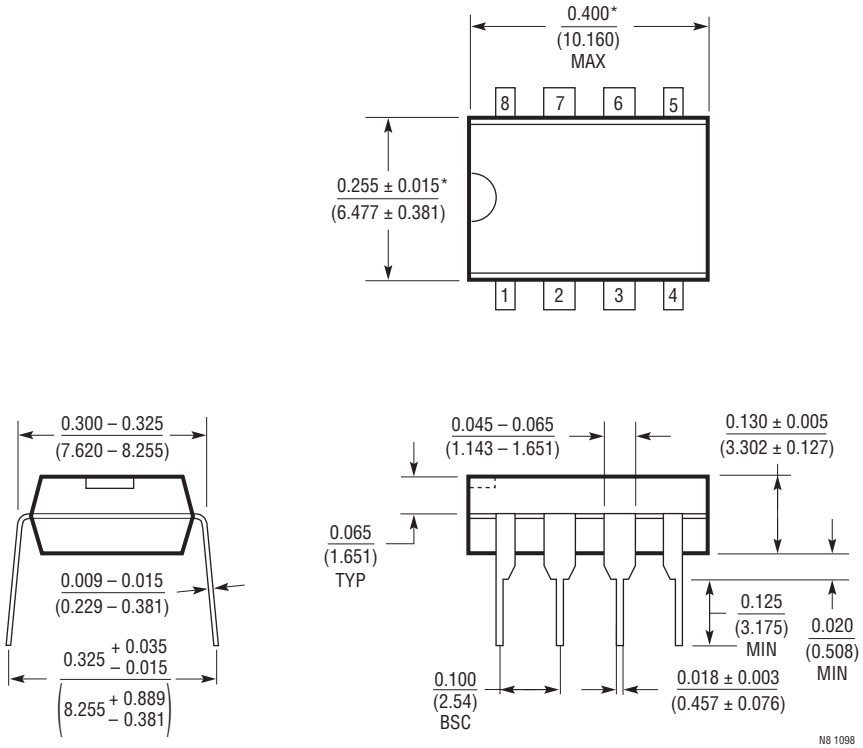
Figure A5

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

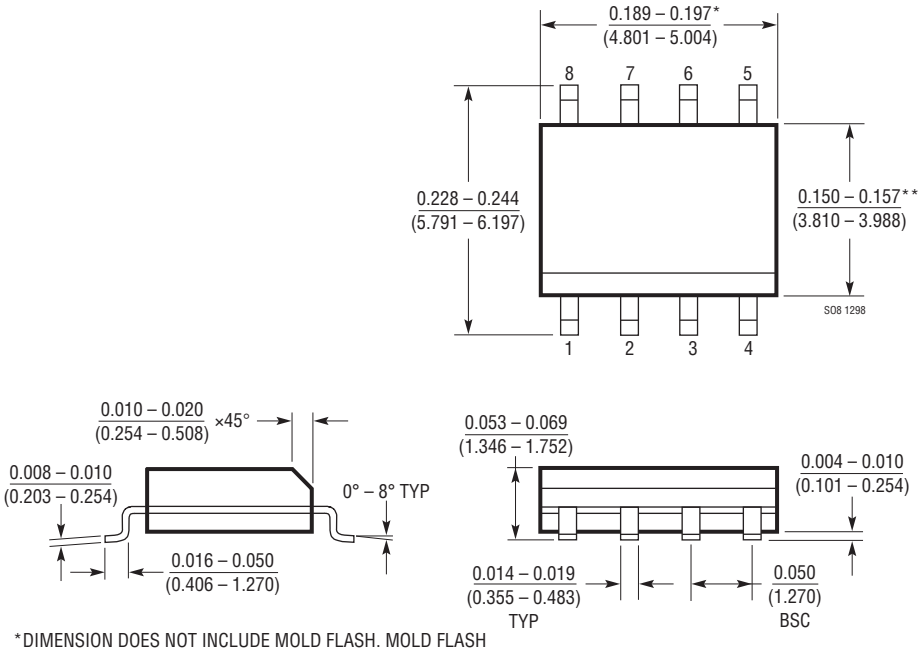
N8 Package
8-Lead PDIP (Narrow .300 Inch
(Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

APPLICATIONS INFORMATION

1Hz to 10MHz V-to-F Converter

The LT1016 and the LT1122 FET input amplifier combine to form a high speed V-to-F converter in Figure 16. A variety of techniques is used to achieve a 1Hz to 10MHz output. Overrange to 12MHz (V_{IN} = 12V) is provided. This circuit's dynamic range is 140dB, or seven decades, which is wider than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than monolithic V-to-F's now available. The theory of operation is based on the identity Q = CV.

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge, Q, to a summing node, Σ. The circuit's input furnishes a comparison current at the summing node. This difference current is integrated in A1's 68pF feedback capacitor. The amplifier controls the circuit's output pulse generator, closing feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency that permits enough charge pumping to offset the input signal. Thus, the output frequency is linearly related to the input voltage.

To trim this circuit, apply 6.000V at the input and adjust the 2kΩ pot for 6.000MHz output. Next, excite the circuit with a 10.000V input and trim the 20k resistor for 10.000MHz output. Repeat these adjustments until both points are fixed. Linearity of the circuit is 0.03%, with full-scale drift of 50ppm/°C. The LTC1050 chopper op amp servos the integrator's noninverting input and eliminates the need for a zero trim. Residual zero point error is 0.05Hz/°C.

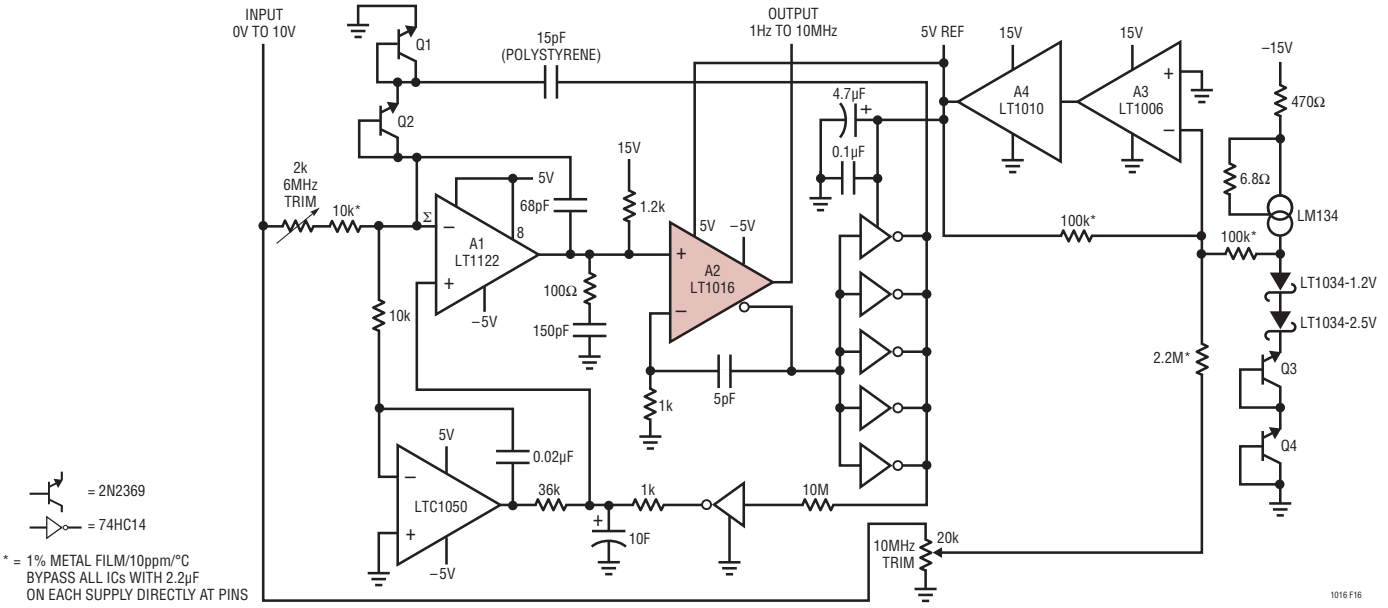


Figure 16. 1Hz to 10MHz V-to-F Converter. Linearity is Better Than 0.03% with 50ppm/°C Drift

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1116	12ns Single Supply Ground-Sensing Comparator	Single Supply Version of LT1016, LT1016 Pinout and Functionality
LT1394	7ns, UltraFast, Single Supply Comparator	6mA, 100MHz Data Rate, LT1016 Pinout and Functionality
LT1671	60ns, Low Power, Single Supply Comparator	450µA, Single Supply Comparator, LT1016 Pinout and Functionality
LT1711/LT1712	Single/Dual 4.5ns 3V/5V/±5V Rail-to-Rail Comparators	Rail-to-Rail Inputs and Outputs
LT1713/LT1714	Single/Dual 7ns 3V/5V/±5V Rail-to-Rail Comparators	5mA per Comparator, Rail-to-Rail Inputs and Outputs
LT1715	Dual 150MHz 4ns 3V/5V Comparator	150MHz Toggle Rate, Independent Input/Output Supplies
LT1719/LT1720/LT1721	Single/Dual/Quad 4.5ns 3V/5V Comparators	4mA per Comparator, Ground-Sensing Rail-to-Rail Inputs and Outputs

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0601 1.5K REV C • PRINTED IN USA