



separator technology allowing for ease of testing and use. The LPC47N227 supports both 1Mbps and 2Mbps data rates and vertical recording operation at 1Mbps Data Rate.

The LPC47N227 also features a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI nCLKRUN support, relocatable configuration ports and three DMA channel options. Both on-chip UARTs are compatible with the NS16C550. One UART includes additional support for a Serial Infrared Interface that complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats (used by Sharp and other PDAs), as well as Consumer IR.

The parallel port is compatible with IBM PC/AT architectures, as well as IEEE 1284 EPP and ECP. The parallel port ChiProtect circuitry prevents damage caused by an attached powered printer when the LPC47N227 is not powered.

The LPC47N227 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. The LPC47N227 also features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the FDC, parallel port, and UARTs.

The LPC47N227 supports the ISA Plug-and-Play Standard (Version 1.0a) and provides the recommended functionality to support Windows '95/'98 and PC99. The I/O Address, DMA Channel and Hardware IRQ of each device in the LPC47N227 may be reprogrammed through the internal configuration registers. There are 192 I/O address location options, a Serialized IRQ interface, and three DMA channels.

ORDERING INFORMATION

Order Numbers:

LPC47N227-MT for 100 Pin TQN, Lead-free RoHS Compliant Package

LPC47N227-MV for 100 Pin STQN, Lead-free RoHS Compliant Package



80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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PRODUCT PREVIEW

The block diagram illustrates the internal architecture of the LPC1114 microcontroller. Key components include:

- Configuration Registers**: Connected to the CONTROL, ADDRESS, DATA bus.
- ACPI BLOCK**: Connected to the CONTROL, ADDRESS, DATA bus.
- SERIAL IRQ**: Receives SER_IRQ and PCI_CLK signals; outputs LAD0-LAD3, nLDRQ, nLPCPD, and nCLKRUN.
- LPC BUS INTERFACE**: Manages external communication signals.
- SMSC PROPRIETARY 82077 COMPATIBLE VERTICAL FLOPPY DISK CONTROLLER CORE**: Interfaces with the digital data separator and provides control signals like nMTR0, nDS0, nDIR, nSTEP, etc.
- DIGITAL DATA SEPARATOR PRE-COMPENSATION**: Processes data signals (nWDATA, nRDATA) and provides clock signals (WCLOCK, RCLOCK).
- MULTI-MODE PARALLEL PORT/FDC MUX**: Controls PD[0:7], BUSY, SLCT, PE, nERROR, nACK, nSLCTIN, nALF, nINIT, and nSTROBE.
- GENERAL PURPOSE I/O**: Controls GP pins (GP10-GP14), GP2/GP23, GP3/GP24, GP4, and IRQIN1/IRQIN2/FDC_PP.
- 16C550 COMPATIBLE SERIAL PORT 1**: Controls TXD1, nRTS1, nDTR1, nCTS1, RXD1, nDSR1, nDCD1, and nRI1.
- 16C550 COMPATIBLE SERIAL PORT 2 WITH INFRARED INTERFACE**: Controls IRTX2, IRMODE*, TXD2, nRTS2, nDTR2, IRRX2, IRRX3*, RXD2, nCTS2, nDSR2, nDCD2, and nRI2.
- CLOCK GEN**: Provides the main CLOCK signal from V_{TR}, V_{CC}, and V_{SS}.
- SMI, PME, WDT**: Status and control registers outputting nIO_SMI* and nIO_PME.

* Denotes Multifunction Pins

PACKAGE OUTLINES

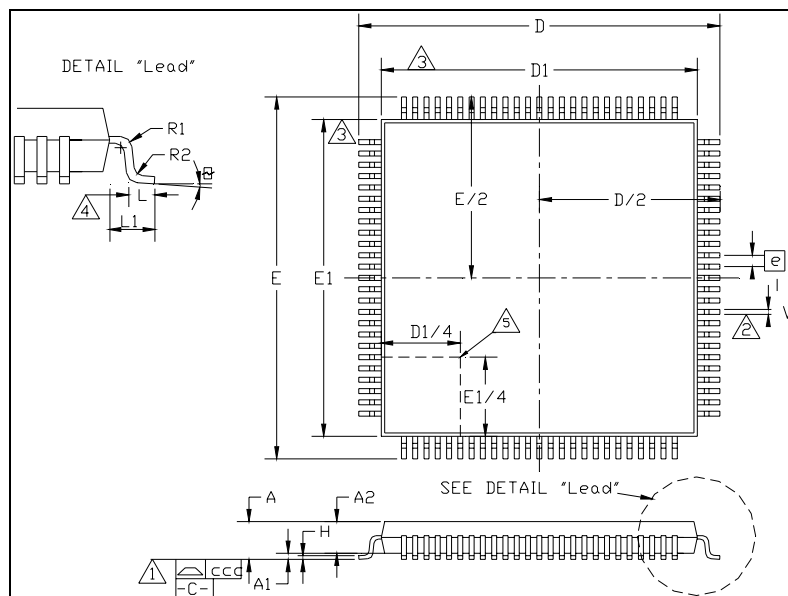


FIGURE 1 – 100 PIN TQN LEAD-FREE PACKAGE OUTLINE

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.60	Overall Package Height
A1	0.05	~	~	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	15.80	16.00	16.20	X Span
D/2	7.90	8.00	8.10	¹/₂ X Span Measure from Centerline
D1	13.90	14.00	14.10	X body Size
E	15.80	16.00	16.20	Y Span
E/2	7.90	8.00	8.10	¹/₂ Y Span Measure from Centerline
E1	13.90	14.00	14.10	Y body Size
H	~	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
θ	0°	~	8°	Lead Foot Angle
W	~	0.25	~	Lead Width
R1	~	0.20	~	Lead Shoulder Radius
R2	~	0.20	~	Lead Foot Radius
ccc	~	~	0.0762	Coplanarity (Assemblers)
ccc	~	~	0.08	Coplanarity (Test House)

Notes:

¹ Controlling Unit: millimeter

² Tolerance on the position of the leads is ± 0.04 mm maximum.

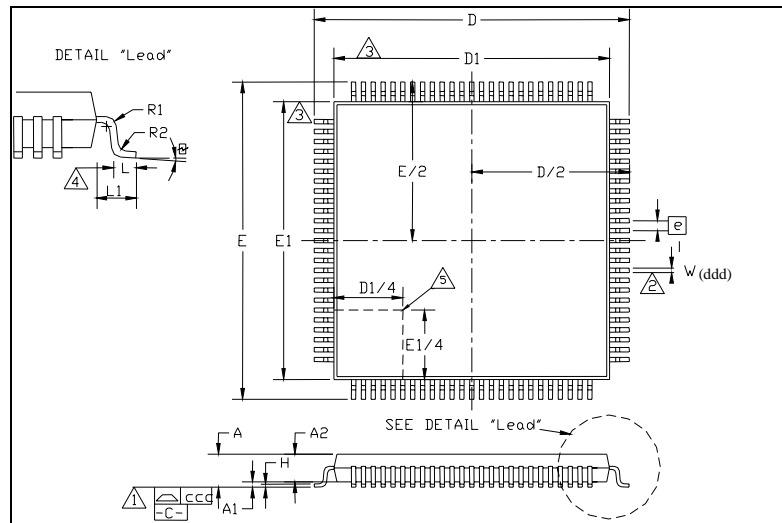
³ Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.

⁴ Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane is 0.78-1.08 mm.

⁵ Details of pin 1 identifier are optional but must be located within the zone indicated.

⁶ Shoulder widths must conform to JEDEC MS-026 dimension 'S' of a minimum of 0.20mm.

PRODUCT PREVIEW


FIGURE 2 – 100 PIN STQN LEAD-FREE PACKAGE OUTLINE

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	13.80	14.00	14.20	X Span
D/2	6.90	7.00	7.10	¹/₂ X Span Measure from Centerline
D1	11.80	12.00	12.20	X body Size
E	13.80	14.00	14.20	Y Span
E/2	6.90	7.00	7.10	¹/₂ Y Span Measure from Centerline
E1	11.80	12.00	12.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
θ	0°	3.5°	7°	Lead Foot Angle
W	0.13	0.16	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	.0762	Coplanarity (Assemblers)
ccc	~	~	0.08	Coplanarity (Test House)
ddd	~	~	0.035	True Position Spread (Bent Leads)

Notes:

- ¹ Controlling Unit: millimeter
- ² Minimum space between protrusion and an adjacent lead is .007 mm.
- ³ Details of pin 1 identifier are optional but must be located within the zone indicated.
- ⁴ Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
- ⁵ Shoulder widths must conform to JEDEC MS-026 dimension 'S' of a minimum of 0.20mm.