

LPC47M182

Description

The LPC47M182 is a 3.3V (5V tolerant) PC99a/PC2001 compliant Advanced I/O controller for Desktop PCs. The device, which implements the Low Pin Count (LPC) interface, includes I/O functionality as well as Motherboard GLUE logic into a 128-pin package. This is a space saving solution on the motherboard resulting in lower cost. The LPC47M182 also provides 13 general purpose pins, which offer flexibility to the system designer, and two Fan Tachometer Inputs. The LPC47M182's LPC interface supports LPC I/O and DMA cycles.

The LPC47M182 includes complete legacy I/O: a keyboard interface; Microchip's true CMOS 765B floppy disk controller with advanced digital data separator; two 16C550A compatible UARTs; one Multi-Mode parallel port including ChiProtect circuitry plus EPP and ECP. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures, in addition, it provides data overflow and underflow protection. The Microchip's patented advanced digital data separator allows for ease of testing and use. The parallel port is compatible with IBM PC/AT architecture, as well as IEEE 1284 EPP and ECP. The LPC47M182 incorporates sophisticated power control circuitry (PCC) which includes support for keyboard and mouse wake up events as well as PME support. The PCC supports multiple low power-down modes. The LPC47M182 is ACPI 1.0b/2.0 compatible.

The Motherboard GLUE logic includes various power management logic; including generation of nRSMRST, Power OK signal generation, 5V main and standby reference generation. There are also three LEDs to indicate power status and hard drive activity. The translation circuit converts 3.3V signals to 5V signals. Also included is SMBus main power well to resume power well isolation circuitry.

The LPC47M182 supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, DMA Channel and hardware IRQ of each logical device in the LPC47M182 may be reprogrammed through the internal configuration registers. There are up to 480 (960 for Parallel Port) I/O address location options, a Serialized IRQ interface, and three DMA channels. On chip, Interrupt Generating Registers enable external software to generate IRQ1 through IRQ15 on the Serial IRQ Interface.

The LPC47M182's Enhanced Digital Data Separator does not require any external filter components and is therefore easy to use and offers lower system costs and reduced board area. The LPC47M182 is register compatible with Microchip's proprietary 82077AA core.

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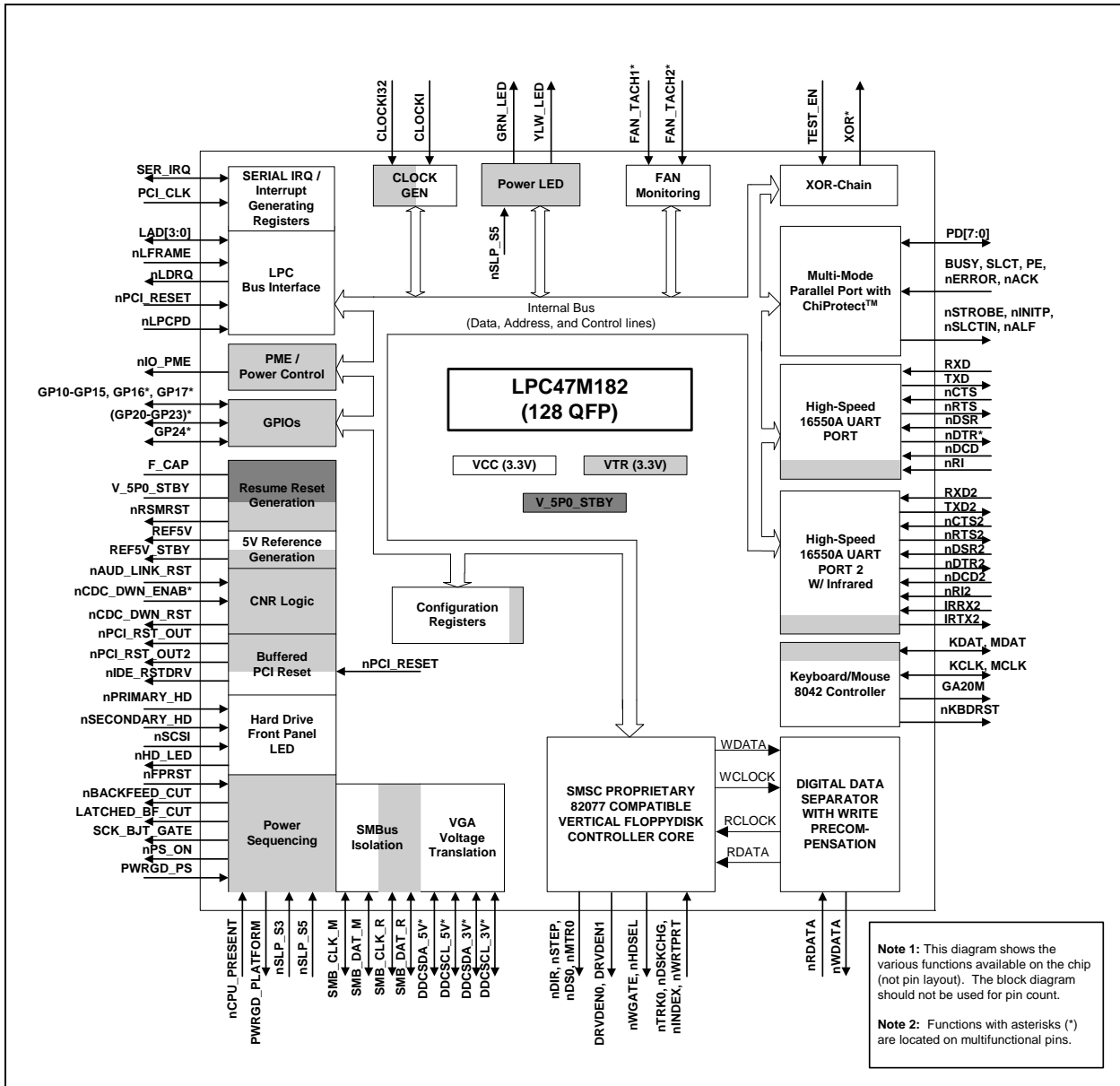
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LPC47M182

BLOCK DIAGRAM

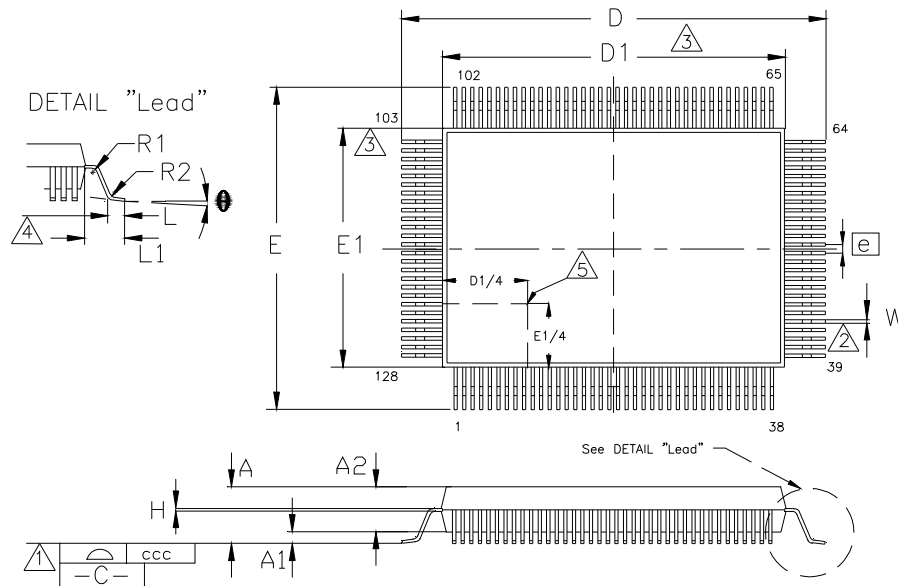
FIGURE 1: LPC47M182 BLOCK DIAGRAM



PACKAGE OUTLINE

Note: For the most current package drawings, see the Microchip Packaging Specification at: <http://www.microchip.com/packaging>.

FIGURE 2: 128-PIN QFP PACKAGE, 14 X 20 X 2.7 MM BODY, 3.2 MM FOOTPRINT



	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.00	23.20	23.40	X Span
D1	19.90	20.00	20.10	X body Size
E	17.00	17.20	17.40	Y Span
E1	13.90	14.00	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.60	~	Lead Length
e	0.50 Basic			Lead Pitch
θ	0°	~	7°	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.30	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Note 1: Controlling Unit: millimeter.

2: Tolerance on the position of the leads is ± 0.04 mm maximum.

3: Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.

4: Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

5: Details of pin 1 identifier are optional but must be located within the zone indicated.

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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001809A (08-27-14)	Replaces previous SMSC version Rev. 1.9 (03-23-07)	

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