TABLE OF CONTENTS

LIST OF FIGURES

PRODUCT DESCRIPTION

The Le78D11 VoSLAC device contains high performance circuits that provide A/D and D/A conversion for two sets of voice (codec), loop supervision, and line diagnostic functions. Fixed function DSP resources in the device are used to perform modem detection, DTMF detection, ADPCM voice compression, and echo cancellation. Although the device offers a high degree of programmability, the available WinSLAC and VoicePath™ software packages allow the user to easily configure and control the Voice Line Circuits (VLC) and the programmable filter coefficients and loop supervision data are easily calculated.

The main functions that can be observed and controlled through the Le78D11 VoSLAC device are:

- Off Hook detection
- Ring trip detection
- Line Fault Indication
- Ground Key detection
- DTMF detection
- Fax and Modem tone (1100 Hz and 2100 Hz) detection
- DC Loop Current Limit
- Ring Generation
- Subscriber line impedance matching
- Metering Signal Generation
- Line Circuit test

In order for the Le78D11 VoSLAC device to accomplish the above functions, it must receive input from the Zarlink Le77D11 devices, which sense the following parameters and scale them appropriately for the Le78D11 VoSLAC device:

- V_{IN}: A metallic AC voltage that is proportional to the upstream AC loop current
- I_{MT}: A current that is proportional to the DC + AC loop current
- $\overline{F}$: A logic Low indicates a fault or ground key condition

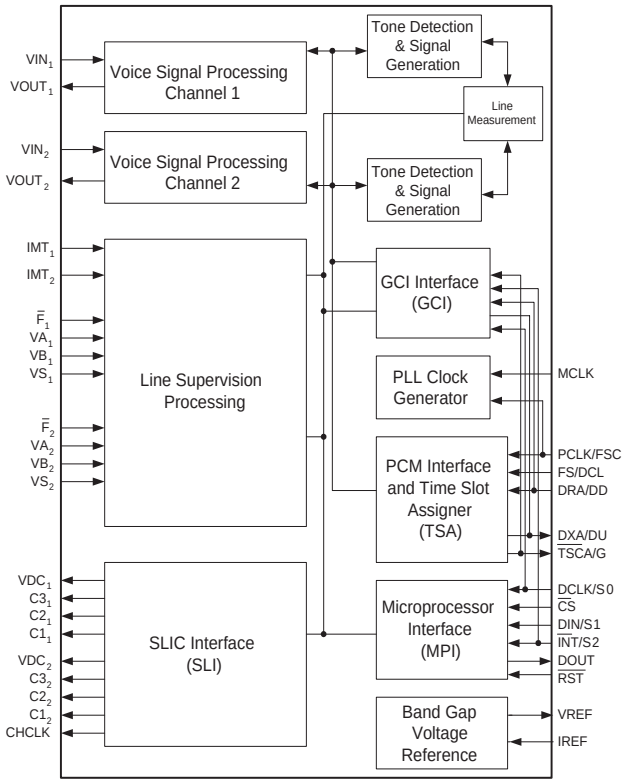
The Le78D11 VoSLAC device then outputs the following to the Le77D11 SLIC device:

- V_{DC}: DC loop current limit threshold control voltage
- V_{OUT}: Downstream voice and low level metering signals or internal ringing or test signals

The Le78D11 device performs the codec and filter functions associated with the 4-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals. The user programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the 2-wire termination impedance, and provide frequency distortion adjustment (equalization) of the receive and transmit paths. An Adaptive Transhybrid Balance filter is included that allows the Le78D11 VoSLAC device to dynamically adjust to changing line conditions minimizing objectionable echo. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's complement, 8-bit companded A-law or µ-law, or 32 kbit/s or 24 kbit/s ADPCM.

BLOCK DESCRIPTIONS

Figure 1. Le78D11 VoSLAC Device Block Diagram



The following provides an overview of the functions of the Le78D11 VoSLAC device. Detailed descriptions and command sets are provided in the *Le77D11/Le78D11 Chip Set User's Guide* (document ID# 080716).

The Le78D11 VoSLAC device supports two digital interface modes: (1) PCM/MPI, where voice and control data are carried over separate serial interfaces, and (2) GCI, where the voice and control data are combined onto a single serial bus. The two modes are exclusive and the associated pins have dual functions. The naming convention for the pins lists the PCM/MPI interface function first then the GCI function.

PCM Interface and Time Slot Assigner (TSA)

The Le78D11 VoSLAC device powers up in PCM/MPI mode. If a signal is detected on PCLK (PCM Clock) and FS (Frame Sync) is toggling at a slower rate, the PCM interface and time slot assigner functions are maintained. This block uses five signals: PCLK, FS, DXA, DRA and TSCA.

The PCM Interface is a synchronous serial mode of communication between the system and the Le78D11 VoSLAC device for exchanging the encoded voice signals on a "PCM highway". This highway uses FS as a nominally 8kHz synchronization (frame) reference and PCLK as a data strobe that determines the rate at which the data is shifted out of the DXA pin and into the DRA pin. The Le78D11 VoSLAC device transmits/ receives either 8-bits of (A-law/μ-law) compressed voice data, 4bits of 32 kb/s ADPCM data, 3 bits of 24 kb/s ADPCM data, or 16-bits of linear two's complement voice data every frame. The PCLK frequency can be any multiple of the FS frequency from 128 kHz to 8.192 MHz for compressed data, and from 256 kHz to 8.192 MHz for linear data. The position of the data within the frame is controlled by the TSA and determined by a combination of three programmable variables. The first is the Transmit and Receive Clock Slot Register which allows setting from 0 to 7 PCLK periods of clock skew in the system. The second is the XE bit, also in the Transmit and Receive Clock Slot Register, which selects the clock edge used for transmitting or receiving data. Finally, the Transmit and Receive Timeslot Register allows the data for each channel to be offset within a frame by 8 bit increments or timeslots.

Microprocessor Interface (MPI)

The Le78D11 VoSLAC device Microprocessor Interface (MPI) is used in conjunction with PCM operation. It is a simple synchronous serial interface. It consists of six signals: reset ($\overline{RST}$), serial data in (DIN), serial data out (DOUT), data clock (DCLK), a chip select ($\overline{CS}$) and an Interrupt ($\overline{INT}$). The serial input consists of 8-bit commands sent by the external controller to the Le78D11 VoSLAC device that can be followed with additional bytes of input data or can be followed by the Le78D11 VoSLAC device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bits are shifted in/out with respect to the DCLK while $\overline{CS}$ is Low. The MPI will not accept a command or data byte of less than 8 bits; if more than 8 bits are

sent while $\overline{CS}$ is Low, only the last 8 bits will be interpreted as the command or data byte when CS makes a transition to the High state. DCLK may be stopped in the High or Low state indefinitely without loss of information, but CS must only go high when DCLK is High. All data bytes are read or written one at a time, with $\overline{CS}$ going High for at least the minimum off period before the next byte can be read or written.

The Le78D11 VoSLAC device is designed such that a single $\overline{CS}$ can be used to interface several Le78D11 VoSLAC devices to the system controller. This is accomplished by daisy chaining several devices together. (Refer to the *Le77D11/Le78D11 Chip Set User's Guide*, document ID# 080716, for more information.)

The Le78D11 VoSLAC device can also be used with micro controllers that do not have separate DIN and DOUT pins, but only contain a single bidirectional serial data pin. This is accomplished by connecting the DOUT and DIN pins of the Le78D11 VoSLAC device together and tying them to the bidirectional DIO pin of the micro controller.

The Le78D11 VoSLAC device allows writing filter coefficient parameters to only one channel, thereby programming each channel separately. When writing filter coefficients or device parameters, only one channel should be enabled in the EC register, thereby programming each channel separately.

General Circuit Interface (GCI) Mode

The Le78D11 VoSLAC device switches between PCM/MPI and GCI modes, depending on the pin assignment of FS/DCL and PCLK/FSC. The Le78D11 VoSLAC device powers-up assuming a PCM interface and therefore assumes PCLK is on the pin labeled PCLK/FSC and Frame Sync is on the pin labeled FS/DCL. While in PCM mode, if forty-eight or more cycles are detected on DCL between two rising edges of FSC, the Le78D11 VoSLAC device enters GCI mode. If at any time while the part is in GCI mode, a valid MPI command sequence appears on the DCLK/ S0 and $\overline{CS}$ pins, the part immediately reverts to PCM/MPI mode. This is detected by counting eight low-to-high transitions of DCLK/S0 with $\overline{CS}$ low.

GCI Channel Assignment

In the channel control block, the 8 kHz FSC pulse identifies the beginning of a frame, and all GCI downstream and upstream channels are referenced to it.

When the GCI mode pin (TSCA/G) is connected to DGND, the Le78D11 VoSLAC device selects standard GCI mode supporting two voice channels per GCI channel. Each device occupies a single GCI channel, and eight devices can be controlled over a single GCI bus. Logic inputs DCLK/S0, DIN/S1 and INT/S2 on the Le78D11 VoSLAC device determine the GCI channel assignment. These pins are normally hard-strapped to the selected channel. Downstream data coming in on the DD pin is extracted from the data stream and sent to the DSP core and control logic for sequential processing while data from the DSP and control circuits is sent out on the upstream DU pin.

When TSCA/G is connected to VCCD, the Le78D11 VoSLAC device selects a special mode of GCI operation where only one voice channel occupies each GCI channel, and the B2 voice channel is not used. When the single bearer channel mode is used, four Le78D11 VoSLAC devices handle the maximum of eight subscribers on the GCI bus. In this case, the S2 pin is ignored and the S1 and S0 pins identify the group of two GCI channels assigned to the Le78D11 VoSLAC device. This mode provides for support of 16 bit linear voice data over the GCI interface.

GCI Bus Format and Command Structure

The GCI bus provides communication for both control and voice data to the Le78D11 VoSLAC device. Each GCI bus consists of eight, four-byte GCI channels that contain voice and control information. Depending on the GCI mode, the Le78D11 VoSLAC device sends one or two complete GCI channels upstream on the DU pin and receives one or two channels from the downstream DD pin every 125 µs.

The four-byte GCI channels contain the following:

- One or Two voice bearer channels
  - For standard GCI mode, B1 and B2 are reserved for voice channels 1 and 2.
  - In single bearer channel mode, B2 is unused except when linear PCM mode is selected. In this case B1 and B2 data bytes are combined.
- One Monitor (M) channel for reading and writing control data and coefficients to the chip set.
- One Signaling and Control (SC) channel containing a 6-bit Command/Indicate (C/I) field for control information and a two bit field with Monitor Receive and Monitor Transmit (MR and MX) bits for handshaking functions. All principal signaling (real time critical) information is carried in the C/I field.

PLL Clock Generator

The PLL clock generator derives the Le78D11 VoSLAC device's internal DSP clock (49.152 MHz) and system clock (16.384 MHz) from a 512 kHz reference input This input can come from a number of sources depending on the device mode of operation.

In the GCI mode, the Le78D11 VoSLAC device automatically detects whether a 2.048 MHz or 4.096 MHz data clock (DCL) is being used and programs the Device Configuration Register 1 accordingly to provide the required reference.

In the PCM/MPI mode, the reference input clock can be derived from either PCLK or MCLK. The clock being supplied must be communicated to the Le78D11 VoSLAC device using the MPI by specifying its source and frequency in Device Configuration

Register 1. If the PCLK or MCLK frequency is not an exact multiple of 512 kHz, the difference must be communicated to the Le78D11 VoSLAC device by programming the Master Clock Correction Register.

If the PCLK frequency falls outside the range of 512 kHz to 8.192 MHz, then the MCLK pin must be selected as the reference input clock. In this case MCLK must still be synchronous to PCLK/FSC.

SLIC Device Interface (SLI)

The SLIC Interface logic block controls the state of each Le77D11 device channel through the $C3_i$, $C2_i$, and $C1_i$ control pins. The SLIC state presented on these pins is decoded from the programmed VoSLAC device state. In the PCM/MPI mode, the VoSLAC device state is controlled by using the “Write VoSLAC Channel State” command, and by the downstream C/I field in GCI mode.

The SLIC device loop current limit is controlled by the voltage output on the VDC pin. The VDC output can be programmed to one of seven different levels using the “Write VoSLAC Channel State” command, providing a wide range of loop current settings.

Finally, the chopper clock output (CHCLK) can be programmed to either 85.3 or 256kHz operation, with a 10% high duty cycle. (applicable to the Le77D21 device only)

Table 1. Device Operating States

C3	C2	C1	Le77D11 Device Operating Mode	Le77D21 Device Operating Mode	Description
0	0	0	Low Power Standby	Low Power Standby	Voice transmission disabled. Maximum loop current capability and loop current sensing range are reduced.
0	0	1	Disconnect	Disconnect	SLIC channel is shut down and presents a high impedance to the line. Switching power supply is shut off.
0	1	0	Normal Active	Normal Active	SLIC channel fully operational. A (TIP) is more positive than B(RING). Also used for on-hook transmission.
0	1	1	Reverse Polarity	Reverse Polarity	Similar to normal active, but DC polarity is reversed so that the B(Ring) lead is more positive than the A (TIP) lead. Also used for on-hook transmission.
1	0	0	Ringing	Ringing	Ringing state with V_{AB} set to $K_R \bullet V_{IN}$. The switching supply maintains minimum headroom for the sourcing and sinking amplifiers in order to maximize power efficiency.
1	0	1	Line Test State	Line Test State	Similar to ringing state with reduced bias currents for lower noise. Loop current sensing range is limited. See IMT pin specifications.
1	1	0	Reserved	Active + Test Load	Normal Active with test switch enabled. (applicable to **Le77D21** device only)
1	1	1	Reserved	Ringing + Test Load	Ringing with test switch enabled. (applicable to **Le77D21** device only)

Line Supervision Processing

The loop supervision functions include loop, ring trip, ground key and fault detection. To perform these functions, the Le78D11 VoSLAC device uses the following signals:

- Metallic current (IMT_i*)
  - The Le77D11 device sets IMT_i to 1/500th the loop current. It is converted to a voltage, V_{IMT}, by either an internal or external (programmable) 4.7K resistor placed between the IMT_i pin and VREF. The full scale for the IMT input is 204 µA, which corresponds to a metallic current of 102 mA.
- Logic level fault indication ($\overline{F}_i$)
  - The Le77D11 device’s fault detection outputs, $\overline{F}_1$ and $\overline{F}_2$, are driven low when a longitudinal current fault or foreign voltage occurs.
- Tip (VA_i), Ring (VB_i) and Sense (VS_i) voltages
  - External 475K resistors placed between the voltages being sensed and the VA_i, VB_i and VS_i Le78D11 VoSLAC device inputs allow voltages up to +/-100V to be measured. Then either internal or external (programmable) 4.7K resistors are placed between the VA_i, VB_i and VS_i Le78D11 VoSLAC device inputs and VREF to form voltage dividers.

Note:

** "i" denotes channel number.*

Loop Detection

Loop detection is enabled for all Le78D11 device channel states except Disconnect and Ringing. The Le78D11 VoSLAC device detects an off-hook condition using the Hook Switch current threshold (ITH) variable. Every 500 µs the IMT value coming from the Le77D11 device is compared to ITH. When the result has stayed constant for the duration of the programmed debounce interval, the Hook bit will be set accordingly. The threshold levels and debounce periods are independently programmable.

Ring Trip Detection

Ring trip detection is mutually exclusive to Loop detection. In the ringing state, the Le78D11 VoSLAC device computes the mean square current in the ringing current IMT waveform over one cycle of ringing. The result of this computation is compared to RTSL, a programmable ring trip threshold. The integration period is programmable in 4 ms increments through the ring trip period parameter, RTSLP, which should be chosen to be close to the period of the ringing voltage (i.e. 12 for 20 Hz ringing and 10 for 25 Hz, default is 11 = 44ms).

Using ARR set to Zero, after the Le78D11 VoSLAC device transitions from ringing to ringtrip, the device should next be programmed to enter a non-ringing state.

Thermal Overload

When the die temperature around the two-wire interface of a Le77D11 device channel reaches approximately 165º C, the Le77D11 device pulls the corresponding IMT_i pin above the IMT TEMPA threshold voltage. The Le78D11 VoSLAC device sets the TEMPA bit in the Signaling Register.

DC Fault Detection

Foreign DC voltages can be detected using the VFTD threshold. VFTD is compared against the output of a low pass 5 Hz filter whose input is VA+VB. Whenever the output is greater than VFTD, the DCFAULT bit in the signaling register is set.

B-to-ground faults that produce currents within the range of normal ground key currents cannot be recognized as a fault. However, this type of fault can be recognized as a ground key that persists for an excessively long time.

AC Fault Detection

Low level power crosses can occur that fail to activate any of the external protection devices. In this situation, the chip set must differentiate between unacceptable power cross voltage levels and low level longitudinal levels that do not affect the operation of the Voice over Broadband SLIC/VoSLAC device line card. This is controlled by the AC fault threshold VFTA. VFTA is compared against $|X_i|$, where X_i is the AC portion of $VA_i + VB_i$, which is rectified and averaged over a 44 ms period. Whenever the sum is greater than VFTA, the ACFAULT bit in the signaling register is set.

Loss of Power

When either of the VS_i voltages sensed by the Le78D11 VoSLAC device drops below a programmable threshold, TVS, the Le78D11 VoSLAC device signals this condition by setting the appropriate VS_i bits in the Global Device Status register. The polarity of the voltage is inverted: negative VS voltages will read back as positive values. When setting the sense threshold using the “Write Loop Supervision Parameter" command, a positive value should be used when monitoring negative voltages.

Clock Failure Alarm (CFAIL)

The internal 16.384 MHz system clock produced by the PLL is validated by comparing it with the frame sync signal which is assumed to be always toggling at an 8 kHz rate. The number of 16.384 MHz system clocks that occur between the rising edges of the frame sync signal are constantly monitored and if the number of system clocks exceed 2052 or fall below 2044, the Le78D11 VoSLAC device indicates this condition by setting the CFAIL bit located in the Global Device Status Register. During the time CFAIL is set, the Le78D11 VoSLAC device digital signal processor is halted, preventing processing errors due to an inaccurate system clock.

Voice Signal Processing

The principle function of the Le78D11 VoSLAC device is to handle the analog-to-digital and digital-to-analog conversions, along with the compression and expansion functions in order to interface the analog voice signal to the digital backplane. The Le78D11 VoSLAC device may be programmed to perform A-law or µ-law companding, ADPCM compression, or 16-bit linear two's complement conversion.

In addition, the Le78D11 VoSLAC device has a number of digital filters that provide gain adjustments, distortion correction and equalization, 2-wire impedance matching, and 4-wire echo cancellation. Coefficient generation software (WinSLAC™) is available for optimizing the programmable filters in order to satisfy the system transmission requirements of multiple markets. From the Le78D11 VoSLAC device's point of view, the signal path from the digital-to-analog side is the receive path, while the analog-to-digital direction is the transmit path.

Codec Function

The companding type (A-law/µ-law/ADPCM) is software programmable and may be disabled to send the 16-bit linear two's complement sequence directly to the backplane. When ADPCM at 32 kbps or 24 kbps (as defined in ITU recommendation G.726.

ADPCM) is selected, data is output in the normal 8-bit PCM time slot. The data is output in the most significant bits of the time slot, and the unused bits (the 4 LSBs for 32 kbps, the 5 LSBs for 24 kbps) are filled with zeroes.

Two-Wire Impedance Matching

Two programmable digital feedback paths are provided in the Le78D11 VoSLAC device that allow some components of the transmit signal (V_{IN}) back into the receive path (V_{OUT}) in order to modify the effective two-wire input impedance of the Le77D11 device. The objective is to program each of these feedback paths to create an impedance match at tip and ring in order to minimize two-wire echo.

Frequency Response Correction and Equalization

The Le78D11 VoSLAC device contains digital, programmable filters in both the receive and transmit directions that can be programmed for line equalization or correction of any attenuation distortion introduced by input impedance matching.

4-Wire Echo Cancellation

A digital, programmable balance filter is used to cancel 4-wire echo by summing a filtered version of the receive signal into the transmit path. The purpose of the this filter is to replicate an inverted echo signal so that the actual echo will be eliminated from the transmit path. In the Le78D11 VoSLAC device, this filter has a single tap IIR component and 13 taps for the FIR portion, with a sampling rate of 16 kHz. The Le78D11 VoSLAC device may be programmed with static filter coefficients based on expected line conditions. It may also be placed in adaptive balance mode, in which case the DSP uses an adaptive algorithm to modify the filter coefficients in order to minimize the 4-wire echo. The Le78D11 VoSLAC device decides when to update the filter coefficients and when to stop adaptation based on user programmable control parameters.

Gain Adjustments

The Le78D11 VoSLAC device has programmable gain blocks in both receive and transmit paths.

The transmit path has two programmable gain blocks. The AX gain block is immediately before the A/D converter (ADC) and gives a gain of 0 dB or +6.02 dB. The digital GX block is designed to provide a gain from 0 to +12dB with better than 0.1db step size. Other gains up to a maximum of 15.6dB may be programmed, including the ability to cut-off the transmit signal.

The receive path has two programmable loss blocks. The AR analog gain occurs immediately after the D/A converter (DAC) and may be programmed to be 0 dB or –6 dB. The digital GR block is designed to provide from 0 to –12dB of loss with better than 0.1dB step size. Additional loss may be programmed, including the ability to cut-off the receive path.

Tone Detection and Signal Generation

Dual Tone Multi-Frequency (DTMF) Detection

DTMF allows signaling using voice frequency signals. This function is typically used for telephone keypad tone dialing. The Le78D11 VoSLAC device decodes the dual tone signals into a 4-bit number and puts it into the signaling register with indication that a new digit has been detected.

Modem/Fax Tone Detection

When the relative power in the frequency band of 2100 ± 20 Hz or 1100 ± 38 Hz is greater than 6 dB with respect to the power outside the band, then a modem/fax tone is detected. There are modem/fax tone detectors in both the receive and transmit paths of the Le78D11 VoSLAC device. If either tone detector determines that a modem/fax tone is present, the TONE bit transitions from 0 to 1 and an interrupt may be generated. The DTMF3:DTMF0 bits in the signaling register indicate which tone was detected (0011 = 1100 Hz, 0001 = 2100 Hz). Once a modem/fax tone is detected, the TONE bit remains high until the HOOK bit transitions from 1 to 0. The detection of an on hook transition automatically resets the TONE bit to 0.

Signal Generation

The Le78D11 VoSLAC device has three tone generators available per channel for general call progress tone generation and test signal generation. In addition, the following special purpose tone generation functions are available.

Ringing Generation

The Voice Access chip set can generate and output a ringing signal without the need for an external ringing generator and ring relay. Both trapezoidal and sine wave ringing signals can be generated from the Le78D11 signal generator A. The ringing frequency, amplitude, DC offset, and crest factor for trapezoidal waveforms are programmable. Internal ringing is always initiated synchronous to the line voltage V_{AB}, and may be terminated after a ring trip detection, either immediately (ZXR = 1), or at the zero crossing (ZXR = 0).

DTMF Generation

DTMF generation can be accomplished easily with command 66h/67h Write/Read Signal Generator B Control. This command automatically programs Signal Generator B with one of the 16 standard DTMF tones.

FSK Generation

The Le78D11 VoSLAC device has the ability to generate phase continuous FSK tones at a 1200 baud rate. These tones can be used for a variety of purposes such as Calling Number Delivery (CND), better known as Caller ID, and Visual Message Waiting

Indication (VMWI). It allows the called Customer Premises Equipment (CPE) to receive a calling party's name and directory number along with the date and time of the call.

There are a number of protocols defined, which the chip set can support. In one case the information is sent between the first and second ring bursts, starting as early as 500 ms after the first ring, and ending at least 200 ms before the second ring burst. The information is sent using analog, phase coherent FSK at a 1200 bps rate. The Le78D11 VoSLAC device is designed to provide this feature and can be programmed to initiate or terminate the Caller ID stream as required.

Teletax Generation

Teletax signals send call charge information to the subscriber equipment. These signals are normally sent during the Active Normal mode. The Le78D11 VoSLAC device supports teletax through metering tone bursts which are summed into the receive path DAC and output on VOUT. The 12 or 16 kHz metering burst ramps up over 20ms to the metering target level, MVO, when the teletax state is selected, and ramps back down when the active state is selected. MVO is specified as the peak value of the metering voltage (0 to 1020 mV) at the VOUT pin. If the ABRUPT bit is set, the 12 or 16 kHz signal ramps up or down almost immediately (< 5 ms).

Line Measurement

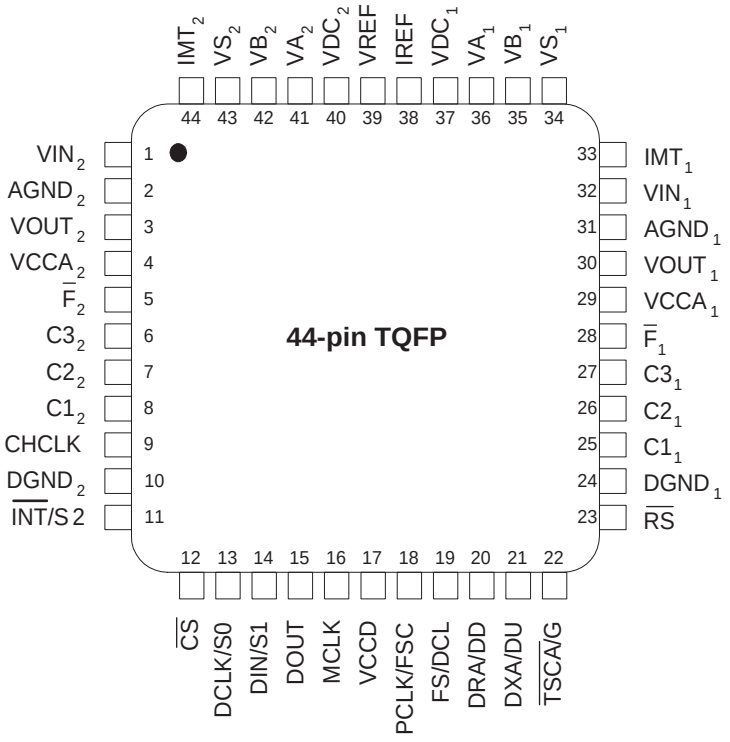
There is one line measurement block per Le78D11 VoSLAC device, which allows measurement of various line and circuit parameters such as leakage resistance, line capacitance, ringer capacitance, receiver off hook, foreign voltage, idle channel noise, echo gain, etc. Most tests are performed in combination with appropriate signal generation. When a line measurement is initiated, the adaptive feature of the echo cancellation filter is frozen for both channels. The line measurement block automatically connects to the enabled channel.

The Le78D11 VoSLAC device returns incorrect Rloop values in Polarity Reversal states. To measure loop resistance in the Polarity Reversal state, the user must read Vab and Vimt, then compute the resistance. Disable Filter 1 and Filter 2 before taking the line measurements on Vimt or Vab inputs (CLM1=001 or CLM1=0110).

Band Gap Voltage Reference

All analog reference voltages are derived from a band gap reference with a very low temperature coefficient. Bias currents are derived from the IREF pin current.

CONNECTION DIAGRAM



Note:

1. Pin 1 is marked for orientation.

PIN DESCRIPTIONS

Pin Name	Type	Description
Power		
$AGND_1$, $AGND_2$		Analog section ground return for each channel
$DGND_1$, $DGND_2$		Digital section ground returns
$VCCA_1$, $VCCA_2$		+3.3 VDC supplies to the analog section in each channel
VCCD		+3.3 VDC supply to all digital sections
PCM Interface		
DRA/DD	Input*	PCM mode, the receive PCM data is input serially through the DRA pin. The data input is received every 125 µs and is shifted in, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. For the GCI mode, downstream receive and control data is accepted on this pin.
DXA/DU	Output*	For the PCM highway, the transmit PCM data is transmitted serially through the DXA pin. The transmission data output is available every 125 µs and is shifted out, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. DXA is high impedance between bursts and while the device is in the inactive mode. For the GCI mode, upstream transmit and signaling data is transferred on this pin.
FS/DCL	Input*	For PCM operation, this pin functions as the Frame Sync input. PCM operation is selected by the presence of an 8 kHz Frame Sync signal on this pin in conjunction with the PCLK (see below). This 8 kHz pulse identifies the beginning of a frame. The Le78D11 VoSLAC device references individual time slots with respect to this input, which must be synchronized to PCLK. In GCI mode, the rate at which data is shifted into or out of the pin is a derivative of this DCL clock.
MCLK	Input*	For PCM backplane operation, a DSP master clock is connected to this pin. A signal is required only for PCM backplane operation when PCLK is not used as the master clock. MCLK can be a wide variety of frequencies. Upon initialization the MCLK input is disabled, and relevant circuitry is driven by PCLK. The MCLK connection is established under user control. This pin is not used in GCI mode, and should be tied to ground.
PCLK/FSC	Input*	For PCM operation, this pin is the PCM Clock input. PCM operation is selected by the presence of a PCLK signal on this pin in conjunction with the FS on the FS pin (see below). This clock determines the rate at which PCM data is serially shifted into and out of the PCM ports. PCLK must be an integer multiple of the FS frequency. The minimum clock frequency for linear/ companded data plus signaling data is 256 kHz. For GCI operation, this pin functions as Frame Sync. The FSC signal is an 8 kHz pulse that identifies the beginning of a frame. The Le78D11 VoSLAC device references individual time slots with respect to this input, which must be synchronized to DCL.
$\overline{TSCA}$/G	Output (PCM) Input (GCI)*	For PCM backplane operation, $\overline{TSCA}$ is active low when PCM data is output on the DXA pin. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VCCD. When GCI mode is selected, one of two GCI modes may be selected by connecting $\overline{TSCA}$/G to DGND or VCCD.
MPI Interface		
$\overline{CS}$	Input*	For PCM backplane operation, a logic low placed on this pin enables serial data transmission into, or out of, the DIN/DOUT pin. Not used in GCI mode (pin should be pulled high in GCI mode).
DCLK/S0	Input*	Data clock for the MPI control interface. For GCI operation, this pin is device address bit 0.
DIN/S1	Input*	For PCM backplane operation, control data is serially written into the Le78D11 VoSLAC device via the DIN pin with the MSB first. The data clock (DCLK) determines the data rate. This pin may also be tied to DOUT, on systems using a single bi-directional data line (Bit 7 in register DCR2 must be low when DIN is tied to DOUT). For GCI operation, this pin is device address bit 1.
DOUT	Output*	For PCM backplane operation, control data is serially read out of the Le78D11 VoSLAC device via the DOUT pin with the MSB first. The data clock (DCLK) determines the data rate. This pin may also be tied to DIN, on systems using a single bi-directional data line (Bit 7 in register DCR2 must be low when DIN is tied to DOUT). This pin is not used in GCI mode, and must remain unconnected.
$\overline{INT}$/S2	Output (PCM) Input (GCI)*	For PCM operation, when a subscriber line requires service, this pin goes to a logic 0 to interrupt a higher level processor. Several registers work together to control operation of the interrupt: Signaling and Global Interrupt Registers with their associated Mask Registers, and the Interrupt Register. See the description at configuration register 6 (Mask) for operation. Logic drive is selectable between open drain and TTL-compatible outputs. In GCI mode, this pin functions as device address bit 2.
$\overline{RS}$	Input*	Active low reset for the Le78D11 VoSLAC device.

Pin Name	Type	Description
Line State Control		
$C1_1$, $C2_1$, $C3_1$ $C1_2$, $C2_2$, $C3_2$	Output	Per channel outputs which control the Le77D11 device line states.
VDC_1, VDC_2	Output	Sets a programmable current limit threshold for the DC feed in the Le77D11 device. Connects to the corresponding RDC1 and RDC2 pins of the Le77D11 device through the R_{DCi} resistors.
$\overline{F}_1$, $\overline{F}_2$	Input*	Fault detect pin for channels 1 and 2. A low indicates a fault for the respective channel, which can be triggered by large longitudinal voltages or ground key.
CHCLK	Output	Software programmable 256 or 85.3 kHz clock for the switching regulator in the Le77D11 device (applicable to the Le77D11 device only).
Line Supervision Processing Inputs		
IMT_1, IMT_2	Input	Connects to the IMTi leads of the Le77D11 device. $I_{IMT} = I_{LOOP} \bullet K_{DC}$
VA_1, VA_2, VB_1, VB_2	Input	Connects to the A_I and B_I leads of the Le77D11 through a 475 kΩ resistor.
VS_1, VS_2	Input	General purpose voltage sense inputs of the Le77D11 devices can connect to high voltage supplies through a 475 kΩ resistor.
Voice Data		
VIN_1, VIN_2	Input	These pins are the inputs for the analog transmit signals (VOUTi) from the Le77D11 device. The Le78D11 VoSLAC device converts these signals to digital words and processes them. After processing, they are multiplexed into serial time slots and sent out of the DXA pin.
$VOUT_1$, $VOUT_2$	Output	The Le78D11 VoSLAC device extracts and processes voice data from time slots on DRA serial data port. After processing, the Le78D11 VoSLAC device converts the voice data to analog signals and outputs it at these pins to the Le77D11 device.
Band Gap Voltage Reference		
IREF	Input	A 69.8 k external resistor (R_{REF}) connected between this pin and analog ground generates an accurate, on-chip reference current for the A/D's and D/A's on the Le78D11 chip.
VREF	Output	This pin provides a 1.4 V, single ended reference to the Le77D11 device to which the Le78D11 VoSLAC device is connected.

Note:

** 5 V tolerant pin.*

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods can affect device reliability.

Storage Temperature	–60ºC < T_A < +125ºC
Ambient Temperature, under Bias	-40ºC ≤ T_A ≤ + 85ºC
Ambient relative humidity (non condensing)	5 to 95%
V_{CCA} with respect to DGND	–0.4 to + 4.0 V
V_{CCA} with respect to V_{CCD}	–0.4 to + 0.4 V
V_{CCD} with respect to DGND	–0.4 to + 4.0 V
AGND with respect to DGND	±50 mV
5 V tolerant digital pins with respect to DGND	–0.4 to 5.5V or V_{CCD} + 2.37 V, whichever is smaller
Any other pin with respect to DGND	–0.4 to V_{CCD} +0.4 V
Latch up immunity (any pin)	±100 mA

Package Assembly

The standard (non-green) package devices are assembled with industry-standard mold compounds, and the leads possess a tin/lead (Sn/Pb) plating. These packages are compatible with conventional SnPb eutectic solder board assembly processes. The peak soldering temperature should not exceed 225°C during printed circuit board assembly.

The green package devices are assembled with enhanced environmental compatible lead (Pb), halogen, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Zarlink guarantees the performance of this device over commercial (0° to 70°C) and industrial (–40° to 85°C) temperature ranges by conducting electrical characterization over each range, and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	-40ºC ≤ T_A ≤ + 85ºC
Ambient Relative Humidity	15 to 85%

Electrical Maximum Ranges

Analog Supply V_{CCA}	+3.3 V ± 5% V_{CCD} ± 50mV
Digital Supply V_{CCD}	+3.3 V ± 5%
DGND	0 V
AGND	±10 mV
5V Tolerant Digital Pins	DGND to +5.25V

ELECTRICAL CHARACTERISTICS

Power Dissipation

Description	Test Conditions	Min	Typ	Max	Unit
Le78D11 VoSLAC device Power Dissipation	Two channels Standby		100	120	mW
	One channel Active, one channel Standby		140	160	
	Two channels Active		180	210	

SPECIFICATIONS

System Specifications

The performance targets defined in this section are for a system using the VE770 series chip set. Specifications for the Le77D11 device are published separately.

No	Item	Condition	Min	Typ	Max	Unit	Note
1	Peak Ringing Voltage	Ringing mode, R_L = 1500 Ω,		70	90	V	
2	Output Impedance during internal ringing	Ringing mode, Le78D11 VoSLAC device generating internal ringing		200		Ω	
3	Sinusoidal Ringing THD	Ringing mode, R_L = 1500 Ω generating internal sinusoidal ringing		2		%	
Signaling Performance Limits							
1	Hook switch threshold	ITH = 10 mA	7		13	mA	
2	Hook switch hysteresis	All ITH settings		10		%	2.
3	Internal Ring Trip Accuracy	RTSL = 2.2 W	–20		+20	%	

Device DC Specifications

Typical values are for TA = 25ºC and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges given in *Operating Ranges* except where noted.

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Digital Input Low Voltage				0.80	V	1.
2	Digital Input High Voltage		2.0				1.
3	Digital Input Leakage Current (except MCLK)	0 < V < V_{CCD}	–15		+15	µA	
		Otherwise	–120		+180		
4	MCLK Digital Input Leakage Current	0 to 5.35 V	–120		+180		
5	Digital Input hysteresis ($\overline{F}_i$, PCLK, FS, MCLK, DIN, DRA)		0.15	0.225	0.3	V	1.
6	Digital Output Low Voltage (all digital pins)	I_{OL} = 1 mA			0.4		
7	Digital Output Low Voltage ($\overline{INT}$, $\overline{TSCA}$)	I_{OL} = 14 mA			0.4		
8	Digital Output High Voltage (All outputs except $\overline{INT}$ in open drain mode and $\overline{TSCA}$)	I_{OH} = 400 µA	V_{CCD} –0.4				
9	Digital Output source impedance	Drive low		400		Ω	
		Drive high		1000			
10	Digital Output leakage current, high impedance state	0 < V < V_{CCD}	–15		+15	µA	
		Otherwise	–120		+180		
11	VIN_i Input voltage range (Relative to V_{REF})	AX = 0 dB		±1.02		Vpk	4.
		AX = 6.02 dB		±0.51			
12	Offset voltage allowed on VIN_i		–50		+50	mV	
13	VIN_i Input Impedance			1.0		MΩ	
14	VIN_i Leakage Current		–10		10	µA	
15	VREF Output voltage	Load current = 0 to 10 mA Source or Sink	1.344	1.4	1.456	V	
16	Output drive current for VREF		10	25		mA	
17	Capacitance load on VREF or $VOUT_i$		0		200	pF	1.
18	$VOUT_i$ Output Voltage range (Relative to V_{REF})	AR = 0 dB		±1.02		Vpk	4.
		AR = -6.02 dB		±0.51			

No.	Item	Condition	Min	Typ	Max	Unit	Note
19	$VOUT_i$ offset Voltage	DISN off	–40		+40	mV	4.
		DISN on	–80		+80		
20	$VOUT_i$ Output leakage current	$0 < V_{OUT} < V_{CCA}$	–10		10	µA	
21	Input Impedance for VA_i, VB_i, and VS_i pins	Internal resistor mode		3490		Ω	
		External resistor mode		1		MΩ	
22	Input impedance for IMT_i pins	Internal resistor mode		3525		Ω	1.
		External resistor mode		1		MΩ	1.
23	Maximum input current for VA_i, VB_i, VS_i and IMT_i pins	Internal resistor mode			950	µA	
24	Input leakage current for VA_i, VB_i, VS_i and IMT_i pins	External resistor mode	–1		+1		
25	IMT TEMPA threshold voltage		2.4	2.65	3.0	V	
26	IMT TEMPA duration		125			µs	2.
27	VDC voltage accuracy	0.2 to 1.4 V	–70		+70	mV	

Transmission Specifications

Table 2. 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

Signal at Digital Interface	Transmit	Receive	Unit
A-law digital mW or equivalent (0 dBm0)	0.5026	0.5026	Vrms
µ-law digital mW or equivalent (0 dBm0)	0.4987	0.4987	
±5,800 peak linear coded sine wave	0.5026	0.5025	

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Gain accuracy, D-A or A-D	0 dBm0, 1014 Hz AR = AX = GR = GX = 0 dB, DISN, R, X, B and Z filters disabled	–0.25	0	+0.25	dB	
	A-D + D-A	Temperature = 70ºC	–0.15	0	+0.15		3.
	A-D + D-A	Variation over temperature	–0.1	0	+0.10		
2	Level set error (Error between setting and actual value)	A-D AX + GX D-A AR + GR	–0.1	0	0.1		
3	GX step size	$0 \leq GX < 12$ dB			0.1		1.
4	GR step size	$-12 \leq GR \leq 0$ dB			0.1		1.
5	DISN gain accuracy	Gdisn = –0.9375 to +0.9375 Vin = 0 dBm0		+0.2			1.
6	DRA to DXA gain in full digital loop back mode	0 dBm0, 1014 Hz AR=AX=GR=GX=0 dB, DISN, R, X, B and Z filters disabled	–0.3		+0.3		
7	Single frequency distortion	0 dBm0, 1014 Hz			-46		
8	Second harmonic distortion	0 dBm0, 1014 Hz TX RX			 -46 -55		
9	Idle Channel Noise, $VOUT_i$	Digital input = 0 A-Law			-78	dBm0p	5.
		Digital input = 0 µ-law			12	dBrnC0	
10	Idle Channel Noise, DXA	V_{INi} = 0 VAC A-Law			-69	dBm0p	
		V_{INi} = 0 VAC µ-law			16	dBrnC0	
11	Coder Offset decision value, Xn	A-D, Input signal = 0V	–7		+7	Bits	
12	PSRR (V_{CC}) Image frequency	Input: 4.8 to 7.8 kHz, 200 mV p-p Measure 8000 Hz-Input frequency A-D	 37	 55		dB	1.
		D-A	37	55			

No.	Item	Condition	Min	Typ	Max	Unit	Note
13	Crosstalk TX to RX same channel RX to TX	0 dBm0 300 Hz to 3400 Hz 0 dBm0 300 Hz to 3400 Hz			–75 –75	dBm0	
14	Crosstalk TX/RX to TX Between channels TX/RX to RX	0 dBm0 300 Hz to 3400 Hz 0 dBm0 300 Hz to 3400 Hz			–76 –78	dBm0	
15	End-to-end group delay	B = Z = 0; X = R = 1			525	µS	2., 6.
16	Maximum metering voltage	12.0 kHz or 16.0 kHz AR = 0 dB		±1.02		Vpk	4.
17	Metering voltage accuracy (MTRA)	12.0 kHz or 16.0 kHz, 0.5 Vpk	–0.7		+0.7	dB	
18	Metering noise	0.5 Vpk (MVO = 3F) from 0 to 80 kHz		–40			2.
19	Metering frequency accuracy (MTRA)	12.0 kHz or 16.0 kHz	–0.1		+0.1	%	2., 7.
20	IMT_i accuracy		–1.5 – 15%		+1.5 + 15%	V	
21	VA, VB and VS accuracy		–2.5– 20%		+2.5 + 20%		

Note:

1. *Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
2. *Guaranteed by design.*
3. *Overall 1.014 kHz insertion loss error of the Voice Access chip set is guaranteed to be ≤ 0.34 dB*
4. *These voltages are referred to V_{REF}*
5. *When relative levels (dBm0) are used, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.*
6. *The group delay specification is defined as the sum of the minimum values of the group delays for the transmit and the receive paths. It is valid only when channels 1 and 2 occupy consecutive time slots in the frame and PCLK frequency is 1.536 Mhz or higher. Programming channels in nonconsecutive time slots or using a PCLK frequency less than 1.536 Mhz may add 1 frame delay in the group delay measurements. See Figure 4 for group delay distortion.*
7. *Accuracy depends on the PCLK's (or MCLK's) accuracy.*

TRANSMIT AND RECEIVE PATHS

In this section, the transmit path is defined from the analog input of the Le78D11 VoSLAC device (VINi) to the DXA/DU PCM voice output of the Le78D11 VoSLAC device A-law/µ-law/linear speech compressor. The receive path is defined from the DRA/DD PCM voice input to the Le78D11 VoSLAC device speech expander to the analog output of the Le78D11 VoSLAC device (VOUTi).

- All limits defined in this section are tested with B = 0, Z = 0 and X = R = 1.
- When AR is enabled, a nominal gain of –6.02 dB is added to the analog section of the receive path.
- When AX is enabled, a nominal gain of +6.02 dB is added to the analog section of the transmit path.
- When relative levels (dBm0) are used in any of the following transmission characteristics, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.
- These transmission characteristics are valid for 0º to 70ºC.

Attenuation Distortion

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 2 and Figure 3. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

Figure 2. Transmit Path Attenuation vs. Frequency

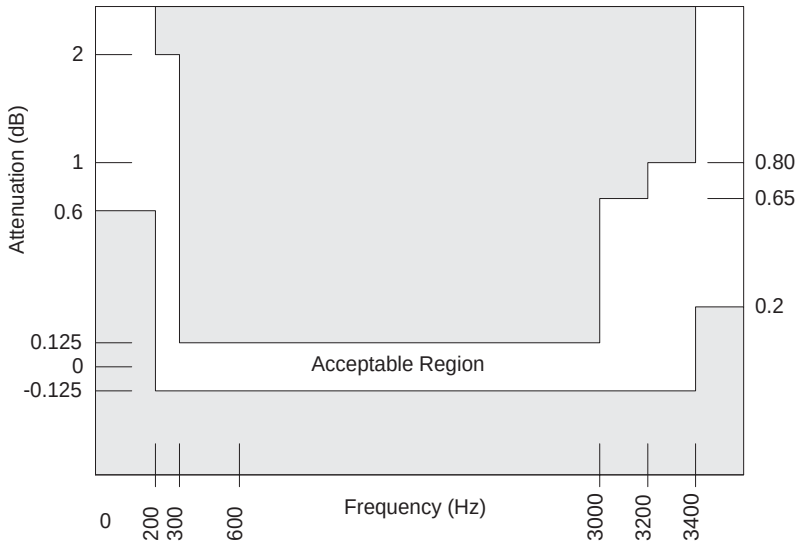
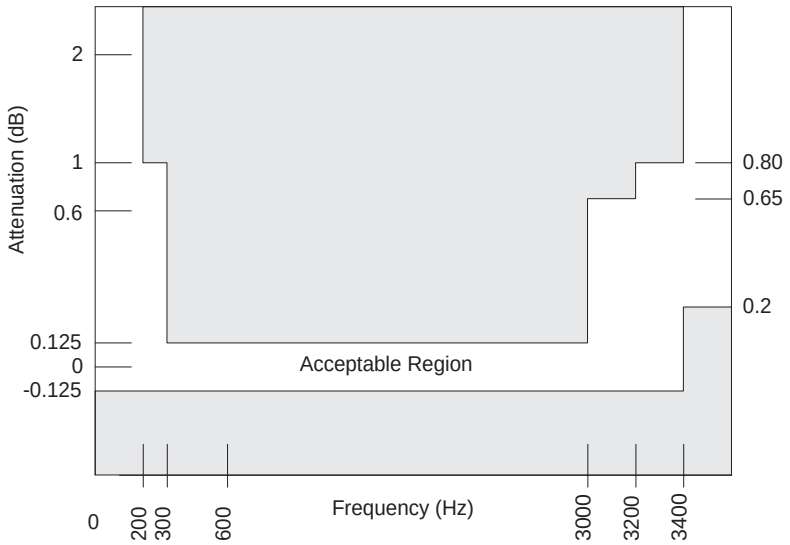


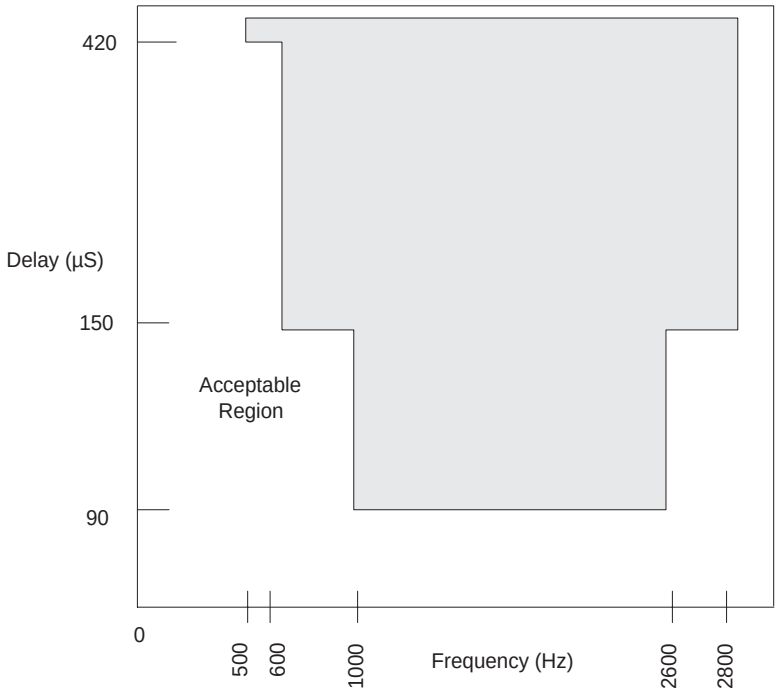
Figure 3. Receive Path Attenuation vs. Frequency



Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 4. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

Figure 4. Group Delay Distortion



Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 5 (A-law) and Figure 6 (µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

Figure 5. A-law Gain Linearity with Tone Input (Both Paths)

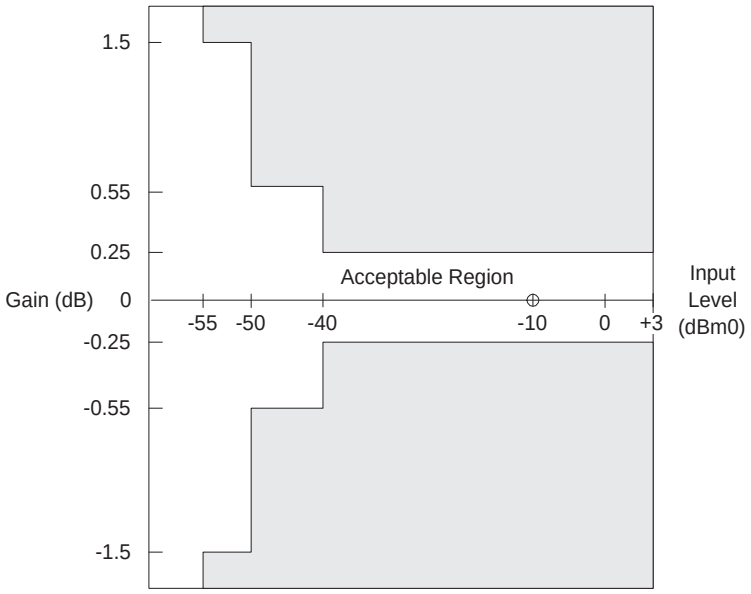
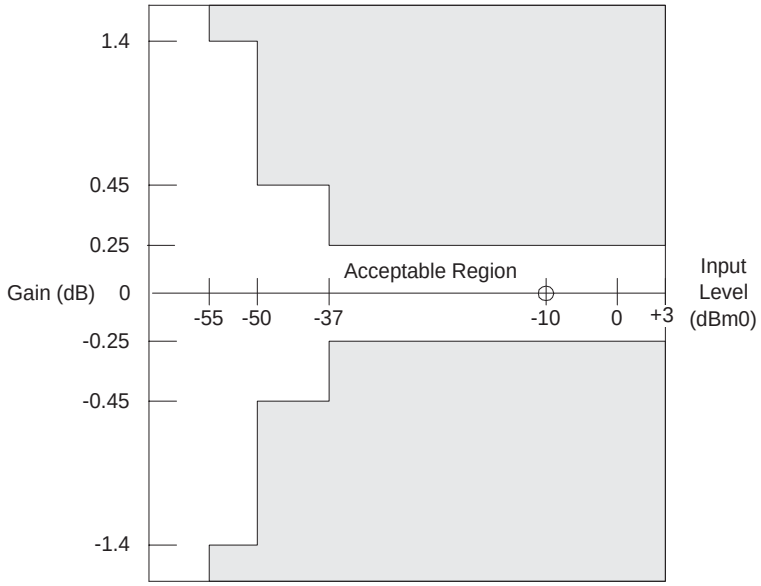


Figure 6. μ-law Gain Linearity with Tone Input (Both Paths)

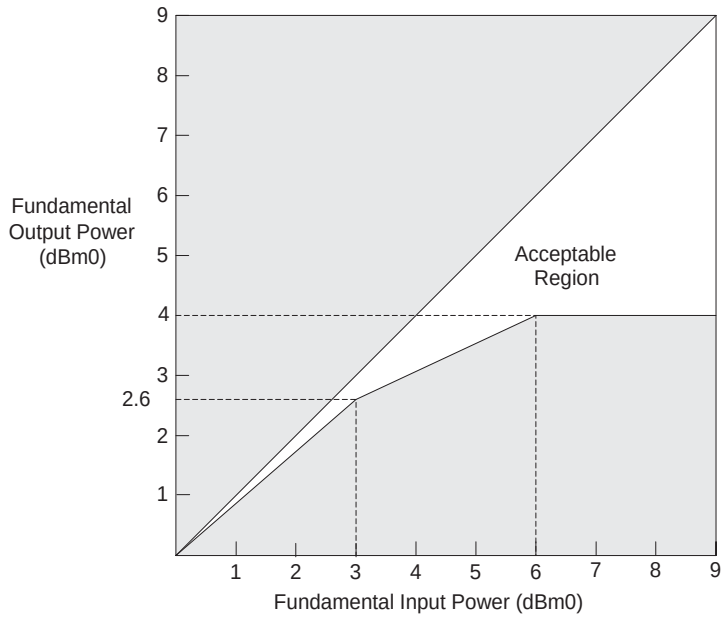


Overload Compression

Figure 7 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. 1 dB < GX ≤ + 12 dB
2. –12 dB ≤ GR < –1 dB
3. Digital voice output connected to digital voice input.
4. Measurement analog to analog.

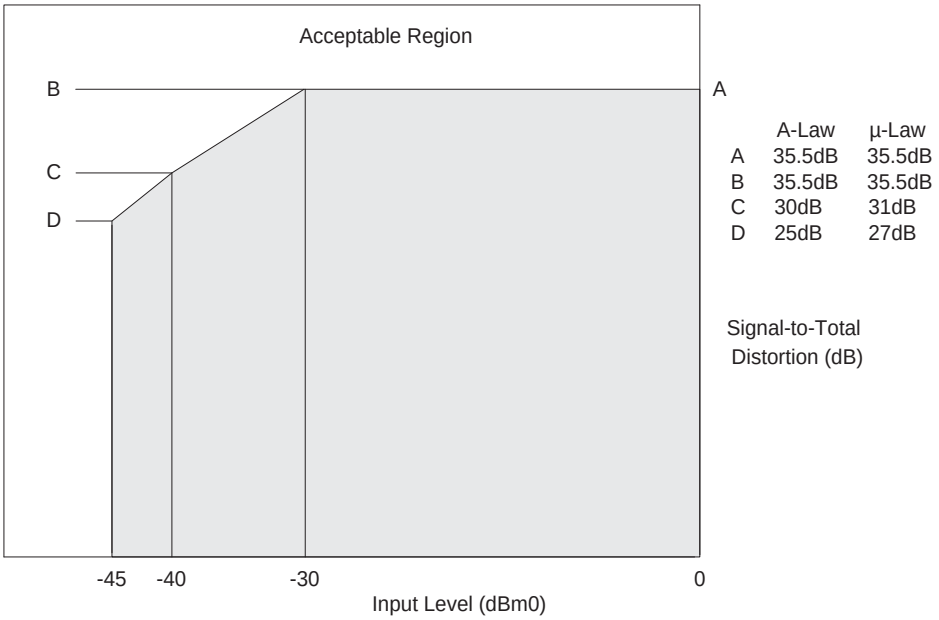
Figure 7. A/A Overload Compression



Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 8 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

Figure 8. Total Distortion with Tone Input (Both Paths)



Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 to 300 Hz and 3.4 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

Intermodulation Distortion

Two sine wave signals of different frequencies (f_1 and f_2, not harmonically selected), ranging from 300 to 3400 Hz, of equal levels between –4 and –21 dBm0, do not produce $2*(f_1 - f_2)$ products greater than –42 dB relative to the level of the two input signals.

A sinusoidal wave in the frequency band from 300 to 3400 Hz with an input level of –9 dBm0 along with a 50 Hz signal with an input level of –23 dBm0, do not produce intermodulation products exceeding –56 dBm0.

The specifications are valid for either transmission path.

Discrimination Against Out-of-Band Input Signals

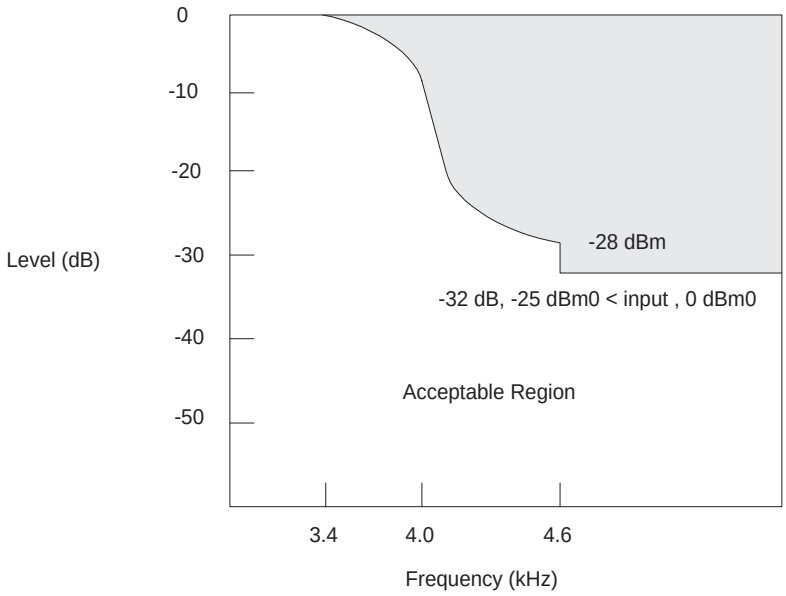
When an out-of-band sine wave signal of frequency f, and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table..

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 9
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB

The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:

$$\text{Attenuation (db)} = 14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)$$

Figure 9. Discrimination Against Out-of-Band Signals



Discrimination Against 12- and 16-kHz Metering Signals

If the Le78D11 VoSLAC device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones also may appear at the VIN terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz or 16 kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the analog input voltage range.

Spurious Out-of-Band Signals at the Analog Output

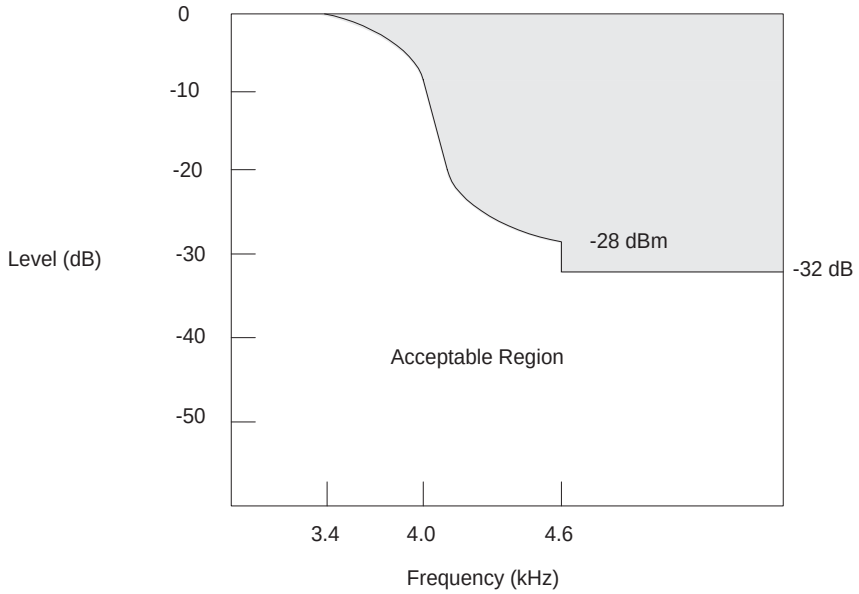
With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 10. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = \left[-14 - 14\sin\left(\frac{\pi(f - 4000)}{1200}\right)\right] \text{dBm0}$$

Figure 10. Spurious Out-of-Band Signals



SWITCHING CHARACTERISTICS

The following are the switching characteristics over operating range (unless otherwise noted). Min and max values are valid for all digital outputs with a 100 pF load, except DOUT, DXA, $\overline{INT}$, and $\overline{TSCA}$ which are valid with 150 pF loads.

Microprocessor Interface

See Figure 11 and Figure 12 for the microprocessor interface timing diagrams.

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	122			ns	
2	t_{DCH}	Data clock HIGH pulse width	48				
3	t_{DCL}	Data clock LOW pulse width	48				
4	t_{DCR}	Rise time of clock			15		
5	t_{DCF}	Fall time of clock			15		
6	t_{ICSS}	Chip select setup time, Input mode	30		t_{DCY}–10		
7	t_{ICSH}	Chip select hold time, Input mode	0		t_{DCH}–20		
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{DCY}$			
9	t_{ICSO}	Chip select off time, Input mode	2000				1.
10	t_{IDS}	Input data setup time	25				
11	t_{IDH}	Input data hold time	30				
12	t_{OLH}	SLIC output valid			300		
13	t_{OCSS}	Chip select setup time, Output mode	30		t_{DCY}–10		
14	t_{OCSH}	Chip select hold time, Output mode	0		t_{DCH}–20		
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{DCY}$			
16	t_{OCSO}	Chip select off time, output Mode	2000				1.
17	t_{ODD}	Output data turn on delay			50		2.
18	t_{ODH}	Output data hold time	3				
19	t_{ODOF}	Output data turn off delay			50		
20	t_{ODC}	Output data valid	0		50		
21	t_{RST}	Reset pulse width	50			µs	

Figure 11. Microprocessor Interface (Input Mode)

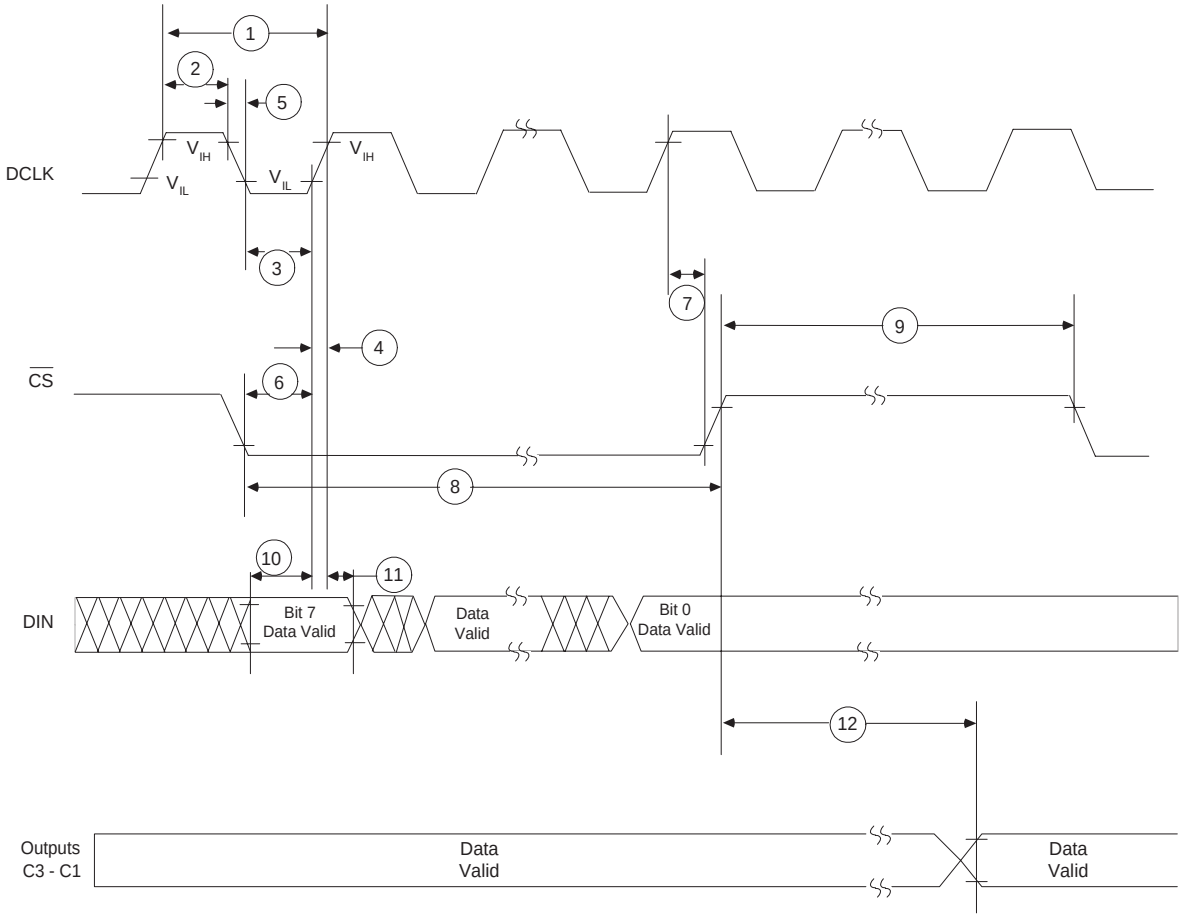
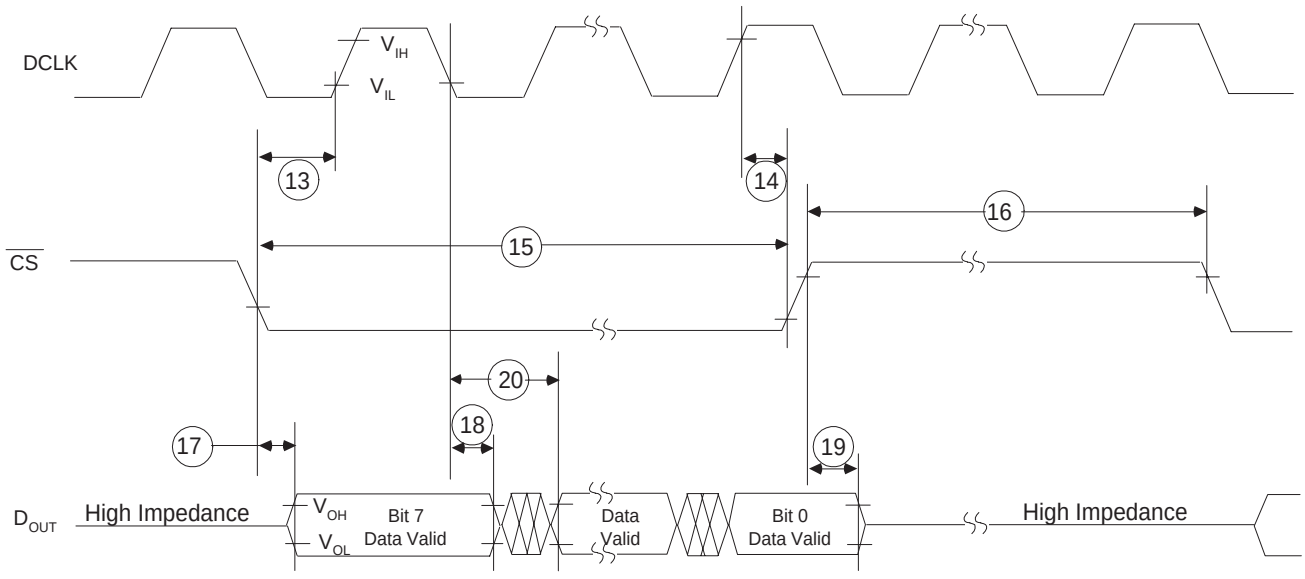


Figure 12. Microprocessor Interface (Output Mode)



PCM Interface

See Figure 13 and Figure 14 for the PCM interface timing diagrams.

A pull up resistor to VCCD of 240 Ω is attached to $\overline{\text{TSCA}}$

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM clock period	0.122		7.8125	µs	3.
23	t_{PCH}	PCM clock HIGH pulse width	48			ns	
24	t_{PCL}	PCM clock LOW pulse width	48				
25	t_{PCF}	Fall time of clock			15		
26	t_{PCR}	Rise time of clock			15		
27	t_{FSS}	FS setup time	30		t_{PCY}–30		
28	t_{FSH}	FS hold time	50				
29	t_{TSD}	Delay to $\overline{\text{TSCA}}$ valid	5		80		4.
30	t_{TSO}	Delay to $\overline{\text{TSCA}}$ off	5				4., 5.
31	t_{DXD}	PCM data output delay	5		70		
32	t_{DXH}	PCM data output hold time	5		70		
33	t_{DXZ}	PCM data output delay to high Z	10		70		
34	t_{DRS}	PCM data input setup time	25				
35	t_{DRH}	PCM data input hold time	5				
36	t_{FST}	PCM or frame sync jitter time	–97		97		

Figure 13. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

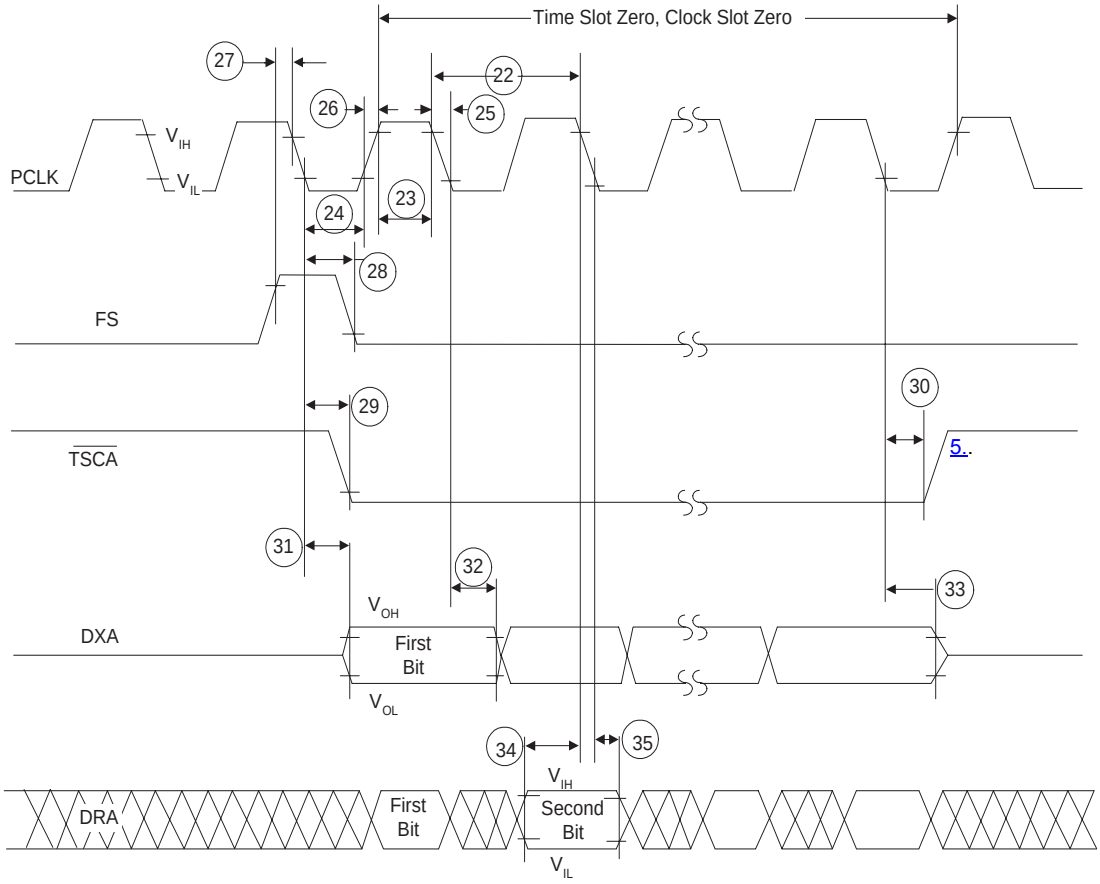
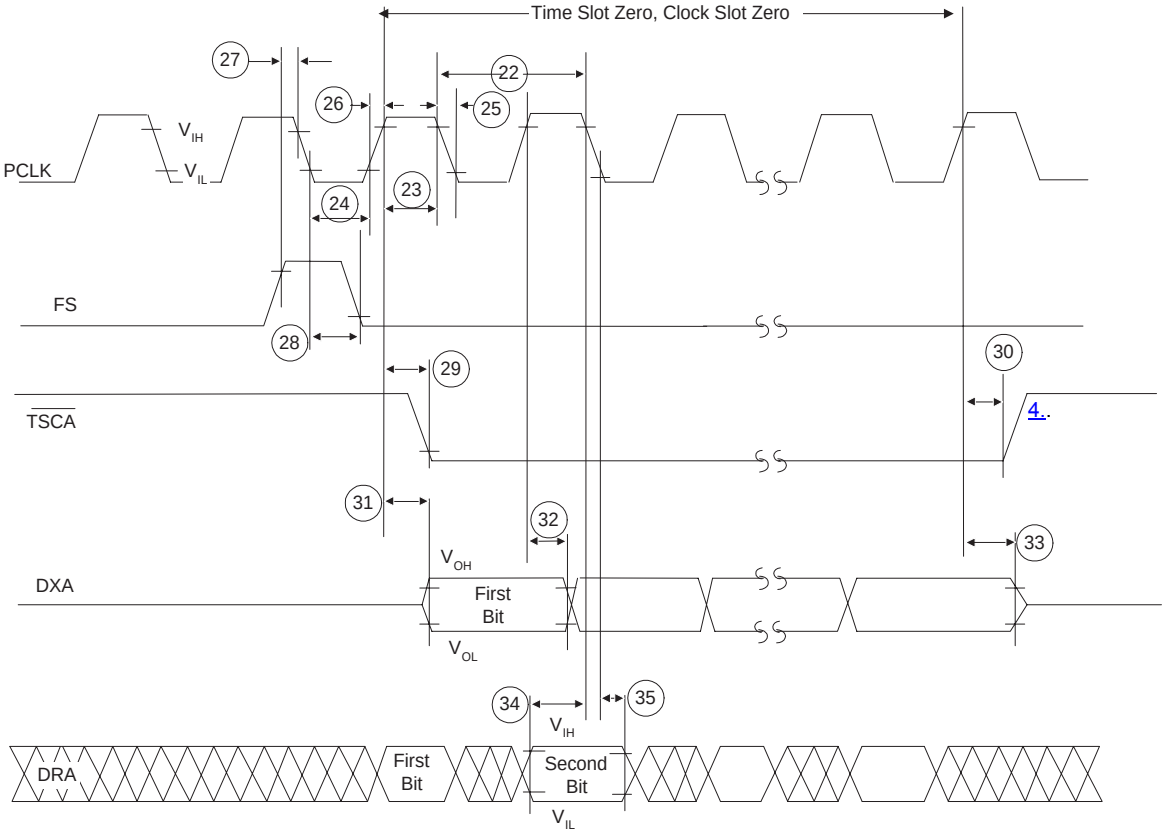


Figure 14. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)



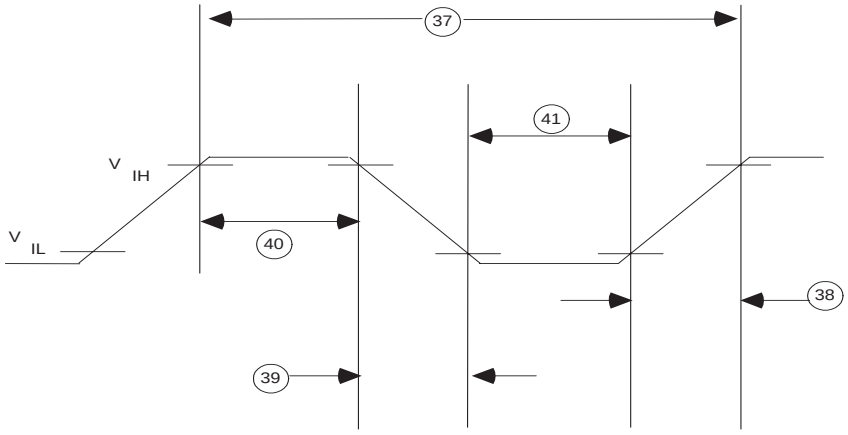
Master Clock

For 2.048 MHz ±100 PPM, 4.096 MHz ±100 PPM, or 8.192 MHz ±100 PPM operation.

See Figure 15 for the Master Clock timing diagram.

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
37	t_{MCY}	Period: 2.048 MHz	488.23	488.28	488.33	ns	6.
		Period: 4.096 MHz	244.11	244.14	244.17		
		Period: 8.192 MHz	122.05	122.07	122.09		
38	t_{MCR}	Rise time of clock			15		
39	t_{MCF}	Fall time of clock			15		
40	t_{MCH}	MCLK HIGH pulse width	48				
41	t_{MCL}	MCLK LOW pulse width	48				

Figure 15. Master Clock Timing

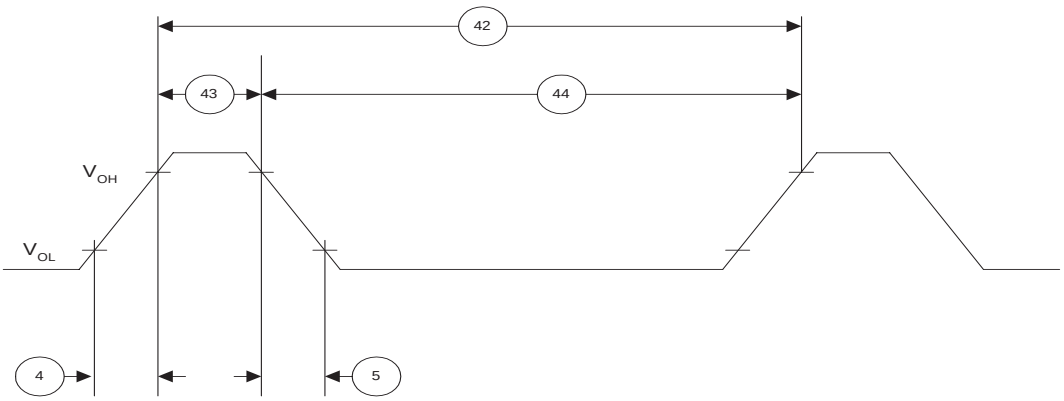


Chopper Clock

See Figure 16 for the Chopper Clock timing diagram.

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
42	t_{CHCLKY}	Chopper Clock Period, CHP = 0 (default)		11.71875		µs	7.
		Chopper Clock Period, CHP = 1		3.90625			
43	t_{CHCLKH}	Chopper clock high time		t_{CHCLKY} • 0.09375			
44	t_{CHCLKL}	Chopper clock low time		t_{CHCLKY} • 0.90625			

Figure 16. Chopper Clock Timing



GCI Interface

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
45	t_R, t_F	Rise/fall time			60	ns	
46	t_{DCL}	Period, F_{DCL} = 2048 kHz	488.23	488.28	488.33		
		F_{DCL} = 4096 kHz	244.11	244.14	244.17		
47	t_{WH}, t_{WL}	Pulse width	90				
48	t_{SF}	Setup time	70		t_{DCL}–50		
49	t_{HF}	Hold time	50				
50	t_{WFH}	High pulse width	130				
51	t_{DDC}	Delay from DCL edge			100		
52	t_{DDF}	Delay from FS edge			150		
53	t_{SD}	Data setup	twH+20				
54	t_{HD}	Data hold	50				

Note:

1. *The Le78D11 VoSLAC device requires 2.0 µs between MPI operations. If the MPI is being accessed while the MCLK (or PCLK if combined with MCLK) input is not active, a Chip Select Off time of 20 µs is required when accessing coefficient RAM.*

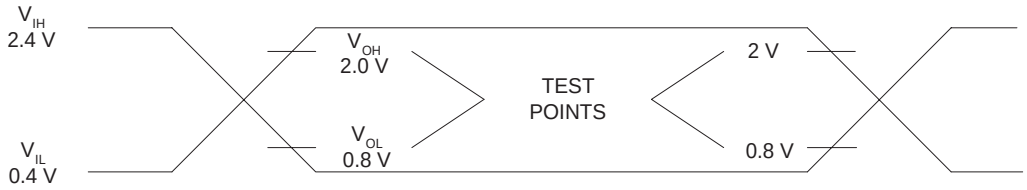
   Immediately after reset, $t_{ICSO} = \frac{2\mu s \cdot 8.192\ MHz}{f_{PCLK}}$ *, where f_{PCLK} is the applied PCLK frequency. Once DCR1 is programmed for the applied PCLK and MCLK, t_{ICSO} is per table specification.*

2. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
3. *The PCM clock (PCLK) frequency must be an integer multiple of the frame sync (FS) frequency and synchronous to the MCLK frequency. The actual PCLK rate is dependent on the number of channels allocated within a frame. A PCLK of 1.544 MHz can be used for standard US transmission systems. The minimum clock frequency is 128 kHz using companded data, and 256kHz using linear data to allow simultaneous access to both channels.*

4. *$\overline{TSCA}$ is delayed from FS by (TTS •8 +TCS) • t_{PCY}, where TTS is the transmit time slot and TCS is the transmit clock slot.*
5. *t_{TSO} is defined as the time at which the output driver turns off. The actual delay time is dependent on the load circuitry. At 8.192 MHz the maximum load capacitance on $\overline{TSCA}$ is 150 pF using the minimum pull-up resistance of 240 Ω.*
6. *PCLK and MCLK are required to be integer multiples of the frame sync (FS) frequency. Frame sync. is expected to be an accurate 8kHz pulse train. If PCLK or MCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*
7. *Chopper clock accuracy is relative to PLL input reference clock accuracy (i.e. PCLK or MCLK).*

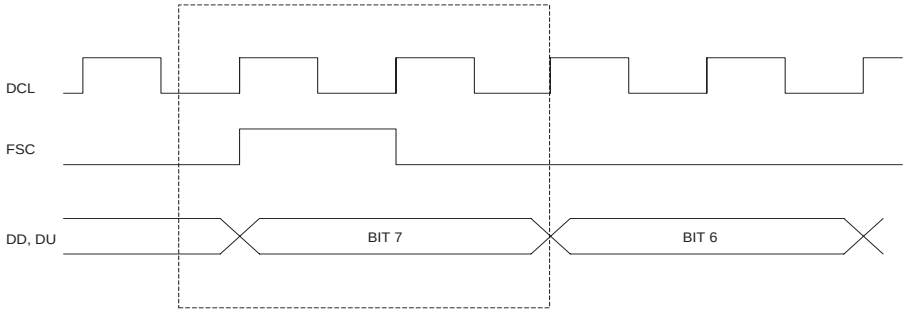
Switching Waveforms

Figure 17. Input and Output Waveforms for AC tests



VCC = 3.3 V +5%, AGND = DGND = 0 V

Figure 18. 4.096 MHz DCL GCI Operation



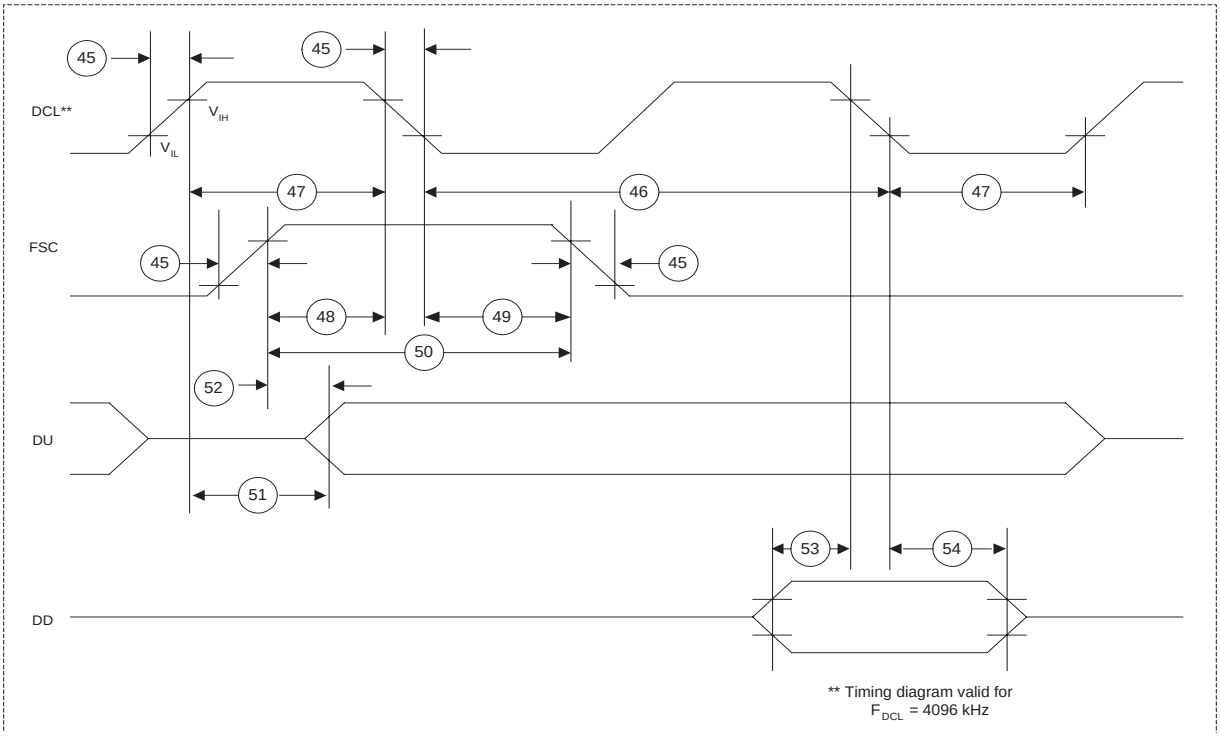
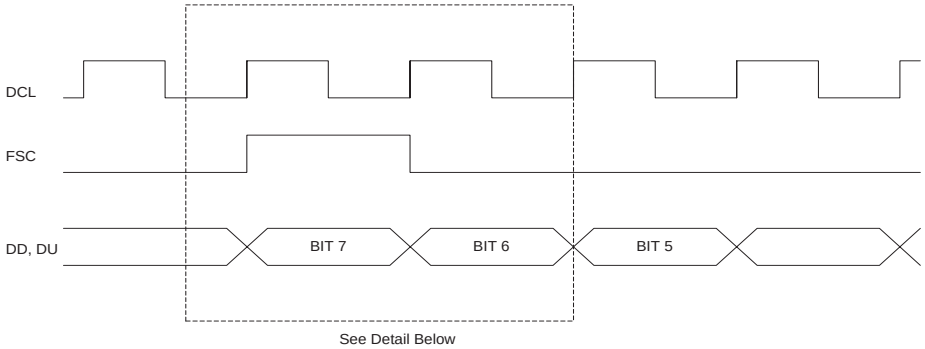
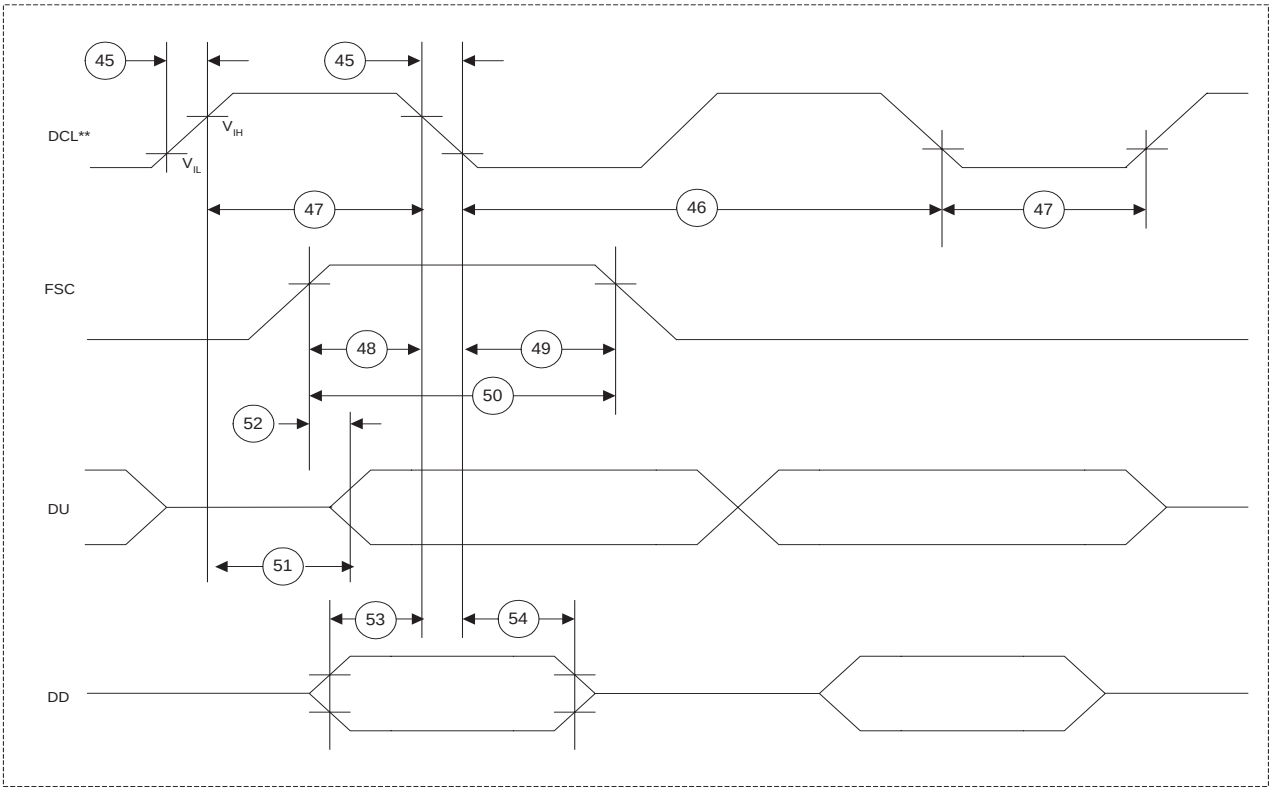
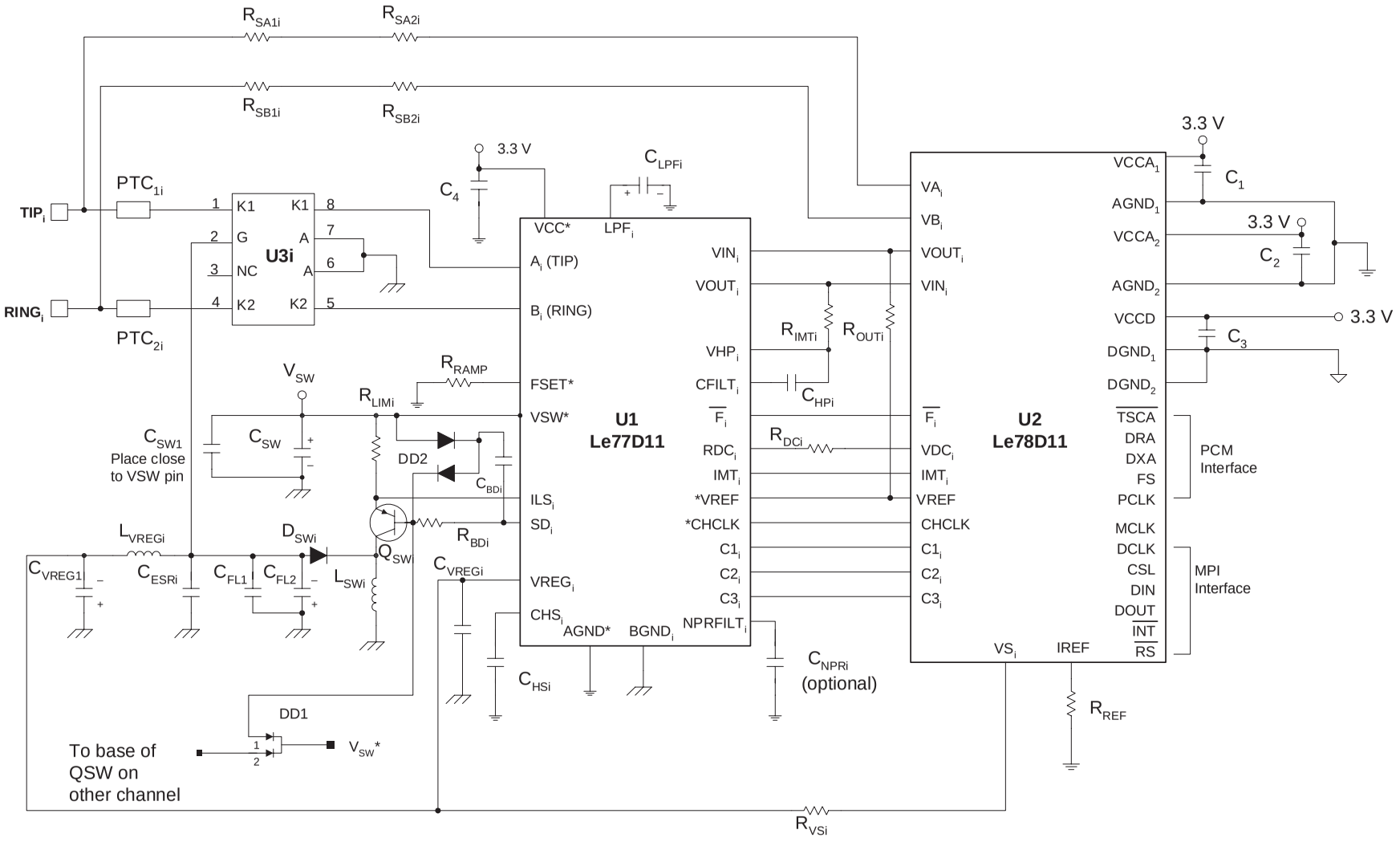


Figure 19. 2.048 MHz DCL GCI Operation





SINGLE CHANNEL APPLICATION CIRCUIT WITH THE LE77D11 DEVICE



Note:

** denotes pins that are common to both channels.*

i = per channel component/pin

Protection is voltage tracking device

APPLICATION CIRCUIT PARTS LIST FOR THE LE77D11 DEVICE

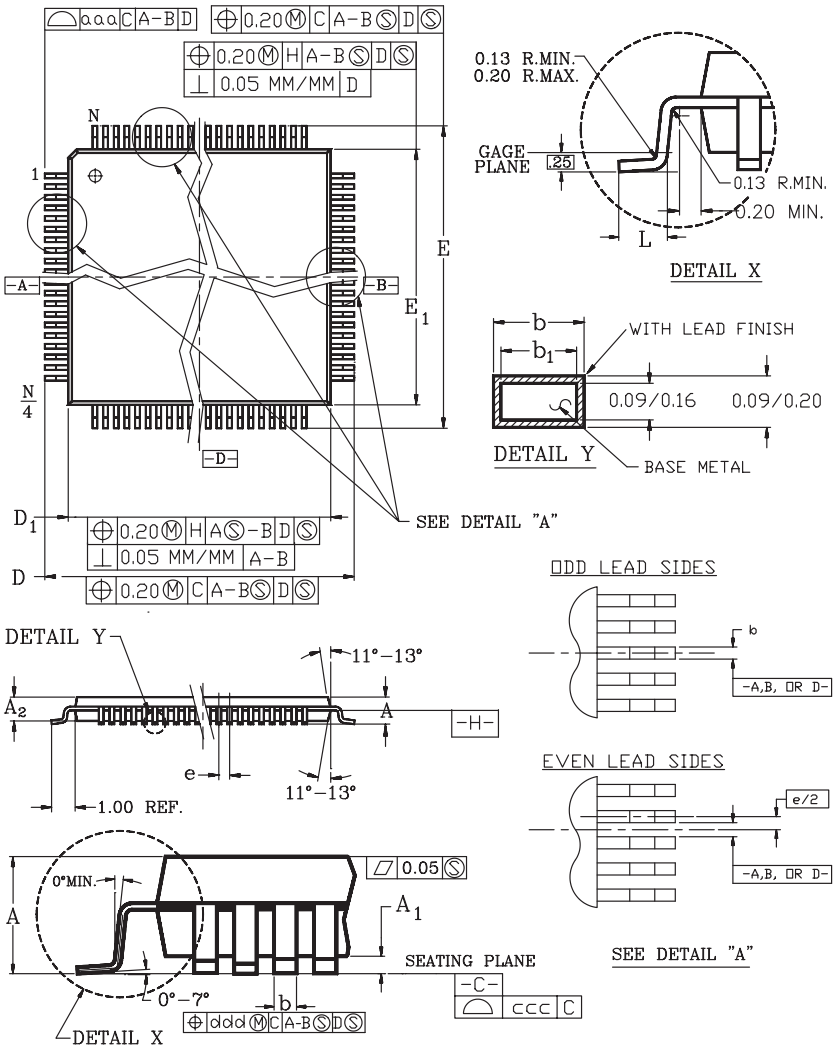
The following list defines the parts and part values for a low cost solution required to meet target specification limits for 70 V_{PK} ringing with V_{SW} = 12 V for two channels of the line card. The protection circuit is not included.

Item	Quantity (see note 1)	Type	Value	Tol.	Rating	Comments	Note
C_{HSi}	2	Capacitor	1 nF	10%	50 V	Panasonic / ECJ-1VB1H102K, 0603	
C_{BDi}	2	Capacitor	27 nF	10%	16 V	Kemet C0603C273K5RAC	
C_1, C_2, C_3, C_4	4	Capacitor	100 nF	10%	16 V	Panasonic / ECJ-1VF1C104Z, 0603	
C_{ESRi}	2	Capacitor	0.1 µF	10%	200 V	CalChip GMC31X7R104K200NT	
C_{NPRi}	2	Capacitor	100 nF	10%	16 V	Panasonic / ECJ-1VB1C104K (optional)	
C_{VREGi}	2	Capacitor	100 nF	10%	200 V	CalChip GMC31X7R104K200NT	
C_{HPi}	2	Capacitor	1.5 µF	10%	6.3 V	Panasonic / ECJ-2YB0J155K,0805	
C_{LPFi}	2	Capacitor	4.7 µF Tantalum	20%	6.3 V	Panasonic ECS-TOJY475R	
C_{FL1}, C_{FL2} C_{VREG1}	6	Capacitor	1.0 µF, ESR < 40 mΩ	10%	200 V	Tecate CMC-300/105KX1825T060	
C_{SW}	1	Capacitor	220 µF Alum. Elect.	20%	25 V	Nichicon / UPW1E221MPH	
C_{SW1}	1	Capacitor	100 nF	10%	50 V	DIGI-KEY / PCC1840CT-ND,0805	
D_{SWi}	2	Diode	ES2C		2 A	General Semi. / ES2C	
DD1	1	Diode	4148-SOT		600 mA	Fairchild / MMBD4148CC	
DD2, DD3	2	Diode	BAV99TA		250 mA	Zetex / BAV99TA (DIGI-KEY # BAV99ZXTR-ND)	
L_{SWi}	2	Inductor	47 µH		2.95 A	Cooper Coiltronics / DR127-470	
L_{VREGi}	2	Inductor	150 µH		205 mA	Coilcraft 1812LS154X_B	
PTC_{1i}, PTC_{2i}	4	PTC	50 Ω		250 V	AsiaCom / MZ2L-50R	
Q_{SWi}	2	PNP Transistor	FZT955		140 V	Zetex / FZT955	
R_{LIMi}	2	Resistor	0.1 Ω,	5%	1/4 W	Panasonic ERJ-14RSJR10U / DIGI-KEY P10SCT-ND	
R_{BDi}	2	Resistor	180 Ω	1%	1/4 W	Panasonic ERJ-6ENF1820V	
R_{DCi}	2	Resistor	20 K	1%	1/16 W	Panasonic / ERJ-3EKF2002V	
R_{REF}	1	Resistor	69.8 K	1%	1/16 W	Panasonic / ERJ-3EKF6982V	
R_{IMTi}	2	Resistor	100 K	1%	1/16 W	Panasonic / ERJ-3EKF1003V	
R_{RAMP}	1	Resistor	280 K	1%	1/16 W	Panasonic / ERJ-3EKF2803V	
R_{VSi}	2	Resistor	475 K	1%	1/16 W	Panasonic / ERJ-3EKF4753V	
R_{SA1i}, R_{SB1i}, R_{SA2i}, R_{SB2i}	8	Resistor	237 k	1%	1/8 W	Panasonic / ERJ-8ENF2373V	
R_{OUTi}	2	Resistor	10 k	1%	1/16 W	Panasonic / ERJ-3KF1002V	
$U3_i$	2	Protector				Bourns / TISP61089BDR	

Note:

1. Quantities required for a complete two-channel solution.

PHYSICAL DIMENSIONS



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
D		12 BSC	
D1		10 BSC	
E		12 BSC	
E1		10 BSC	
L	0.45	0.60	0.75
N		44	
e		0.80 BSC	
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
ccc		0.10	
ddd		0.20	
aaa		0.20	

JEDEC #: MS-026 (C) ACB

Notes:
1. All dimensions and toleerances conform to ANSI Y14.5-1982.
2. Datum plane -H- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.
3. Dimensions “D1” and “E1” do not include mold protrusion. Allowable protrusion is 0.254mm per side. Dimensions “D1” and “E1” include mold mismatch and are determined at Datum plane -H- .
4. Dimension “B” does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the “b” dimension at maximum material condition. Dambar can not be located on the lower radius or the foot.
5. Controlling dimensions: Millimeter.
6. Dimensions “D” and “E” are measured from both innermost and outermost points.
7. Deviation from lead-tip true position shall be within ±0.076mm for pitch >0.5mm and within ±0.04 for pitch ≤0.5mm.
8. Lead coplanarity shall be within: (Refer to 06-500)
   1- 0.10mm for devices with lead pitch of 0.65-0.80mm.
   2- 0.076mm for devices with lead pitch of 0.50mm.
   Coplanarity is measured per specification 06-500.
9. Half span (center of package to lead tip) shall be 15.30 ± 0.165mm {.602”±.0065”}.
10. “N” is the total number of terminals.
11. The top of package is smaller than the bottom of the package by 0.15mm.
12. This outline conforms to Jedec publication 95 registration MS-026
13. The 160 lead is a compliant depopulation of the 176 lead MS-026 variation BGA.

44-Pin TQFP

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision B1 to C1

- In *Power Dissipation*, added Max values
- In *System Specifications*, first paragraph, removed T_A = 0 to 70°C
- In *Transmission Specifications*, Maximum metering voltage, added typ value of ±1.02 V and condition of AR = 0 dB

Revision C1 to D1

- Added OPN for green package in *Ordering Information*, on page 1
- Added *Package Assembly*, on page 13
- Removed all references to VoSLIC-ABS device
- Modified application circuits and parts lists to reflect the 90-V_{PK} ringing application in the VE 770 series
- Added specifications for IMT accuracy and VA, VB, and VS accuracy in *Transmission Specifications*, on page 15
- Updated IMT Tempa Threshold voltage specification in *Device DC Specifications*, on page 14

Revision D1 to D2

- Enhanced format of package drawing in *Physical Dimensions*, on page 31
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

For more information about all Zarlink products visit our Web Site at

www.zarlink.com