

**ORDER NUMBER(S):**

**LAN89303AM (Tray) FOR 56-PIN, QFN, ROHS-COMPLIANT PACKAGE**

**LAN89303AMR (Tape & Reel) FOR 56-PIN, QFN, ROHS-COMPLIANT PACKAGE**

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## General Description

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The LAN89303AM is a full featured, 3 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN89303AM combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers and serial management. The LAN89303AM complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

At the core of the device is the high performance, high efficiency 3 port Ethernet Switch Fabric. The Switch Fabric contains a 3 port VLAN layer 2 Switch Engine that supports untagged, VLAN tagged and priority tagged frames. The Switch Fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32k of buffer RAM allows for the storage of multiple packets while forwarding operations are completed and a 512 entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block within the Switch Fabric. All aspects of the Switch Fabric are managed via the Switch Fabric configuration and status registers, which are indirectly accessible via the system control and status registers.

The LAN89303AM provides 3 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half-duplex 10BASE-T and 100BASE-TX operation. The LAN89303AM provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the third MAC are used to connect the Switch Fabric to an external MAC or PHY. In MAC mode, the device can be connected to an external PHY via the MII/Turbo MII interface. In PHY mode, the device can be connected to an external MAC via the MII/RMII/Turbo MII interface. All ports support automatic or manual full-duplex flow control or half-duplex backpressure (forced collision) flow control. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while decreasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the device.

The integrated I<sup>2</sup>C and SMI slave controllers allow for full serial management of the device via the integrated I<sup>2</sup>C or MII interface, respectively. The inclusion of these interfaces allows for greater flexibility in the incorporation of the device into various designs. It is this flexibility which allows the device to operate in 2 different modes and under various management conditions. In both MAC and PHY modes, the device can be SMI managed or I<sup>2</sup>C managed. This flexibility in management makes the LAN89303AM a candidate for virtually all switch applications.

The LAN89303AM contains an I<sup>2</sup>C master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the device at reset. The I<sup>2</sup>C management slave and master EEPROM controller share common pins.

In addition to the primary functionality described above, the LAN89303AM provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter and 6-bit configurable GPIO/LED interface.

The LAN89303AM's performance, features and small size make it an ideal solution for applications in the automotive market. Targeted applications include interfaces for diagnostics, gateway services, in-vehicle engineering development, manufacturing testing and legislated inspections.

Block Diagram

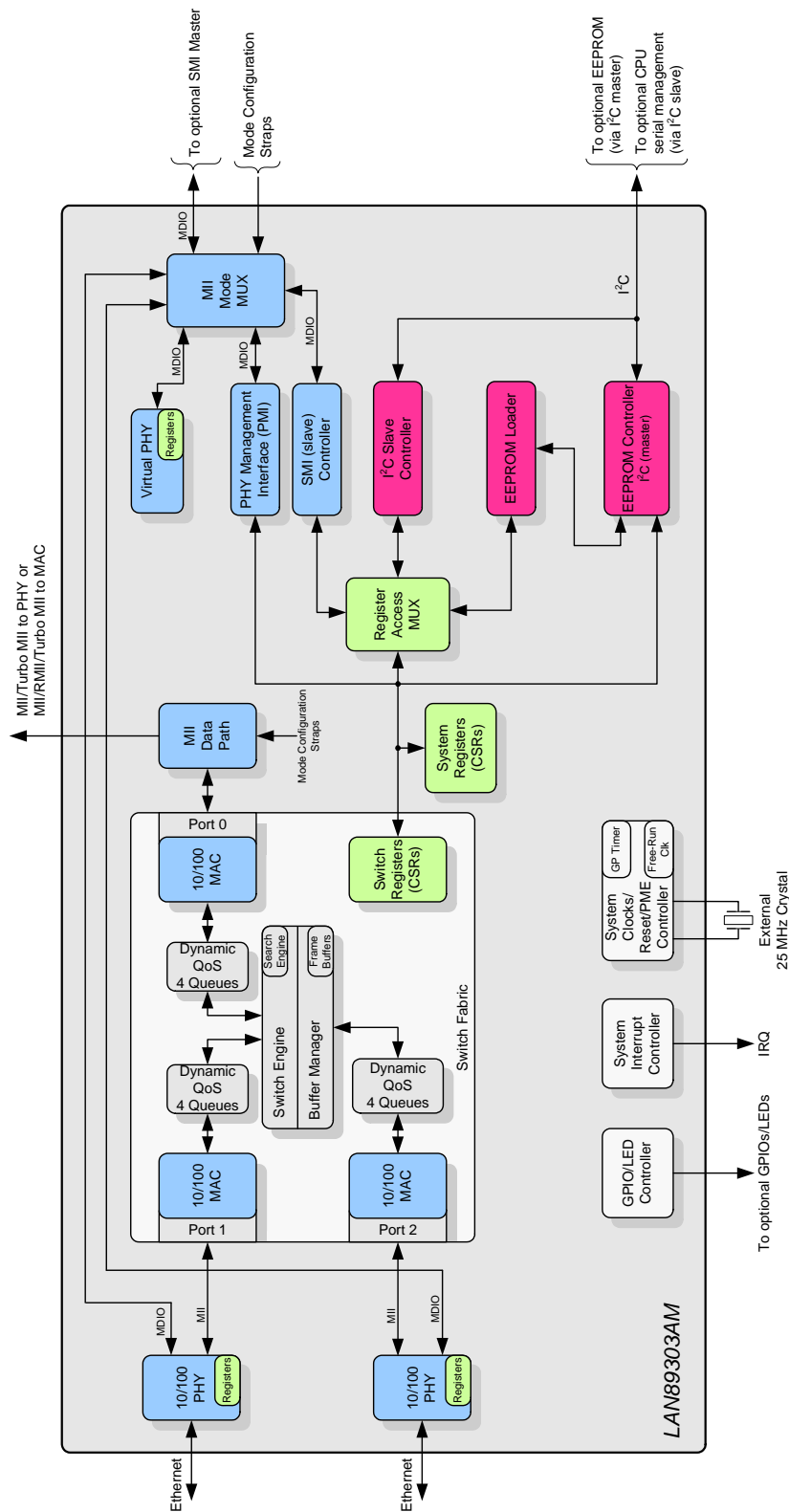
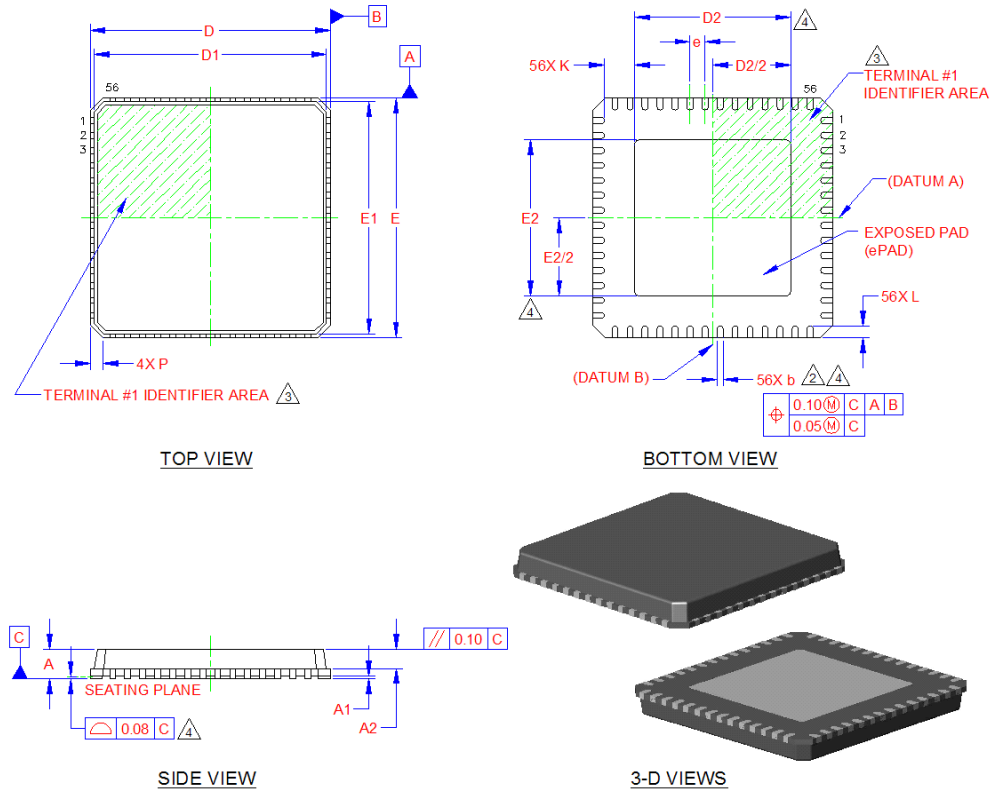


Figure 1 Internal Block Diagram

## Package Outline



**Figure 2 56-QFN Package Definition**

**Table 1 56-QFN Dimensions**

	MIN	NOMINAL	MAX	REMARKS
A	0.80	0.85	0.90	Overall Package Height
A1	0	0.01	0.05	Standoff
A2	0.60	0.65	0.70	Mold Cap Thickness
D/E	7.90	8.00	8.10	X/Y Body Size
D1/E1	7.65	7.75	7.85	X/Y Mold Cap Size
D2/E2	5.10	5.20	5.30	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.23	0.30	Terminal Width
K	-	1.00	-	Center Pad to Pin Clearance
P	0.24	0.42	0.60	Package Corner Chamfer
e	0.50 BSC			Terminal Pitch

**Notes:**

1. All dimensions are in millimeters unless otherwise noted.
2. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.
4. Bilateral coplanarity zone applies to the exposed pad and the perimeter terminals.

## Further Information

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