ispClock Family Handbook
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November 2009 Handbook HB1006

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ispClock™5600A Family

In-System Programmable, Enhanced Zero-Delay Clock Generator with Universal Fan-Out Buffer

June 2008 Data Sheet DS1019

Features

8MHz to 400MHz Input/Output Operation

Low Output to Output Skew (<50ps)

Low Jitter Peak-to-Peak

Up to 20 Programmable Fan-out Buffers

- Programmable output standards and individual enable controls
  - LVTTL, LVCMOS, HSTL, eHSTL, SSTL, LVDS, LVPECL, Differential HSTL, SSTL
- Programmable output impedance
  - 40 to 70¾ in 5¾ increments
- Programmable slew rate
- Up to 10 banks with individual V_{CCO} and GND
  - 1.5V, 1.8V, 2.5V, 3.3V

Fully Integrated High-Performance PLL

- Programmable lock detect
- Multiply and divide ratio controlled by
  - Input divider (1 to 40)
  - Feedback divider (1 to 40)
  - Five output dividers (2 to 80)
- Programmable on-chip loop filter
- Compatible with spread spectrum clocks

Precision Programmable Phase Adjustment (Skew) Per Output

- 16 settings; minimum step size 156ps
  - Locked to VCO frequency
- Up to +/- 12ns skew range
- Coarse and fine adjustment modes

Up to Five Clock Frequency Domains

Flexible Clock Reference and External Feedback Inputs

- Programmable input standards
  - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, SSTL
- Clock A/B selection multiplexer
- Feedback A/B selection multiplexer
- Programmable termination

All Inputs and Outputs are Hot Socket Compliant

Four User-programmable Profiles Stored in E²CMOS® Memory

- Supports both test and multiple operating configurations

Full JTAG Boundary Scan Test In-System Programming Support

Exceptional Power Supply Noise Immunity

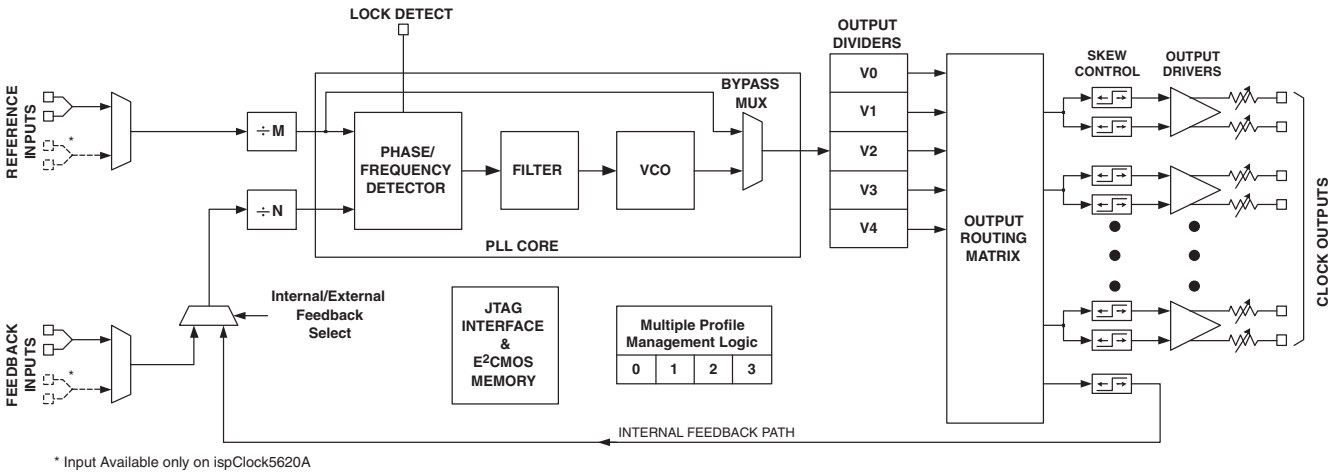
Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges

100-pin and 48-pin TQFP Packages

Applications

- Circuit board common clock generation and distribution
- PLL-based frequency generation
- High fan-out clock buffer
- Zero-delay clock buffer

Product Family Block Diagram



* Input Available only on ispClock5620A

General Description and Overview

The ispClock5610A and ispClock5620A are in-system-programmable high-fanout enhanced zero delay clock generators designed for use in high performance communications and computing applications. The ispClock5610A provides up to 10 single-ended or five differential clock outputs, while the ispClock5620A provides up to 20 single-ended or 10 differential clock outputs. Each pair of outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, LVTTL, LVCMOS, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile E^2CMOS memory.

The ispClock5600A's PLL and divider systems supports the synthesis of multiple clock frequencies derived from the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken internally from the output of any of the five V-dividers, or externally through FBKA+/- or FBKB+/- pins.

The core functions of all members of the ispClock5600A family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5610A and ispClock5620A.

Table 1-1. ispClock5600A Family Members

Device	Ref. Input Pairs	Feedback Input Pairs	Clock Outputs
ispClock5610A	1	1	10
ispClock5620A	2	2	20

Figure 1-1. ispClock5610A Functional Block Diagram

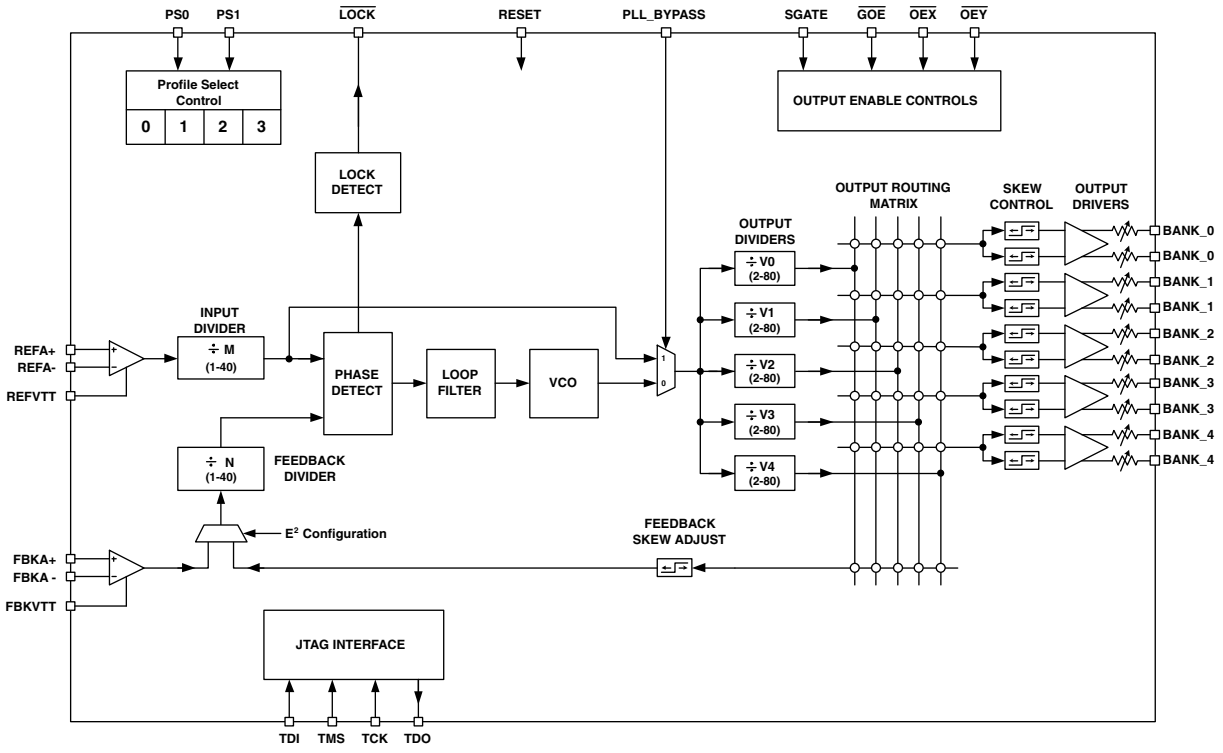
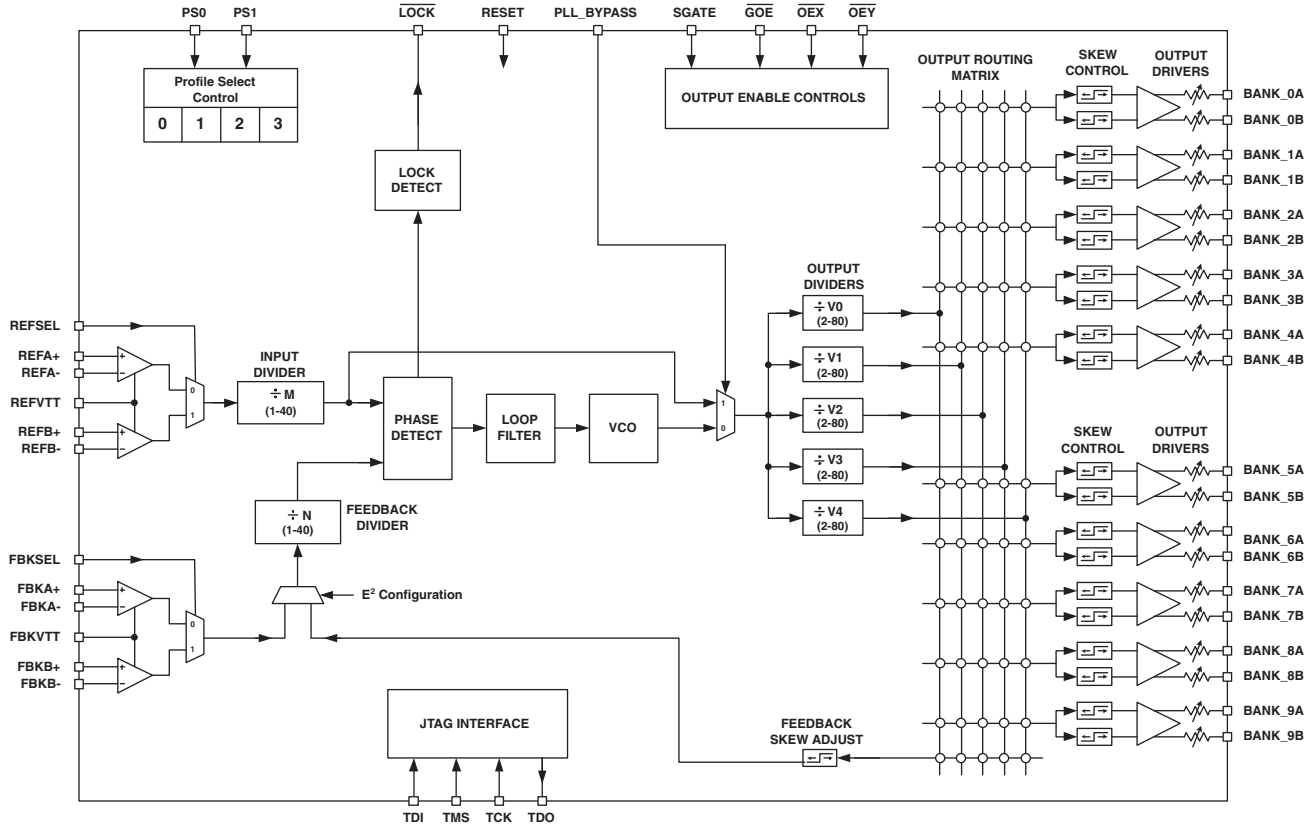


Figure 1-2. ispClock5620A Functional Block Diagram



Absolute Maximum Ratings

	ispClock5600A
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 130°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	ispClock5600A		Units
			Min.	Max.	
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		2.25	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	V_{CC} Turn-on Ramp Rate	All supply pins	—	0.33	V/µs
T_{JOP}	Operating Junction Temperature	Commercial	0	130	°C
		Industrial	-40	130	
T_A	Ambient Operating Temperature	Commercial	0	70[1]	°C
		Industrial	-40	85[1]	

1. Device power dissipation may also limit maximum ambient operating temperature.

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard		V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL		3.0	3.3	3.6	—	—	—	—	—	—
LVCMOS 1.8V		1.71	1.8	1.89	—	—	—	—	—	—
LVCMOS 2.5V		2.375	2.5	2.625	—	—	—	—	—	—
LVCMOS 3.3V		3.0	3.3	3.6	—	—	—	—	—	—
SSTL1.8		1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—
SSTL2 Class 1		2.375	2.5	2.625	1.15	1.25	1.35	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL3 Class 1		3.0	3.3	3.6	1.30	1.50	1.70	V_{REF} - 0.05	V_{REF}	V_{REF} + 0.05
HSTL Class 1		1.425	1.5	1.575	0.68	0.75	0.90	—	0.5 x V_{CCO}	—
eHSTL Class 1		1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—
LVPECL (Differential)		3.0V	3.3V	3.6V	—	—	—	—	—	—
LVDS	V_{CCO} = 2.5V	2.375	2.5V	2.625	—	—	—	—	—	—
	V_{CCO} = 3.3V	3.0	3.3	3.6	—	—	—	—	—	—

Note: '—' denotes V_{REF} or V_{TT} not applicable to this logic standard

E²CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max.	Units
I_{CCD}	Core Supply Current[3]	ispClock5610A f_{VCO} = 800MHz	110	125	mA
		ispClock5620A f_{VCO} = 800MHz	130	150	mA
I_{CCA}	Analog Supply Current[3]	f_{VCO} = 800MHz	5.5	7	mA
I_{CCO}	Output Driver Supply Current (per Bank)	V_{CCO} = 1.8V[1], LVCMOS, f_{OUT} = 266MHz	16	18	mA
		V_{CCO} = 2.5V[1], LVCMOS, f_{OUT} = 266MHz	21	27	mA
		V_{CCO} = 3.3V[1], LVCMOS, f_{OUT} = 266MHz	27	38	mA
		V_{CCO} = 3.3V[2], LVDS, f_{OUT} = 400MHz	8	10	mA
I_{CCJ}	JTAG I/O Supply Current (static)	V_{CCJ} = 1.8V		300	µA
		V_{CCJ} = 2.5V		400	µA
		V_{CCJ} = 3.3V		400	µA

1. Supply current consumed by each bank, both outputs active, 5pF load.
2. Supply current consumed by each bank, 100¾, 5pf differential load.
3. All unused REFCLK and feedbacks connected to ground.

DC Electrical Characteristics – Single-ended Logic

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	12[2, 3]	-12[2, 3]
LVCMOS 1.8V	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	12[2, 3]	-12[2, 3]
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	12[2, 3]	-12[2, 3]
SSTL2 Class 1	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54[2]	V_{CCO} - 0.81[1]	7.6	-7.6
SSTL3 Class 1	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.9[2]	V_{CCO} - 1.3[1]	8	-8
HSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[3]	V_{CCO} - 0.4[2]	8	-8
eHSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[3]	V_{CCO} - 0.4[2]	8	-8

1. Specified for 40¾ internal series output termination.
2. Specified for Ý20¾ internal series output termination, fast slew rate setting.
3. For slower slew rate setting I_{OH}, I_{OL} = 8mA.

DC Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage	V_{THD} ð 100mV	$V_{THD}/2$	—	2.0	V
		V_{THD} ð 150mV	$V_{THD}/2$		2.325	V
V_{THD}	Differential Input Threshold		±100	—	—	mV
V_{IN}	Input Voltage		0	—	2.4	V
V_{OH}	Output High Voltage	R_T = 100¾	—	1.375	1.60	V
V_{OL}	Output Low Voltage	R_T = 100¾	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	R_T = 100¾	250	400	480	mV
ΔV_{OD}	Change in V_{OD} Between H and L		—	—	50	mV
V_{OS}	Output Voltage Offset	Common Mode Output Voltage	1.10	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to GND	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to Each Other	—	—	12	mA

DC Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input Voltage High	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.17	—	V_{CCD} - 0.88	V
		V_{CCD} = 3.3V	2.14	—	2.42	
V_{IL}	Input Voltage Low	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.81	—	V_{CCD} - 1.48	V
		V_{CCD} = 3.3V	1.49	—	1.83	
V_{OH}	Output High Voltage[1]	V_{CCO} = 3.0 to 3.6V	V_{CCO} - 1.07	—	V_{CCO} - 0.88	V
		V_{CCO} = 3.3V	2.23	—	2.42	
V_{OL}	Output Low Voltage[1]	V_{CCO} = 3.0 to 3.6V	V_{CCO} - 1.81	—	V_{CCO} - 1.62	V
		V_{CCO} = 3.3V	1.49	—	1.68	

1. 100¾ differential termination.

Electrical Characteristics – Differential SSTL18

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CCO}	Output Supply Voltage		1.71	1.8	1.89	V
V_{IL}	Low-Logic Level Input Voltage				0.61	V
V_{IH}	Hi Logic Level Input Voltage		1.17			V
V_{SWING}	AC Differential Output Voltage		0.64			V
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} -175mV		V_{REF} +175mV	V
TCKD	Clock Duty Cycle	Load Conditions (Figure 1-6)	45		55	%

Electrical Characteristics – Differential SSTL2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.225	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.62		3.225	V
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} - 200 mV		V_{REF} + 200 mV	V
TCKD	Clock Duty Cycle	Load Conditions (Figure 1-6)	45		55	%

Electrical Characteristics – Differential HSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Output Supply Voltage		1.425	1.5	1.575	V
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		V_{CCD}	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		V_{CCD}	V
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V
TCKD	Clock Duty Cycle	Load Conditions (Figure 1-6)	45		55	%

Electrical Characteristics – Differential eHSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Output Supply Voltage		1.7	1.8	1.9	V
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		V_{CCD}	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		V_{CCD}	V
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V
TCKD	Clock Duty Cycle	Load Conditions (Figure 1-6)	45		55	%

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	Note 3	—	120	150	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	8	10	pF
		Note 6	—	13.5	15	pF

1. Applies to clock reference inputs when termination ‘open’.
2. Applies to TDI, TMS inputs.
3. Applies to REFSEL, PS0, PS1, $\overline{GOE}$, SGATE and PLL_BYPASS, FBKSEL, OEX, OEY.
4. Applies to all logic types when in tristated mode.
5. Applies to OEX, OEY, TCK, RESET inputs.
6. Applies to REFA+, REFA-, REFB+, REFB-, FBKA+, FBKA-, FBKB+, FBKB-.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
t_{IOI} Input Adders[2]					
LVTTL_in	Using LVTTL Standard	0	0	0	ps
LVCMOS18_in	Using LVCMOS 1.8V Standard	-99	80	315	ps
LVCMOS25_in	Using LVCMOS 2.5V Standard	0	0	0	ps
LVCMOS33_in	Using LVCMOS 3.3V Standard	0	0	0	ps
SSTL18_in	Using SSTL18 Standard	10	360	642	ps
SSTL2_in	Using SSTL2 Standard	64	420	679	ps
SSTL3_in	Using SSTL3 Standard	34	380	630	ps
HSTL_in	Using HSTL Standard	231	672	1064	ps
eHSTL_in	Using eHSTL Standard	128	514	846	ps
LVDS_in	Using LVDS Standard	118	426	651	ps
LVPECL_in	Using LVPECL Standard	201	593	937	ps
t_{IOO} Output Adders[1, 3]					
LVTTL_out	Output Configured as LVTTL Buffer	116	395	553	ps
LVCMOS18_out	Output Configured as LVCMOS 1.8V Buffer	155	510	730	ps
LVCMOS25_out	Output Configured as LVCMOS 2.5V Buffer	124	387	592	ps
LVCMOS33_out	Output Configured as LVCMOS 3.3V Buffer	116	395	553	ps
SSTL2_out	Output Configured as SSTL2 Buffer	-109	66	209	ps
SSTL3_out	Output Configured as SSTL3 Buffer	-97	78	242	ps
SSTL18_out_diff	Output Configured as SSTL18 Buffer (Differential)	-153	41	228	ps
HSTL_out_diff	Output Configured as HSTL Buffer (Differential)	-4	180	402	ps
eHSTL_out_diff	Output Configured as eHSTL Buffer (Differential)	-16	173	375	ps
SSTL_out_diff	Output Configured as SSTL2 Buffer (Differential)	-146	83	305	ps
LVDS_out	Output Configured as LVDS Buffer	0	0	0	ps
LVPECL_out	Output Configured as LVPECL Buffer	-187	-17	57	ps
t_{IOS} Output Slew Rate Adders[1]					
Slew_1	Output Slew_1 (Fastest)	—	0	—	ps
Slew_2	Output Slew_2	—	330	—	ps
Slew_3	Output Slew_3	—	660	—	ps
Slew_4	Output Slew_4 (Slowest)	—	1320	—	ps

1. Measured under standard output load conditions. See Figures 1-3-1-5.
2. All input adders referenced to LVCMOS33.
3. All output adders referenced to LVDS.

Output Rise and Fall Times – Typical Values[1, 2]

Output Type	Slew 1 (Fastest)		Slew 2		Slew 3		Slew 4 (Slowest)		Units
	t_R	t_F	t_R	t_F	t_R	t_F	t_R	t_F	
LVTTL	0.54	0.76	0.60	0.87	0.78	1.26	1.05	1.88	ns
LVCMOS 1.8V	0.75	0.69	0.88	0.78	0.83	1.11	1.20	1.68	ns
LVCMOS 2.5V	0.57	0.69	0.65	0.78	0.99	0.98	1.65	1.51	ns
LVCMOS 3.3V	0.55	0.77	0.60	0.87	0.78	1.26	1.05	1.88	ns
SSTL18	0.55	0.40	—	—	—	—	—	—	ns
SSTL2	0.50	0.40	—	—	—	—	—	—	ns
SSTL3	0.50	0.45	—	—	—	—	—	—	ns
HSTL	0.60	0.45	—	—	—	—	—	—	ns
eHSTL	0.55	0.40	—	—	—	—	—	—	ns
LVDS[3]	0.25	0.20	—	—	—	—	—	—	ns
LVPECL[3]	0.20	0.20	—	—	—	—	—	—	ns

1. See Figures 1-3-1-5 for test conditions.
2. Measured between 20% and 80% points.
3. Only the 'fastest' slew rate is available in LVDS and LVPECL modes.

Output Test Loads

Figures 1-3-1-5 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 1-3. CMOS Termination Load

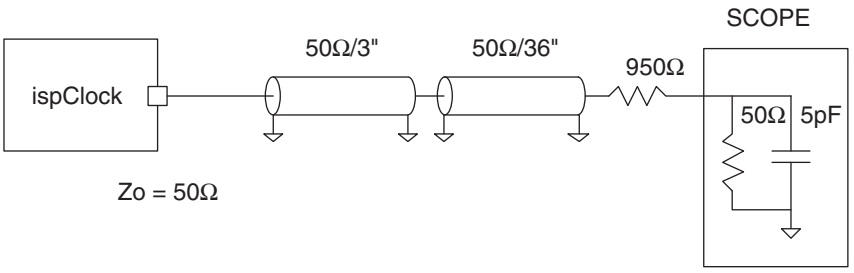


Figure 1-4. eHSTL/HSTL/SSTL Termination Load

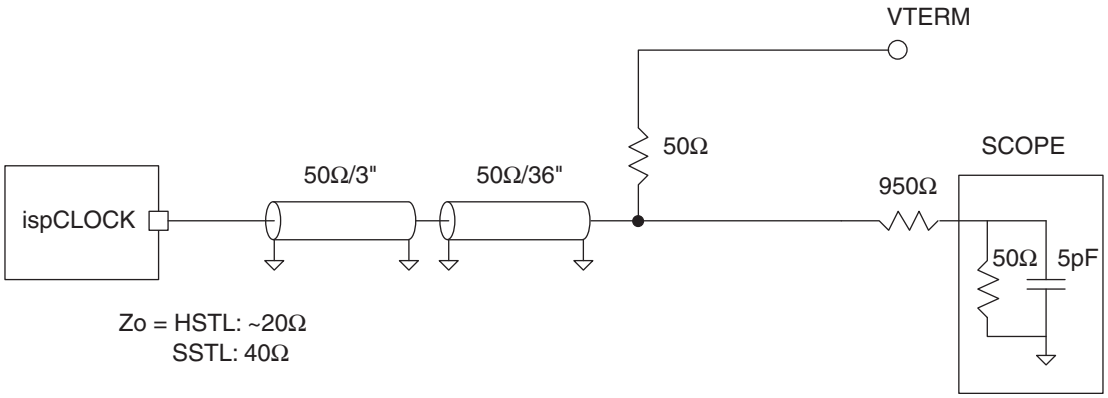


Figure 1-5. LVDS/LVPECL Termination Load

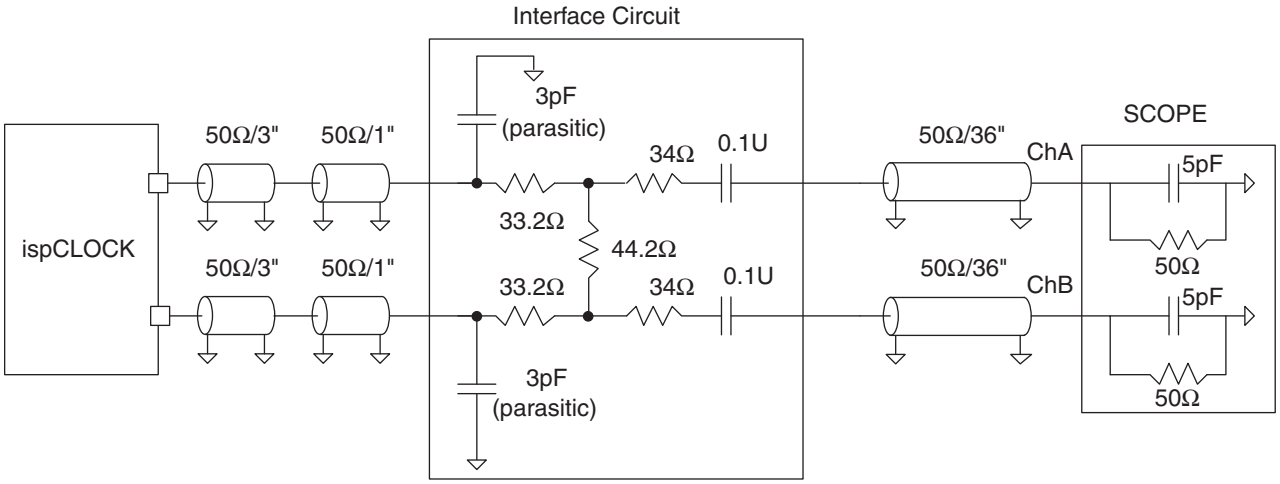
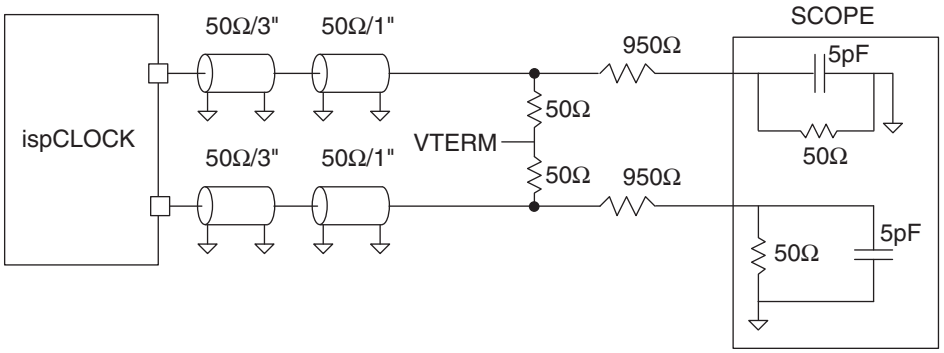


Figure 1-6. Differential HSTL/SSTL Termination Load



Programmable Input and Output Termination Characteristics

Symbol	Parameter	Conditions	V_{CCO} Voltage	Min.	Typ.	Max.	Units
R_{IN}	Input Resistance	Rin=40¾ setting		36	—	44	¾
		Rin=45¾ setting		40.5	—	49.5	
		Rin=50¾ setting		45	—	55	
		Rin=55¾ setting		49.5	—	60.5	
		Rin=60¾ setting		54	—	66	
		Rin=65¾ setting		59	—	71.5	
		Rin=70¾ setting		61	—	77	
R_{OUT}	Output Resistance[1]	RoutÝ20¾ setting	VCCO=3.3V	—	15	—	¾
			VCCO=2.5V	—	15	—	
			VCCO=1.8V	—	16	—	
			VCCO=1.5V	—	14	—	
		RoutÝ40¾ setting	VCCO=3.3V	-9%	40	9%	
			VCCO=2.5V	-11%	40	11%	
			VCCO=1.8V	-13%	41	13%	
		RoutÝ45¾ setting	VCCO=3.3V	-10%	45	10%	
			VCCO=2.5V	-12%	45	12%	
			VCCO=1.8V	-14%	48	14%	
		RoutÝ50¾ setting	VCCO=3.3V	-8%	50	8%	
			VCCO=2.5V	-9%	50	9%	
			VCCO=1.8V	-13%	54	13%	
		RoutÝ55¾ setting	VCCO=3.3V	-9%	55	9%	
			VCCO=2.5V	-11%	55	11%	
			VCCO=1.8V	-13%	59	13%	
		RoutÝ60¾ setting	VCCO=3.3V	-8%	59	8%	
			VCCO=2.5V	-9%	59	9%	
			VCCO=1.8V	-14%	63	14%	
		RoutÝ65¾ setting	VCCO=3.3V	-8%	65	8%	
			VCCO=2.5V	-9%	64	9%	
			VCCO=1.8V	-13%	69	13%	
		RoutÝ70¾ setting	VCCO=3.3V	-9%	72	9%	
			VCCO=2.5V	-10%	70	10%	
			VCCO=1.8V	-12%	74	12%	

1. Guaranteed by characterization.

Performance Characteristics – PLL

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
f_{REF}, f_{FBK}	Reference and feedback input frequency range			8		400	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference and feedback input clock HIGH and LOW times	M-Divider and N-Divider not bypassed.		1.25			ns
t_{RINP}, t_{FINP}	Reference and feedback input rise and fall times	Measured between 20% and 80% levels				5	ns
M_{DIV}	M-divider range			1		40	
N_{DIV}	N-Divider range			1		40	
f_{PFD}	Phase detector input frequency range[2]			8		400	MHz
f_{VCO}	VCO operating frequency			320		800	MHz
V_{DIV}	Output Divider range	Even integer values only		2		80	
f_{OUT}	Output frequency range[1]	Fine Skew Mode, f_{VCO} = 800MHz	All differential options	4		400	MHz
			All single-ended options	4		266	MHz
		Coarse Skew Mode, f_{VCO} = 800MHz		2.5		200	MHz
t_{JIT} (cc)	Output adjacent-cycle jitter[6] (1000 cycle sample)	f_{PFD} Š 100MHz				70	ps (p-p)
t_{JIT} (per)	Output period jitter[6] (10000 cycle sample)	f_{PFD} Š 100MHz				12	ps (RMS)
$t_{JIT(\phi)}$	Reference clock to output jitter[6] (2000 cycle sample)	f_{PFD} Š 100MHz				50	ps (RMS)
$t\phi$	Static phase offset[5]			-100		200	ps
t_{DELAY}	Reference clock to output delay	Internal feedback mode[4]			2.25		ns
DC	Output duty cycle	Output type LVCMOS 3.3V[3] f_{OUT} >100 MHz		45		55	%
$t_{PDBY-PASS}$	Reference clock to output propagation delay	M=1, V=2	Input: LVPECL Output: LVPECL	6.2		8.8	ns
			Input: LVCMOS Output: LVCMOS	6		8.25	ns
t_{LOCK}	PLL lock time	From Power-up event			150		µs
		From Reset event			15		µs
t_{RELOCK}	PLL relock time	To same reference frequency			15		µs
		To different frequency			150		µs
PSR	Power supply rejection, period jitter vs. power supply noise	$f_{IN} = f_{OUT}$ = 100MHz $V_{CCA} = V_{CCD} = V_{CCO}$ modulated with 100kHz sinusoidal stimulus			0.05		$\frac{ps(RMS)}{mV(p\text{-}p)}$

1. In PLL Bypass mode (PLL_BYPASS = HIGH), output will support frequencies down to 0Hz (divider chain is a fully static design).
2. Dividers should be set so that they provide the phase detector with signals of 8MHz or greater for loop stability.
3. See Figures 1-3-1-5 for output loads.
4. Input and outputs LVPECL mode
5. Inserted feedback loop delay < 7ns
6. Measured with f_{OUT} = 100MHz, f_{VCO} = 600MHz, input and output interface set to LVPECL.

Timing Specifications

Skew Matching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-output Skew	Between any two identically configured and loaded outputs regardless of bank.	—	—	50	ps

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKRANGE}$	Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 320 MHz	—	5.86	—	ns
		Fine Skew Mode, f_{VCO} = 800 MHz	—	2.34	—	
		Coarse Skew Mode, f_{VCO} = 320 MHz	—	11.72	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	4.68	—	
SK_{STEPS}	Skew Steps per range		—	16	—	
t_{SKSTEP}	Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 320 MHz	—	390	—	ps
		Fine Skew Mode, f_{VCO} = 800 MHz	—	156	—	
		Coarse Skew Mode, f_{VCO} = 320 MHz	—	780	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	312	—	
t_{SKERR}	Skew Time Error[3]	Fine skew mode	—	30	—	ps
		Coarse skew mode	—	50	—	

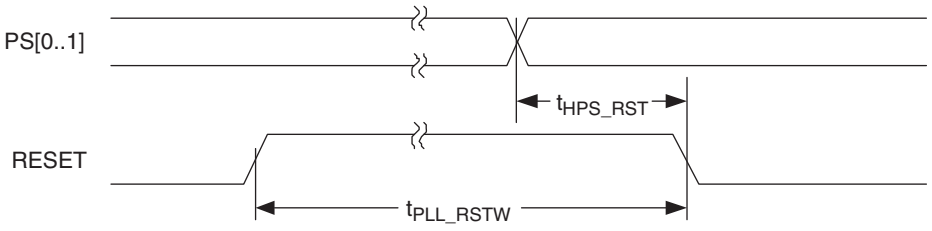
1. Skew control range is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 15/(8 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 15/(4 \times f_{VCO})$.
2. Skew step size is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(4 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, $\overline{OEX}$ or $\overline{OEY}$ to Output Disabled/ Enabled		—	10	20	ns
$t_{DIS/GOE}$	Delay Time, $\overline{GOE}$ to Output Disabled/Enabled		—	10	20	ns
$t_{SUSGATE}$	Setup Time, SGATE to Output Clock Start/ Stop		3	—	—	cycles[1]
t_{PLL_RSTW}	PLL Reset Pulse Width[2]		1	—	—	ms
t_{RSTW}	Logic Reset Pulse Width[3]		20	—	—	ns
t_{HPS_RST}	Hold time for RESET past change in PS[0..1]		20	—	—	ns

1. Output clock cycles for the particular output being controlled.
2. Will completely reset PLL.
3. Will only reset digital logic.

Figure 1-7. RESET and Profile Select Timing



Timing Specifications (Cont.)

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_H	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

Timing Diagrams

Figure 1-8. Erase (User Erase or Erase All) Timing Diagram

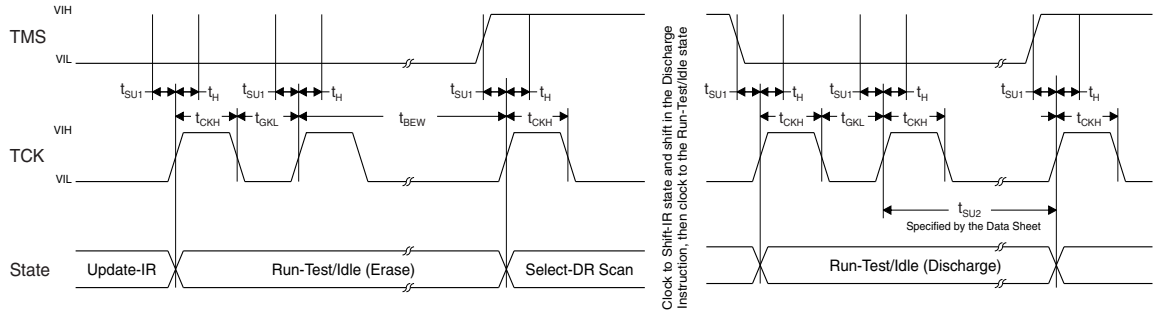


Figure 1-9. Programming Timing Diagram

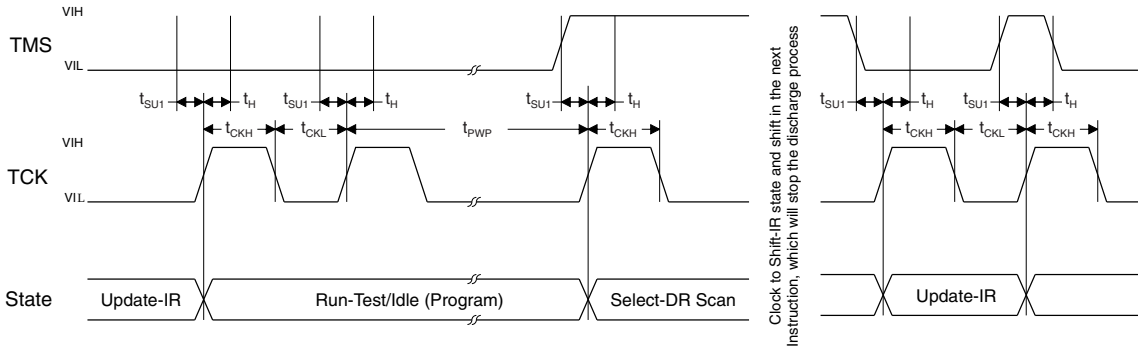


Figure 1-10. Verify Timing Diagram

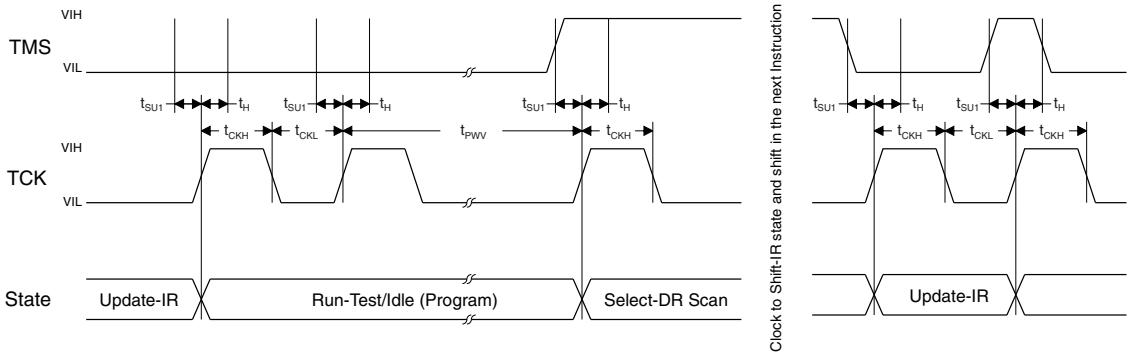
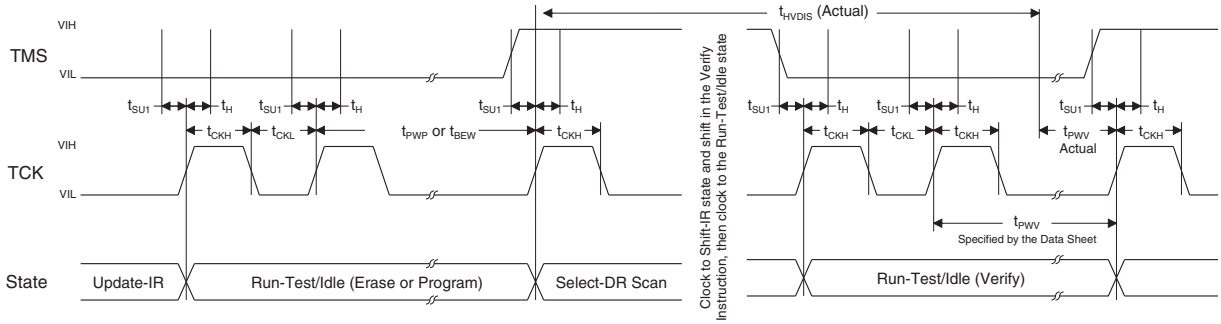
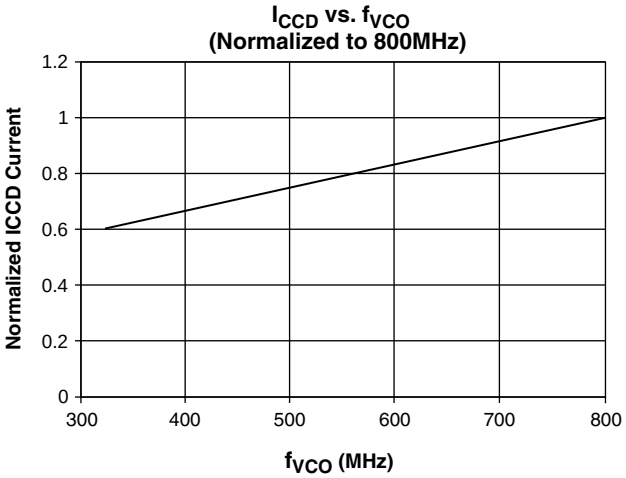
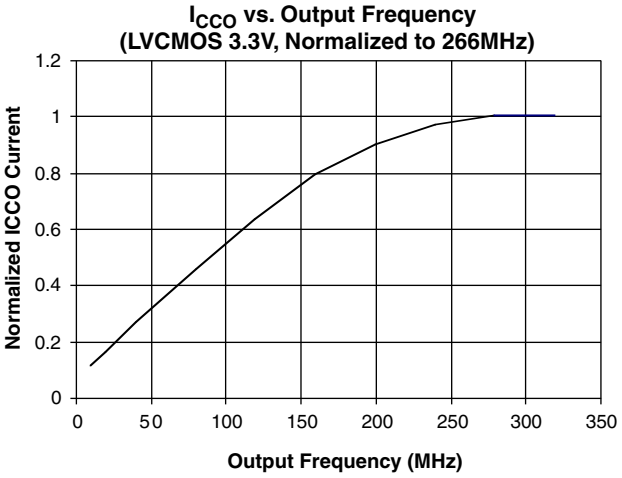


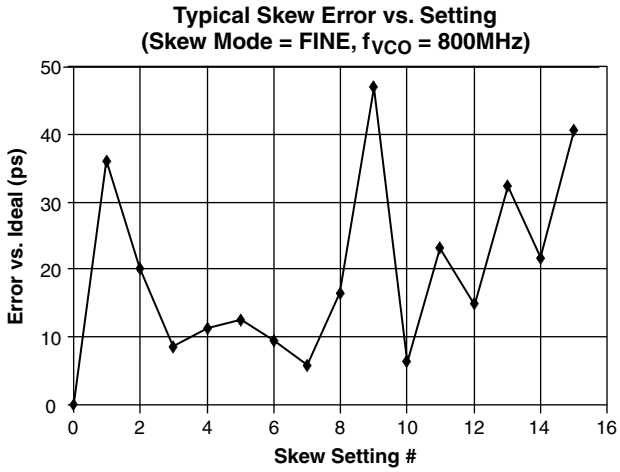
Figure 1-11. Discharge Timing Diagram

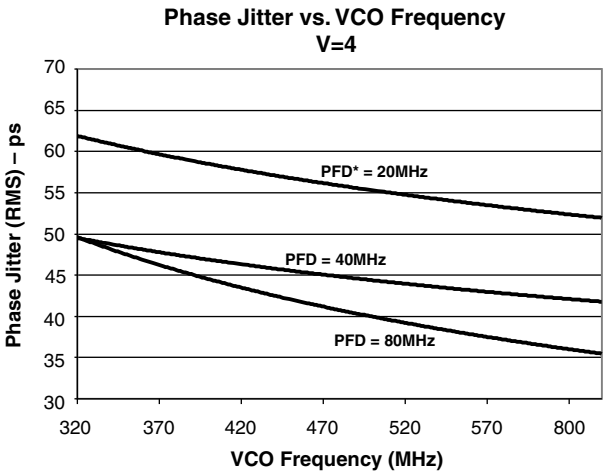


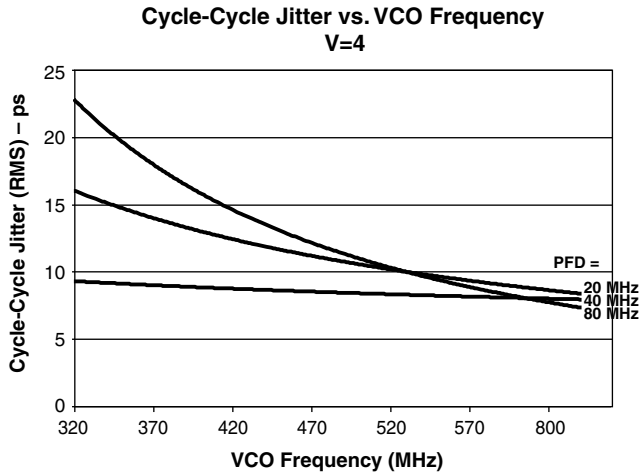
Typical Performance Characteristics

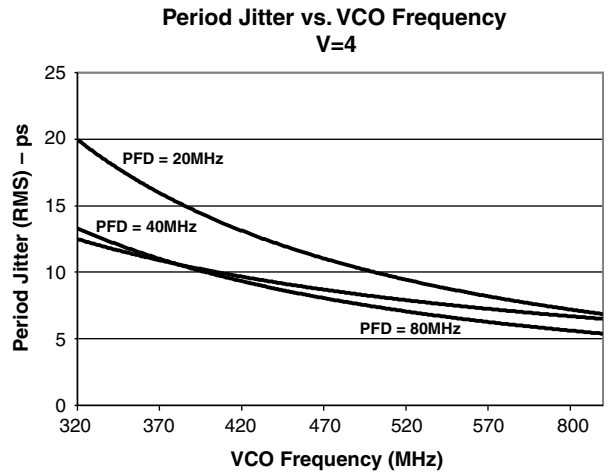






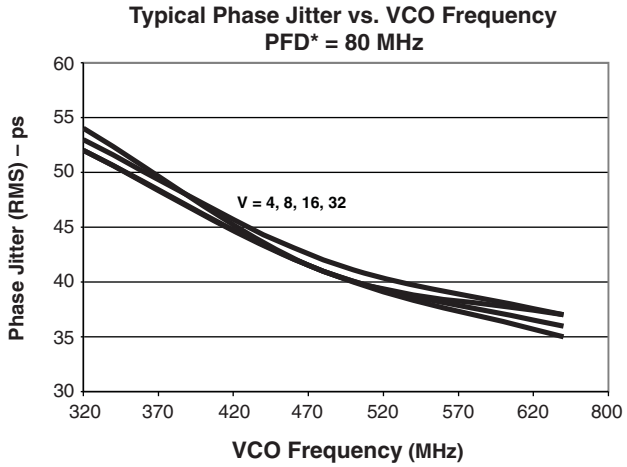


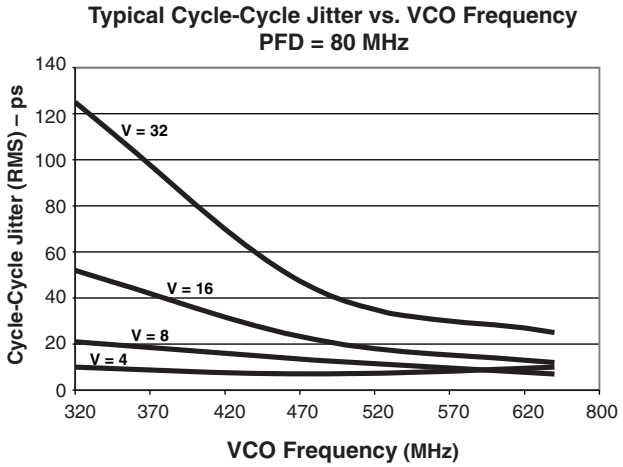


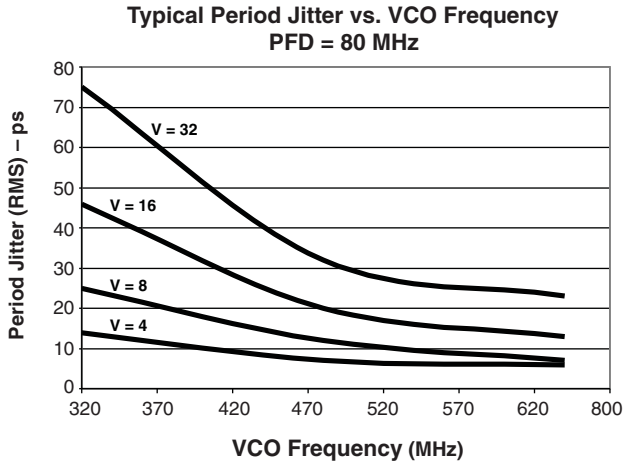


*PFD = Phase/Frequency Detector

Typical Performance Characteristics (Cont.)







*PFD = Phase/Frequency Detector

Detailed Description

PLL Subsystem

The ispClock5600A provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Additionally, a set of programmable input, output and feedback dividers (M, N, V[1..5]) is provided to support the synthesis of different output frequencies.

Phase/Frequency Detector

The ispClock5600A provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI}$, $t_{CLOCKLO}$) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter.

A lock-detection feature is also associated with the PFD. When the ispClock5600A is in a LOCKED state, the LOCK output pin goes LOW. The lock detector has two operating modes: Phase Lock Detect mode and Frequency

Lock Detect mode. In Phase Lock Detect mode, the LOCK signal is asserted if the phases of the reference and feedback signals match, whereas in Frequency Lock Detect mode the LOCK signal is asserted when the frequencies of the feedback and reference signals match. The option for which mode to use is programmable and may be set using PAC-Designer software (available from the Lattice website at www.latticesemi.com).

In Phase Lock Detect mode the lock detector asserts the LOCK signal as soon as a lock condition is determined.

In Frequency Lock Detect mode, however, the PLL must be in a locked condition for a set number of phase detector cycles before the LOCK signal will be asserted. The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 to 256.

When the lock condition is lost the LOCK signal will be de-asserted immediately in both Phase Lock Detect and Frequency Lock Detect modes.

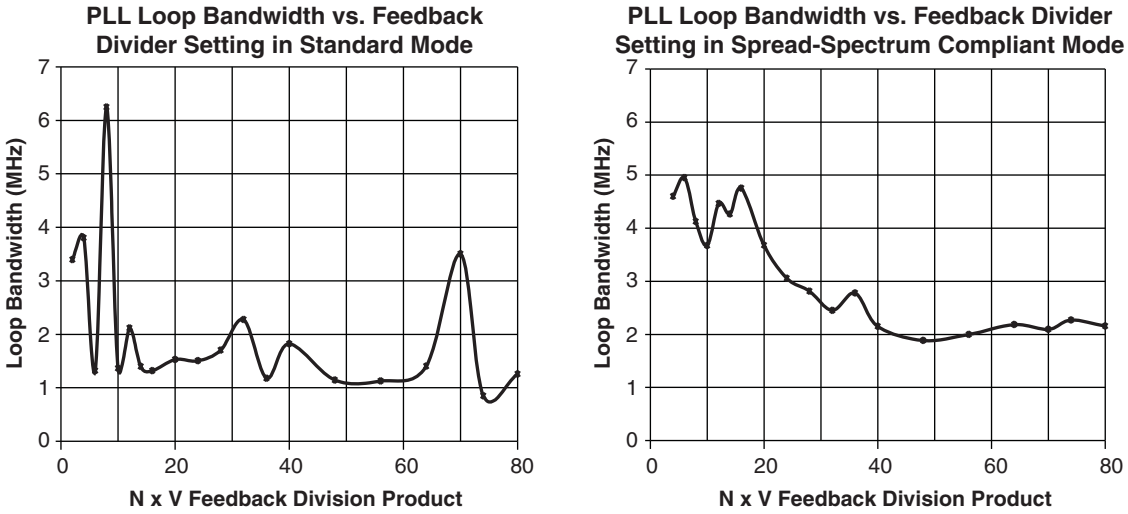
Loop Filter: The loop filter parameters for each profile are automatically selected by the PAC-Designer software depending on the following:

- Individual profile VCO operating frequency
- Individual profile NxV product
- Maximum VCO operating frequency across all used profiles

Spread Spectrum Support: The reference clock inputs of the ispClock5600A device are spread spectrum clock tolerant. The tolerance limits are:

- Center spread ±0.125% to ±2%
- Down spread -0.25% to -4%
- 30-33kHz modulation frequency

Figure 1-12. PLL Loop Bandwidth vs. Feedback Divider Setting (Nominal)



VCO

The ispClock5600A provides an internal VCO which provides an output frequency ranging from 320MHz to 800MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to generate output clock skew as a function of the total VCO period. Using the VCO as the basis for controlling output skew allows for highly precise and consistent skew generation, both from device-to-device, as well as channel-to-channel within the same device.

M-, N-, and V-Dividers

The ispClock5600A incorporates a set of programmable dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input.

The input, or M-Divider prescales the input reference frequency, and can be programmed with integer values over the range of 1 to 40. To achieve low levels of output jitter, it is best to use the smallest M-Divider value possible.

The feedback, or N-Divider prescales the feedback frequency and like the M-Divider, can also be programmed with integer values ranging from 1 to 40.

Each one of the five output, or V-Dividers can be independently programmed to provide even division ratios ranging from 2 to 80.

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V-Divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{N \times V_{fbk}}{M \times V_k} \quad (1)$$

where

f_k is the frequency of V-Divider k
f_{ref} is the input reference frequency
M and N are the input and feedback divider settings
V_{fbk} is the setting of the V-Divider used to close the PLL feedback path
V_k is the setting of the V-Divider used to provide output k

Note that because the feedback may be taken from any V-Divider, V_k and V_{fbk} may refer to the same divider.

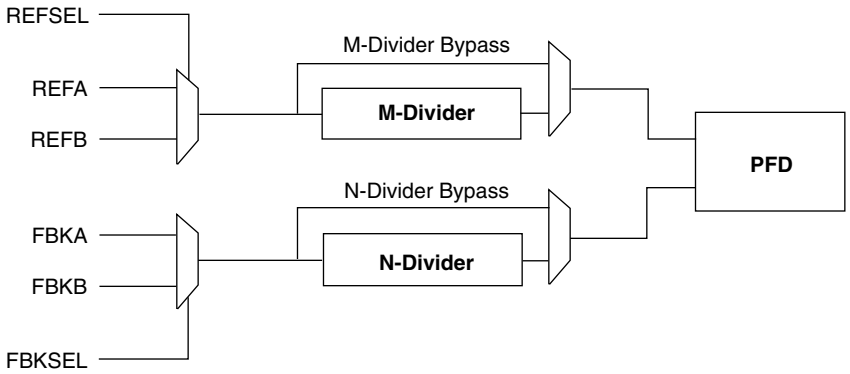
Because the VCO has an operating frequency range spanning 320 MHz to 800 MHz, and the V-Dividers provide division ratios from 2 to 80, the ispClock5600A can generate output signals ranging from 5 MHz to 400 MHz. For performance and stability reasons, however, there are several constraints which should be followed when selecting divider values:

- Use the smallest feasible value for the M-Divider
  - The output frequency from the M (and N) divider should be greater or equal to 8 MHz.
- The product of the N-Divider and the V-Divider used to close the PLL's feedback loop should be less than or equal to 80 (N x V_{fbk} ð 80)

M-Divider and N-Divider Bypass Mode

The M-Divider and the N-Divider in the ispClock5600A device can be bypassed using PAC-Designer software. M and N-Dividers should be bypassed in applications that require glitchless switching between reference and feedback clocks. However, the frequencies of these clocks should be close. If M and N-Dividers are not bypassed, one should ensure that $t_{CLOCKHI}$ and $t_{CLOCKLO}$ specifications are not violated. Otherwise, activation of the reset signal is necessary to ensure reliable switchover.

Figure 1-13. M-Divider and N-Divider Bypass Mode



Note: Bypassing M- and N-Dividers also results in reducing the number of output frequency combinations generated from a single reference clock input.

PLL_BYPASS Mode

The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the output of the M-Divider is routed directly to the inputs of the V-Dividers. In PLL_BYPASS mode, the nominal values of the V-Dividers are halved, so that they provide division ratios ranging from 1 to 40. The output frequency for a given V-Divider (f_k) will be determined by

$$f_k = \frac{f_{ref} \times 2}{M \times V_k} \quad (2)$$

Please note that PLL_BYPASS mode is provided primarily for testing purposes. When PLL_BYPASS mode is enabled, features such as lock detect and skew generation are unavailable.

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

The ispClock5610A provides one input signal pair for reference input and one input pair for external feedback, while the ispClock5620A provides two pairs for reference signals and two pairs for feedback. To select between reference and feedback inputs, the ispClock5620A provides two CMOS-compatible digital inputs called REFSEL and FBKSEL. Table 1-2 shows the behavior of these two control inputs.

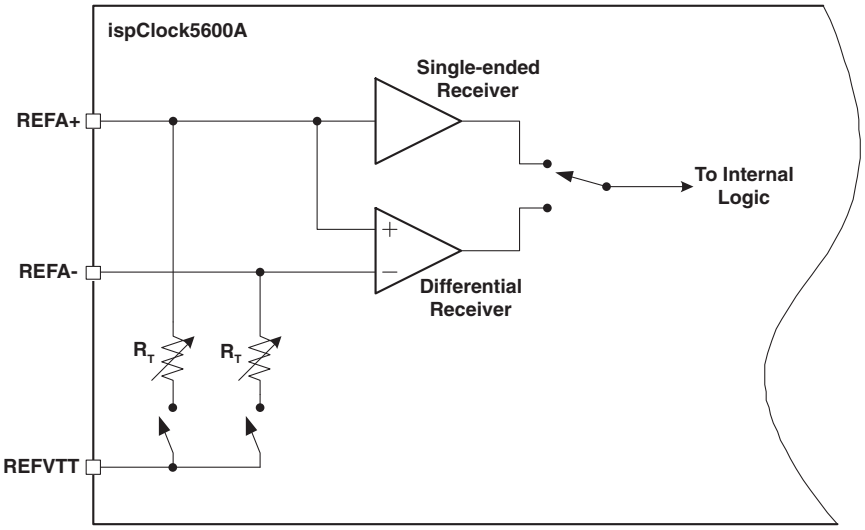
Table 1-2. REFSEL and FBKSEL Operation for ispClock5620A

REFSEL	Selected Input Pair	FBKSEL	Selected Input Pair
0	REFA+/-	0	FBKA+/-
1	REFB+/-	1	FBKB+/-

- LVTTL (3.3V)
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- eHSTL
- Differential SSTL1.8
- Differential SSTL2
- Differential SSTL3
- Differential HSTL
- LVDS
- LVPECL (differential, 3.3V)

Each input also features internal programmable termination resistors, as shown in Figure 1-14. Note that all reference inputs (REFA+, REFA-, REFB+, REFB-) terminate to the REFVTT pin, while all feedback inputs (FBKA+, FBKA-, FBKB+, FBKB-) terminate to the FBKVTT pin.

Figure 1-14. ispClock5600A Clock Reference and Feedback Input Structure (REFA+/- Pair Shown)

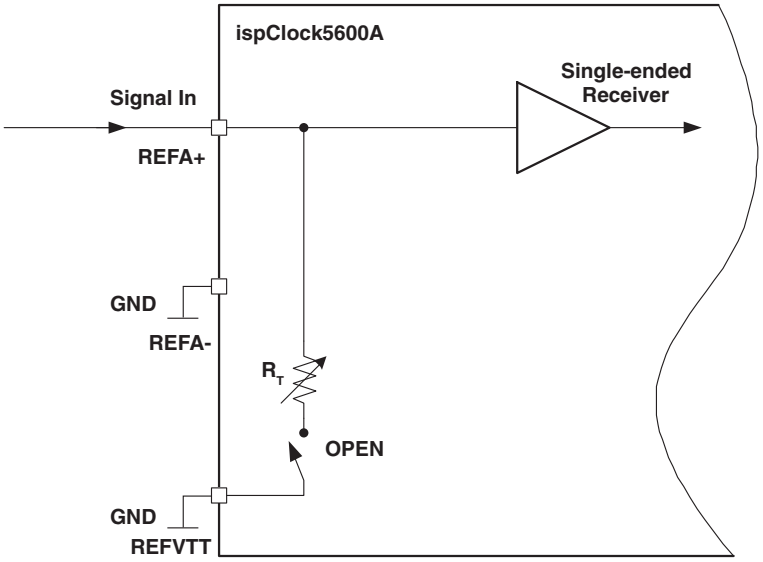


The following usage guidelines are suggested for interfacing to supported logic families.

LVTTL (3.3V), LVCMOS (1.8V, 2.5V, 3.3V)

The receiver should be set to LVCMOS or LVTTL mode, and the input signal should be connected to the '+' terminal of the input pair (e.g. REFA+). The '-' input terminal should be connected to GND. In addition, REFVTT should also be tied to GND. CMOS transmission lines are generally source terminated, so all termination resistors should be set to the OPEN state. Figure 1-15 shows the proper configuration. Please note that because switching thresholds are different for LVCMOS running at 1.8V, there is a separate configuration setting for this particular standard.

Figure 1-15. LVCMOS/LVTTL Input Receiver Configuration



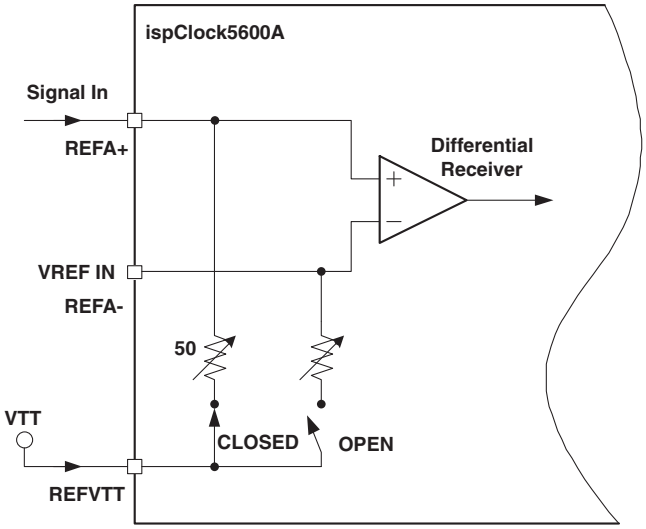
HSTL, eHSTL, SSTL2, SSTL3

The receiver should be set to HSTL/SSTL mode, and the input signal should be fed into the '+' terminal of the input pair. The '-' input terminal should be tied to the appropriate V_{REF} value, and the associated REFVTT or FBKVTT terminal should be tied to a V_{TT} termination supply. The positive input's terminating resistor should be engaged and set to 50¾. Figure 1-16 shows an appropriate configuration. Refer to the "Recommended Operating Conditions - Supported Logic Standards" table in this data sheet for suitable values of V_{REF} and $V_{TT.}$ If one of the REF or FBK

pairs is not used, tie the unused pins REF+ and REF- to GND. In addition, if external feedback is not used, tied FBVTT to GND.

One important point to note is that the termination supplies must have low impedance and be able to both source and sink current without experiencing fluctuations. These requirements generally preclude the use of a resistive divider network, which has an impedance comparable to the resistors used, or of commodity-type linear voltage regulators, which can only source current. The best way to develop the necessary termination voltages is with a regulator specifically designed for this purpose. Because SSTL and HSTL logic is commonly used for high-performance memory busses, a suitable termination voltage supply is often already available in the system.

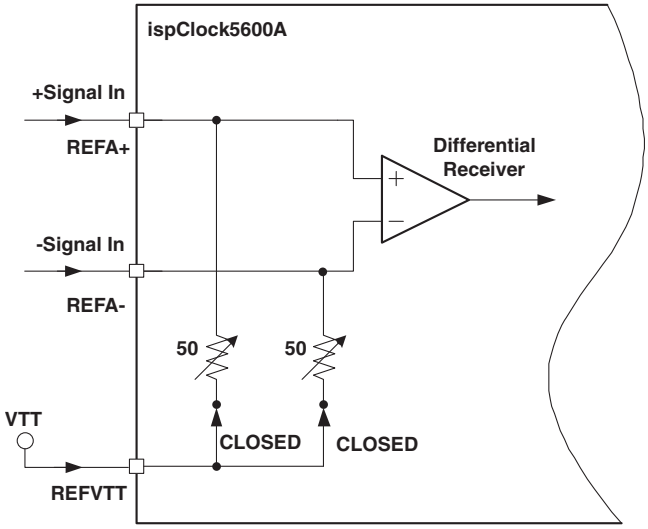
Figure 1-16. SSTL2, SSTL3, eHSTL, HSTL Receiver Configuration



Differential HSTL and SSTL

HSTL and SSTL are sometimes used in a differential form, especially for distributing clocks in high-speed memory systems. Figure 1-17 shows how ispClock5600A reference input should be configured for accepting these standards. The major difference between differential and single-ended forms of these logic standards is that in the differential case, the REFA- input is used as a signal input, not a reference level, and that both terminating resistors are engaged and set to 50¾. If one of the REF or FBK pairs is not used, tie the unused REF+ and REF- pins to GND. If external feedback is not used, tie FBVTT to GND as well.

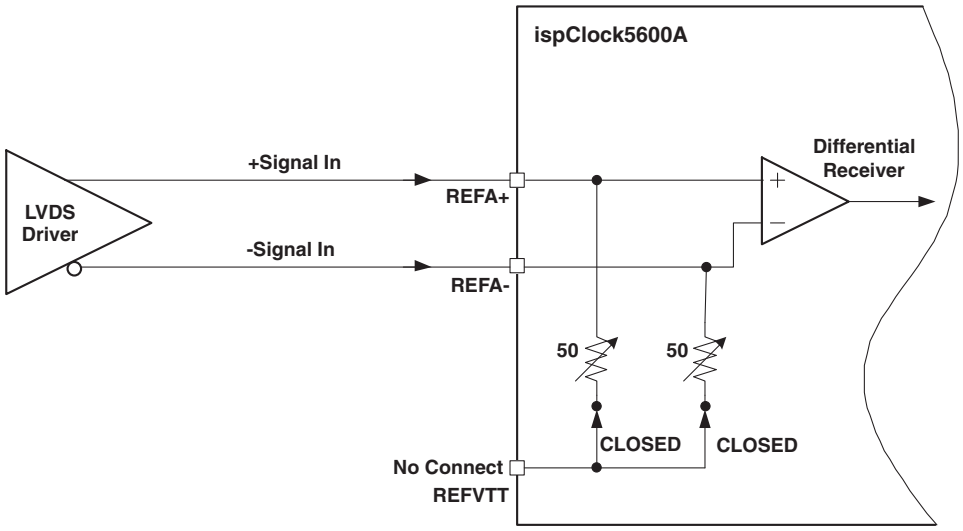
Figure 1-17. Differential HSTL/SSTL Receiver Configuration



LVDS/Differential LVPECL

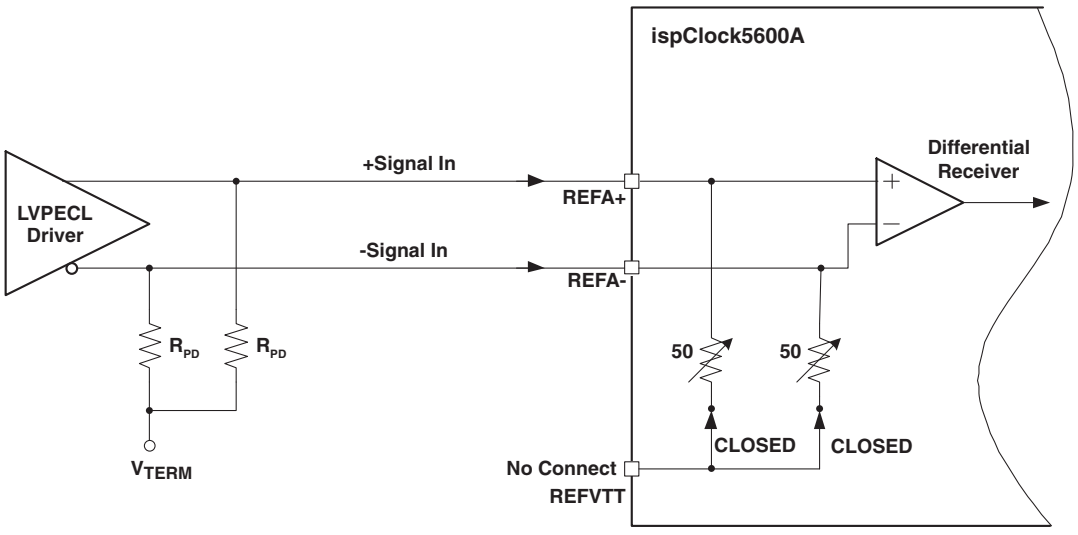
The receiver should be set to LVDS or LVPECL mode as required and both termination resistors should be engaged and set to 50¾. The associated REFVTT or FBKVTT pin, however, should be left unconnected. This creates a floating 100¾ differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 1-18.

Figure 1-18. LVDS Input Receiver Configuration



Note that while a floating 100¾ resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. When interfacing to an LVPECL input signal, the ispClock5600A's internal termination resistors should not be used for this pull-down function, as they may be damaged from excessive current. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 1-19)

Figure 1-19. LVPECL Input Receiver Configuration



Please note that while the above discussions specify using 50¾ termination impedances, the actual impedance required to properly terminate the transmission line and maintain good signal integrity may vary from this ideal. The

actual impedance required will be a function of the driver used to generate the signal and the transmission medium used (PCB traces, connectors and cabling). The ispClock5600A's ability to adjust input impedance over a range of 40¾ to 70¾ allows the user to adapt his circuit to non-ideal behaviors from the rest of the system without having to swap out components.

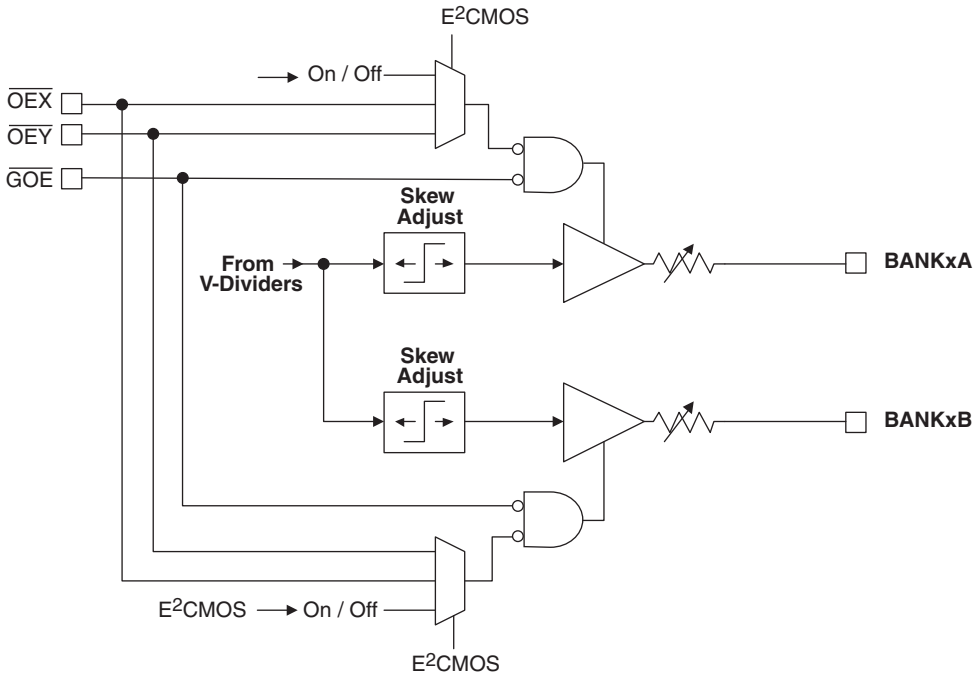
Output Drivers

The ispClock5600A provide banks of configurable, internally-terminated high-speed dual-output line drivers. The ispClock5610A provides five driver banks, while the ispClock5620A provides ten. Each of these driver banks may be configured to provide either a single differential output signal, or a pair of single-ended output signals. Programmable internal source-series termination allows the ispClock5600A to be matched to transmission lines with impedances ranging from 40 to 70 Ohms. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by external control lines. Additionally, each can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 1-20 shows a block diagram of a typical ispClock5600A output driver bank and associated skew control.

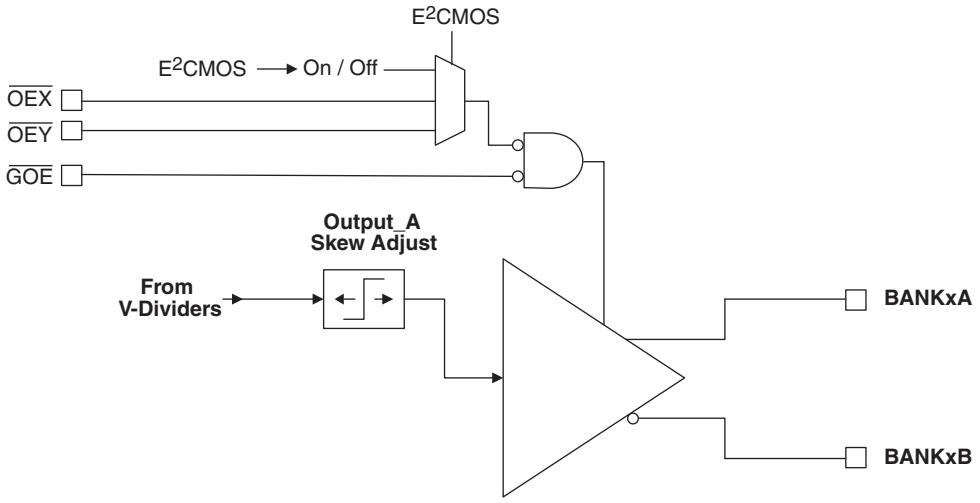
Because of the high edge rates which can be generated by the ispClock5600A's clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respective output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GND0 pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 1-20. ispClock5600A Output Driver and Skew Control



(a) Single-ended Configuration Output Driver and Skew Control



(b) Differential Configuration Output Driver and Skew Control

Each of the ispClock5600A's output driver banks can be configured to support the following logic outputs:

- LVTTL
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- eHSTL
- LVDS
- Differential LVPECL (3.3V)
- Differential SSTL18, SSTL2, SSTL3, HSTL, eHSTL

To provide LVTTL, LVCMOS, SSTL2, SSTL3, HSTL and eHSTL outputs, the CMOS output drivers in each bank are enabled. These circuits provide logic outputs which swing from ground to the VCCO supply rail. The choice of VCCO to be supplied to a given bank is determined by the logic standard to which that bank is configured. Because each pair of outputs has its own VCCO supply pin, each bank can be independently configured to support a different logic standard. Note that the two outputs associated with a bank must necessarily be configured to the same logic standard. The source impedance of each of the two outputs in each bank may be independently set over a range of 40¾ to 70¾ in 5¾ steps. A low impedance option (Ý20¾) is also provided for cases where low source termination is desired on a given output.

Control of output slew rate is also provided in LVTTL, LVCMOS, SSTL2, SSTL3, HSTL and eHSTL output modes. Four output slew-rate settings are provided, as specified in the "Output Rise Times" and "Output Fall Times" tables in this data sheet.

To provide LVDS and differential LVPECL outputs, a separate internal driver is used which provides the correct LVDS or LVPECL logic levels when operating from a 3.3V VCCO. Because both LVDS and differential LVPECL transmission lines are normally terminated with a single 100¾ resistor between the '+' and '-' signal lines at the far end, the ispClock5600A's internal termination resistors are not available in these modes. Also note that output slew-rate control is not available in LVDS or LVPECL mode, and that these drivers always operate at a fixed slew-rate.

Polarity control (true/inverted) is available for all output drivers. In the case of single-ended output standards, the polarity of each of the two output signals from each bank may be controlled independently. In the case of differential output standards, the polarity of the differential pair may be selected.

Suggested Usage

Figure 1-21 shows a typical configuration for the ispClock5600A's output driver when configured to drive an LVTTL or LVCMOS load. The ispClock5600A's output impedance should be set to match the characteristic impedance of the transmission line being driven. The far end of the transmission line should be left open, with no termination resistors.

Figure 1-21. Configuration for LVTTL/LVCMOS Output Modes

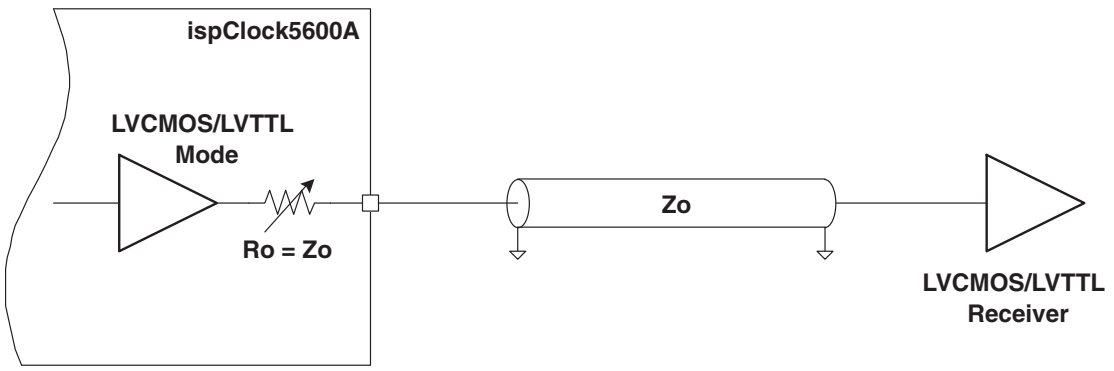


Figure 1-22 shows a typical configuration for the ispClock5600A's output driver when configured to drive SSTL2, SSTL3, HSTL or eHSTL loads. The ispClock5600A's output impedance should be set to 40¾ for driving SSTL2 or SSTL3 loads and to the Ý20¾ setting for driving HSTL and eHSTL. The far end of the transmission line must be terminated to an appropriate VTT voltage through a 50¾ resistor.

Figure 1-22. Configuration for SSTL2, SSTL3, and HSTL Output Modes

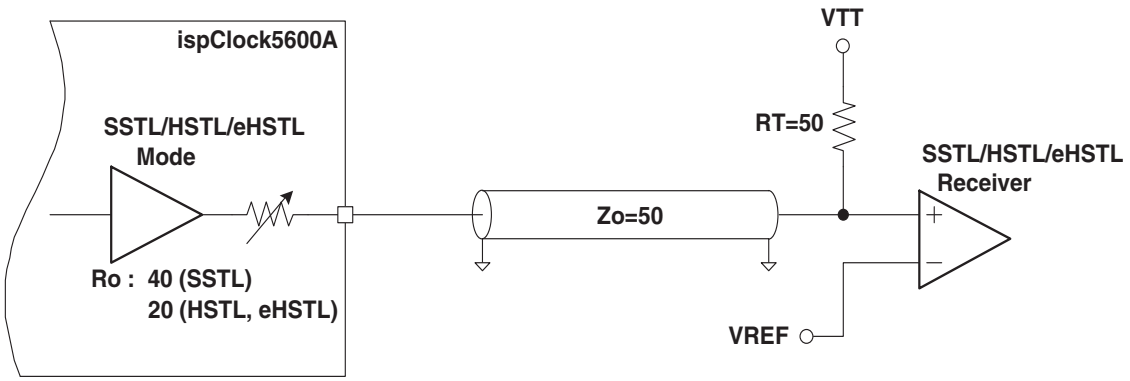
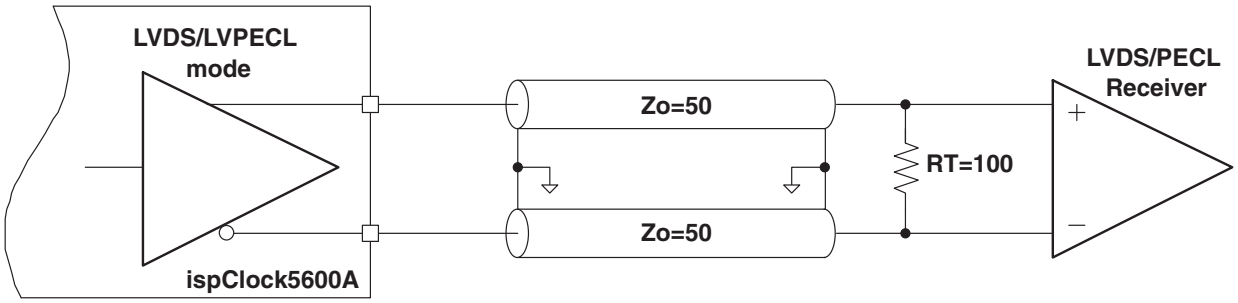


Figure 1-23 shows a typical configuration for the ispClock5600A's output driver when configured to drive LVDS or differential LVPECL loads. The ispClock5600A's output impedance is disengaged when the driver is set to LVDS or LVPECL mode. The far end of the transmission line must be terminated with a 100¾ resistor across the two signal lines.

Figure 1-23. Configuration for LVDS and LVPECL Output Modes



Note that when in LVPECL output mode, the ispClock5600A's output driver provides an internal pull-down, unlike a typical bipolar LVPECL driver. For this reason no external pull-down resistors are necessary and the driver may be terminated with a single 100¾ resistor across the signal lines. For proper operation, pull-down resistors should NOT be used with the ispClock5600A's LVPECL output mode.

Output Enable Controls

The ispClock5600A family provides the user with several options for enabling and disabling output pins, as well as suspending the output clock. In addition to providing the user with the ability to reduce the device's power consumption by turning off unused drivers, these features can also be used for functional testing purposes. The following input pins are used for output enable functions:

- $\overline{\text{GOE}}$ – global output enable
- $\overline{\text{OEX}}$, $\overline{\text{OEY}}$ – secondary output enable controls
- SGATE – synchronous output control

Additionally, internal E^2CMOS configuration bits are provided for the purpose of modifying the effects of these external control pins.

When $\overline{GOE}$ is HIGH, all output drivers are forced into a high-Z state, regardless of any internal configuration. When $\overline{GOE}$ is LOW, the output drivers may also be enabled or disabled on an individual basis, and optionally controlled by the $\overline{OEX}$ and $\overline{OEY}$ pins. Internal E^2CMOS configuration is used to establish whether the output driver is always enabled (when $\overline{GOE}$ pin is LOW), never enabled (permanently off), or selectively enabled by the state of either $\overline{OEX}$ or $\overline{OEY}$.

Synchronous output gating is provided by ispClock5600A devices through the use of the SGATE pin. The SGATE pin does not disable the output driver, but merely forces the output to either a high or low state, depending on the output driver's polarity setting. If the output driver polarity is true, the output will be forced LOW when SGATE is brought LOW, while if it is inverted, the output will be forced HIGH. A primary feature of the SGATE function is that the clock output is enabled and disabled synchronous to the selected internal clock source. This prevents the generation of partial, 'runt', output clock pulses, which would otherwise occur with simple combinatorial gating schemes. The SGATE is available to all clock outputs and is selectable on a bank-by-bank basis.

Table 1-3 shows the behavior of the outputs for various combinations of the output enables, SGATE input, and E^2CMOS configuration.

Table 1-3. Clock Output Enable Functions

$\overline{GOE}$	$\overline{OEX}$	$\overline{OEY}$	E^2 Configuration	Output
X	X	X	Always OFF	High-Z
0	X	X	Always ON	Clock Out
0	0	X	Enable on OEX	Clock Out
0	1	X	Enable on OEX	High-Z
0	X	0	Enable on OEY	Clock Out
0	X	1	Enable on OEY	High-Z
1	X	X	n/a	High-Z

Table 1-4. SGATE Function

SGATE	Bank Controlled by SGATE?	Output Polarity	Output
X	NO	True	Clock
X	NO	Inverted	Inverted Clock
0	YES	True	LOW
0	YES	Inverted	HIGH
1	YES	True	Clock
1	YES	Inverted	Inverted Clock

Skew Control Units

Each of the ispClock5600A's clock outputs is supported by a skew control unit which allows the user to insert an individually programmable delay into each output signal. This feature is useful when it is necessary to de-skew clock signals to compensate for physical length variations among different PCB clock paths.

Unlike the skew adjustment features provided in many competing products, the ispClock5600A's skew adjustment feature provides exact and repeatable delays which exhibit extremely low channel-to-channel and device-to-device variation. This is achieved by deriving all skew timing from the VCO, which results in the skew increment being a linear function of the VCO period. For this reason, skews are defined in terms of 'unit delays', which may be programmed by the user over a range of 0 to 15. The ispClock5600A family also supports both 'fine' and 'coarse' skew modes. In fine skew mode, the unit skew ranges from 156ps to 390 ps, while in the coarse skew mode unit skew varies from 312ps to 780ps. The exact unit skew (TU) may be calculated from the VCO frequency (f_{vco}) by using the following expressions:

For fine skew mode, For coarse skew mode,

$$TU = \frac{1}{8f_{vco}} \qquad TU = \frac{1}{4f_{vco}} \tag{5}$$

When an output driver is programmed to support a differential output mode, a single skew setting is applied to both the BANKxA+ and BANKxB- signals. When the output driver is configured to support a single-ended output standard, each of the two single-ended outputs may be assigned independent skews.

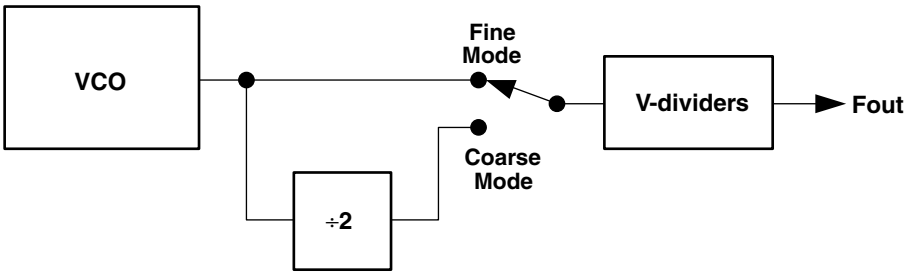
By using the internal feedback path, and programming a skew into the feedback skew control, it is possible to implement negative timing skews, in which the clock edge of interest appears at the ispClock5600A's output before the corresponding edge is presented at the reference input. When the feedback skew unit is used in this way, the resulting negative skew is added to whatever skew is specified for each output. For example, if the feedback skew is set to 6TU, BANK1's skew is 8TU and BANK2's skew is 3TU, then BANK1's effective output skew will be 2TU (8TU-6TU), while BANK2's effective skew will be -3TU (3TU-6TU). This negative skew will manifest itself as BANK2's outputs appearing to lead the input reference clock, appearing as a negative propagation delay.

Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Coarse Skew Mode

The ispClock5600A family provides the user with the option of obtaining longer skew delays at the cost of reduced time resolution through the use of coarse skew mode. Coarse skew mode provides unit delays ranging from 312ps (f_{VCO} = 800MHz) to 780ps (f_{VCO} = 320MHz), which is twice as long as those provided in fine skew mode. When coarse skew mode is selected, an additional divide-by-2 stage is effectively inserted between the VCO and the V-divider bank, as shown in Figure 1-24. When assigning divider settings in coarse skew mode, one must account for this additional divide-by-two so that the VCO still operates within its specified range (320-800MHz).

Figure 1-24. Additional Factor-of-2 Division in Coarse Mode



When one moves from fine skew mode to coarse skew mode with a giveN-Divider configuration, the VCO frequency will attempt to double to compensate for the additional divide-by-2 stage. Because the f_{VCO} range is not increased, however, one must modify the feedback path V-divider settings to bring f_{VCO} back into its specified operating range (320MHz to 800MHz). This can be accomplished by dividing all V-divider settings by two. All output frequencies will remain unchanged from what they were in fine mode. One drawback of moving from fine skew mode into coarse skew mode is that it may not be possible to maintain consistent output frequencies, as only those V-divider settings which are multiples of four (in fine mode) may be divided by two. For example, a V-divider setting of 24 will divide down to 12, which is also a legal V-divider setting, whereas an initial setting of 26 would divide down to 13, which is not a valid setting.

When one moves from coarse skew mode to fine skew mode, the extra divide-by-two factor is removed from between the VCO and the V-divider bank, halving the VCO's effective operating frequency. To compensate for this change, all of the V-dividers must be doubled to move the VCO back into its specified operating range and maintain consistent output frequencies. The only situation in which this may be a problem is when a V-divider initially in

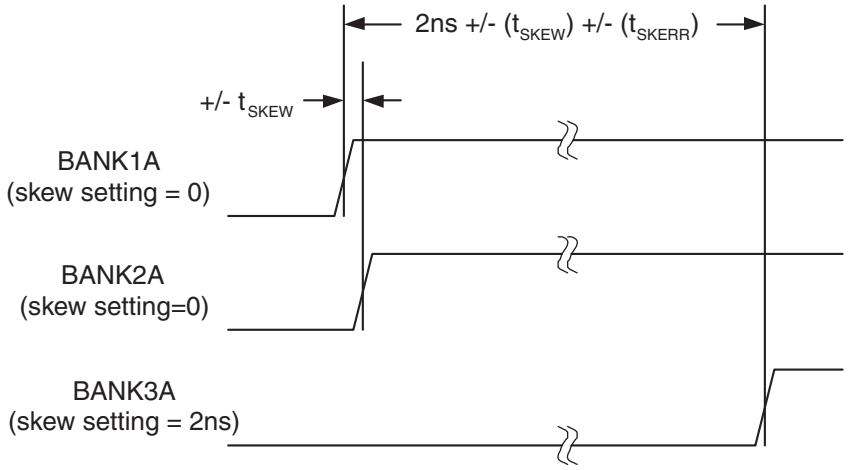
coarse mode has a value greater than 40, as the corresponding fine skew mode setting would be greater than 80, which is not supported.

Output Skew Matching and Accuracy

Understanding the various factors which relate to output skew is essential for realizing optimal skew performance in the ispClock5600A family of devices.

In the case where two outputs are identically configured, and driving identical loads, the maximum skew is defined by $t_{SKEW,}$ which is specified as a maximum of 50ps. In Figure 1-25 the Bank1A and BANK2A outputs show the skew error between two matched outputs.

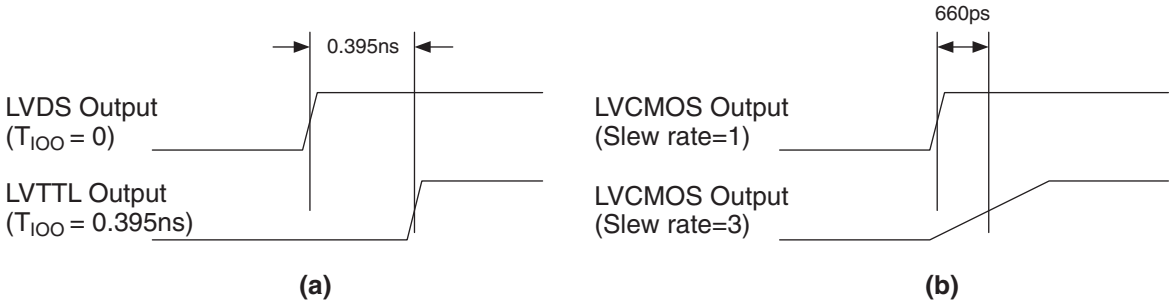
Figure 1-25. Skew Matching Error Sources



One can also program a user-defined skew between two outputs using the skew control units. Because the programmable skew is derived from the VCO frequency, as described in the previous section, the absolute skew is very accurate. The typical error for any non-zero skew setting is given by the t_{SKERR} specification. For example, if one is in fine skew mode with a VCO frequency of 500MHz, and selects a skew of 8TU, the realized skew will be 2ns, which will typically be accurate to within +/-30 ps. An example of error vs. skew setting can be found in the chart 'Typical Skew Error vs. Setting' in the typical performance characteristics section. Note that this parameter adds to output-to-output skew error only if the two outputs have *different* skew settings. The Bank1A and Bank3A outputs in Figure 1-25 show how the various sources of skew error stack up in this case. Note that if two or more outputs are programmed to the same skew setting, then the contribution of the t_{SKERR} skew error term does not apply.

When outputs are configured or loaded differently, this also has an effect on skew matching. If an output is set to support a different logic type, this can be accounted for by using the t_{IOO} output adders specified in the Table 'Switching Characteristics'. That table specifies the additional skew added to an output using LVDS as a baseline. For instance, if one output is specified as LVTTL (t_{IOO} = 0.395ns), and another output is specified as LVDS (t_{IOO} = 0ns), then one could expect 0.395ns of additional skew between the two outputs. This timing relationship is shown in Figure 1-26a.

Figure 1-26. Output Timing Adders for Logic Type (a) and Output Slew Rate (b)

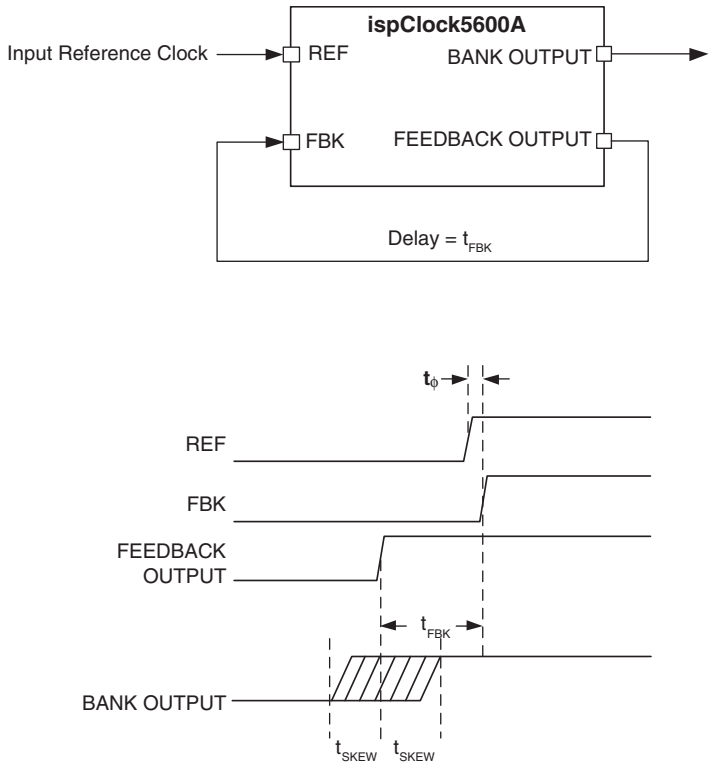


Similarly, when one changes the slew rate of an output, the output slew rate adders (t_{IOS}) can be used to predict the resulting skew. In this case, the fastest slew setting (1) is used as the baseline against which other slews are measured. For example, in the case of outputs configured to the same logic type (e.g. LVCMOS 1.8V), if one output is set to the fastest slew rate (1, t_{IOS} = 0ps), and another set to slew rate 3 (t_{IOS} = 660ps), then one could expect 660ps of skew between the two outputs, as shown in Figure 1-26b.

Static Phase Offset and Input-Output Skew

The ispClock5600A's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. In external feedback mode (Figure 1-27) the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase error. Note that any propagation delays (t_{FBK}) in the external feedback path drive the phase of the output signal *backwards* in time as measured at the output. For this reason, if zero input-to-output delays are required in external feedback mode, the length of the signal path between the output pin and the feedback pin should be minimized.

Figure 1-27. External Feedback Mode and Timing Relationships (Input, Output and Feedback Use the Same Logic Standard)



Internal Feedback Mode

In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Profile Select

The ispClock5600A stores all internal configuration data in on-board E^2CMOS memory. Up to four independent configuration profiles may be stored in each device. The choice of which configuration profile is to be active is specified thought the profile select inputs PS0 and PS1, as shown in Table 1-5.

Table 1-5. Profile Select Function

PS1	PS0	Active Profile
0	0	Profile 0
0	1	Profile 1
1	0	Profile 2
1	1	Profile 3

Each profile controls the following internal configuration items:

- M-Divider setting
- N-Divider setting
- V-Divider settings
- Output skew settings
- Internal feedback skew settings
- Internal vs. external feedback selection

The following settings are independent of the selection of active profile and will apply regardless of which profile is selected:

- Input logic configuration
  - Logic family
  - Input impedance
- Output bank logic configuration
  - Logic family
  - V-divider signal source
  - Enable/SGATE control options
  - Output impedance
  - Slew rate
  - Signal inversion
- V-divider to be used as feedback source
- Fine/Coarse skew mode selection
- UES string

If any of the above items are modified, the change will apply across all profiles. In some cases this may cause unanticipated behavior. If multiple profiles are used in a design, the suitability of the profile independent settings must be considered with respect to each of the individual profiles.

When a profile is changed by modifying the values of the PS0 and PS1 inputs, it is necessary to assert a RESET signal to the ispClock5600A to restart the PLL and resynchronize all the internal dividers.

RESET and Power-up Functions

To ensure proper PLL startup and synchronization of outputs, the ispClock5600A provides both internally generated and user-controllable external reset signals. An internal reset is generated whenever the device is powered up. An external reset may be applied by asserting a logic HIGH at the RESET pin. Asserting RESET resets all internal dividers, and will cause the PLL to lose lock. On losing lock, the VCO frequency will begin dropping. The length of time required to regain lock is related to the length of time for which RESET was asserted.

When the ispClock5600A begins operating from initial power-on, the VCO starts running at a very low frequency (<100 MHz) which gradually increases as it approaches a locked condition. To prevent invalid outputs from being applied to the rest of the system, it is recommended that either the SGATE, $\overline{OEX}$, or $\overline{OEY}$ pins be used to control the outputs based on the status of the LOCK pin. Holding the SGATE pin LOW during power-up will result in the BANK outputs being asserted HIGH or LOW (depending on inversion status) until SGATE is brought HIGH. Asserting $\overline{OEX}$ or $\overline{OEY}$ high will result in the BANK outputs being held in a high-impedance state until the $\overline{OEX}$ or $\overline{OEY}$ pin is pulled LOW.

When either of the minimum $t_{CLOCKHI}$ or $t_{CLOCKLO}$ specifications is violated, the RESET pin should be activated to insure proper behavior of the PLL and outputs.

Thermal Management

In applications where a majority of the ispClock5610A or ispClock5620A's outputs are active and operating at or near maximum output frequency (266MHz for single ended and 400MHz for differential outputs), package thermal limitations may need to be considered to ensure a successful design. Thermal characteristics of the packages employed by Lattice Semiconductor may be found in the document *Thermal Management* which may be obtained at www.latticesemi.com.

The maximum current consumption of the digital and analog core circuitry for ispClock5620A is 150mA worst case (I_{CCD} + I_{CCA}), and each of the output banks may draw up to 38mA worst case (LVCMOS 3.3V, CL=5pF, f_{OUT}=266 MHz, both outputs in each bank enabled). This results in a total device dissipation:

$$P_{DMAX} = 3.3V \times (10 \times 38mA + 150mA) = 1.75W \quad (3)$$

With a maximum recommended operating junction temperature (T_{JOP}) of 130°C for an industrial grade device, the maximum allowable ambient temperature (T_{AMAX}) can be estimated as

$$T_{AMAX} = T_{JOP} - PD_{MAX} \times \Theta_{JA} = 130°C - 1.75W \times 36.9°C/W = 65.4°C \quad (4)$$

where Θ_{JA} = 36.9°C/W for the 100 TQFP package. Θ_{JA} = 68°C/W for the 48 TQFP package in still air.

The above analysis represents the worst-case scenario. Significant improvement in maximum ambient operating temperature can be realized with additional cooling. Providing a 200 LFM (Linear Feet per Minute) airflow reduces Θ_{JA} to 33°C/W for the 100 TQFP package, which results in a maximum ambient operating temperature of 71°C.

In practice, however, the absolute worst-case situation will be relatively rare, as not all outputs may be running at maximum output frequency in a given application. Additionally, if the internal VCO is operating at less than its maximum frequency (800MHz), it requires less current on the VCCD pin. In these situations, one can estimate the effective I_{CCO} for each bank and the effective I_{CCD} for the digital core functions based on output frequency and VCO frequency. Normalized curves relating current to operating frequency for these parameters may be found in the Typical Performance Characteristics section.

While it is possible to perform detailed calculations to estimate the maximum ambient operating temperature from operating conditions, some simpler rule-of-thumb guidance can also be obtained through the derating curves shown in Figure 1-28. The curves in Figure 1-28a show the maximum ambient operating temperature permitted when operating a given number of output banks at the maximum output frequency (266MHz for single ended and 400MHz for differential outputs). Note that it is assumed that both outputs in each bank are active.

Figure 1-28. Maximum Ambient Temperature vs. Number of Active Output Banks

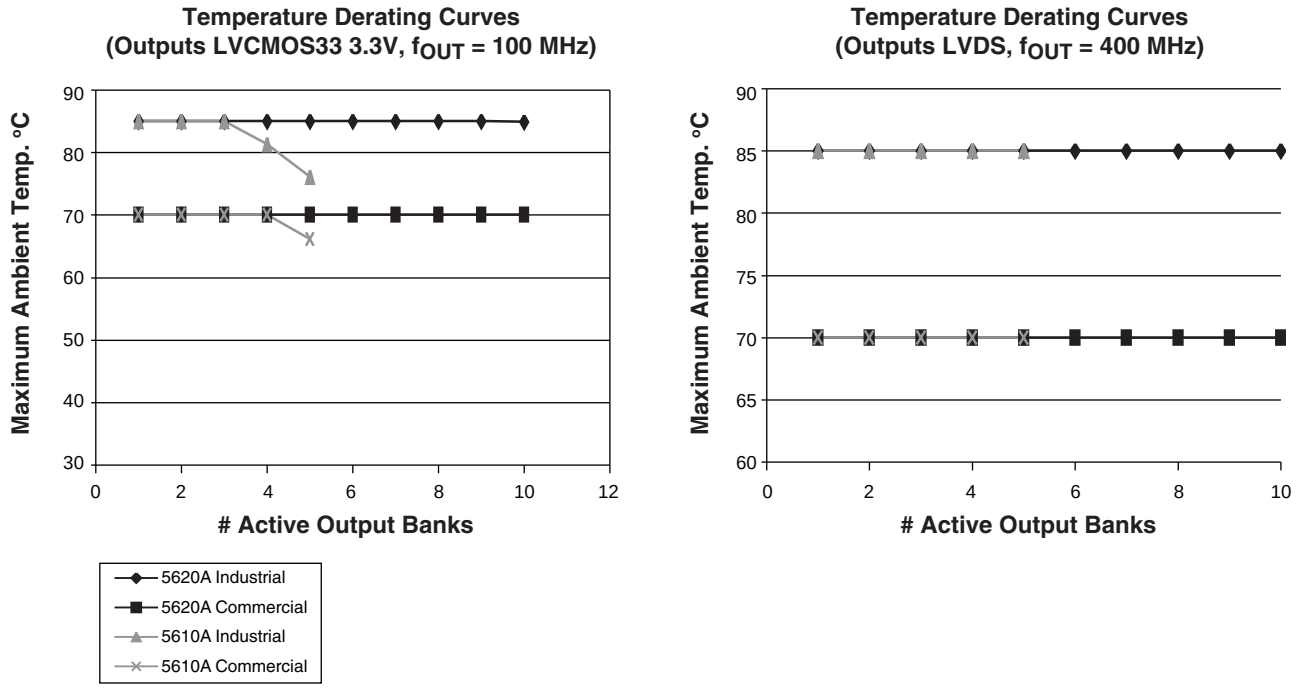


Figure 1-28b shows another derating curve, derived under the assumption that the output frequency is 100MHz. For many applications, 100MHz outputs will be a more realistic scenario. Comparing the maximum temperature limits of Figure 1-28b with Figure 1-28a, one can see that significantly higher operating temperatures are possible in LVCMOS 3.3V output mode with more outputs at 100MHz than at 400MHz.

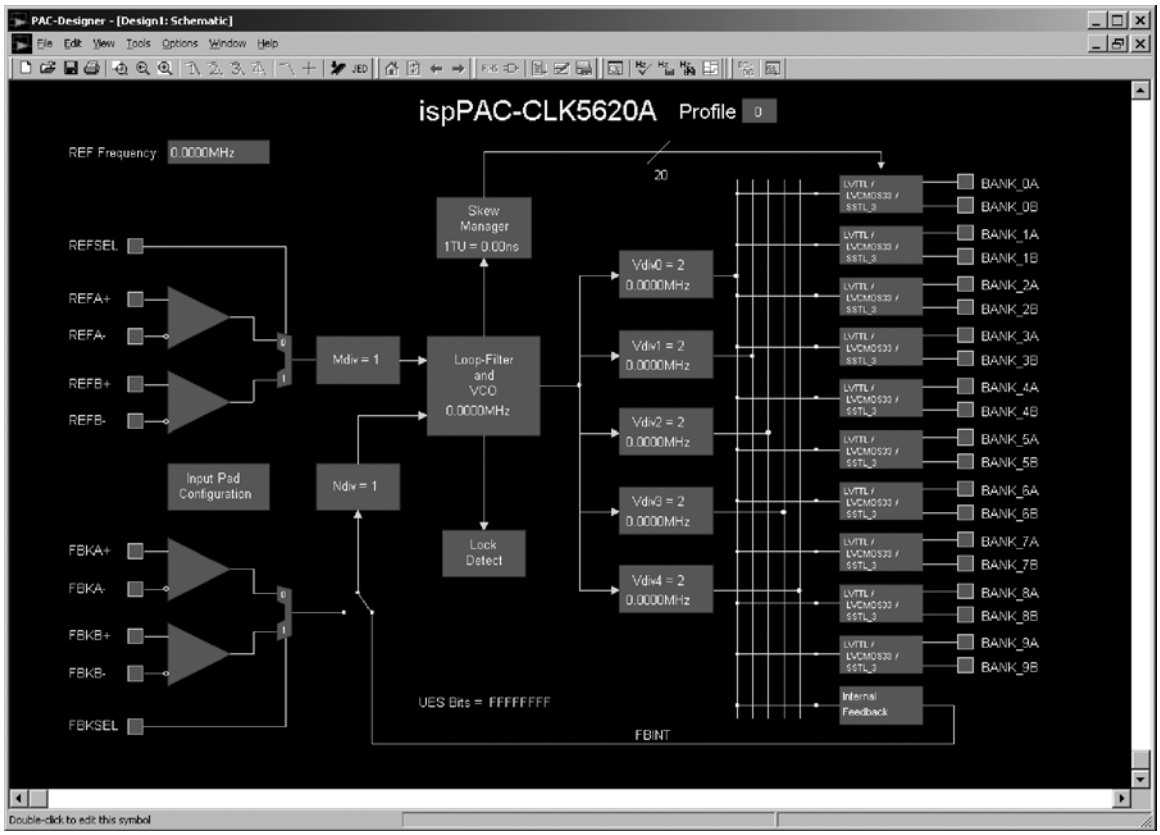
The examples above used LVCMOS 3.3V logic, which represents the maximum power dissipation case at higher frequencies. For optimal operation at very high frequencies (> 150 MHz) LVDS/LVPECL will often be the best choice from a signal integrity standpoint. For LVDS-configured outputs, the maximum ICCO current consumption per bank is low enough that both the ispClock5610A and ispClock5620A can operate all outputs at maximum frequency over their complete rated temperature range, as shown in Figure 1-28c.

Note that because of variations in circuit board mounting, construction, and layout, as well as convective and forced airflow present in a given design, actual die operating temperature is subject to considerable variation from that which may be theoretically predicted from package characteristics and device power dissipation.

Software-Based Design Environment

Designers can configure the ispClock5600A using Lattice's PAC-Designer software, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispClock5600A. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation. PAC-Designer is available for download from the Lattice website at www.latticesemi.com. The PAC-Designer schematic window, shown in Figure 1-29 provides access to all configurable ispClock5600A elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved and downloaded to devices.

Figure 1-29. PAC-Designer Design Entry Screen



In-System Programming

The ispClock5600A is an In-System Programmable (ISP™) device. This is accomplished by integrating all E^2CMOS configuration control logic on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^2CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispClock5600A instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

A user electronic signature (UES) feature is included in the E^2CMOS memory of the ispClock5600A. This consists of 32 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Electronic Security

An electronic security “fuse” (ESF) bit is provided in every ispClock5600A device to prevent unauthorized readout of the E^2CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can not be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Production Programming Support

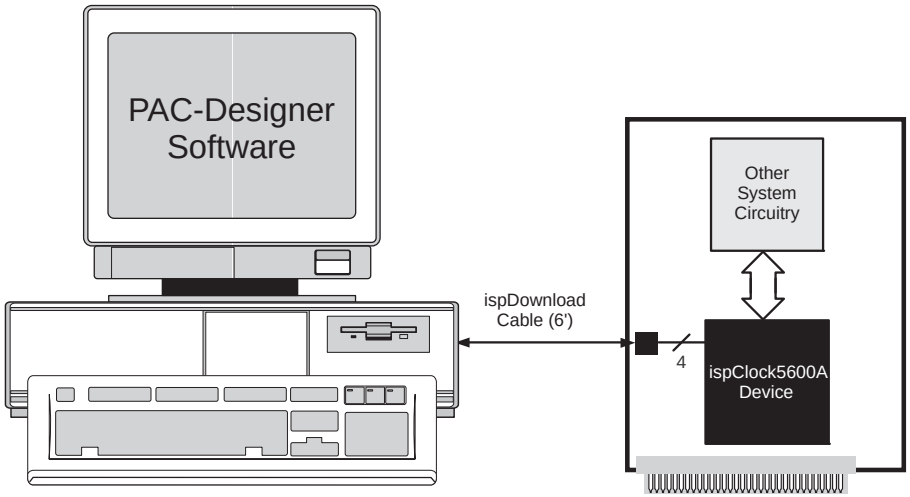
Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user’s specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

Evaluation Fixture

Included in the basic ispClock5600A Design Kit is an engineering prototype board that can be connected to the parallel port of a PC using a Lattice ispDOWNLOAD® cable. It demonstrates proper layout techniques for the ispClock5600A and can be used in real time to check circuit operation as part of the design process. Input and output connections (SMA connectors for all RF signals) are provided to aid in the evaluation of the ispClock5600A for a given application. (Figure 1-30).

Part Number	Description
PAC-SYSTEMCLK5620A	Complete system kit, evaluation board, ispDOWNLOAD cable and software.
PACCLK5620A-EV	Evaluation board only, with components, fully assembled.

Figure 1-30. Download from a PC



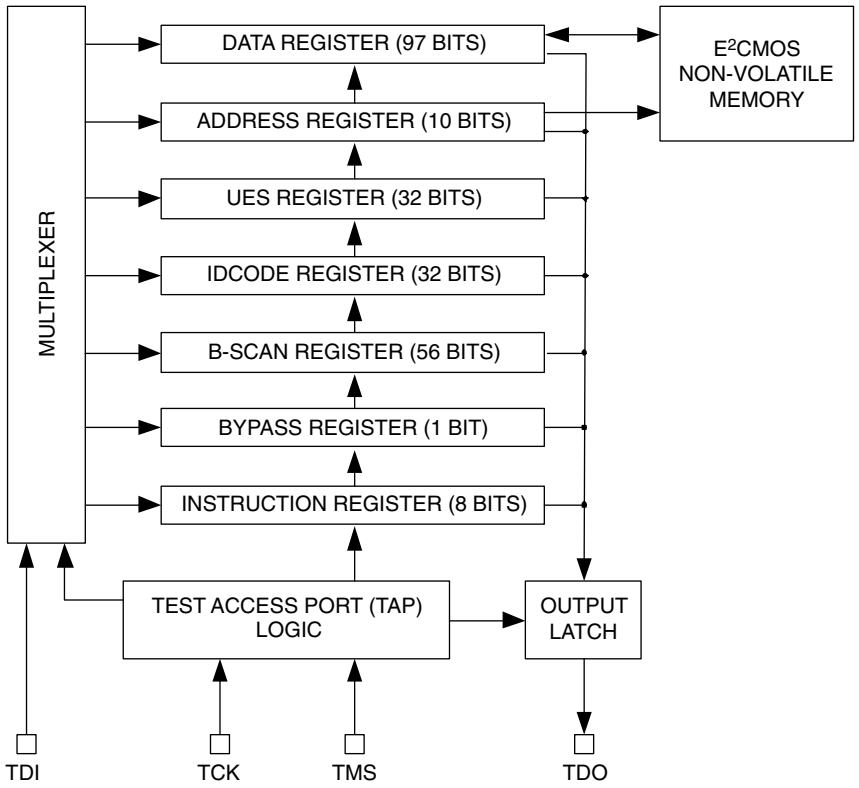
IEEE Standard 1149.1 Interface (JTAG)

Serial Port Programming Interface Communication with the ispClock5600A is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispClock5600A both as a serial programming interface, and for boundary scan test purposes. A brief description of the ispClock5600A JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990 (which now includes IEEE Std. 1149.1a-1993).

Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispClock5600A. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E^2CMOS cells. It is these non-volatile cells that store the configuration of the ispClock5600A. A set of instructions are defined that access all data registers and perform other internal control operations. For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. Figure 1-31 shows how the instruction and various data registers are organized in an ispClock5600A.

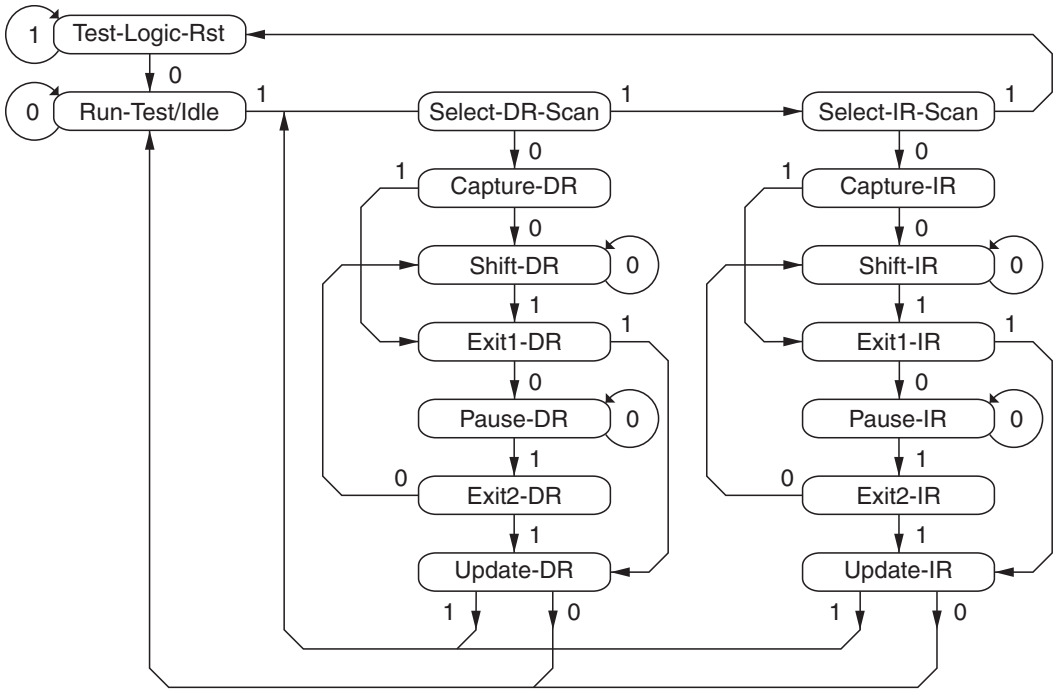
Figure 1-31. ispClock5600A TAP Registers



TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the TMS input as shown in Figure 1-32. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run- Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

Figure 1-32. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain. From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispClock5600A contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified.

For ispClock5600A, the instruction word length is eight bits. All ispClock5600A instructions available to users are shown in Table 1-6.

The following table lists the instructions supported by the ispClock5600A JTAG Test Access Port (TAP) controller:

Table 1-6. ispClock5600A TAP Instruction Table

Instruction	Code	Description
EXTEST	0000 0000	External Test.
ADDRESS_SHIFT	0000 0001	Address register (10 bits)
DATA_SHIFT	0000 0010	Address column data register (89 bits)
BULK_ERASE	0000 0011	Bulk Erase
PROGRAM	0000 0111	Program column data register to E^2
PROGRAM_SECURITY	0000 1001	Program Electronic Security Fuse
VERIFY	0000 1010	Verify column
DISCHARGE	0001 0100	Fast VPP Discharge
PROGRAM_ENABLE	0001 0101	Enable Program Mode
IDCODE	0001 0110	Address Manufacturer ID code register (32 bits)
USERCODE	0001 0111	Read UES data from E^2 and addresses UES register (32 bits)
PROGRAM_USERCODE	0001 1010	Program UES register into E^2
PROGRAM_DISABLE	0001 1110	Disable Program Mode
HIGHZ	0001 1000	Force all outputs to High-Z state
SAMPLE/PRELOAD	0001 1100	Capture current state of pins to boundary scan register
CLAMP	0010 0000	Drive I/Os with boundary scan register
INTEST	0010 1100	Performs in-circuit functional testing of device.
ERASE DONE	0010 0100	Erases the ‘Done’ bit only
PROG_INCR	0010 0111	Program column data register to E^2 and auto-increment address register
VERIFY_INCR	0010 1010	Load column data register from E^2 and auto-increment address register
PROGRAM_DONE	0010 1111	Programs the ‘Done’ Bit
NOOP	0011 0000	Functions Similarly to CLAMP instruction
BYPASS	1xxx xxxx	Bypass - Connect TDO to TDI

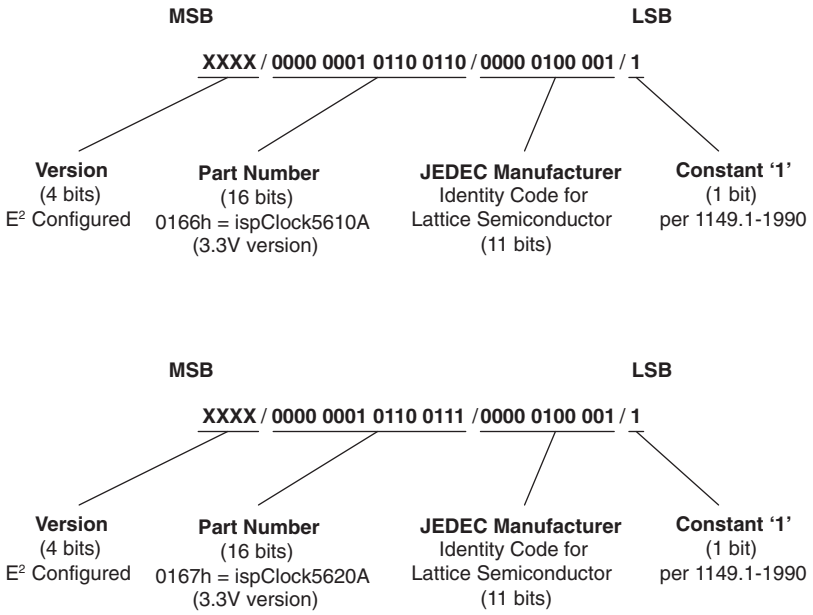
BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispClock5600A. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (111111).

The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The bit code for this instruction is defined by Lattice as shown in Table 1-6.

The **EXTEST** (external test) instruction is required and will place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispClock5600A and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device type and version code (Figure 1-33). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 1-6.

Figure 1-33. ispClock5600A Family ID Codes



In addition to the four instructions described above, there are 20 unique instructions specified by Lattice for the ispClock5600A. These instructions are primarily used to interface to the various user registers and the E^{2}CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device, including boundary scan operations. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 1-6.

PROGRAM_ENABLE – This instruction enables the ispClock5600A's programming mode.

PROGRAM_DISABLE – This instruction disables the ispClock5600A's programming mode.

BULK_ERASE – This instruction will erase all E^{2}CMOS bits in the device, including the UES data and electronic security fuse (ESF). A bulk erase instruction must be issued before reprogramming a device. The device must already be in programming mode for this instruction to execute.

ADDRESS_SHIFT – This instruction shifts address data into the address register (10 bits) in preparation for either a PROGRAM or VERIFY instruction.

DATA_SHIFT – This instruction shifts data into or out of the data register (90 bits), and is used with both the PROGRAM and VERIFY instructions.

PROGRAM – This instruction programs the contents of the data register to the E^{2}CMOS memory column pointed to by the address register. The device must already be in programming mode for this instruction to execute.

PROG_INCR – This instruction first programs the contents of the data register into E^{2}CMOS memory column pointed to by the address register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

PROGRAM_SECURITY – This instruction programs the electronic security fuse (ESF). This prevents data other than the ID code and UES strings from being read from the device. The electronic security fuse may only be reset by issuing a BULK_ERASE command. The device must already be in programming mode for this instruction to execute.

VERIFY – This instruction loads data from the E^{2}CMOS array into the column register. The data may then be shifted out. The device must already be in programming mode for this instruction to execute.

VERIFY_INCR – This instruction copies the E^2CMOS column pointed to by the address register into the data column register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispClock5600A for a read cycle.

PROGRAM_USERCODE – This instruction writes the contents of the UES register (32 bits) into E^2CMOS memory. The device must already be in programming mode for this instruction to execute.

USERCODE – This instruction both reads the UES string (32 bits) from E^2CMOS memory into the UES register and addresses the UES register so that this data may be shifted in and out.

HIGHZ – This instruction forces all outputs into a High-Z state.

CLAMP – This instruction drives I/O pins with the contents of the boundary scan register.

INTEST – This instruction performs in-circuit functional testing of the device.

ERASE_DONE – This instruction erases the 'DONE' bit only. This instruction is used to disable normal operation of the device while in programming mode until a valid configuration pattern has been programmed.

PROGRAM_DONE – This instruction programs the 'DONE' bit only. This instruction is used to enable normal device operation after programming is complete.

NOOP – This instruction behaves similarly to the CLAMP instruction.

Pin Descriptions

Pin Name	Description	Pin Type	Pin Number	
			ispClock5610A 48 TQFP	ispClock5620A 100 TQFP
VCCO_0	Output Driver ‘0’ VCC	Power	1	3
VCCO_1	Output Driver ‘1’ VCC	Power	5	7
VCCO_2	Output Driver ‘2’ VCC	Power	9	11
VCCO_3	Output Driver ‘3’ VCC	Power	25	15
VCCO_4	Output Driver ‘4’ VCC	Power	29	19
VCCO_5	Output Driver ‘5’ VCC	Power	—	51
VCCO_6	Output Driver ‘6’ VCC	Power	—	55
VCCO_7	Output Driver ‘7’ VCC	Power	—	59
VCCO_8	Output Driver ‘8’ VCC	Power	—	63
VCCO_9	Output Driver ‘9’ VCC	Power	—	67
GNDO_0	Output Driver ‘0’ Ground	GND	4	6
GNDO_1	Output Driver ‘1’ Ground	GND	8	10
GNDO_2	Output Driver ‘2’ Ground	GND	12	14
GNDO_3	Output Driver ‘3’ Ground	GND	28	18
GNDO_4	Output Driver ‘4’ Ground	GND	32	22
GNDO_5	Output Driver ‘5’ Ground	GND	—	54
GNDO_6	Output Driver ‘6’ Ground	GND	—	58
GNDO_7	Output Driver ‘7’ Ground	GND	—	62
GNDO_8	Output Driver ‘8’ Ground	GND	—	66
GNDO_9	Output Driver ‘9’ Ground	GND	—	70
BANK_0A	Clock Output driver 0, ‘A’ output	Output	3	5
BANK_0B	Clock Output driver 0, ‘B’ output	Output	2	4
BANK_1A	Clock Output driver 1, ‘A’ output	Output	7	9
BANK_1B	Clock Output driver 1, ‘B’ output	Output	6	8
BANK_2A	Clock Output driver 2, ‘A’ output	Output	11	13
BANK_2B	Clock Output driver 2, ‘B’ output	Output	10	12
BANK_3A	Clock Output driver 3, ‘A’ output	Output	27	17
BANK_3B	Clock Output driver 3, ‘B’ output	Output	26	16
BANK_4A	Clock Output driver 4, ‘A’ output	Output	31	21
BANK_4B	Clock Output driver 4, ‘B’ output	Output	30	20
BANK_5A	Clock Output driver 5, ‘A’ output	Output	—	53
BANK_5B	Clock Output driver 5, ‘B’ output	Output	—	52
BANK_6A	Clock Output driver 6, ‘A’ output	Output	—	57
BANK_6B	Clock Output driver 6, ‘B’ output	Output	—	56
BANK_7A	Clock Output driver 7, ‘A’ output	Output	—	61
BANK_7B	Clock Output driver 7, ‘B’ output	Output	—	60
BANK_8A	Clock Output driver 8, ‘A’ output	Output	—	65
BANK_8B	Clock Output driver 8, ‘B’ output	Output	—	64
BANK_9A	Clock Output driver 9, ‘A’ output	Output	—	69
BANK_9B	Clock Output driver 9, ‘B’ output	Output	—	68
VCCA	Analog VCC for PLL circuitry	Power	13	30
GNDA	Analog Ground for PLL circuitry	GND	14	31

Pin Descriptions (Continued)

Pin Name	Description	Pin Type	Pin Number	
			ispClock5610A 48 TQFP	ispClock5620A 100 TQFP
VCCD	Digital Core VCC	Power	24, 33	47, 71
GNDD	Digital GND	GND	23, 48	46, 93
VCCJ	JTAG interface VCC	Power	36	74
REFA+	Clock Reference A positive input[3]	Input	18	38
REFA-	Clock Reference A negative input[3]	Input	19	39
REFB+	Clock Reference B positive input[3]	Input	—	42
REFB-	Clock Reference B negative input[3]	Input	—	41
REFSEL	Clock Reference Select input (LVCMOS)	Input[1]	—	43
REFVTT	Termination voltage for reference inputs	Power	20	40
FBKA+	Clock feedback A positive input [3]	Input	15	32
FBKA-	Clock feedback A negative input[3]	Input	16	33
FBKB+	Clock feedback B positive input[3]	Input	—	36
FBKB-	Clock feedback B negative input[3]	Input	—	35
FBKSEL	Clock feedback select input (LVCMOS)	Input[1]	—	37
FBKVTT	Termination voltage for feedback inputs	Power	17	34
TDO	JTAG TDO Output line	Output	35	73
TDI	JTAG TDI Input line	Input[2]	39	84
TCK	JTAG Clock Input	Input	38	83
TMS	JTAG Mode Select	Input[2]	37	82
$\overline{\text{LOCK}}$	PLL Lock indicator, LOW indicates PLL lock	Output	34	72
SGATE	Synchronous output gate	Input[1]	40	85
$\overline{\text{GOE}}$	Global Output Enable	Input[1]	42	87
$\overline{\text{OEX}}$	Output Enable 1	Input[1]	21	44
$\overline{\text{OEY}}$	Output Enable 2	Input[1]	22	45
PS0	Profile Select 0	Input[1]	44	89
PS1	Profile Select 1	Input[1]	43	88
PLL_BYPASS	PLL Bypass	Input[1]	47	92
RESET	Reset PLL	Input[1]	41	86
TEST1	Test Input 1 - connect to GNDD	Input	46	91
TEST2	Test Input 2 - connect to GNDD	Input	45	90
n/c	No internal connection	n/a	—	1, 2, 23, 24, 25, 26, 27, 28, 29, 48, 49, 50, 75, 76, 77, 78, 79, 94, 97, 98, 99, 100
Reserved	Factory use only - Do not connect	n/a	—	80, 81, 95, 96

1. Internal pull-down resistor.
2. Internal pull-up resistor.
3. Must be connected to GNDD if this pin is not used.

Detailed Pin Descriptions

VCCO_[0..9], GNDO_[0..9] – These pins provide power and ground for each of the output banks. In the case when an output bank is unused, its corresponding VCCO pin may be left unconnected or preferably should be tied to ground. ALL GNDO pins should be tied to ground regardless of whether the associated bank is used or not. When a bank is used, it should be individually bypassed with a capacitor in the range of 0.01 to 0.1µF as close to its VCCO and GNDO pins as is practical.

BANK_[0..9]A, BANK_[0..9]B – These pins provide clock output signals. The choice of output divider (V0-V4) and output driver type (CMOS, LVDS, SSTL, etc.) may be selected on a bank-by-bank basis. When the outputs are configured as pairs of single-ended outputs, output impedance and slew rate may be selected on an output-by-output basis.

VCCA, GNDA – These pins provide analog supply and ground for the ispClock5600A family's internal analog circuitry, and should be bypassed with a 0.1µF capacitor as close to the pins as is practical. To improve noise immunity, it is suggested that the supply to the VCCA pin be isolated from other circuitry with a ferrite bead.

VCCD, GNDD – These pins provide digital supply and ground for the ispClock5600A family's internal digital circuitry, and should be bypassed with a 0.1µF capacitor as close to the pins as is practical. to improve noise immunity it is suggested that the supply to the VCCD pins be isolated with ferrite beads.

VCCJ – This pin provides power and a reference voltage for use by the JTAG interface circuitry. It may be set to allow the ispClock5600A family devices to function in JTAG chains operating at voltages differing from VCCD.

REFA+, REFA-, REFB+, REFB- – These input pins provide the inputs for clock signals, and can accommodate either single ended or differential signal protocols by using either just the '+' pins, or both the '+' and '-' pins. Two sets of inputs are provided to accommodate the use of different signal sources and redundant clock sources.

REFSEL – This input pin is used to select which clock input pair (REFA+/- or REB+/-) is selected for use as the reference input. When REFSEL=0, REFA+/- is used, and when REFSEL=1, REFB+/- is used.

REFVTT – This pin is used to provide a termination voltage for the reference inputs when they are configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases.

FBKA+, FBKA-, FBKB+, FBKB- – These input pins provide the inputs for feedback sense of output clock signals, and can accommodate either single ended or differential signal protocols by using either just the '+' pins, or both the '+' and '-' pins. Two sets of inputs are provided to accommodate the use of alternate feedback signal sources.

FBKSEL – This input pin is used to select which clock input pair (FBKA+/- or FBK+/-) is selected for use as the feedback input. When FBKSEL=0, FBKA+/- is used, and when FBKSEL=1, FBKB+/- is used.

FBKVTT – This pin is used to provide a termination voltage for the feedback inputs when they are configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases.

TDO, TDI, TCK, TMS – These pins comprise the ispClock5600A device's JTAG interface. The signal levels for these pins are determined by the selection of the VCCJ voltage.

$\overline{\text{LOCK}}$ – This output pin indicates that the device's PLL is in a locked condition when it goes low.

SGATE – This input pin provides a synchronous gating function for the outputs, which may be enabled on a bank-by-bank basis. When the synchronous gating function is enabled for a given bank, that bank's outputs will output a clock signal when the SGATE pin is HIGH, and will drive a constant HIGH or LOW when the SGATE pin is LOW. Synchronous gating ensures that when the state of SGATE is changed, no partial clock pulses will appear at the outputs.

$\overline{\text{OEX}}$, $\overline{\text{OEY}}$ – These pins are used to enable the outputs or put them into a high-impedance condition. Each output may be set so that it is always on, always off, enabled by $\overline{\text{OEX}}$ or enabled by $\overline{\text{OEY}}$.

$\overline{\text{GOE}}$ – Global output enable. This pin drives all outputs to a high-impedance state when it is pulled HIGH. $\overline{\text{GOE}}$ also controls the internal feedback buffer, so that bringing $\overline{\text{GOE}}$ high will cause the PLL to lose lock.

PS0, PS1 – These input pins are used to select one of four user-defined configuration profiles for the device.

PLL_BYPASS – When this pin is pulled LOW, the V-dividers are driven from the output of the device's VCO, and the device behaves as a phase-locked loop. When this pin is pulled HIGH, the V-dividers are driven directly from the output of the M-divider, and the PLL functions are effectively bypassed.

RESET – When this pin is pulled HIGH, all on-board counters are reset, and lock is lost.

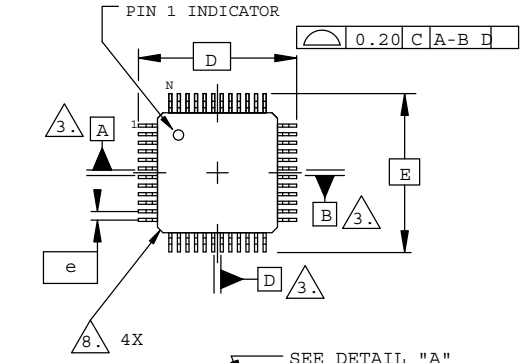
TEST1,TEST2 – These pins are used for factory test functions, and should always be tied to ground.

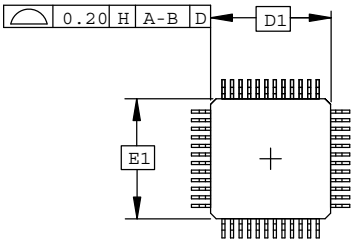
n/c – These pins have no internal connection. We recommend that they be left unconnected.

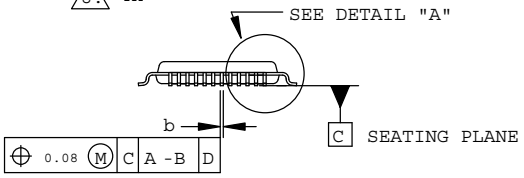
RESERVED – These pins are reserved for factory use and should be left unconnected.

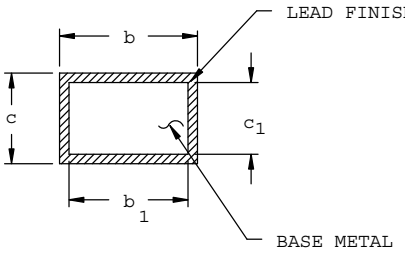
Package Diagrams

48-Pin TQFP (Dimensions in Millimeters)

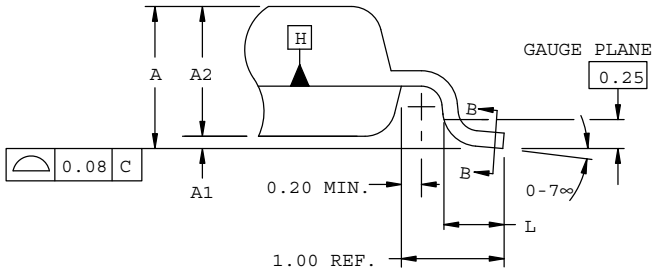








SECTION B - B



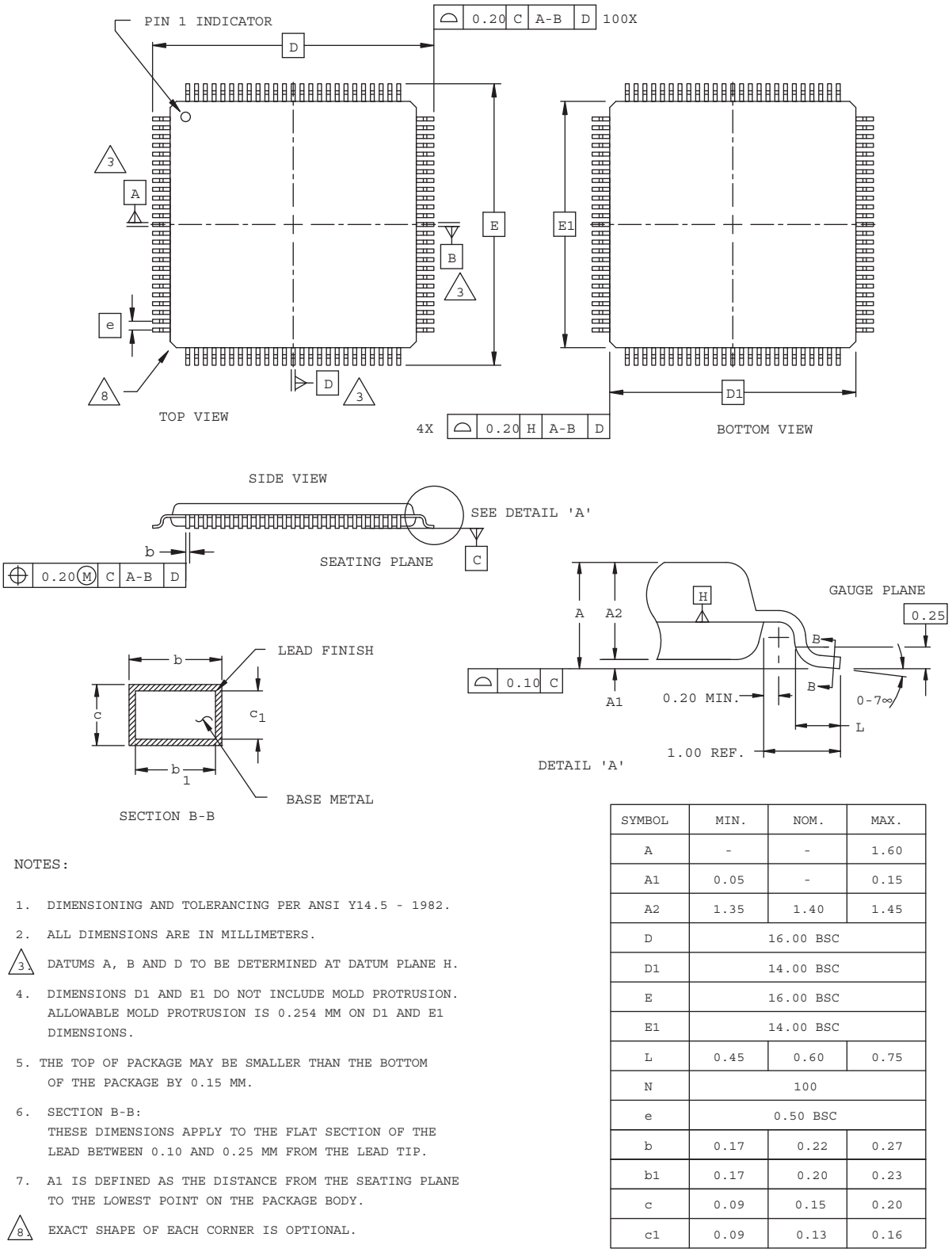
DETAIL "A"

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
5. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MM.
6. SECTION B-B: THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.
7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		9.00 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
N		48	
e		0.50 BSC	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.13	0.16

100-Pin TQFP (Dimensions in Millimeters)



SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		16.00 BSC	
D1		14.00 BSC	
E		16.00 BSC	
E1		14.00 BSC	
L	0.45	0.60	0.75
N		100	
e		0.50 BSC	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.13	0.16

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
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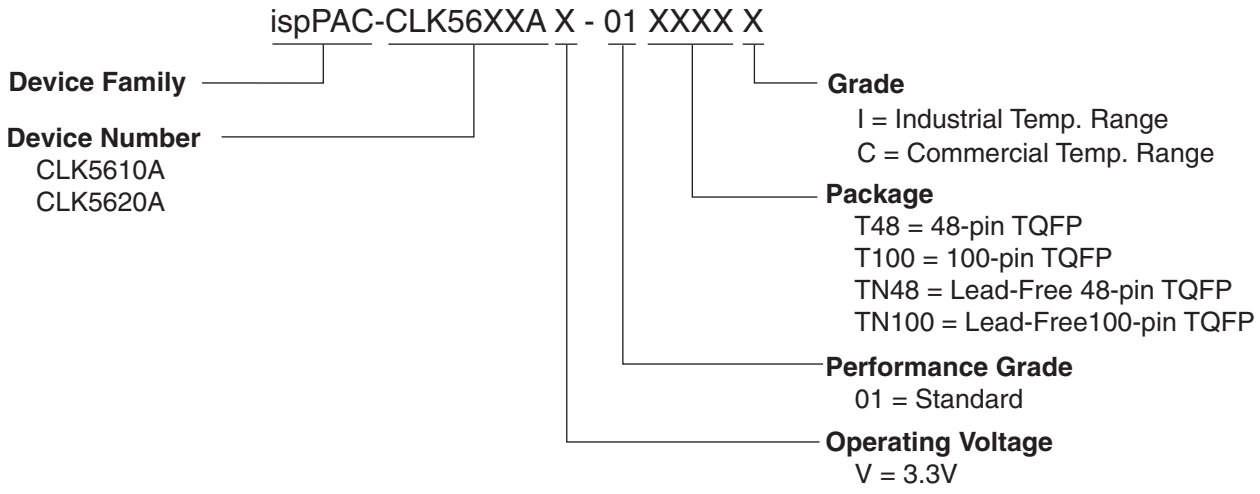
7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Part Number Description



Ordering Information

Conventional Packaging

Commercial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5610AV-01T48C	10	3.3V	TQFP	48
ispPAC-CLK5620AV-01T100C	20	3.3V	TQFP	100

Industrial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5610AV-01T48I	10	3.3V	TQFP	48
ispPAC-CLK5620AV-01T100I	20	3.3V	TQFP	100

Lead-Free Packaging

Commercial

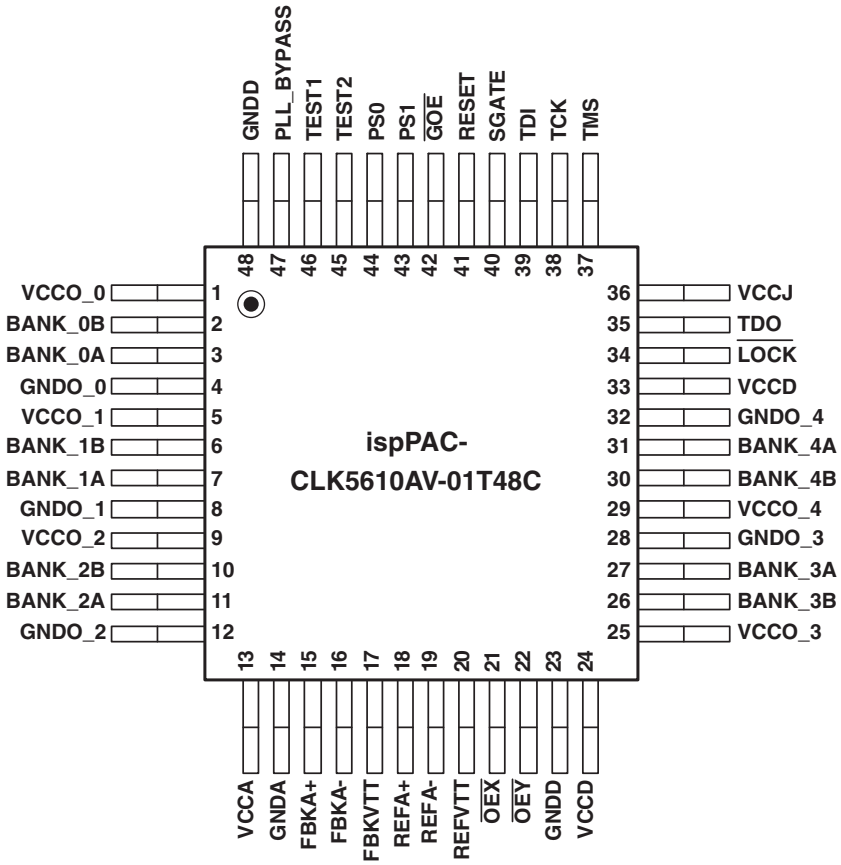
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5610AV-01TN48C	10	3.3V	Lead-Free TQFP	48
ispPAC-CLK5620AV-01TN100C	20	3.3V	Lead-Free TQFP	100

Industrial

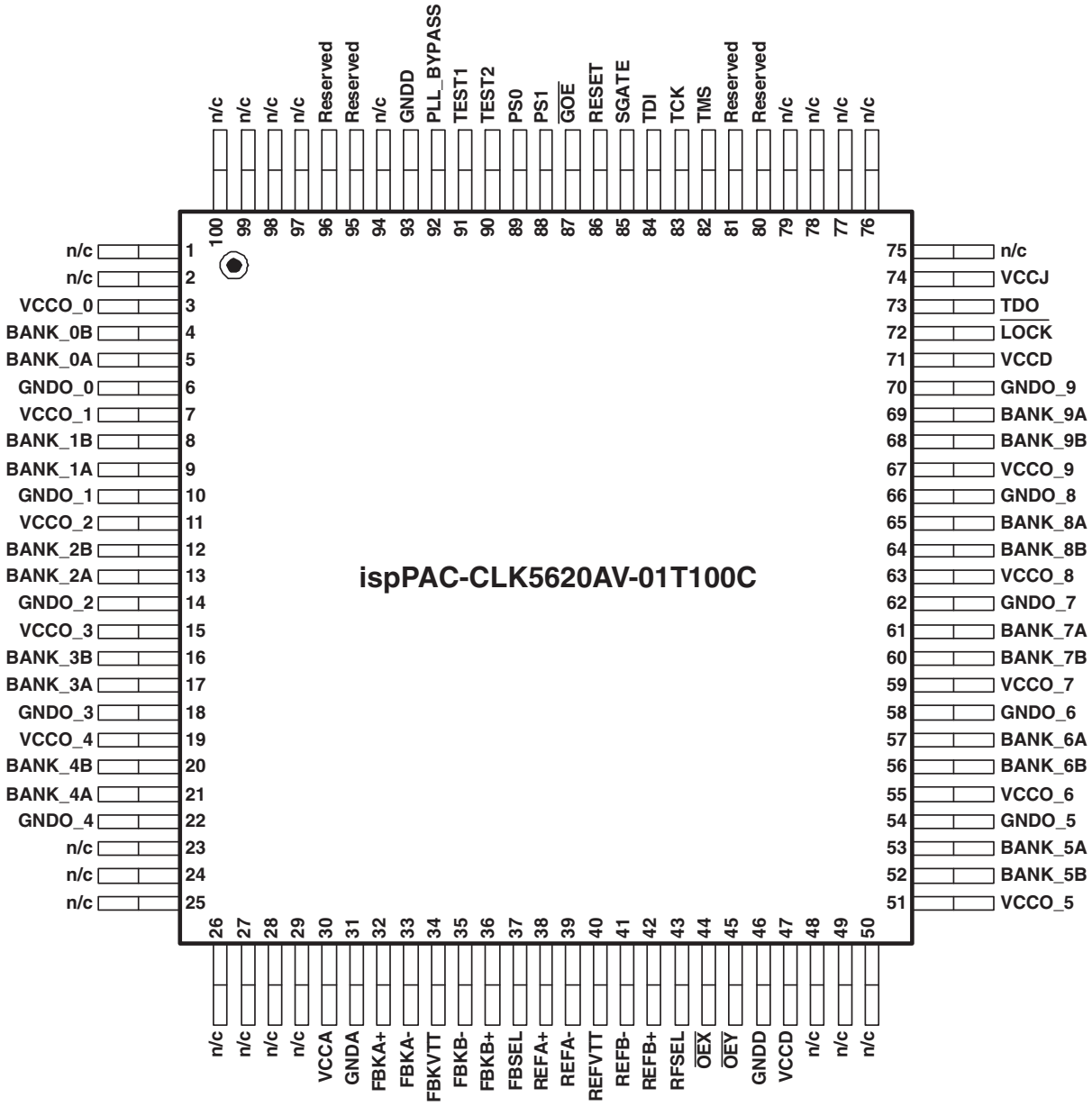
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5610AV-01TN48I	10	3.3V	Lead-Free TQFP	48
ispPAC-CLK5620AV-01TN100I	20	3.3V	Lead-Free TQFP	100

Package Options

ispClock5610A: 48-pin TQFP



ispClock5620A: 100-pin TQFP



Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
March 2007	01.3	Added min. and max. values to Timing Adders for I/O Modes table.
		Added min. and max. values to PLL Bypass Mode operation table.
		Added Phase Lock Detect feature description.
		Added M-Divider and N-Divider Bypass feature description.
		Modified logic standard related timing adder values in the Output Skew Matching Accuracy section and the Static Phase Offset and I/O Skew section.
		PFD frequency limitation for the Static Phase Offset specification is removed.
		Minimum operating voltage for V_{CCJ} is set to 2.25V.
		Updated the I_{CCD} vs. F_{VCO} graph to include 800 MHz VCO frequency operation.
June 2008	01.4	Restructured / reordered sections under "Detailed Description" and "Thermal Management"
		Added a paragraph describing RESET in the "M-Divider and N-Divider Bypass Mode" section.
		Clairified the need for resetting ispClock in the “RESET and Power-up Functions” section.

ispClock™ 5400D Family

In-System Programmable, Ultra-Low Jitter Zero Delay and Fan-Out Buffer, Differential

November 2009 Preliminary Data Sheet DS1025

Features

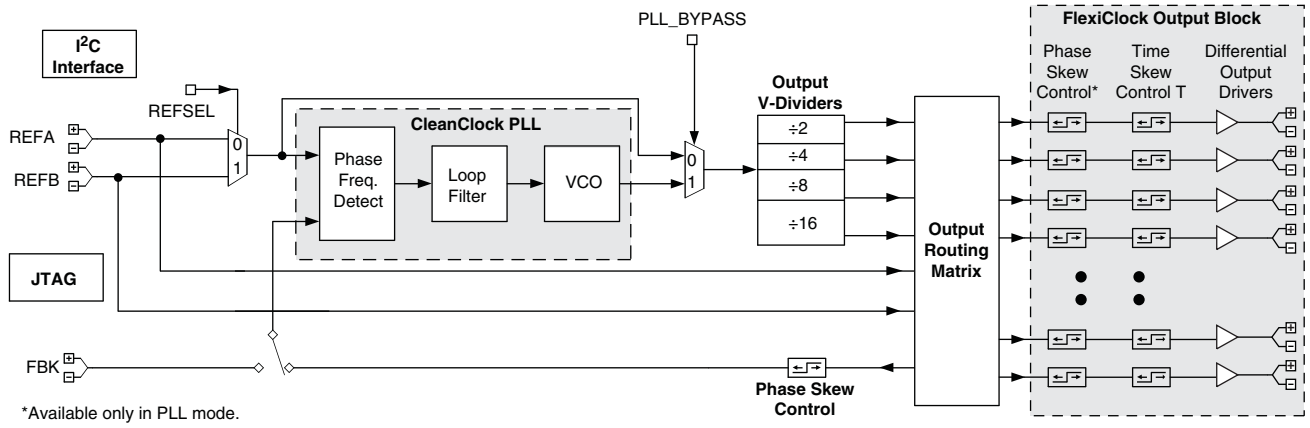
CleanClock™ PLL

- **Ultra Low Period Jitter 2.5ps**
- **Ultra Low Phase Jitter 6.5ps**
- **Fully Integrated High-Performance PLL**
  - Programmable lock detect
  - Four output dividers
  - Programmable on-chip loop filter
  - Compatible with Spread Spectrum clocks
  - Internal/external feedback
- **Flexible Clock Reference and External Feedback Inputs**
  - Programmable differential input reference/feedback standards
    - LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS
  - Programmable termination
  - Clock A/B selection multiplexer

FlexiClock™ I/O

- **40 MHz to 400 MHz Input/Output Operation**
- **Dual Programmable Skew Per Output**
  - Programmable phase adjustment
    - 16 settings; minimum step size 156 ps
    - Up to +/- 9.4 ns skew range
    - Coarse and fine adjustment modes
  - Programmable time delay adjustment
    - 16 settings; 18 ps
- **Dynamic Skew Control Through I^2C**
- **Low Output-to-Output Skew (<100ps)**
- **Up to 10 Programmable Fan-out Buffers**
  - Programmable differential output standards and individual enable controls
    - LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS
  - Up to 10 banks with individual VCCO and GND
    - 1.5V, 1.8V, 2.5V, 3.3V
- **All I/Os are Hot Socket Compliant**
- **Operating Modes**
  - Fan-out buffer with programmable output skew control
  - Zero delay buffer with dual programmable skew controls
- **Dynamic Reconfiguration through I^2C**
- **Full JTAG Boundary Scan Test In-System Programming Support**
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0° to 70°C) and Industrial (-40° to 85°C) Temperature Ranges**
- **48-Pin and 64-pin QFNS Packages**
- **Applications**
  - Low-cost clock source for SERDES
  - ATCA, MicroTCA, AMC, PCI Express
  - Differential Clock Distribution
  - Generic Source Synchronous Clock Management
  - Zero-delay clock buffer

ispClock5400D Family Functional Diagram



General Description

The ispClock5400D family integrates a CleanClock PLL and a FlexiClock Output block. The CleanClock PLL provides an ultra-low-jitter clock source to a set of four V-dividers. The FlexiClock output block receives the clock output from these V-dividers through an output switch matrix and distributes them to the output pin using a programmable logic interface. There are two members in the ispClock5400D family, the ispClock5410D (10-output FlexiCLock block) and the ispClock5406D (6-output FlexiClock block). Each of the outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, SSTL, HSTL, MLVDS, HCSL) and output frequency. In addition, the skew of each of the outputs can be independently controlled. All configuration information is stored on-chip in non-volatile E^2CMOS® memory.

The ispClock5400D devices provide extremely low propagation delay (zero-delay) from input to output using the CleanClock PLL. The PLL VCO output clock frequency is divided down by a set of four V- dividers. The output frequencies from these V-dividers, $f_{VCO} \div 2$, $f_{VCO} \div 4$, $f_{VCO} \div 8$ and $f_{VCO} \div 16$ are connected to the output routing matrix. The output routing matrix enables any output pin to derive its clock from any of the V-dividers outputs. Additionally, the reference input clock can be connected directly to any output through the output routing matrix.

The FlexiClock block supports dual skew mechanisms: Phase Skew Control and Time Skew Control. These skew control mechanisms enable fixed output clock skew control during power-up and variable skew during operation.

The ispClock5400D device can be configured to operate in four modes: zero delay buffer mode, dual non-zero delay buffer mode, non-zero delay buffer mode with output dividers, and combined zero-delay and non-zero delay buffer mode.

The I^2C interface can be used to dynamically control the ispClock5400D configuration: Output clock frequency, Phase Skew, Time skew, Fan-out buffer mode, Output enable.

The core functions of both members of the ispClock5400D family are identical. Table 2-1 summarizes the ispClock5400D device family.

Table 2-1. ispClock5400D Family

Device	Number of Programmable Differential Clock Inputs	Number of Programmable Differential Outputs
ispClock5410D	2	10
ispClock5406D	2	6

Figure 2-1. ispClock5410D Functional Block Diagram

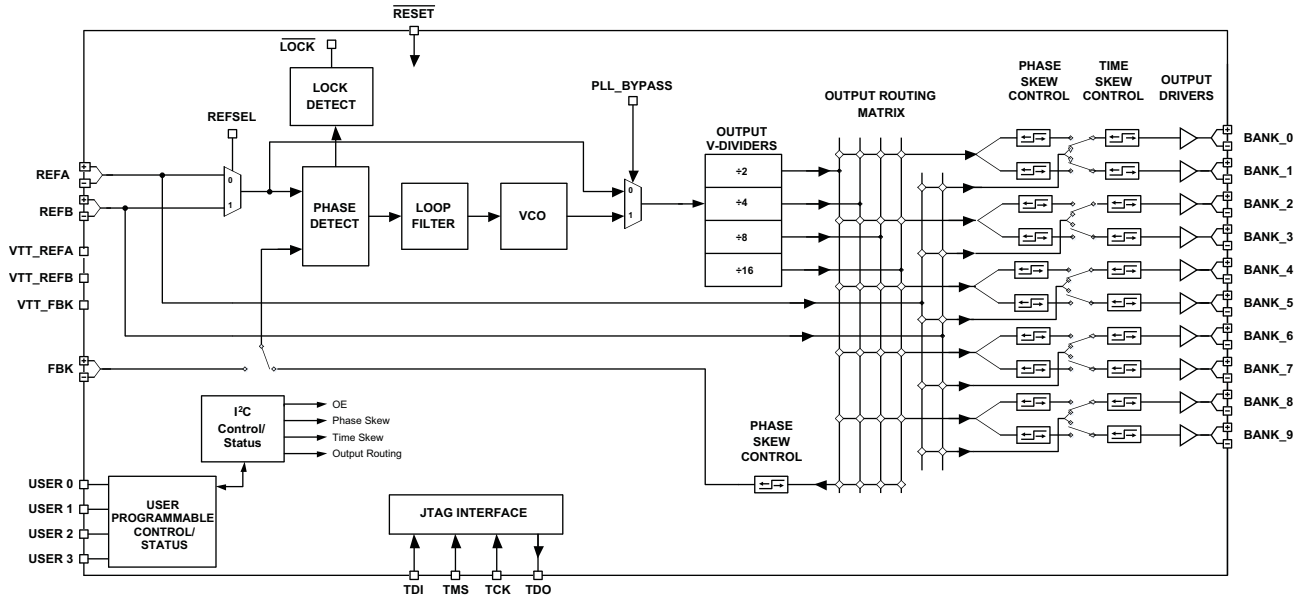
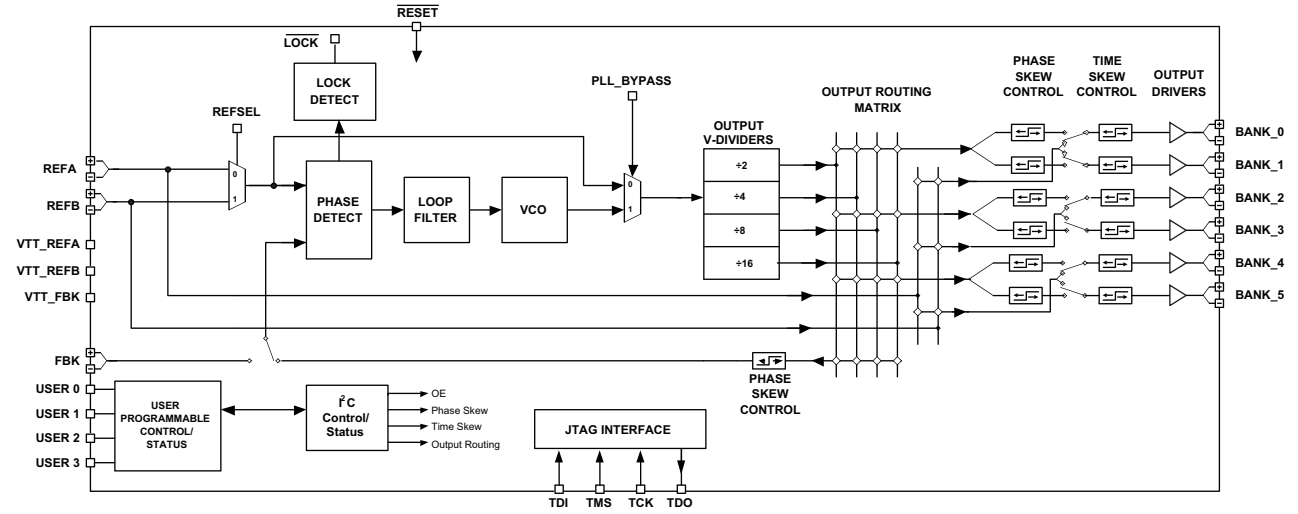


Figure 2-2. ispClock5406D Functional Block Diagram



Absolute Maximum Ratings

	ispClock5400D
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 125°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		2.25	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	V_{CC} Turn-on Ramp Rate	All supply pins	—	0.33	V/µs
T_{JCOM}	Junction Temperature	Commercial	0	85	°C
T_{JIND}		Industrial	-40	100	

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard	V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
HCSL	3.135	3.3	3.465						
SSTL15	1.425	1.5	1.575	0.7	0.75	0.8		0.5 x V_{CCO}	
SSTL18	1.7	1.8	1.9	0.84	0.9	0.95		0.5 x V_{CCO}	
SSTL2 Class 1	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
HSTL Class 1	1.4	1.5	1.6	0.68	0.75	0.9		0.5 x V_{CCO}	
eHSTL Class 1	1.65	1.8	1.95	0.84	0.9	0.95		0.5 x V_{CCO}	
LVPECL	2.97	3.3	3.63						
LVDS25	2.25	2.5	2.75						
LVDS33	2.97	3.3	3.63						
MLVDS	2.25	2.5	2.75						

ESD Performance

Pin Group	ESD Stress	Min.	Units
All pins	HBM	2000	V
	CDM	1000	V

E²CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max	Units
I_{CCD}	Core Supply Current[1]	f_{VCO} = 800MHz, Internal Feedback	94	99	mA
		PLL Bypassed	65	71	mA
$I_{CCDADDER}$	Incremental ICCD Per Active Output	f_{OUT} = 400 MHz	2.8	3.2	mA
$I_{CCDADDER-TSK}$	Incremental ICCD for the First T-Skew Block		4.0	4.9	mA
$I_{CCDADDER-HCSL}$	Incremental ICCD For the First HCSL Output		4.0	5.2	mA
$I_{CCDADDER-REFB}$	Incremental ICCD Due to Active REFB INPUT	F_{IN} = 400 MHz	6.0	10	mA
I_{CCA}	Analog Supply Current[1]	f_{VCO} = 800MHz, Internal Feedback	23	30	mA
I_{CCO}	Output Driver Supply Current	Output Logic Standard = SSTL15, f_{OUT} = 400MHz	21	22	mA
		Output Logic Standard = SSTL18 f_{OUT} = 333MHz	24	27	mA
		Output Logic Standard = SSTL2 f_{OUT} = 267MHz	34	37	mA
		Output Logic Standard = HSTL f_{OUT} = 333MHz	19	21	mA
		Output Logic Standard = eHSTL f_{OUT} = 333MHz	19	21	mA
		Output Logic Standard = LVPECL f_{OUT} = 400MHz	20	22	mA
		Output Logic Standard = LVDS33 f_{OUT} = 400MHz	10	11	mA
		LVDS25 f_{OUT} = 400MHz	8	9	mA
		Output Logic Standard = MLVDS f_{OUT} = 266MHz	16	19	mA
		Output Logic Standard = HCSL[2] f_{OUT} = 150MHz	22	24	mA
I_{CCJ}	JTAG I/O Supply Current (Static)	V_{CCJ} = 2.5V	350	500	µA
		V_{CCJ} = 3.3V	350	500	µA

1. All unused REFCLK and FBK pins grounded. Fin = 50 MHz, internal feedback.
2. 6x HCSL current setting.

DC Electrical Characteristics – Single-Ended Logic for USER, RESET and JTAG Pins

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	4	-4
LVCMOS 1.8V[1]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	4	-4
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	4	-4
User I/O in I²C Mode	-0.3	0.3 x V_{CCD}	0.7 x V_{CCD}	3.6V	0.4	V_{CCD} - 0.4	8	—

1. User and reset pins only.

Differential Input Characteristics (Applicable to REFA, REFB, FBK)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage - LVDS		0.1	—	2.35	V
V_{THD}	Differential Input Threshold - LVDS	100mV < V_{ICM} < 300mV	±100	—	—	mV
		300mV <V_{ICM} < 2.35V	±50	—	—	mV
V_{IX}	Input Pair Differential Crosspoint Voltage	SSTL15, SSTL18, HSTL, eHSTL, LVPECL, HCSL	0.3		2.35	V

Output Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	R_T = 100Ω	—	1.375	1.6	V
V_{OL}	Output Low Voltage	R_T = 100Ω	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	R_T = 100Ω	250	400	450	mV
ΔV_{OD}	Change in V_{OD} Between H and L		—	—	50	mV
V_{OS}	Output Voltage Offset	Common Mode Output Voltage	1.1	1.2	1.375	V
ΔV_{OS}	Change in V_{OD} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to GND, LVDS25	—	—	24	mA
		V_{OD} = 0V, Outputs Shorted to GND, LVDS33			35	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to Each Other	—	—	5	mA
DC_{CKOUT}	Output Clock Duty Cycle		48		52	%
DC-ERROR	Error in Duty Cycle[1]	LVDS25 (Figure 2-3)	-50		50	ps
		LVDS33 (Figure 2-3)	-65		65	ps
t_{RF}	Rise and Fall Time[1]	LVDS25 (Figure 2-3)	250		550	ps
		LVDS33 (Figure 2-3)	260		400	ps

1. Measured at f_{OUT} = 400 MHz.

Output Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage[1]	V_{CCO} = 3.0V to 3.6V	V_{CCO} - 1.1	—	V_{CCO} - 0.88	V
		V_{CCO} = 3.3V	2.20	—	2.42	V
V_{OL}	Output Low Voltage[1]	V_{CCO} = 3.0V to 3.6V	V_{CCO} - 1.86	—	V_{CCO} - 1.62	V
		V_{CCO} = 3.3V	1.44	—	1.68	V
V_{OD}	Output Voltage Differential		0.6	—	1	V
DC_{CKOUT}	Output Clock Duty Cycle[2]	Figure 2-3	47		53	%
t_{RF}	Rise and Fall Time[2]	Figure 2-3	300		400	ps

1. 100Ω differential termination.
2. Measured at f_{OUT} = 400 MHz.

Electrical Characteristics – Differential SSTL15

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	V_{CCO} = 1.425V (Test Circuit) I_{OH} = -8mA	V_{CCO} - 0.4			V
V_{OL}	Output Low Voltage	V_{CCO} = 1.425V (Test Circuit) I_{OL} = 8mA			0.4	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 2-6	$V_{CCO}/2$ - 0.1		$V_{CCO}/2$ + 0.1	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 2-6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 2-6	350		460	ps

1. Measured at f_{OUT} = 400 MHz.

Electrical Characteristics – Differential SSTL18

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -9mA, V_{CCO} = 1.7V	1.1			V
V_{OL}	Output Low Voltage	I_{OL} = 9mA, V_{CCO} =1.7V			0.6	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 2-6	$V_{CCO}/2$ - 0.05		$V_{CCO}/2$ + 0.2	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 2-6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 2-6	230		380	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – Differential SSTL2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{CCO} = 2.3V	1.74			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CCO} = 2.3V			0.56	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 2-6	V_{REF} - 200 mV		V_{REF} + 200 mV	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 2-6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 2-6	260		400	ps

1. Measured at f_{OUT} = 267 MHz.

Electrical Characteristics – Differential HSTL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8.1mA, V_{CCO} = 1.4V	V_{CCO} - 0.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.1mA, V_{CCO} =1.4V			0.4	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 2-5	$V_{CCO}/2$ - 0.1		$V_{CCO}/2$ + 0.1	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 2-5	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 2-5	300		460	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – Differential eHSTL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8.1mA, V_{CCO} = 1.65V	V_{CCO} - 0.45			V
V_{OL}	Output Low Voltage	I_{OL} = 8.1mA, V_{CCO} =1.65V			0.45	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 2-5	V_{CCO}/2 - 0.05		V_{CCO}/2 + 0.2	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 2-5	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 2-5	250		400	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – MLVDS

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage Magnitude	Figure 2-8b	480		650	mV
ΔV_{OD}	Change in Differential Output Voltage Magnitude Between Logic States	Figure 2-8b	-50		+50	mV
V_{OS}	Output Voltage Offset	Figure 2-8a	1		1.4	V
ΔV_{OS}	Change in V_{OS} Between H and L		-50		50	mV
V_{OC}	Output Open Circuit Steady State Voltage		0		2.4	V
I_{SAB}	Output Short Circuit Current, Outputs Shorted				24	mA
I_{SA}	Output Short Circuit Current	Figure 2-8c			43	mA
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 2-4	48		52	%
t_{RF}	Rise and Fall Time[1]	Figure 2-4	280		510	ps

1. Measured at f_{OUT} = 266 MHz.

Electrical Characteristics – HCSL

Symbol	Description	Conditions	Min.	Max.	Units
V_{OX}	Output Differential Pair Crosspoint Voltage	Crossing Point at Max. Swing of 0.7V	250	550	mV
ΔV_{OX}	V_{OX} Variation Across All Edges			140	mV
V_{OH}	Output High Voltage	Figure 2-7	1.3		V
t_R	Edge Rate Rising	Differential[1] (Figure 2-7)	0.6	4	V/ns
t_F	Edge Rate Falling	Differential[1] (Figure 2-7)	0.6	4	V/ns

1. Differential output signal, ±150mV from 0V crossing.

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	USER[3:0], Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	USER[3:0]	—	80	120	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	5	7	pF
		Note 1	—		8	pF

1. Applies to clock reference inputs and feedback inputs when termination ‘open’.
2. Applies to TDI, TDO, TMS and $\overline{\text{RESET}}$ inputs.
3. Applies to USER[0..3] pins.
4. Applies to all logic types when in tristated mode.
5. Applies to TCK, $\overline{\text{RESET}}$ and USER inputs.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
t_{IOO} Output Adders[1, 2]					
SSTL2_out	Output Configured as SSTL2 Buffer		0.4		ns
SSTL18_out	Output Configured as SSTL18 Buffer		-0.6		ns
SSTL15_out	Output Configured as SSTL15 Buffer		-0.5		ns
HSTL_out	Output Configured as HSTL Buffer		-0.5		ns
eHSTL_out	Output Configured as eHSTL Buffer		-0.6		ns
MLVDS_out	Output Configured as MLVDS Buffer		0.25		ns
HCSL_out	Output Configured as HCSL		0.35		ns
LVDS25_out	Output Configured as LVDS25		0.25		ns
LVPECL_out	Output Configured as LVPECL		0		ns

1. Measured under standard output load conditions, see Figures 2-3 to 2-8.
2. All output adders referenced to LVDS33.

Output Test Loads

Figures 2-3 to 2-8 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 2-3. LVDS/LVPECL Termination Load

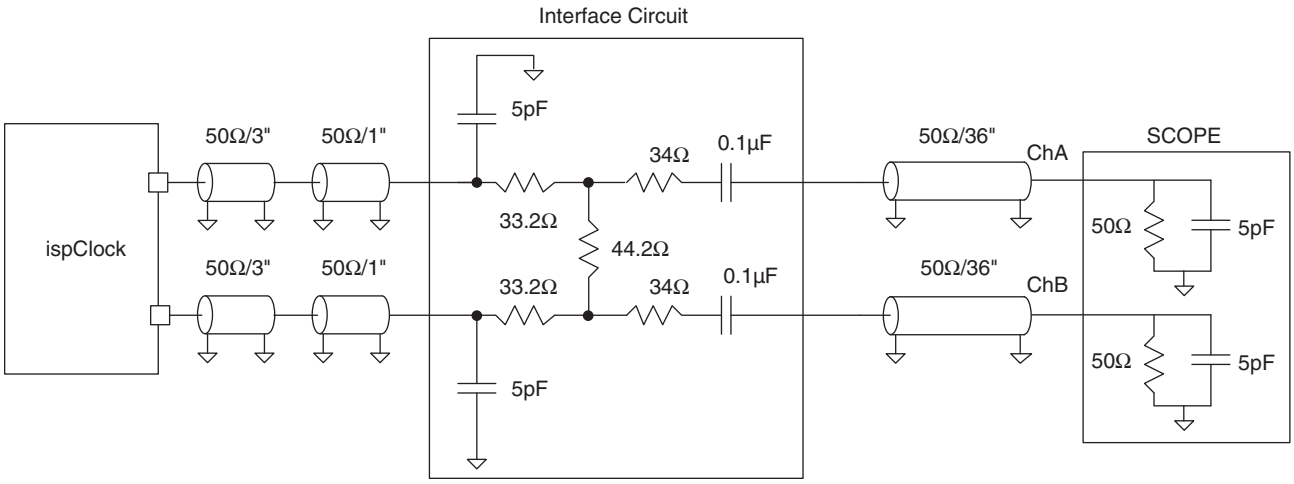


Figure 2-4. MLVDS Termination Load

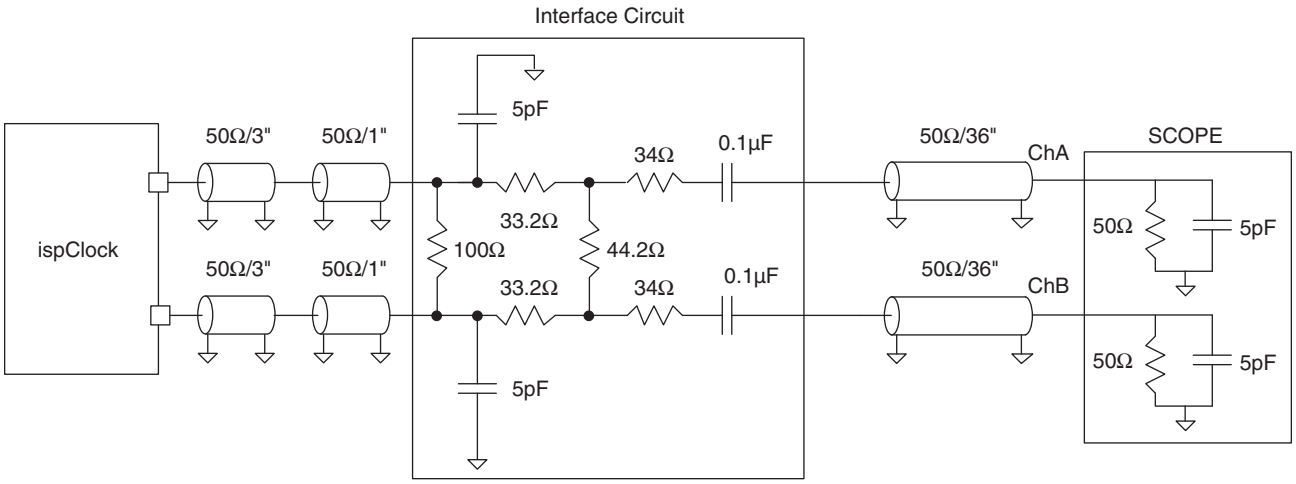


Figure 2-5. Differential HSTL Termination Load

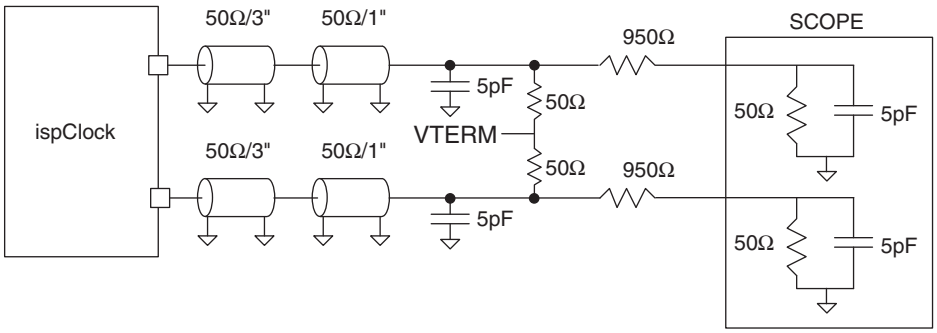


Figure 2-6. Differential SSTL Termination Load

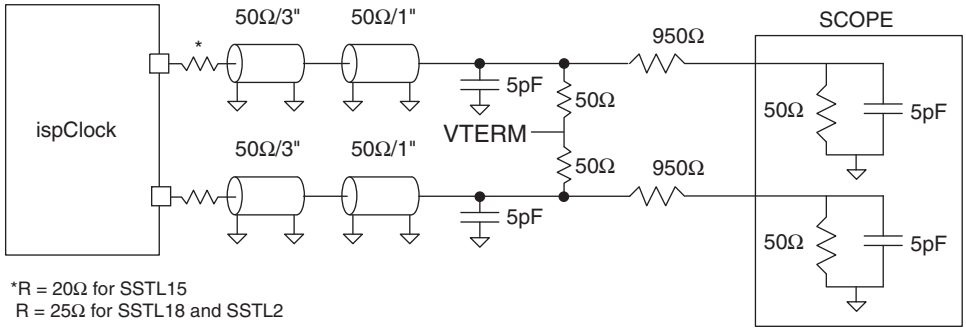


Figure 2-7. HCSL Termination Load

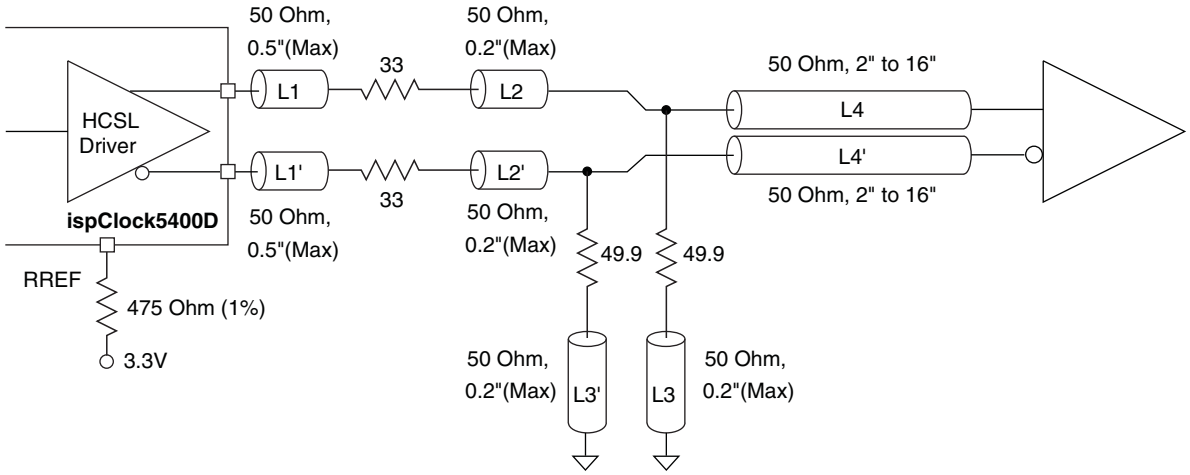
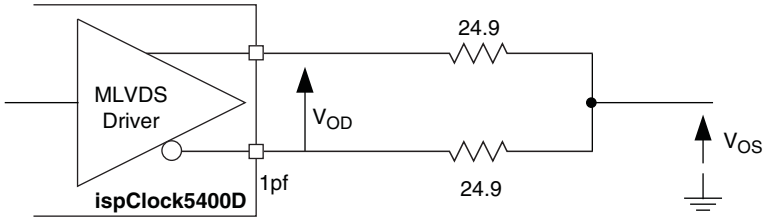
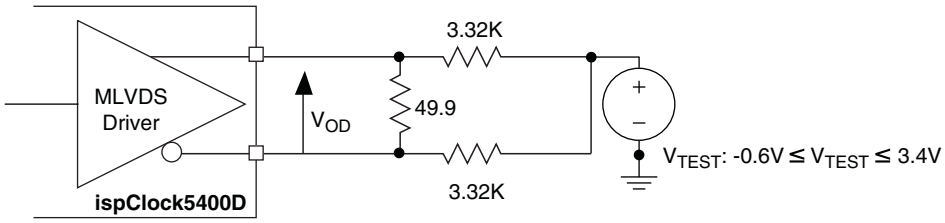


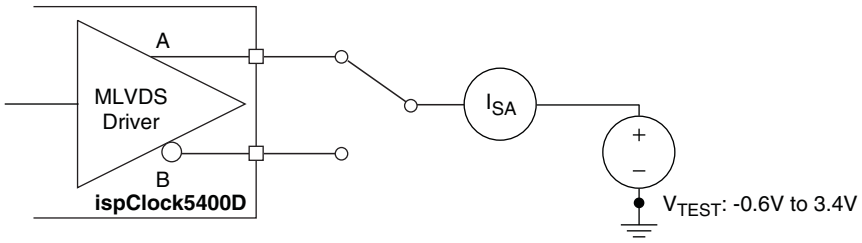
Figure 2-8. MLVDS Termination Load



(a) Common Mode Output Voltage Test Circuit



(b) Differential Output Voltage Test Circuit



(c) Short Circuit Curreent (I_{SA}) Test Circuit

Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{REF}, f_{FBK}	Reference and Feedback Input Frequency Range		40[1]		400[7]	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference and Feedback Input Clock HIGH and LOW Times		900			ps
t_{RINP}, t_{FINP}	Reference and Feedback Input Rise and Fall Times	Measured Between 20% and 80% Levels			5	ns
f_{PFD}	Phase Detector Input Frequency Range		40		400[7]	MHz
f_{VCO}	V_{CO} Operating Frequency		400		800	MHz
V_{DIV}	Output Divider Range (Power of 2)		2		32	
f_{OUT}	Output Frequency Range[1]	Fine Skew Mode	25		400[5]	MHz
		Coarse Skew Mode	12.5		200[5]	MHz
t_{JIT} (cc)	Output Adjacent-Cycle Jitter[4] (1000-Cycle Sample)				29	ps (p-p)
t_{JIT} (per)	Output Period Jitter[4] (10000-Cycle Sample)				2.5	ps (RMS)
$t_{JIT(\phi)}$	Reference Clock to Feedback Jitter (2000-Cycle Sample)[6]			6.5		ps (RMS)
$t\phi$	Static Phase Offset[3]	PFD Input Frequency ≥ 100MHz	-5	45	95	ps
$t\phi_{DYN}$	Dynamic Phase Offset	Spread Spectrum Modulation Index = -0.5%			50	ps
t_{PD_FOB}	Reference to Output Propagation Delay in Non-Zero Delay Buffer Mode[2]	Time Skew Control Disabled		6		ns
$t_{PD\_FOB\_TS\_EN}$	Reference to Output Delay in Non-Zero Delay Buffer Mode[2]	Time Skew Control Enabled		7		ns
t_{DELAY}	Reference to Output Delay with Internal Feedback Mode[2]	V=2		4		ns
t_{LOCK}	PLL Lock Time	From Power-up Event		2.5	15	ms
t_{RELOCK}	PLL Relock Time	$f_{IN} = f_{OUT}$ = 100 MHz		2.5		ms

1. In PLL Bypass mode (PLL_BYPASS = HIGH), input and output will support frequencies down to 0Hz (divider chain is a fully static design).
2. Input and outputs LVPECL mode
3. Inserted feedback loop delay < 5ns
4. Measured with f_{OUT} = 100MHz, f_{VCO} = 800MHz, input and output interface set to LVDS, internal feedback.
5. Also dependent on output type.
6. Measured with f_{OUT} = 100MHz, f_{VCO} = 800MHz, input and output interface set to LVPECL, external feedback.
7. In Coarse Skew Mode, maximum input frequency is 200MHz.

Timing Specifications

Skew Matching[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-Output Skew	Between any two identically configured and loaded outputs, regardless of bank, on the same device.	—	—	75	ps
$t_{SKEW-FOB}$		T-skew Disabled			75	ps
$t_{SKEW-FOB-TS-EN}$		T-skew Enabled			100	ps

1. LVPECL outputs.

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{PSKRANGE}$	Phase Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 400 MHz	—	4.68	—	ns
		Fine Skew Mode, f_{VCO} = 800 MHz	—	2.34	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	9.38	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	4.68	—	
PSK_{STEPS}	Phase Skew Steps per Range		—	16	—	
$t_{PSKSTEP}$	Phase Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 400 MHz	—	312	—	ps
		Fine Skew Mode, f_{VCO} = 800 MHz	—	156	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	625	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	312	—	
t_{PSKERR}	Phase Skew Time Error at Any Skew Setting[3]	Fine skew mode	—	10	—	ps
		Coarse skew mode	—	10	—	

1. Skew control range is a function of V_{CO} frequency (f_{VCO}). In fine skew mode $T_{SKRANGE}$ = 15/(8 x f_{VCO}). In coarse skew mode $T_{SKRANGE}$ = 15/(4 x f_{VCO}).
2. Skew step size is a function of V_{CO} frequency (f_{VCO}). In fine skew mode T_{SKSTEP} = 1/(8 x f_{VCO}). In coarse skew mode T_{SKSTEP} = 1/(4 x f_{VCO}).
3. Only applicable to outputs with non-zero skew settings.

Programmable Skew Control – Time Skew

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
$t_{T-SK-RANGE}$	Time-Skew Control Range		—	270	—	ps
$t_{SK-STEPS}$	Number of Time-Skew Steps		—	16	—	ps
$t_{T-SK-STEP}$	Time-skew Step Size		—	18	—	ps
$t_{T-SKERR}$	Step Size Error at Any Skew Setting		—	5	—	ps

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, OEb or GOEb to Output Disabled/Enabled		—	10	20	ns
t_{PLL_RSTW}	PLL $\overline{\text{RESET}}$ Pulse Width		10	—		µs
RST_SLEW	Reset Signal Slew Rate				1	V/µs

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_H	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

I²C Port Characteristics

Symbol	Definition	100KHz		400KHz		Units
		Min.	Max.	Min.	Max.	
F_{I^2C}	I²C clock/data rate		100		400	KHz
$T_{SU;STA}$	After start	4.7		0.6		us
$T_{HD;STA}$	After start	4		0.6		us
$T_{SU;DAT}$	Data setup	250		100		ns
$T_{SU;STO}$	Stop setup	4		0.6		us
$T_{HD;DAT}$	Data hold; SCL= Vih_min = 2.1V	0.3	3.45	0.3	0.9	us
T_{LOW}	Clock low period	4.7		1.3		us
T_{HIGH}	Clock high period	4		0.6		us
T_F	Fall time; 2.25V to 0.65V		300		300	ns
T_R	Rise time; 0.65V to 2.25V		1000		300	ns
$T_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
T_{POR}	Device must be operational after power-on reset	500		500		ms
T_{BUF}	Bus free time between stop and start condition	4.7		1.3		us

Timing Diagrams

Figure 2-9. Erase (User Erase or Erase All) Timing Diagram

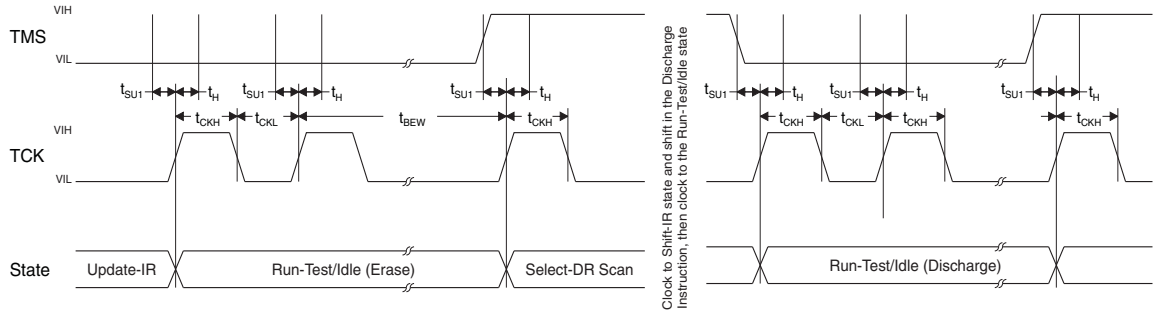


Figure 2-10. Programming Timing Diagram

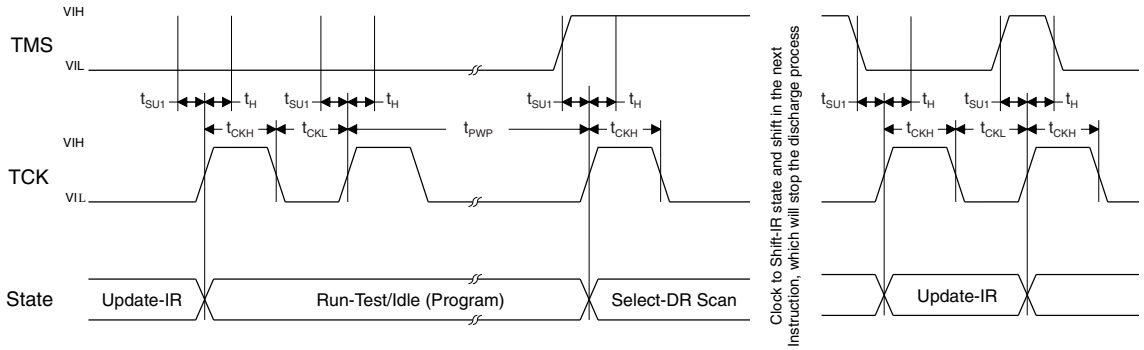


Figure 2-11. Verify Timing Diagram

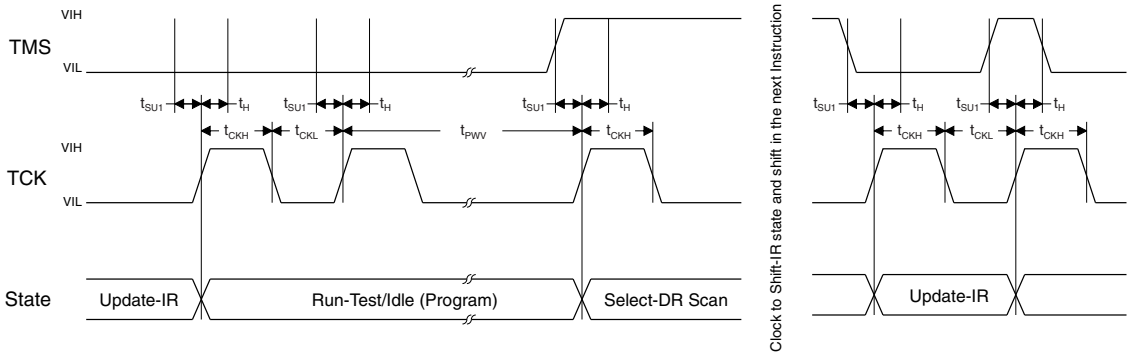
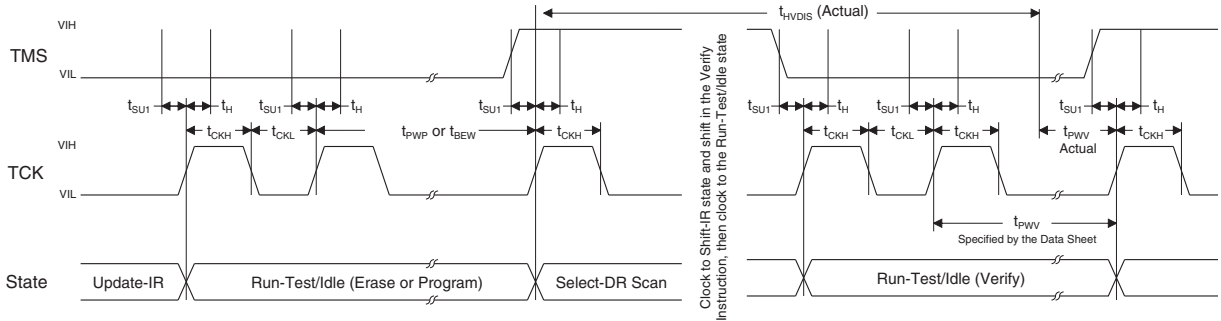
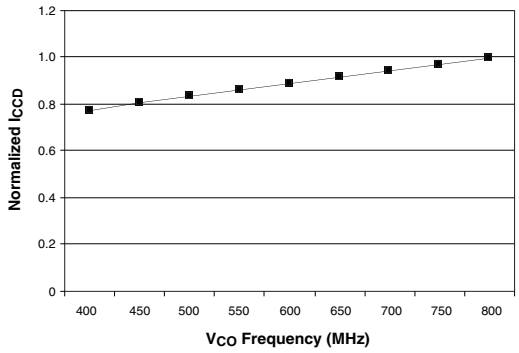


Figure 2-12. Discharge Timing Diagram

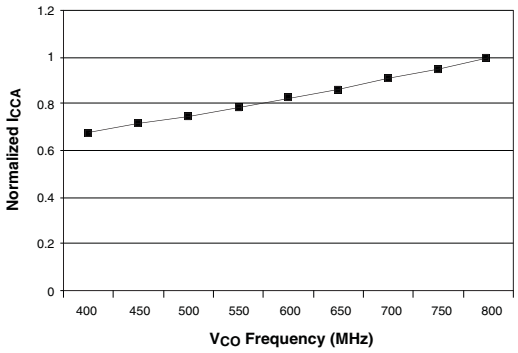


Typical Performance Characteristics

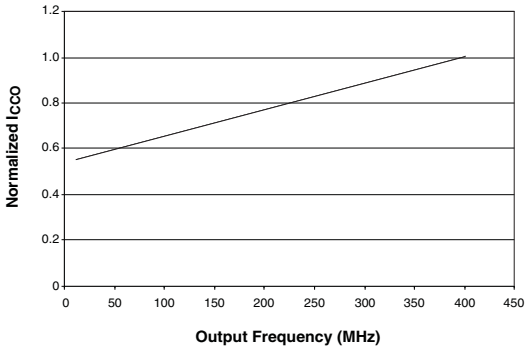
Normalized I_{CCD} vs. V_{CO} Frequency (I_{CCD} Value Normalized to V_{CO} at 800 MHz)



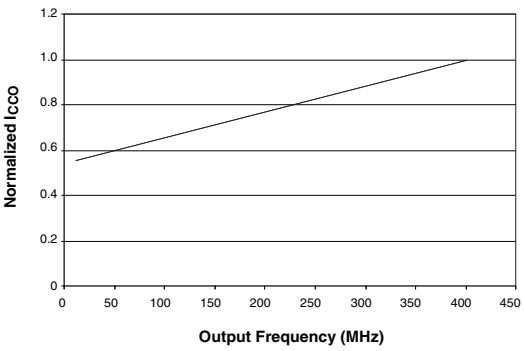
Normalized I_{CCA} vs. V_{CO} Frequency (I_{CCA} Value Normalized to V_{CO} at 800 MHz)



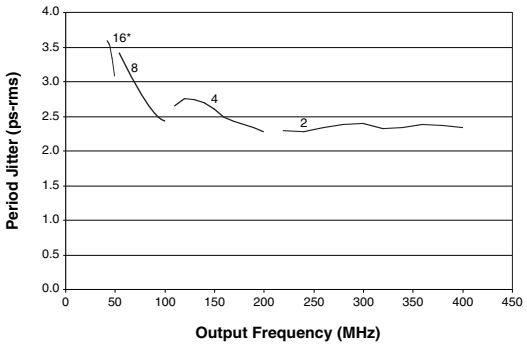
Normalized I_{CCO} vs. Output Frequency (I_{CCO} Value Normalized to Output Clock Frequency at 400 MHz, Output Logic Set to LVDS33)



Normalized I_{CCO} vs. Output Frequency (I_{CCO} Value Normalized to Output Clock Frequency at 400 MHz, Output Logic Set to LVPECL)

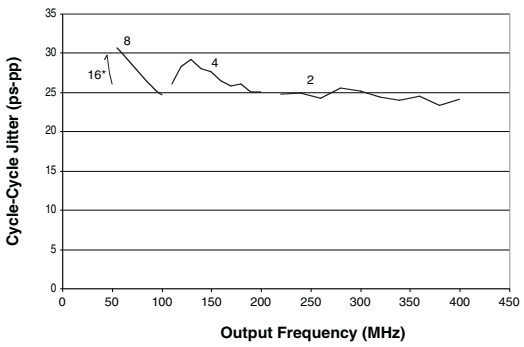


Period Jitter vs. Output Frequency



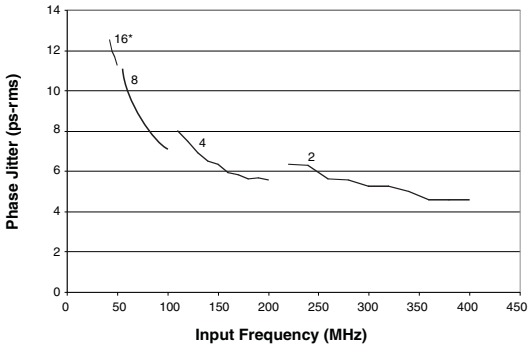
*Feedback V-Divider value.

Cyle-Cycle Jitter vs. Output Frequency



*Feedback V-Divider value.

Phase Jitter vs. Input Frequency



*Feedback V-Divider value.

Detailed Description

CleanClock PLL

The ispClock5400D provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the CleanClock PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Any of the frequencies from the 4-output V-divider can be used as feedback to support the synthesis of different output frequencies.

Phase/Frequency Detector

The ispClock5400D provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI,}$ $t_{CLOCKLO}$) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter. The output of the loop filter controls the VCO.

A lock-detection feature is also associated with the PFD. When the ispClock5400D is in a LOCKED state, the LOCK output signal is asserted (programmable high or low). The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 through 256. The LOCK output from the PFD can be routed to one of the USER Programmable pins.

When the lock condition is lost the LOCK signal will be de-asserted immediately.

Loop Filter: The loop filter parameters are automatically selected by the PAC-Designer software depending on the feedback V-divider setting.

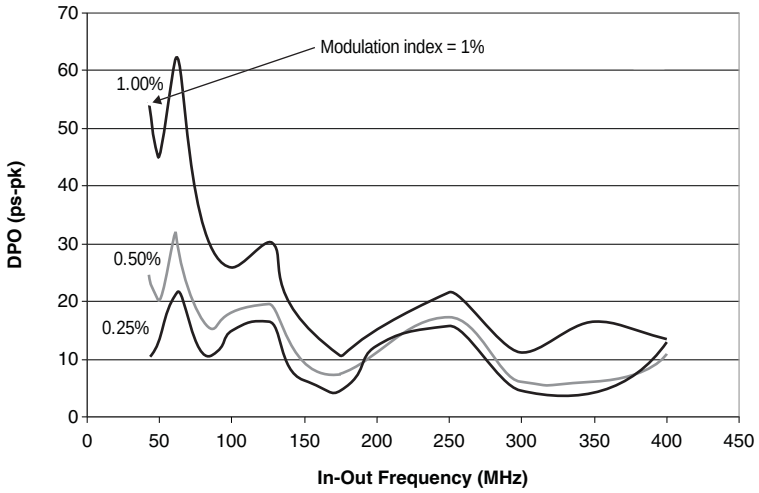
Spread Spectrum Support: The reference clock inputs of the ispClock5400D device are spread spectrum clock compatible. The tolerance limits are:

- Center spread ±0.125% to ±0.25%
- Down spread -0.25% to -0.5%
- 30-33kHz modulation frequency

Table 2-2. PLL Bandwidth

V-Divider	Bandwidth (MHz)
2	9.8
4	7.0
8	4.5
16	2.4

Figure 2-13. Dynamic Phase Offset (DPO)



VCO

The operating frequency of the on-chip VCO of the ispClock5400D ranges from 400MHz to 800MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to set the phase skew step size. Using the VCO as the basis for controlling output phase skew allows for highly precise and consistent phase skew generation, both from device-to-device, as well as channel-to-channel within the same device.

Output V-dividers

The ispClock5400D incorporates a set of four dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input. The division values of these V-dividers are set to 2, 4, 8 and 16. In Coarse Skew Mode, the division values are set to 4, 8, 16 and 32.

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V-divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{V_{fbk}}{V_k} \quad (1)$$

where

f_K is the frequency of V-divider k
f_{REF} is the input reference frequency
V_{FBK} is the division ratio of the V-divider used to close the PLL feedback path
V_K is the output divider K

Note that because the feedback may be taken from any V-divider, V_k and V_{fbk} may refer to the same divider.

PLL_BYPASS Mode

The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the reference clock is routed directly to the inputs of the V-dividers. The output frequency for a given V-divider (f_K) will be determined by

$$f_k = \frac{f_{REF}}{V_K} \quad (2)$$

When PLL_BYPASS mode is enabled, features such as lock detect and phase skew generation are unavailable. The PLL can be bypassed through I^2C or through the USER pins.

Internal/External Feedback Support

The PLL feedback path can be sourced internally or externally through an output bank. When the internal feedback path is selected, one can use all output pins for clock distribution. The programmable phase skew feature for the feedback path is available in the internal feedback mode. However, both phase and time skew features are available for the feedback path in the external feedback mode.

Reference and External Feedback Inputs

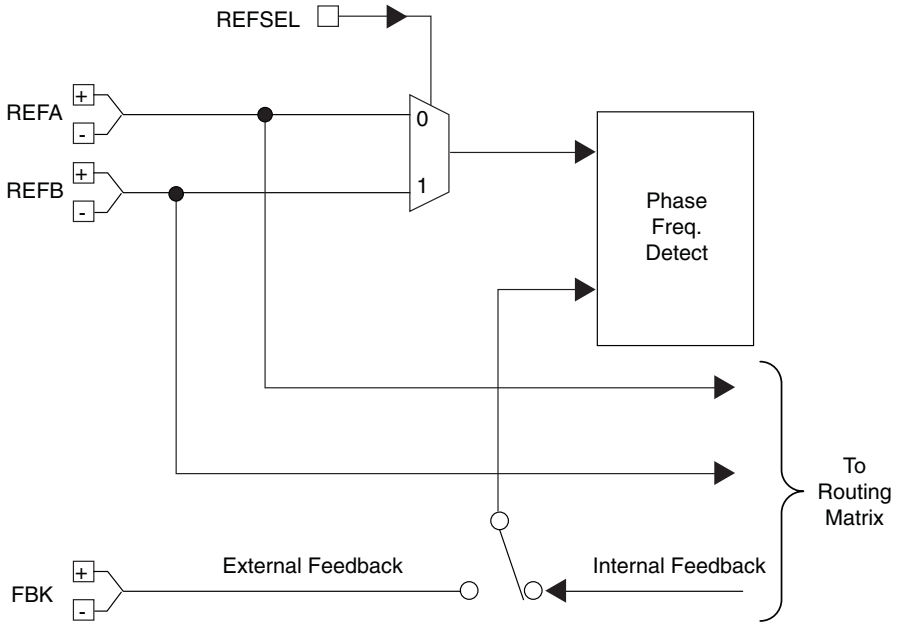
The ispClock5400D provides configurable, internally-terminated inputs for both clock reference and feedback signals.

The reference clock inputs pins (REFA, REFB) can be interfaced with two differential clocks. The active clock selection control through REFSEL signal. The REFSEL signal can be driven either by one of the USER pins or through the I^2C interface.

Supported input logic reference standards:

- LVDS
- LVPECL
- SSTL2
- SSTL18
- SSTL15
- HSTL
- eHSTL
- HCSL
- LVCMOS

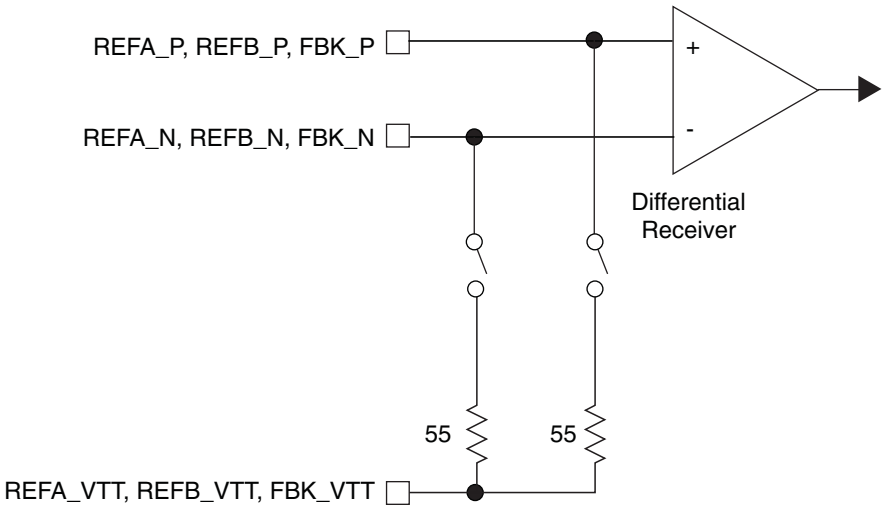
Figure 2-14. Reference and Feedback Input



Input Receiver Termination Configuration

Each input features internal 55 Ohm termination resistors as shown in Figure 2-15. The REFA, REFB and FBK inputs terminate to REFA_VTT, REFB_VTT, and FBK_VTT respectively. If external termination resistors are used, these internal termination resistors can be disconnected through PAC-Designer software.

Figure 2-15. Input Receiver Termination Configuration

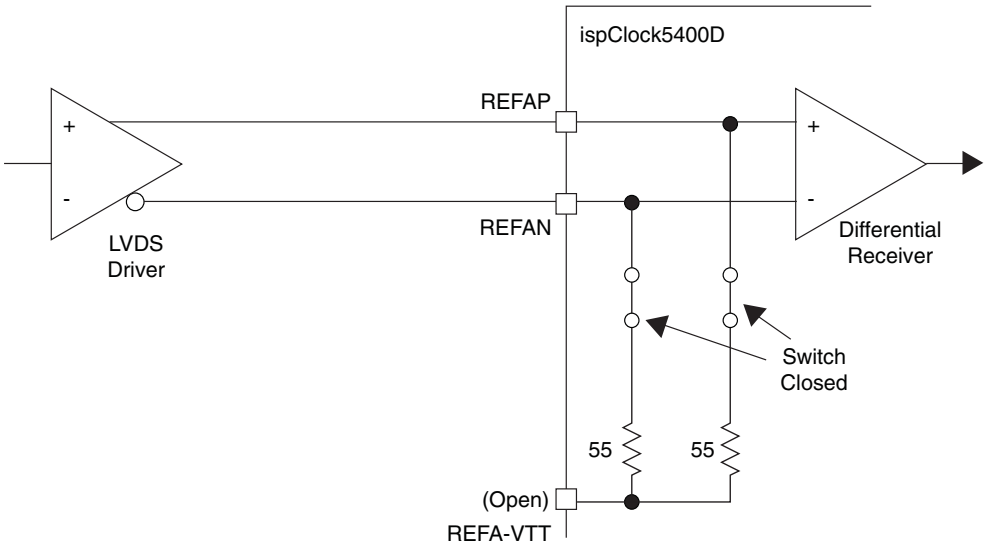


The following usage guidelines are suggested for interfacing to supported logic families.

LVPECL/LVDS

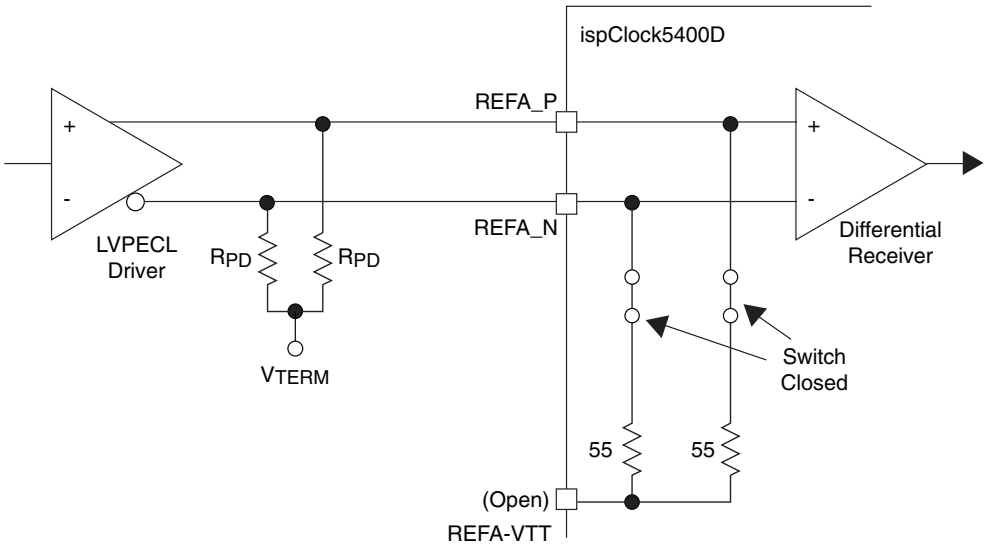
Both termination resistors in the receiver should be engaged. The VTT pin should be left floating. This creates a floating 110Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 2-16.

Figure 2-16. LVDS Input Receiver Configuration



Note that while a floating 110Ω resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 2-17)

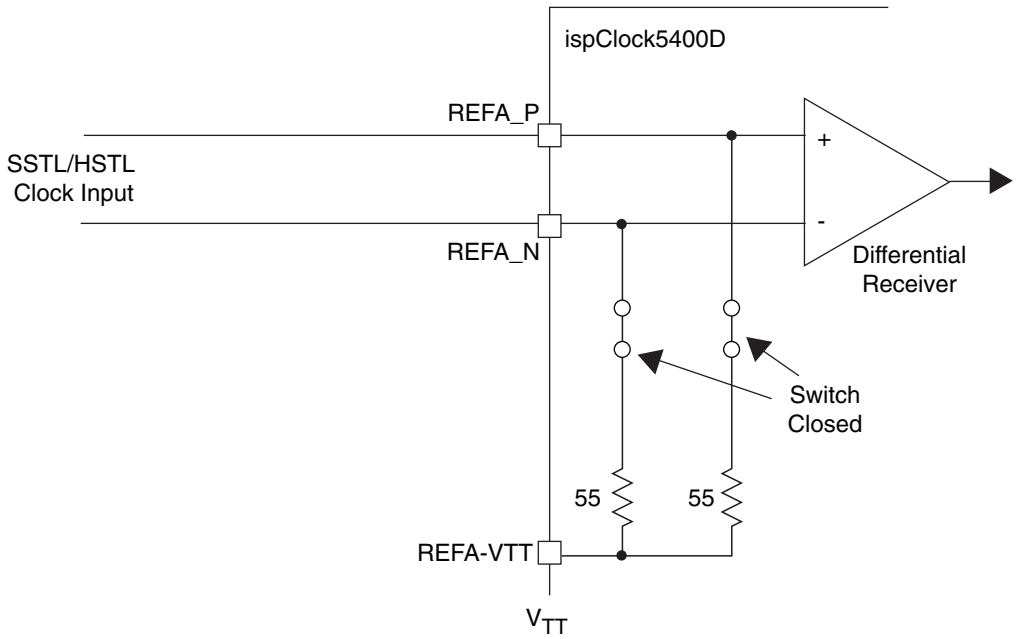
Figure 2-17. LVPECL Input Receiver Configuration



SSTL/HSTL

To interface the ispClock5400D with the SSTL or HSTL signals, close the switch connecting the REFP and REFN signals to termination resistors. Connect the VTT pin to a voltage half of the supply voltage of the clock input.

Figure 2-18. SSTL/HSTL Input Receiver Configuration

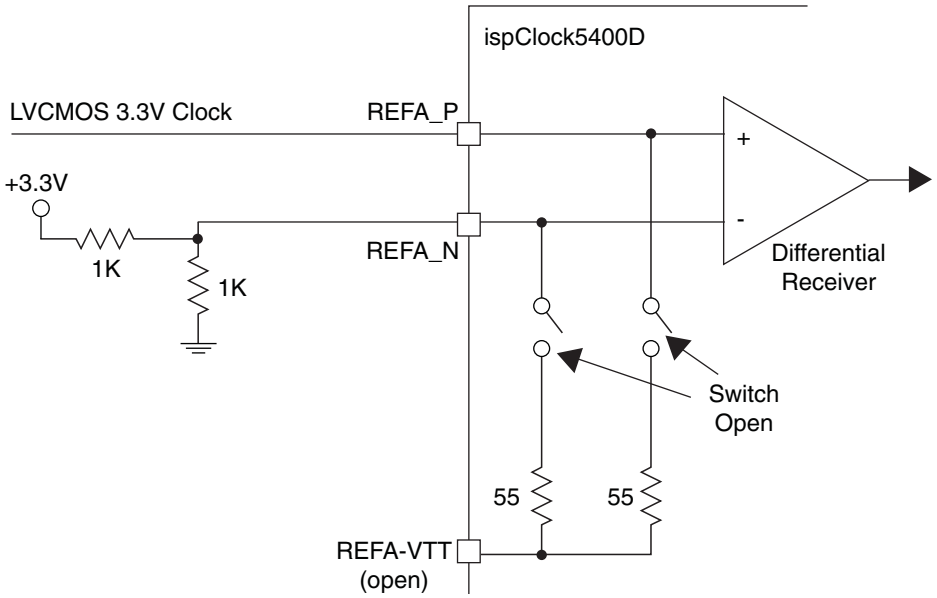


LVCMOS

The ispClock5400D input section can be connected to single ended signals such as the LVCMOS3.3V by connecting it directly to REFAP pin while the threshold is provided by the REFAN terminal at 1.65V (= 3.3V ÷ 2). The threshold reference voltage can be derived by a potential divider using 2, 1K ohm resistors.

Note: To minimize the noise injection into the receiver, the 3.3V at the input of the potential divider should be sufficiently filtered. The GND limb of the potential divider should be connected to the GND pin of the source.

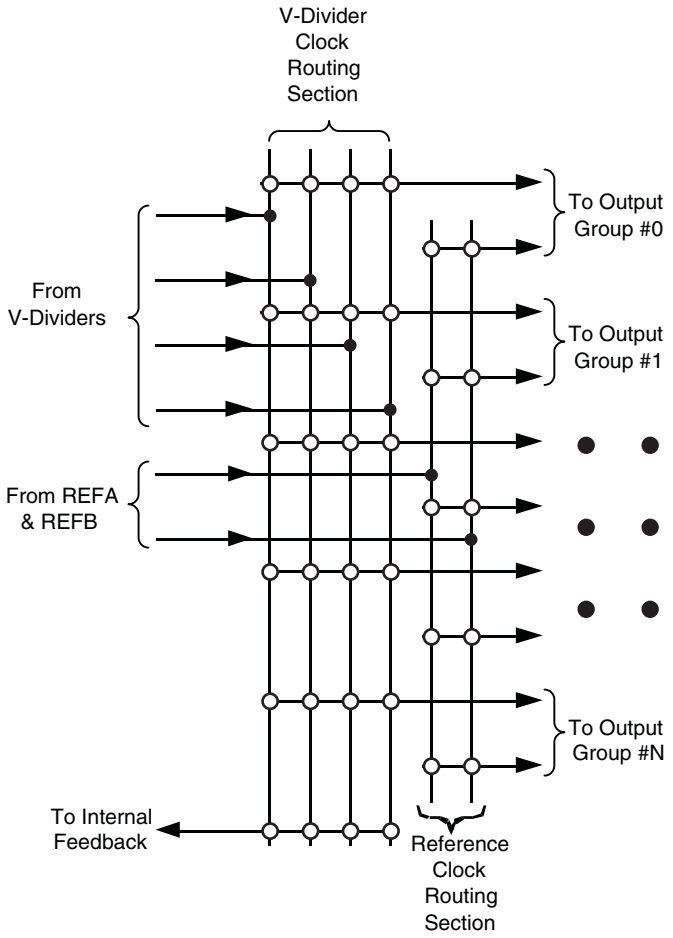
Figure 2-19. LVCMOS Input Receiver Configuration



Output Routing Matrix

There are two sections in the Output Routing Matrix: the V-divider clock routing section and the REF clock routing section. The V-divider routing section enables connecting any output group and the internal feedback path to any of the output V-dividers. The Ref clock routing section can route either of the Ref clocks to any output group.

Figure 2-20. ispClock5400D Output Routing Matrix



FlexiClock Output Section

The FlexiClock output block distributes clock received from the Output Routing Matrix. The signalling interface of each of the differential clock outputs can be individually programmed. The output voltage swing is controlled by the associated output VCC and GND pins. The VCCO, the GNDO and the associated differential clock output pair is called an output bank.There are six output banks in the FlexiClock output section in the ispClock5406D device. The FlexiClock output section the ispClock5610D supports 10 output banks.

Output Groups

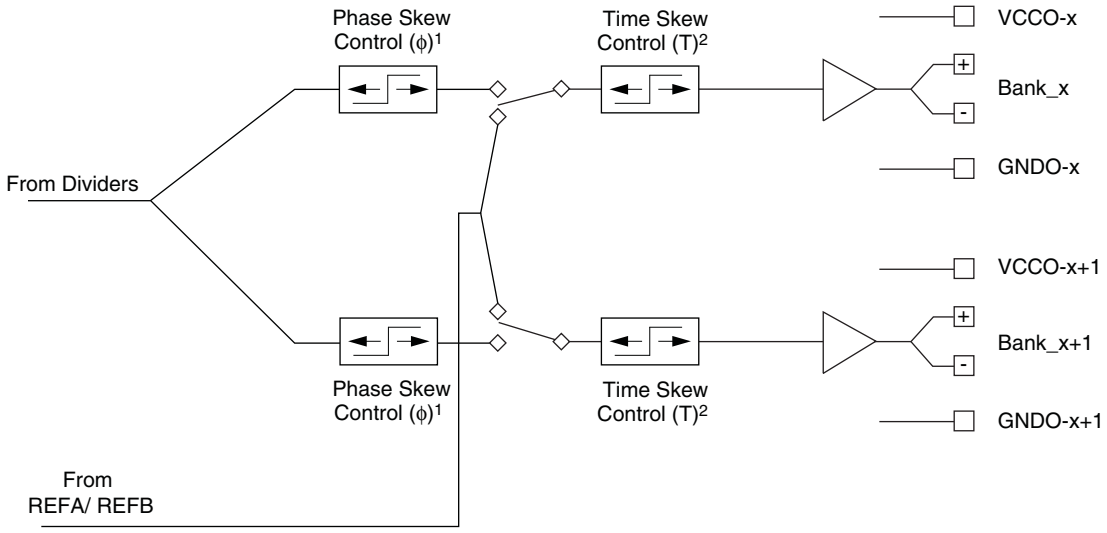
The ispClock5400D provides multiple banks, with each bank supporting a high-speed clock output and the associated VCCO and GND pins. Two adjacent banks form an Output Group (Bank 0 and Bank 1 belong to Group #0, Bank 2 and Bank 3 belong to Group #2, and so on). There are ten banks (five Output Groups) in the ispClock5410D and three output groups in the ispClock5406D device. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by USER pins or through I^2C. Additionally, each bank output clock can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 2-21 shows a block diagram of an ispClock5400D Output Group and its associated skew control. The two outputs in an Output Group share the connection to the Output Routing Matrix.

Because of the high edge rates which can be generated by the ispClock5400D clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respec-

tive output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GNDO pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 2-21. ispClock5400D Output Group and Skew Control



1. Phase Skew Control mechanism is applicable only to outputs connected to one of the V-dividers and when PLL is active.
2. Time Skew Control mechanism is applicable to all outputs.

Each clock output from the output group (Figure 2-21) can be connected to either reference clock or to a V-divider clock. However, both outputs can source only from the same V-divider output or the same reference clock at any time.

The ispClock5400D supports two skew controls: Phase Skew Control (ϕ) and Time Skew Control (T).

The Phase Skew Control mechanism is available only on outputs connected to the V-divider clocks because the Phase Skew Control timing is derived from the VCO. The Phase skew of each output of an Output Group can be individually adjusted.

The Time Skew Control mechanism derives the skew control timing from internal delay lines. The time skew mechanism is available on outputs connected to the V-dividers as well as outputs connected to reference clocks.

The output skew of the clocks connected to the V-dividers can be adjusted by both phase skew and time skew controls.

Each of the ispClock5400D's output driver banks can be configured to support the following logic outputs:

- LVDS
- LVPECL
- SSTL15
- SSTL18
- SSTL2
- HSTL
- eHSTL
- MLVDS
- HCSL

Skew Control Units

The ispClock5400D supports two skew control mechanisms: Phase Skew Control and the Time Skew Control. The Phase Skew Control mechanism delays the output clock by altering its phase angle. The Time Skew control mechanism delays the output clock by delay lines. There are 16 steps of Time Skew and Phase Skew available for each output clock.

Phase Skew Control Units

Each of the ispClock5400D's clock outputs is supported by the Phase Skew Control unit which allows the user to insert an individually programmable delay into each output signal. This feature is useful when it is necessary to de-skew clock signals to compensate for physical length variations among different PCB clock paths.

The ispClock5400D's phase skew adjustment feature provides exact and repeatable delays which exhibit extremely low channel-to-channel and device-to-device variation. This is achieved by deriving all skew timing from the VCO, which results in the skew increment being a linear function of the VCO period. Because the skew time step is determined by the VCO period, the resultant output skew increment/ decrement is equivalent to changing the phase angle of the output clock. The phase skew is measured in terms of 'Phase Unit Delay' (PUD) and represented in nanoseconds. Each output can be individually delayed by up to 15 PUD. The ispClock5400D family also supports both 'fine' and 'coarse' skew modes. In fine skew mode, the unit skew ranges from 156 to 312ps, while in the coarse skew mode unit skew varies from 312 to 625ps. The exact value phase unit delay may be calculated from the VCO frequency (f_{vco}) by using the following expressions:

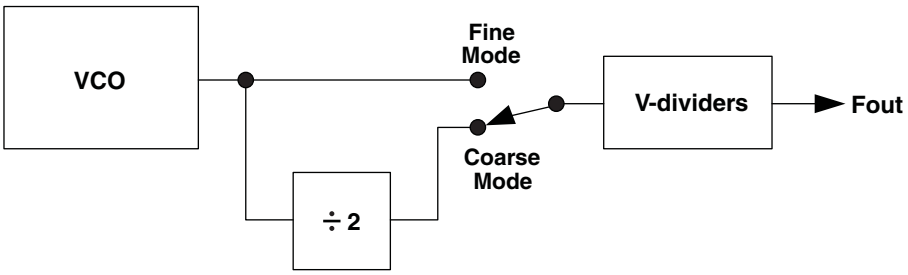
For fine skew mode, $PUD = \frac{1}{8f_{vco}}$ For coarse skew mode, $PUD = \frac{1}{4f_{vco}}$ (5)

Please note that Phase Skew Control is only usable when the PLL is not in bypass mode. In PLL bypass mode, output phase skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay, the time skew delay setting, and the individual delays inherent in the output drivers consistent with the logic standard selected.

Coarse Skew Mode

The ispClock5400D family provides the user with the option of obtaining longer skew delays at the cost of reduced time resolution through the use of coarse skew mode. Coarse skew mode provides phase unit delay ranging from 312ps (f_{VCO} = 800MHz) to 625ps (f_{VCO} = 400MHz), which is twice as long as those provided in fine skew mode. When coarse skew mode is selected, an additional divide-by-2 stage is effectively inserted between the VCO and the V-divider bank, as shown in Figure 2-22. When assigning divider settings in coarse skew mode, one must account for this additional divide-by-two so that the VCO still operates within its specified range (400MHz to 800MHz).

Figure 2-22. Additional Factor-of-2 Division in Coarse Mode



When one moves from fine skew mode to coarse skew mode with a given divider configuration, the VCO frequency will attempt to double to compensate for the additional divide-by-2 stage. Because the f_{VCO} range is not increased, however, one must modify the feedback path V-divider settings to bring f_{VCO} back into its specified operating range (400MHz to 800MHz). This can be accomplished by changing the feedback to the next lower V-divider. All output frequencies will remain unchanged from what they were in fine mode.

Note: Avoid exceeding maximum f_{VCO} when changing skew control between fine and coarse modes.

Time Skew Control Unit

The Time Skew Control mechanism can insert an individually programmable delay into every clock output signal in addition to Phase Skew Control Delay. The Time Skew Control is applicable to outputs configured as Non-Zero Delay Buffers. For outputs configured as Zero Delay Buffer, the Time Skew Control can be used to fine tune the de-skew delay to compensate for the differences in clock trace lengths.

The ispClock5400D provides programmable steps of Time Skew for each output through a 16-step programmable delay line per output. The step size of this delay line, called 'Time Unit Delay' (TUD) is specified by the $t_{T\text{-}SK\text{-}STEP}$ parameter.

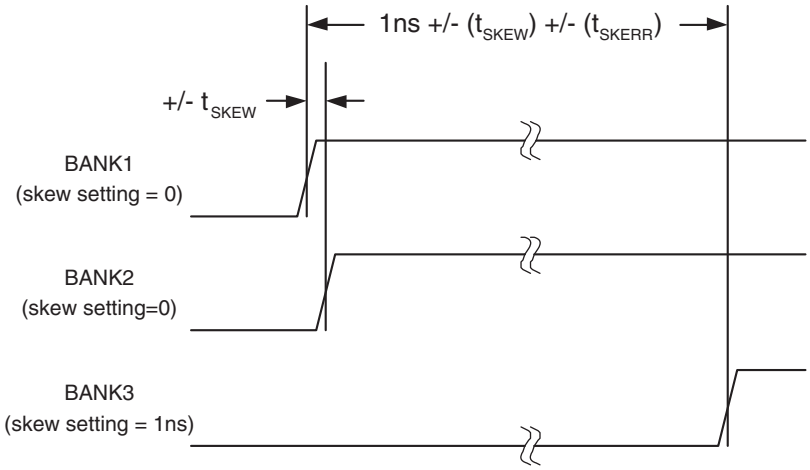
Note: Time Skew step size does not change with the VCO operating frequency.

Output Skew Matching and Accuracy

Understanding the various factors which relate to output skew is essential for realizing optimal skew performance in the ispClock5400D family of devices.

In the case where two outputs are identically configured, and driving identical loads, the maximum skew is defined by the t_{SKEW} parameter. In Figure 2-23 the Bank1 and BANK2 outputs show the skew error between two matched outputs.

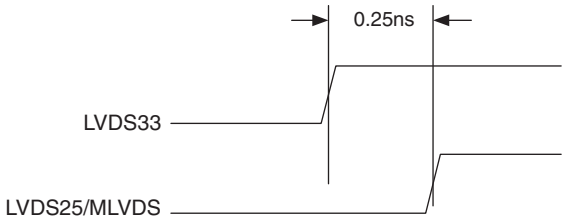
Figure 2-23. Skew Matching Error Sources



One can also program a user-defined skew between two outputs using the phase or Time Skew Control units. The typical error for any non-zero skew setting is given by the t_{PSKERR} and $t_{T\text{-}SKERR}$ specification. For example, if one is in fine skew mode with a VCO frequency of 500MHz, and selects a skew of 4PUD, the realized skew will be 1ns, which will typically be accurate to within +/-10ps. Note that this parameter adds to output-to-output skew error only if the two outputs have *different* skew settings. The Bank1 and Bank3 outputs in Figure 2-23 show how the various sources of skew error stack up in this case. Note that if two or more outputs are programmed to the same skew setting, then the contribution of the t_{SKERR} skew error term does not apply.

When outputs are configured or loaded differently, this also has an effect on skew matching. If an output is set to support a different logic type, this can be accounted for by using the t_{IOO} output adders specified in the table 'Switching Characteristics'. That table specifies the additional skew added to an output using LVDS33 as a baseline. For instance, if one output is specified as LVDS25, it has a delay adder relative to LVDS33 of 0.25ns. If another output is specified as MLVDS, then one would expect 0ns of additional skew between the two outputs due to this adder. This timing relationship is shown in Figure 2-24.

Figure 2-24. Output Timing Adders for Logic Type

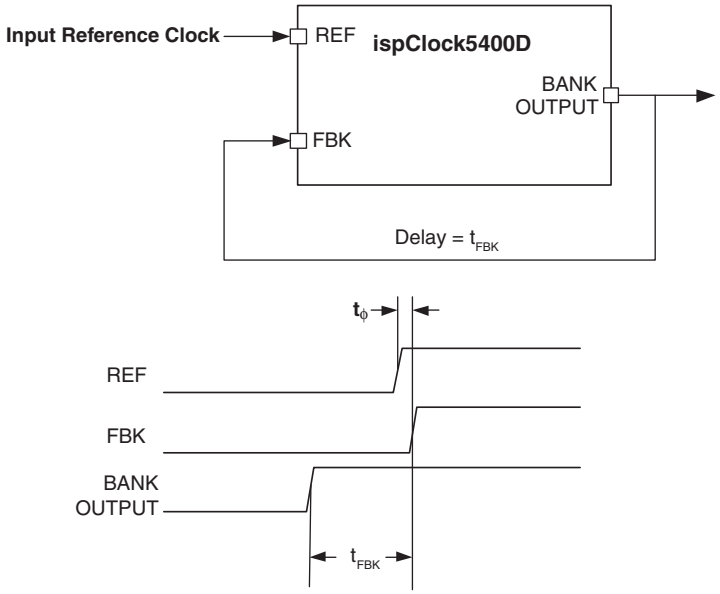


By selecting the same feedback logic type and clock output, the output delay adders for the clock output are automatically compensated for.

Static Phase Offset and Input-Output Skew

The ispClock5400D's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. Using external feedback (Figure 2-25), the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase offset. Note that any propagation delay (t_{FBK}) in the external feedback path drives the phase of the output signal *backwards* in time with respect to input clock phase. For this reason, if zero input-to-output delays are required, the length of the signal path between the output pin and the feedback pin should be minimized.

Figure 2-25. External Feedback Mode and Timing Relationships



ispClock5400D Configurations

The ispClock5400D device can be configured to operate in several modes, including:

- Zero Delay Buffer Mode
- Mixed Zero Delay and Non-Zero Delay Buffer Mode
- Dual Non-Zero Delay Buffer Mode
- Non-Zero Delay Buffer Mode With and Without Output Dividers

The output routing matrix of the ispClock5400D provides up to six independent any-to-any paths from inputs to output pairs:

- From any V-dividers to any Output Group in ZDB mode or PLL Bypass modes
- From either REFA or REFB inputs to any Output Group

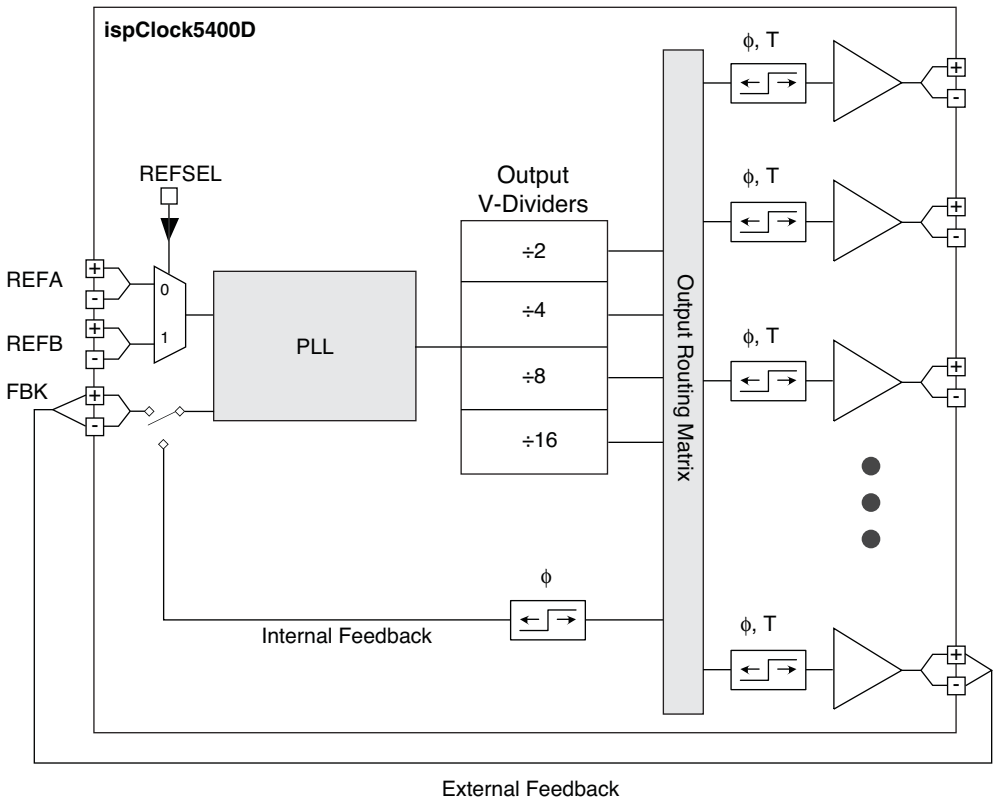
Zero Delay Buffer Mode

Figure 2-26 shows the ispClock5400D device configured to operate in the Zero Delay Buffer mode. The REFSEL signal is used to select the active clock from the two input reference clocks. The active input clock then drives the Phase frequency detector of the PLL. Up to four clock frequencies can be generated from the PLL clock by the use of output V-dividers. Any V-divider output can be connected to any of the Output Group.

The feedback for the PLL can be derived from any of the V-dividers using the internal feedback path. Alternatively, in applications which are sensitive to input to output delay, external feedback path can be used. In both cases, the V-divider used in the feedback path must be selected such that the PLL VCO is operating within the data sheet specified frequency range.

In this mode, both Phase and Time skew control mechanisms are active for all outputs.

Figure 2-26. ispClock5400D Configured as Zero Delay Buffer Mode



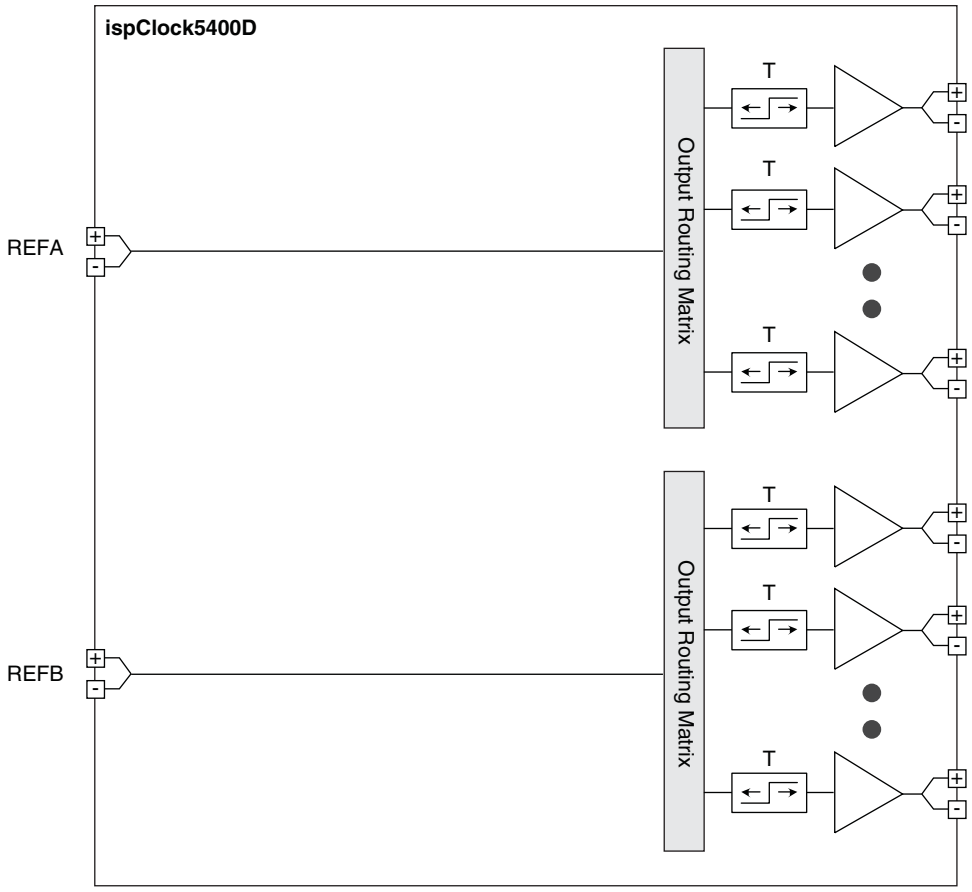
Dual Non-Zero Delay Buffer Mode (Dual Fan-Out Buffer Mode)

Figure 2-27 shows the operation of ispClock5400D configured in the Dual Non-Zero Delay Buffer mode. In this mode the reference clock inputs are directly routed to outputs through the output routing matrix. There is no limit to the number of Output Groups associated with either REFA or REFB.

The output skew of each clock can be independently adjusted using the Time Skew Control only. (The Phase Skew Control mechanism is not available).

Note that in Fan-out Buffer mode the clock outputs match the input frequency and duty cycle. Reset does not disable outputs that are in Fan-out Buffer mode.

Figure 2-27. Dual Non-Zero Delay Buffer Mode



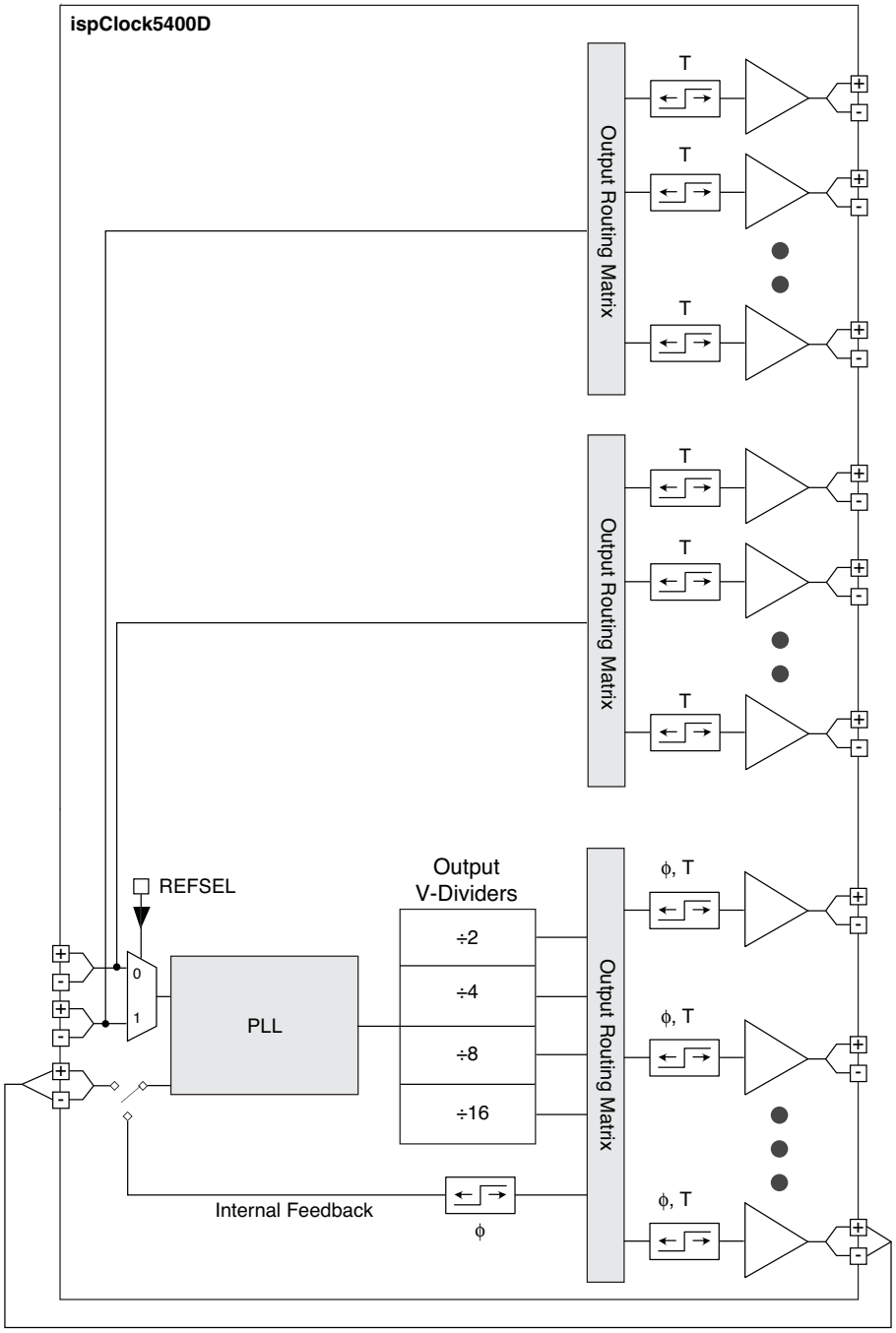
Mixed Zero Delay and Non-Zero Delay (Fan-out) Buffer Mode

Figure 2-28 shows the operation of the ispClock5400D in Mixed Zero Delay and Non Zero Delay modes. In this mode the output switch matrix is configured to route either of the reference clocks directly to two sets of Output Groups, and a zero delay clock through the PLL and V-dividers to the remaining Output Groups.

The Time Skew Control mechanism is available only to outputs directly connected to REFA or REFB. However, both the Phase and Time Skew Control mechanisms are available to clocks connected to V-dividers.

Note that in Fan-out Buffer mode the clock outputs match the input frequency and duty cycle. Reset does not disable outputs that are in Fan-out Buffer mode.

Figure 2-28. Mixed Zero Delay and Non Zero Delay (Fan-out) Buffer Mode



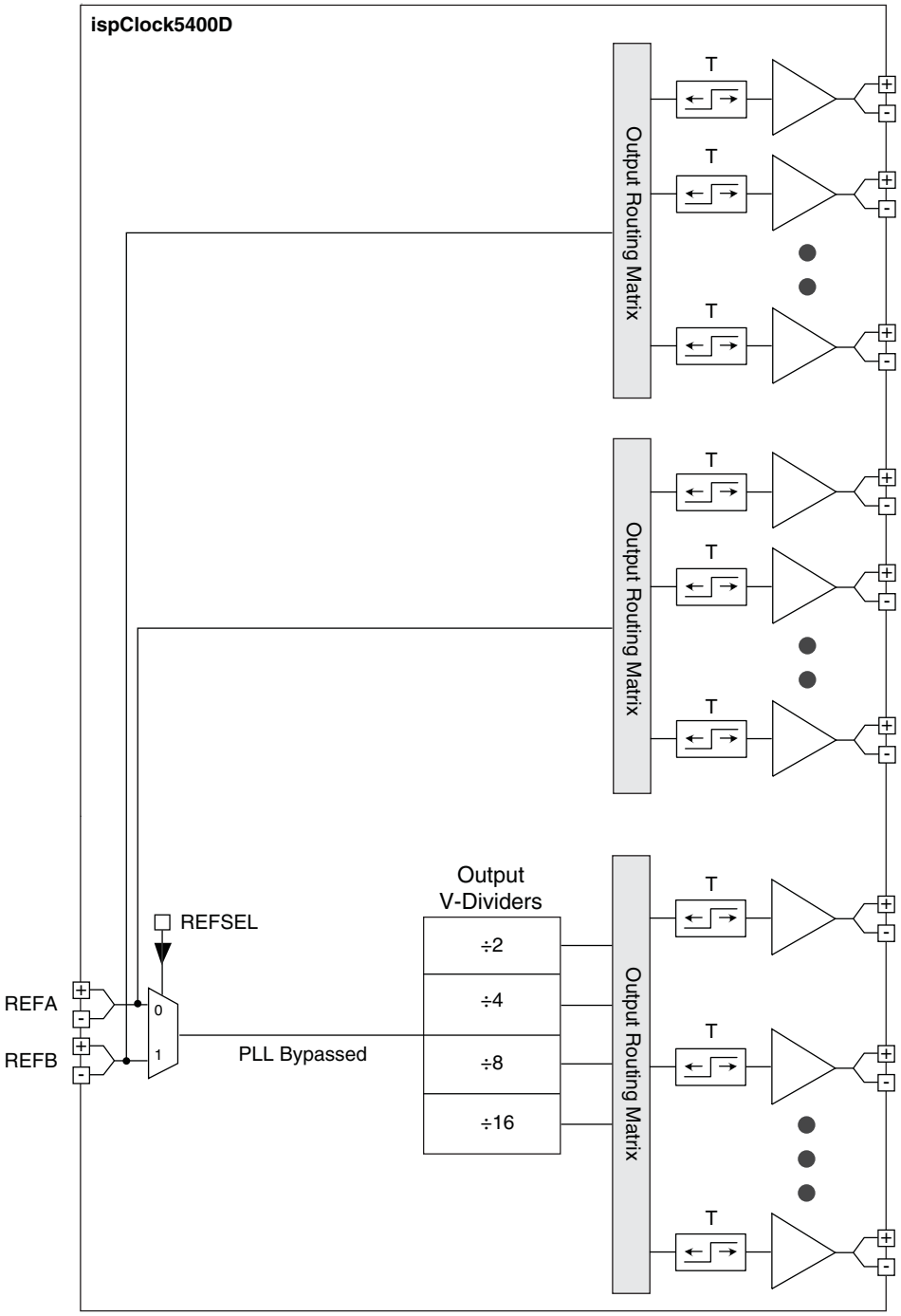
Non-Zero Delay Buffer Mode With and Without Output Clock Dividers

In the Non-Zero Delay Buffer mode shown in Figure 2-29 the Output Routing Matrix completely bypasses the PLL. Each of the single-ended input reference clocks can be routed to any number of available output clocks.

In this mode of operation only the Time Skew Control mechanism is available to all outputs.

Note that in the Non-Zero Delay Buffer mode without output clock dividers, the clock outputs match the input frequency and duty cycle. Reset does not disable outputs that are in the Non-Zero Delay Buffer mode when not using output clock dividers.

Figure 2-29. Non-Zero Delay Fan-out Buffer Mode With and Without Output Clock Division



ispClock5400D Operating Configuration Summary

Table 2-3 summarizes the operating modes of the ispClock5400D.

Table 2-3. ispClock5400D Operating Modes

ispClock5400D Operating Mode	Time Skew Control	Phase Skew Control	Output Clock Frequency Divider
Zero Delay Buffer Mode	Yes	Yes	Yes
Mixed Zero-Delay & Non-Zero Delay Buffer Mode	Yes	Only to Zero Delay Output Clocks	Only to Zero Delay Output Clocks
Dual Non-Zero Delay Fan-out Buffer Mode	Yes	No	No
Non-Zero Delay Fan-out Buffer Mode With and Without Output Clock Dividers	Yes	No	Only to Clocks Sourced From Bypassed PLL

Thermal Management

In applications where a majority of the ispClock5400D's outputs are active and operating at or near maximum output frequency, package thermal limitations may need to be considered to ensure absolute maximum junction temperature is not exceeded. Thermal characteristics of the packages employed by Lattice Semiconductor may be found in the Thermal Management document.

The maximum current consumption of the digital and analog core circuitry for ispClock5406D is 148.2mA worst case (I_{CCD} + I_{CCA} + 6 x $I_{CCADDER}$), and each of the output banks may draw up to 22mA worst case (LVPECL, CL=5pF, f_{OUT}=100 MHz, both outputs in each bank enabled). This results in a total device dissipation:

$$P_{DMAX} = 3.60V \times (6 \times 22mA + 148.2mA) = 1.01W \quad (3)$$

With an absolute maximum junction temperature (limit) of 125°C, the maximum allowable ambient temperature (T_{AMAX}) can be estimated as

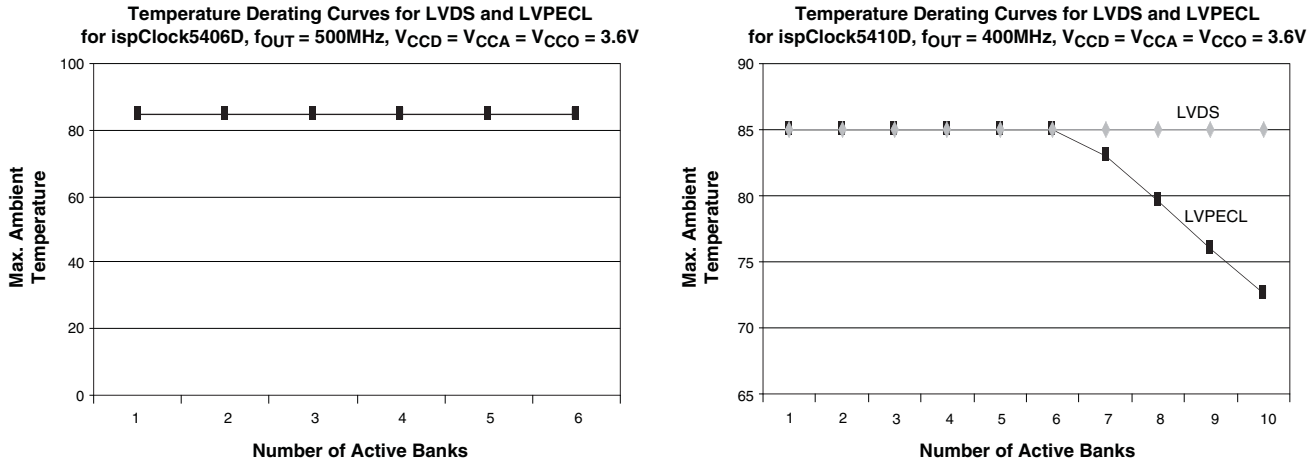
$$T_{AMAX} = T_{JOP} - PD_{MAX} \times \Theta_{JA} = 125°C - 1.01W \times 39.2°C/W = 85°C \quad (4)$$

where Θ_{JA} = 39.2°C/W for the 48 QFNS package in still air and Θ_{JA} = 38.4°C/W for the 64 QFNS package in still air.

The above analysis represents the worst-case scenario. Significant improvement in maximum ambient operating temperature can be realized with additional cooling. Providing a 200 LFM (Linear Feet per Minute) airflow reduces Θ_{JA} to 28.6°C/W for the 48 QFNS package and 26.7°C/W for the 64 QFNS package.

While it is possible to perform detailed calculations to estimate the maximum ambient operating temperature from operating conditions, some simpler rule-of-thumb guidance can also be obtained through the derating curves shown in Figure 2-30 which shows the maximum ambient temperature permitted when operating a given number of output banks at the maximum output frequency.

Figure 2-30. Maximum Ambient Temperature vs. Number of Active Output Banks



Note that because of variations in circuit board mounting, construction, and layout, as well as convective and forced airflow present in a given design, actual die operating temperature is subject to considerable variation from that which may be theoretically predicted from package characteristics and device power dissipation.

Other Features

$\overline{\text{RESET}}$ and Power-up Functions

To ensure proper PLL startup and synchronization of outputs, the ispClock5400D provides both internally generated and user-controllable external reset signals. An internal reset is generated whenever the device is powered up. An external reset may be applied by asserting a logic LOW at the $\overline{\text{RESET}}$ pin. Asserting $\overline{\text{RESET}}$ resets all internal dividers, and will cause the PLL to lose lock. On losing lock, the VCO frequency will begin dropping.

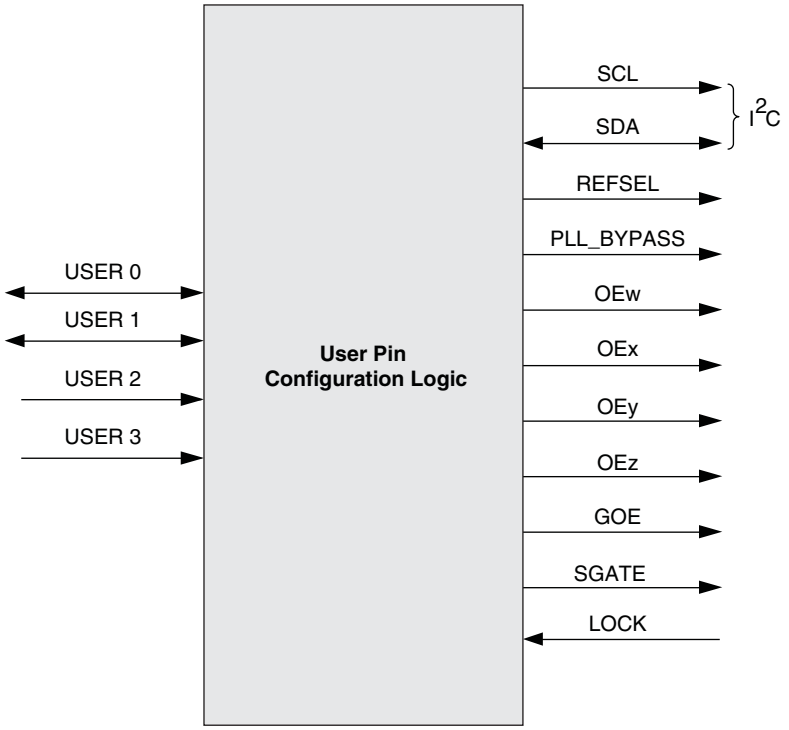
If the $\overline{\text{RESET}}$ pin is not driven by an external logic it should be pulled up to V_{CCD} through a 10kΩ resistor.

USER [0..3] Pins

The ispClock5400D provides a set of four user configurable pins, USER[0..3], which can be configured to control different aspects of the device through external hardware logic. Figure 2-31 shows all the control functions which can be allocated to USER pins. Each of these USER pins can independently be configured as Active low/ Active high with internal pull-up/pull-down resistors. The USER 0 and USER 1 pins support both input and output while USER2 and USER3 only support input.

The configuration logic allocation is stored in the on-chip non-volatile E^2CMOS configuration.

Figure 2-31. ispClock5400D USER[0..3] Pins Configuration



Control/Status Signals That Can be Allocated to USER[0..3] Pins

Each of these control signals, with the exception of SGATE signal can be controlled by the I²C interface or it can be programmed to logic '0' or Logic '1' in from the on-chip, non-volatile E²CMOS configuration.

I²C Interface (SCL, SDA)

The SCL and SDA signals must be assigned to the USER pins in order to control the ispClock5400D device through the I²C interface. Note when I²C is enabled, SCL is connected to USER2 and SDA is connected to USER1 pins.

The details of control functions which can be accessed through the I²C interface are discussed in the I²C Interface section.

REFSEL

The REFSEL signal is used to select the active clock from the two reference clock inputs, REFA and REFB.

Control Signal	Logic State	Output
REFSEL (Active High)	0	REFA Input Selected for PLL
	1	REFB Input Selected for PLL

PLL_BYPASS

The on-chip PLL of the ispClock5400D device can be bypassed by using the PLL_BYPASS signal. If the PLL_BYPASS signal is not routed to the USER pins, it can be controlled by I²C interface only if the PLL_BYPASS bit is programmed as Logic 1 in the on-chip, non-volatile E²CMOS configuration.

Control Signal	Logic State	Output
PLL_Bypass (Active High)	0	PLL Bypassed
	1	PLL Active

OEw, OEx, OEy, OEz, GOE

The ispClock5400D family provides five output control pins for enabling and disabling clock outputs. Any of the OE[w..z] signals can be allocated to control any number of output pins. In addition, the GOE signal disables all the outputs. Note that the OE is an asynchronous signal and it can cause runt clock pulses.

Control Signal	Logic State	Output
OEw, OEx, OEy, OEz, GOE (Active High)	0	Output Active
	1	Output Tristate

SGATE

The SGATE (Synchronous Gate Control) signal turns the clock on or off without generating runt clock pulses. The internal synchronization logic ensures that the output controlled by the SGATE signal completes the clock cycle before settling at logic '0' or logic '1' depending on the output clock invert configuration. Any output can be controlled by the SGATE signal. Because the SGATE signal cannot be controlled by the I^2C interface, this signal should be routed to USER pins if this feature is required.

Control Signal	Logic State	Output
SGATE (Active High)	0	Output Not Controlled by SGATE
	1	Output Disabled By SGATE

LOCK

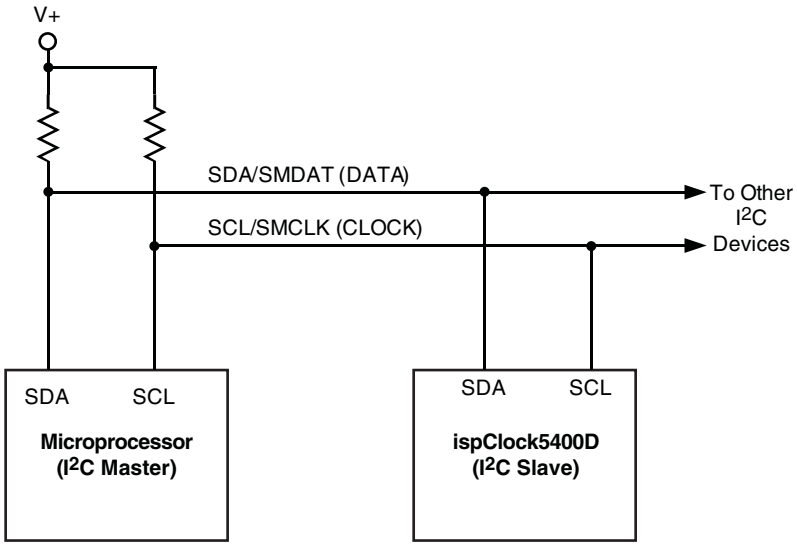
This is the only status signal which can be routed to the USER pins. The lock-detection feature is associated with the PFD in the PLL. When the ispClock5400D is in a LOCKED state, the LOCK output pin goes HIGH or LOW depending on the configuration. The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 through 256. Note that the LOCK signal can be allocated only to the USER 0 pin.

I^2C/SMBus Interface

I^2C and SMBus are low-speed serial interface protocols designed to enable communications among a number of devices on a circuit board. The ispClock5400D supports a 7-bit addressing of the I^2C communications protocol. Figure 2-32 shows a typical I^2C configuration, in which one or more ispClock5400D devices are slaved to a microcontroller. SDA is used to carry data signals, while SCL provides a synchronous clock signal. The 7-bit I^2C address of the ispClock5400D is fully programmable through the JTAG port.

In both the I^2C and SMBus protocols, the bus is controlled by a single MASTER device at any given time. This master device generates the SCL clock signal and coordinates all data transfers to and from a number of slave devices. The ispClock5400D is configured as a slave device and cannot independently coordinate data transfers.

Figure 2-32. ispClock5400D in an I²C/SMBus System



Each slave device on a given I²C bus is assigned a unique address. The ispClock5400D implements the 7-bit addressing portion of the standard. Any 7-bit address can be assigned to the ispClock5400D device by programming through JTAG. When selecting a device address, note that several addresses are reserved by the I²C and/or SMBus standards, and should not be assigned to ispClock5400D devices to assure bus compatibility. Table 2-4 lists these reserved addresses.

Table 2-4. I²C/SMBus Reserved Slave Device Addresses

Address	R/W	I²C Function	SMBus Function
0000 000	0	General Call Address	General Call Address
0000 000	1	Start Byte	Start Byte
0000 001	x	CBUS Address	CBUS Address
0000 010	x	Reserved	Reserved
0000 011	x	Reserved	Reserved
0000 1xx	x	HS Mode Master Code	HS Mode Master Code
0001 000	x	N/A	SMBus Host
0001 100	x	N/A	SMBus Alert Response Alert Response Address
0101 000	x	N/A	Reserved for ACCESS.bus
0110 111	x	N/A	Reserved for ACCESS.bus
1100 001	x	N/A	SMBus Device Default Address
1111 0xx	x	10-Bit Addressing	10-Bit Addressing
1111 1xx	x	Reserved	Reserved

The ispClock5400D's I²C/SMBus interface allows data to be both written to and read from the device. A data write transaction (Figure 2-33) consists of the following operations:

1. Start the bus transaction

2. Transmit the device address (7 bits) along with a low write bit

3. Transmit the address of the register to be written to (8 bits)

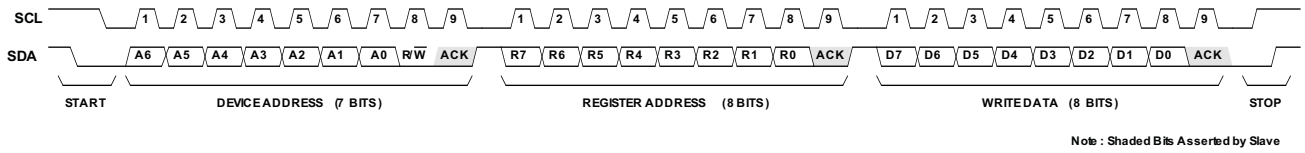
4. Transmit the data to be written (8 bits)

5. Stop the bus transaction

To start the transaction, the master device holds the SCL line high while pulling SDA low. Address and data bits are then transferred on each successive SCL pulse, in three consecutive byte frames of nine SCL pulses. Address and data are transferred on the first eight SCL clocks in each frame, while an acknowledge signal is asserted by the slave device on the ninth clock in each frame. Both data and addresses are transferred in a most-significant-bit-first format.

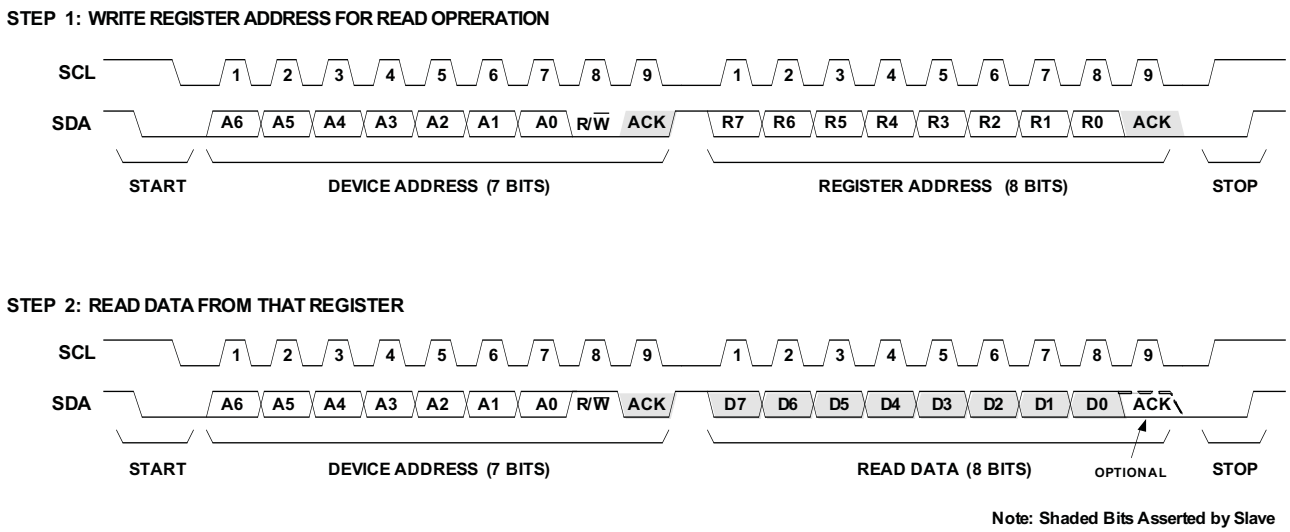
The first frame contains the 7-bit device address, with bit 8 held low to indicate a write operation. The second frame contains the register address to which data will be written, and the final frame contains the actual data to be written. Note that the SDA signal is only allowed to change when the SCL is low, as raising SDA when SCK is high signals the end of the transaction.

Figure 2-33. I²C Write Operation



Reading a data byte from the ispClock5400D requires two separate bus transactions (Figure 2-34). The first transaction writes the register address from which a data byte is to be read. Note that since no data is being written to the device, the transaction is concluded after the second byte frame. The second transaction performs the actual read. The first frame contains the 7-bit device address with the R/W bit held High. In the second frame the ispClock5400D asserts data out on the bus in response to the SCK signal. Note that the acknowledge signal in the second frame is asserted by the master device and not the ispClock5400D.

Figure 2-34. I²C Read Operation



The ispClock5400D provides 28 registers that can be accessed through its I²C interface. These registers provide the user with the ability to control most of the programmable features of the device. Table 2-6 provides a summary of these registers.

Table 2-5. Summary of ispClock5406D I²C Registers

Hex Address	I²C R/W	Value After POR[1]	Bit Assignment								Description
			7	6	5	4	3	2	1	0	
00	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 0, BANK_0 Control
01	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 0, BANK_1 Control
02	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
03	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
04	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 1, BANK_2 Control
05	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 1, BANK_3 Control
06	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
07	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
08	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 2, BANK_4 Control
09	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 2, BANK_5 Control
0A	RW	E²CMOS	0	EN-I-FBK	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Internal Feedback Control
0B		N/A	0	0	0	0	0	0	0	0	Reserved
0C		N/A	0	0	0	0	0	0	0	0	Reserved
0D	RW	E²CMOS	T-SKEW_1-3	T-SKEW_1-2	T-SKEW_1-1	T-SKEW_1-0	T-SKEW_0-3	T-SKEW_0-2	T-SKEW_0-1	T-SKEW_0-0	Output Group 0 Time Skew
0E	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
0F	RW	E²CMOS	T-SKEW_5-3	T-SKEW_5-2	T-SKEW_5-1	T-SKEW_5-0	T-SKEW_4-3	T-SKEW_4-2	T-SKEW_4-1	T-SKEW_4-0	Output Group 1 Time Skew
10	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
11	RW	E²CMOS	T-SKEW_9-3	T-SKEW_9-2	T-SKEW_9-1	T-SKEW_9-0	T-SKEW_8-3	T-SKEW_8-2	T-SKEW_8-1	T-SKEW_8-0	Output Group 2 Time Skew
12	RW	E²CMOS	EN-T-SKEW_5	EN-T-SKEW_4	0	0	EN-T-SKEW_3	0	0	0	Time Skew Mechanism Enable
13	RW	E²CMOS	EN-T-SKEW_2	0	0	EN-T-SKEW_1	EN-T-SKEW_0	0	0	0	Time Skew Mechanism Enable
14	RW	E²CMOS	0	0	0	0	0	0	REFSEL	PLL_BYPASS	PLL Control
15	RW	E²CMOS	FOB-BANK_5	FOB-BANK_4	0	0	FOB-BANK_3	0	0	0	FAN OUT Buffer Selection
16	RW	E²CMOS	FOB-BANK_2	0	0	FOB-BANK_1	FOB-BANK_0	0	0	0	FAN OUT Buffer Selection
17	RW	E²CMOS	FOB-REFSEL_45	0	FOB-REFSEL_23	0	FOB-REFSEL_01	0	0	0	FOB Reference Clock/Output Group
18	W	E²CMOS	1	0	1	1	0	1	0	0	Safe State
19	W	E²CMOS	0	1	0	1	1	0	1	0	Soft Reset
1A	W	E²CMOS	1	1	1	0	1	0	0	1	Full Reset
1B	R	E²CMOS	$\overline{UES07}$	$\overline{UES06}$	$\overline{UES05}$	$\overline{UES04}$	$\overline{UES03}$	$\overline{UES02}$	$\overline{UES01}$	$\overline{UES00}$	UES Byte 0[2]
1C	R	E²CMOS	$\overline{UES15}$	$\overline{UES14}$	$\overline{UES13}$	$\overline{UES12}$	$\overline{UES11}$	$\overline{UES10}$	$\overline{UES09}$	$\overline{UES08}$	UES Byte 1[2]
1D	R	E²CMOS	$\overline{UES23}$	$\overline{UES22}$	$\overline{UES21}$	$\overline{UES20}$	$\overline{UES19}$	$\overline{UES18}$	$\overline{UES17}$	$\overline{UES16}$	UES Byte 2[2]
1E	R	E²CMOS	$\overline{UES31}$	$\overline{UES30}$	$\overline{UES29}$	$\overline{UES28}$	$\overline{UES27}$	$\overline{UES26}$	$\overline{UES25}$	$\overline{UES24}$	UES Byte 3[2]
1F		N/A	0	0	0	0	0	0	0	0	Reserved
20		N/A	0	0	0	0	0	0	0	0	Reserved

1. OE data is not associated with E²CMOS. Bits are 0 after POR.
2. UES register bits are inverted.

Table 2-6. Summary of ispClock5410D I²C Registers

Hex Address	I²C R/W	Value After POR[1]	Bit Assignment								Description
			7	6	5	4	3	2	1	0	
00	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 0, BANK_0 Control
01	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 0, BANK_1 Control
02	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 1, BANK_2 Control
03	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 1, BANK_3 Control
04	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 2, BANK_4 Control
05	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 2, BANK_5 Control
06	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 3, BANK_6 Control
07	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 3, BANK_7 Control
08	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 4, BANK_8 Control
09	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 4, BANK_9 Control
0A	RW	E²CMOS	0	EN-I-FBK	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Internal Feedback Control
0B		N/A	0	0	0	0	0	0	0	0	Reserved
0C		N/A	0	0	0	0	0	0	0	0	Reserved
0D	RW	E²CMOS	T-SKEW_1-3	T-SKEW_1-2	T-SKEW_1-1	T-SKEW_1-0	T-SKEW_0-3	T-SKEW_0-2	T-SKEW_0-1	T-SKEW_0-0	Output Group 0 Time Skew
0E	RW	E²CMOS	T-SKEW_3-3	T-SKEW_3-2	T-SKEW_3-1	T-SKEW_3-0	T-SKEW_2-3	T-SKEW_2-2	T-SKEW_2-1	T-SKEW_2-0	Output Group 1 Time Skew
0F	RW	E²CMOS	T-SKEW_5-3	T-SKEW_5-2	T-SKEW_5-1	T-SKEW_5-0	T-SKEW_4-3	T-SKEW_4-2	T-SKEW_4-1	T-SKEW_4-0	Output Group 2 Time Skew
10	RW	E²CMOS	T-SKEW_7-3	T-SKEW_7-2	T-SKEW_7-1	T-SKEW_7-0	T-SKEW_6-3	T-SKEW_6-2	T-SKEW_6-1	T-SKEW_6-0	Output Group 3 Time Skew
11	RW	E²CMOS	T-SKEW_9-3	T-SKEW_9-2	T-SKEW_9-1	T-SKEW_9-0	T-SKEW_8-3	T-SKEW_8-2	T-SKEW_8-1	T-SKEW_8-0	Output Group 5 Time Skew
12	RW	E²CMOS	EN-T-SKEW_9	EN-T-SKEW_8	EN-T-SKEW_7	EN-T-SKEW_6	EN-T-SKEW_5	0	0	0	Time Skew Mechanism Enable
13	RW	E²CMOS	EN-T-SKEW_4	EN-T-SKEW_3	EN-T-SKEW_2	EN-T-SKEW_1	EN-T-SKEW_0	0	0	0	Time Skew Mechanism Enable
14	RW	E²CMOS	0	0	0	0	0	0	REFSEL	PLL_BYPASS	PLL Control
15	RW	E²CMOS	FOB-BANK_9	FOB-BANK_8	FOB-BANK_7	FOB-BANK_6	FOB-BANK_5	0	0	0	FAN OUT Buffer Selection
16	RW	E²CMOS	FOB-BANK_4	FOB-BANK_3	FOB-BANK_2	FOB-BANK_1	FOB-BANK_0	0	0	0	FAN OUT Buffer Selection
17	RW	E²CMOS	FOB-REFSEL_89	FOB-REFSEL_67	FOB-REFSEL_45	FOB-REFSEL_23	FOB-REFSEL_01	0	0	0	FOB Reference Clock/Output Group
18	W	E²CMOS	1	0	1	1	0	1	0	0	Safe State
19	W	E²CMOS	0	1	0	1	1	0	1	0	Soft Reset
1A	W	E²CMOS	1	1	1	0	1	0	0	1	Full Reset
1B	R	E²CMOS	$\overline{UES07}$	$\overline{UES06}$	$\overline{UES05}$	$\overline{UES04}$	$\overline{UES03}$	$\overline{UES02}$	$\overline{UES01}$	$\overline{UES00}$	UES Byte 0[2]
1C	R	E²CMOS	$\overline{UES15}$	$\overline{UES14}$	$\overline{UES13}$	$\overline{UES12}$	$\overline{UES11}$	$\overline{UES10}$	$\overline{UES09}$	$\overline{UES08}$	UES Byte 1[2]
1D	R	E²CMOS	$\overline{UES23}$	$\overline{UES22}$	$\overline{UES21}$	$\overline{UES20}$	$\overline{UES19}$	$\overline{UES18}$	$\overline{UES17}$	$\overline{UES16}$	UES Byte 2[2]
1E	R	E²CMOS	$\overline{UES31}$	$\overline{UES30}$	$\overline{UES29}$	$\overline{UES28}$	$\overline{UES27}$	$\overline{UES26}$	$\overline{UES25}$	$\overline{UES24}$	UES Byte 3[2]
1F		N/A	0	0	0	0	0	0	0	0	Reserved
20		N/A	0	0	0	0	0	0	0	0	Reserved

1. OE data is not associated with E²CMOS. Bits are 0 after POR.
2. UES register bits are inverted.

I²C Register Descriptions

Output Group [0..4], Bank[0..9] Control – Register Address# [00H..09H]

Two successive address locations control an Output Group. For example, addresses 00H and 01H control Output Group 0 (Bank_0 and Bank_1). The control bits are as follows:

- **INVERT** – Inverts the output clock when reset to 0.
- **OE** – When set to 1, tri-states that output if the output has been programmed to be controlled by I²C. Otherwise, this bit will be ignored. (E²CMOS or USER pin output disable has priority over I²C).
- **FREQ-SEL[1,0]** – Selects the V-divider for that Output Group (shown in the table below). The corresponding bits for the second output of that Output Group should be set to 11.

FREQ-SEL-1	FREQ-SEL-0	V-divider Selection
0	0	÷2
0	1	÷4
1	0	÷8
1	1	÷16

- **P-SKEW[3..0]** – Sets the clock phase skew for that output. The actual delay can be set from 0 to 15 Phase Delay Units.

Internal Feedback Control – Register Address# 0AH

The ispClock5400D PLL feedback can be derived either externally from the FBK pin or internally directly from the Output Routing Matrix. The control bits are as follows:

- **EN-I-FBK** – When set, enables the internal feedback path. The output clock connected to the FBK pins is ignored at that time.
- **FREQ-SEL[1,0]** – Selects the V-divider for the internal feedback clock (shown in the table below).

FREQ-SEL-1	FREQ-SEL-0	V-divider Selection
0	0	÷2
0	1	÷4
1	0	÷8
1	1	÷16

Note: Avoid exceeding maximum f_{VCO} when changing feedback V-divider setting.

- **P-SKEW[3..0]** – Sets the clock phase skew for the internal feedback clock. The actual delay can be set from 0 to 15 Phase Delay Units.

Output Group [0..4] Time Skew Control – Register Address [0DH..11H]

Each byte enables controlling of time skew of both the banks in that output group. For example, Address 0DH controls Time Skew of Bank_0 and Bank_1.

- **T-SKEW_1-[3..0]** – Sets the clock time skew for the Bank_1 clock. The actual delay can be set from 0 to 15 Time Delay Units.
- **T-SKEW_0-[3..0]** – Sets the clock time skew for the Bank_0 clock. The actual delay can be set from 0 to 15 Time Delay Units.

Enable Time Skew Control Mechanism – Register Address [12..13]

Each enable bit, when set, enables the time skew mechanism for that bank. For example, EN-TSKEW_9 bit, when set, enables the Time Skew mechanism for Bank_9 output clock. The Bank_9 output clock skew delay value are determined by T-SKEW_9-[3..0] bits at address location 11H. E²CMOS settings must be such that Time Skew is powered up for any bank for which Time Skew control is desired.

PLL Control – Register Address – 14H

This register selects the active clock routed to the PLL as well as the PLL bypass control.

- **REFSEL** – REFA input clock gets routed to the PLL when this bit is reset to 0 and when set, the REFB input clock will be routed to PLL.
- **PLL_BYPASS** – When reset to 0, bypasses the PLL and deactivates the Phase Skew Control mechanism for all banks. The P-SKEW[3..0] setting will be ignored. However, the T-Skew mechanism can still be activated on a bank-by bank basis.E^2CMOS settings must be such that PLL mode is enabled. E^2CMOS and USER pin control of PLL bypass overrides I^2C control.

Fan-out Buffer (FOB) Selection – Register Address# – [15H..16H]

The Output Routing Matrix connects a clock from either the PLL or directly from either of the reference clocks to an Output Group. The two banks in that Output Group can then be individually configured to output either the clock from the PLL or from the Reference clock using these bits.

For example, the Bank_2 will output Reference clock when FOB-BANK_2 bit is set at register 16.

- **FOB_Bank_[9..0]** – When set, outputs the Reference clock connected to that Output Group.

FOB Reference Clock per Output Group Selection – Register Address# – 17H

Any output group can receive the clock either from the PLL or from the input reference clock. The FOB-REFSEL_01..FOB-REFSEL_04 bits enable the selection between the REFA and REFB clocks. For example, FOB-REFSEL_23 bit, when set, enables REFB clock to Output Group 1 and when reset to 0, enables REFA clock to Output Group 1.

Safe State - Register Address# – 18H, Followed by Data Byte Value = B4H

After a value of B4H is written into the Address location 18H, the ispClock5400D enters the safe state. During this state, all clock outputs are tri-stated. One can use this instruction to stop the output clocks before updating the I^2C registers. Writing a code other than B4H into the same location brings the device back out of the safe state mode; all the clocks will be operational. Safe State tristates all outputs including those that are in Fan-out Buffer mode.

Note: The activation of safe state can result in runt clock output. If runt clocks are not desired, one should disable the clock using the SGATE feature, before entering the safe state.

Soft Reset – Register Address# – 19H, Followed by Data Byte Value = 5AH

The ispClock5400D device enters the Soft Reset state as soon as the 5AH is written into the address location 19H. During this state the PLL, Dividers, Phase and Time Skew blocks are reset. The actual configuration is not changed. Writing a value other than 5AH into address location 19H brings ispClock5400D device out of the soft reset mode and all outputs begin to output clocks with delays as configured. During Soft Reset, differential outputs are low. Note that Soft Reset does not affect outputs that are in Fan-out Buffer mode.

Full Reset - Register Address# – 1AH, Followed by Data Byte Value = E9H

The ispClock5400D device enters full reset state as soon as a value of E9H is written into address location of 1AH. During this state, all configuration registers are updated from the E^2CMOS configuration. All the values loaded by I^2C will be overwritten. This command is equivalent to toggling the RESETb pin of the ispClock5400D device. Writing a value other than E9H to the same location will bring the device out of Full Reset. During Full Reset, differential outputs are low. Note that Full Reset does not affect the outputs that are in Fan-out Buffer mode.

User Electronic Signature (UES) - Register Address# – [1BH..1EH]

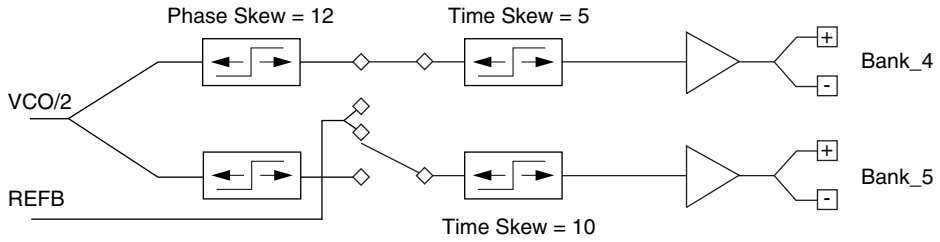
Using the I^2C interface, one can read all 32 bits of programmed UES bits from the locations 1BH to 1FH. Note: These four locations are read only and each of the UES bits is inverted.

Example

The following describes Output Group 2 (Bank_4 and Bank_5) configuration. Refer to Figure 2-35.

- Bank_4 output Non-inverted clock received from V-divider ÷2 (Frequency = VCO Clock/2)
- Bank_5 output Inverted clock Received from REFB
- Phase Skew for Bank_4 output clock set to 12 PUD
- Time Skew for Bank_4 output clock set to 5 TUD
- It is not possible to set Phase Skew for Bank_5 because it does not derive clock from PLL The Phase Skew value set in the register will be ignored.
- Time Skew for Bank_5 output clock set to 10 TUD
- All other banks are not used

Figure 2-35. Example Configuration of ispClock5410D Output Group 2



The I^2C Register Bit values for this configuration are as follows:

Register Address# 04H (Output Group 2, Bank_4 Output Control) = '1000 1100' B
INVERT = 1, OE = 0, FREQ_SEL[1..0] = 00B (0), P-SKEW[3..0] = 1100B (12)

Register Address# 05H (Output Group 2,Bank_5 Output Control) = '0011 0000' B
INVERT = 0, OE = 0, FREQ_SEL[1..0] = 11B, P-SKEW[3..0] = 0000B (0)

Register Address# 0FH (Output Group 2 Time Skew) = '1010 0101B'
T-SKEW_4-[3..0] = 0101B (5 TUD), T-SKEW_5-[3..0] = 1010B (10 TUD)

Register Address# 12H (Time Skew Mechanism Enable) = '0000 1000'B
EN-TSKEW_5 = 1 (T-Skew mechanisms for Banks 6 to 9 have been turned off)

Register Address# 13H (Time Skew Mechanism Enable) = '1000 0000'B
EN-TSKEW_4 = 1 (T-Skew mechanisms for Banks 0 to 3 have been turned off)

Register Address# 15H (Fan out Buffer Selection) = '0000 1000'B
FOB-BANK_5 = 1, (BANK_6 to BANK_9 are connected to V-dividers)

Register Address# 16H (Fan out Buffer Selection) = '0000 0000'B
(BANK_0 to BANK_4 are connected to V-dividers)

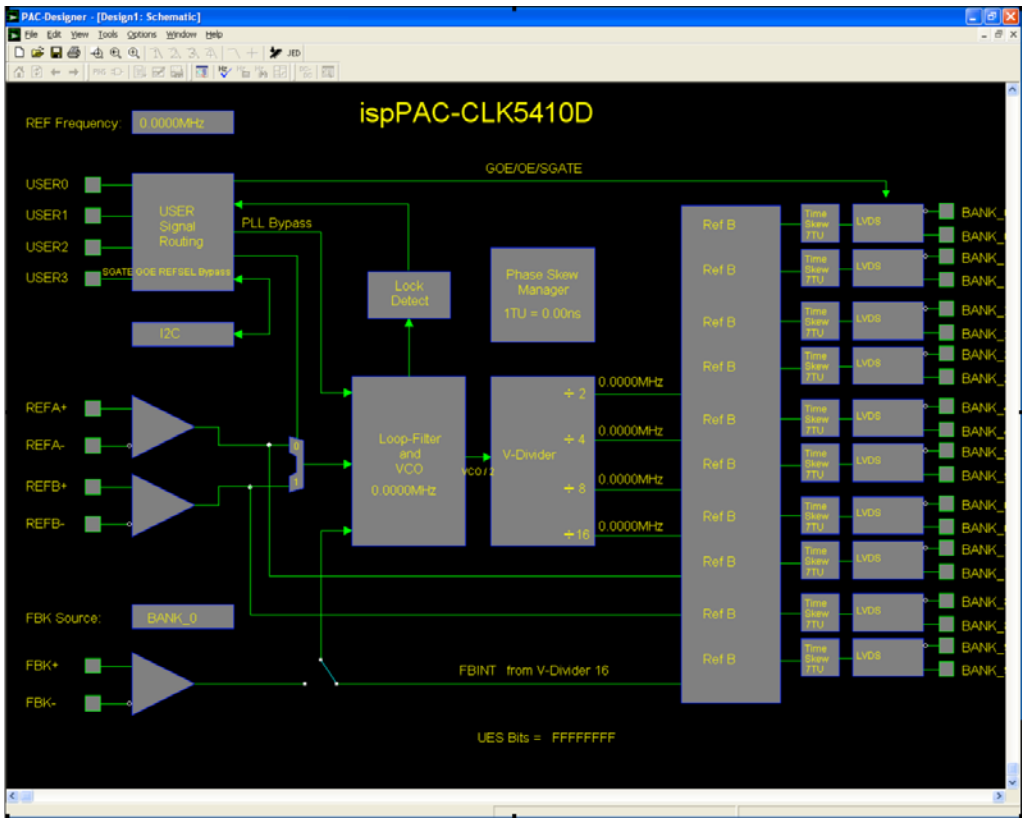
Register Address# 17H (FOB Reference clock per Output Group) = '0010 0000'B
FOB-REFSEL_54 = 1, (REFB Clock is selected for BANK_5 and BANK_4)

Software-Based Design Environment

Designers can configure the ispClock5400D using Lattice's PAC-Designer software, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispClock5400D. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation. PAC-Designer is available for

download from the Lattice web site. The PAC-Designer schematic window, shown in Figure 2-36 provides access to all configurable ispClock5400D elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved and downloaded to devices.

Figure 2-36. PAC-Designer Design Entry Screen



In-System Programming

The ispClock5400D is an In-System Programmable (ISP™) device. This is accomplished by integrating all E^{2}CMOS configuration control logic on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^{2}CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispClock5400D instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

A user electronic signature (UES) feature is included in the E^{2}CMOS memory of the ispClock5400D. This consists of 32 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Electronic Security

An electronic security “fuse” (ESF) bit is provided in every ispClock5400D device to prevent unauthorized readout of the E^{2}CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can not be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Production Programming Support

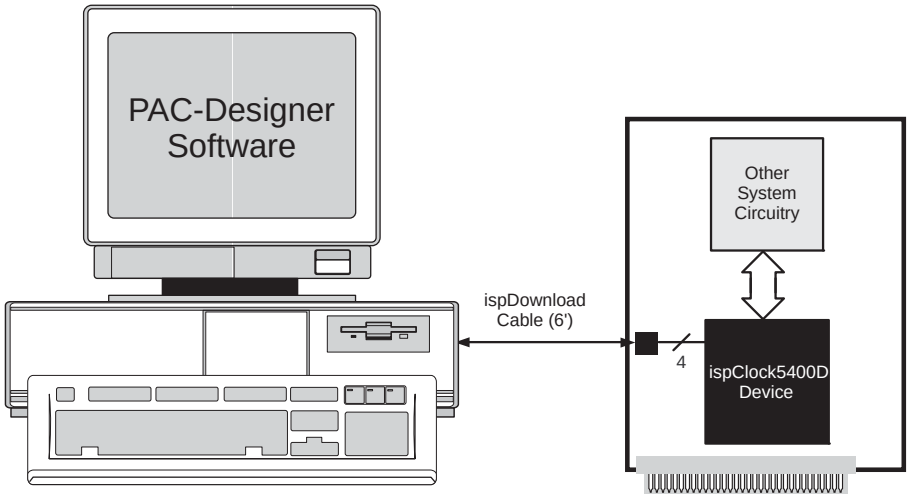
Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user's specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

Evaluation Fixture

Included in the basic ispClock5400D Design Kit is an engineering prototype board that can be connected to the parallel port of a PC using a Lattice ispDOWNLOAD® cable. It demonstrates proper layout techniques for the ispClock5400D and can be used in real time to check circuit operation as part of the design process. Input and output connections (SMA connectors for all RF signals) are provided to aid in the evaluation of the ispClock5400D for a given application. (Figure 2-37).

Part Number	Description
PACCLK5406D-P-EVN	Complete system kit, evaluation board, ispDOWNLOAD cable and software.

Figure 2-37. Download from a PC



IEEE Standard 1149.1 Interface (JTAG)

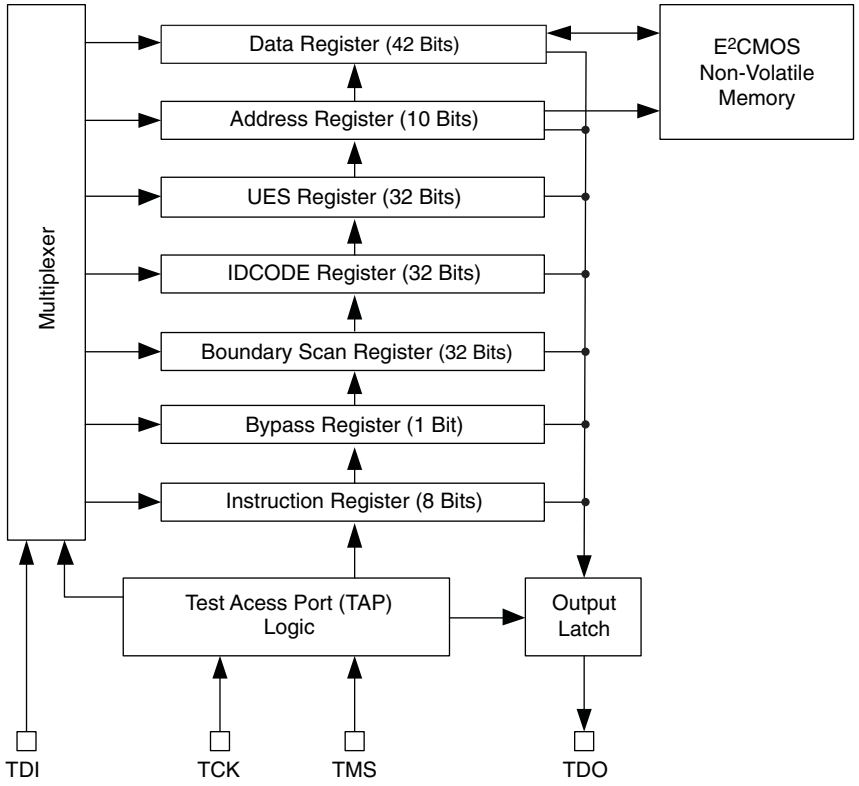
Serial Port Programming Interface Communication with the ispClock5400D is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispClock5400D both as a serial programming interface, and for boundary scan test purposes. A brief description of the ispClock5400D JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990 (which now includes IEEE Std. 1149.1a-1993).

Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispClock5400D. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E^2CMOS cells. It is these non-volatile cells that store the configuration of the ispClock5400D. A set of instructions are defined that access all data registers and perform other internal control operations. For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manu-

facturer. The two required registers are the bypass and boundary-scan registers. Figure 2-38 shows how the instruction and various data registers are organized in an ispClock5400D.

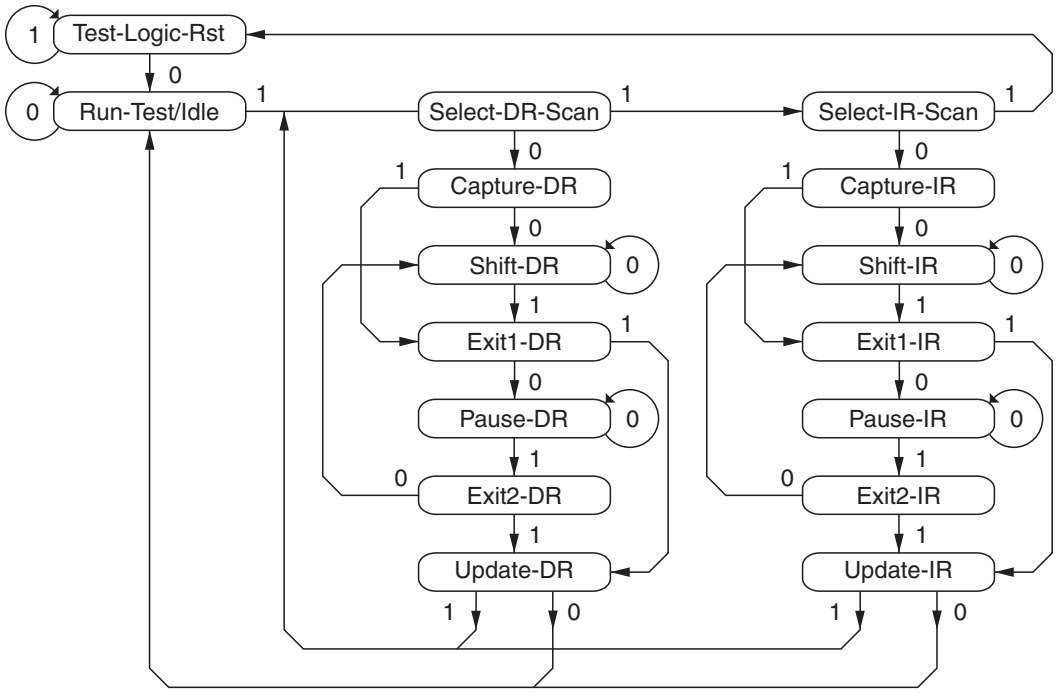
Figure 2-38. ispClock5400D TAP Registers



TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the TMS input as shown in Figure 2-39. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run- Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

Figure 2-39. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain. From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispClock5400D contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified.

For ispClock5400D, the instruction word length is eight bits. All ispClock5400D instructions available to users are shown in Table 2-7.

The following table lists the instructions supported by the ispClock5400D JTAG Test Access Port (TAP) controller:

Table 2-7. ispClock5400D TAP Instruction Table

Instruction	Code	Description
EXTEST	0000 0000	External Test.
ADDRESS_SHIFT	0000 0001	Address register (10 bits)
DATA_SHIFT	0000 0010	Address column data register (42 bits for ispClock5410D and 5406D)
BULK_ERASE	0000 0011	Bulk Erase
PROGRAM	0000 0111	Program column data register to E^2
PROGRAM_SECURITY	0000 1001	Program Electronic Security Fuse
VERIFY	0000 1010	Verify column
DISCHARGE	0001 0100	Fast VPP Discharge
PROGRAM_ENABLE	0001 0101	Enable Program Mode
IDCODE	0001 0110	Address Manufacturer ID code register (32 bits)
USERCODE	0001 0111	Read UES data from E^2 and addresses UES register (32 bits)
PROGRAM_USERCODE	0001 1010	Program UES register into E^2
PROGRAM_DISABLE	0001 1110	Disable Program Mode
HIGHZ	0001 1000	Force all outputs to High-Z state
SAMPLE/PRELOAD	0001 1100	Capture current state of pins to boundary scan register
CLAMP	0010 0000	Drive I/Os with boundary scan register
INTEST	0010 1100	Performs in-circuit functional testing of device.
ERASE DONE	0010 0100	Erases the ‘Done’ bit only
PROG_INCR	0010 0111	Program column data register to E^2 and auto-increment address register
VERIFY_INCR	0010 1010	Load column data register from E^2 and auto-increment address register
PROGRAM_DONE	0010 1111	Programs the ‘Done’ Bit
NOOP	0011 0000	Functions Similarly to CLAMP instruction
BYPASS	1xxx xxxx	Bypass - Connect TDO to TDI

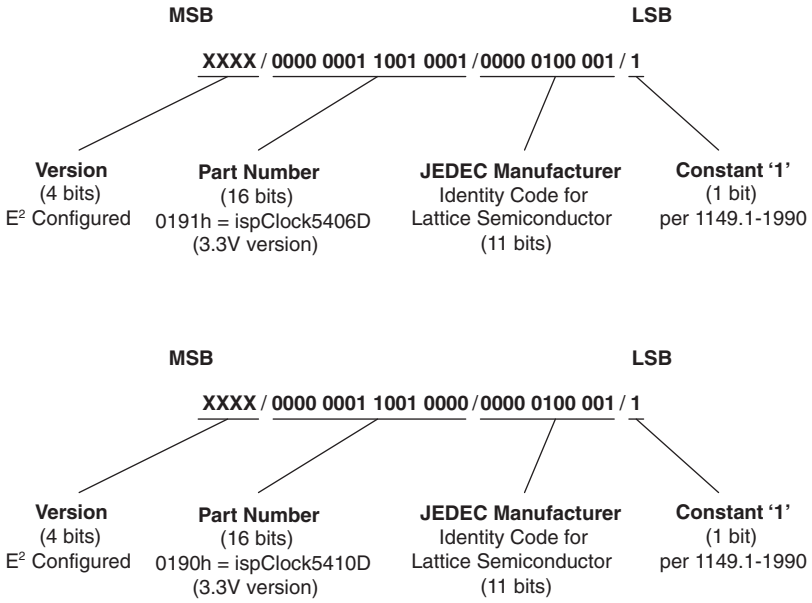
BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispClock5400D. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (111111).

The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The bit code for this instruction is defined by Lattice as shown in Table 2-7.

The **EXTEST** (external test) instruction is required and will place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispClock5400D and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device type and version code (Figure 2-40). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 2-7.

Figure 2-40. ispClock5400D Family ID Codes



In addition to the four instructions described above, there are 20 unique instructions specified by Lattice for the ispClock5400D. These instructions are primarily used to interface to the various user registers and the E^{2}CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device, including boundary scan operations. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 2-7.

PROGRAM_ENABLE – This instruction enables the ispClock5400D programming mode.

PROGRAM_DISABLE – This instruction disables the ispClock5400D programming mode.

BULK_ERASE – This instruction will erase all E^{2}CMOS bits in the device, including the UES data and electronic security fuse (ESF). A bulk erase instruction must be issued before reprogramming a device. The device must already be in programming mode for this instruction to execute.

ADDRESS_SHIFT – This instruction shifts address data into the address register (10 bits) in preparation for either a PROGRAM or VERIFY instruction.

DATA_SHIFT – This instruction shifts data into or out of the data register (43 bits), and is used with both the PROGRAM and VERIFY instructions.

PROGRAM – This instruction programs the contents of the data register to the E^{2}CMOS memory column pointed to by the address register. The device must already be in programming mode for this instruction to execute.

PROG_INCR – This instruction first programs the contents of the data register into E^{2}CMOS memory column pointed to by the address register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

PROGRAM_SECURITY – This instruction programs the electronic security fuse (ESF). This prevents data other than the ID code and UES strings from being read from the device. The electronic security fuse may only be reset by issuing a BULK_ERASE command. The device must already be in programming mode for this instruction to execute.

VERIFY – This instruction loads data from the E^{2}CMOS array into the column register. The data may then be shifted out. The device must already be in programming mode for this instruction to execute.

VERIFY_INCR – This instruction copies the E^2CMOS column pointed to by the address register into the data column register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispClock5400D for a read cycle.

PROGRAM_USERCODE – This instruction writes the contents of the UES register (32 bits) into E^2CMOS memory. The device must already be in programming mode for this instruction to execute.

USERCODE – This instruction both reads the UES string (32 bits) from E^2CMOS memory into the UES register and addresses the UES register so that this data may be shifted in and out.

HIGHZ – This instruction forces all outputs into a High-Z state.

CLAMP – This instruction drives I/O pins with the contents of the boundary scan register.

INTEST – This instruction performs in-circuit functional testing of the device.

ERASE_DONE – This instruction erases the ‘DONE’ bit only. This instruction is used to disable normal operation of the device while in programming mode until a valid configuration pattern has been programmed.

PROGRAM_DONE – This instruction programs the ‘DONE’ bit only. This instruction is used to enable normal device operation after programming is complete.

NOOP – This instruction behaves similarly to the CLAMP instruction.

Pin Descriptions – ispClock5410D, 5406D

Pin Name	Description	Pin Type	Pin Number	
			ispClock5410D 64-Pin QFNS	ispClock5406D 48-Pin QFNS
VCCO_0	VCC For BANK_0 Output Driver	Power	46	33
VCCO_1	VCC For BANK_1 Output Driver	Power	45	32
VCCO_2	VCC For BANK_2 Output Driver	Power	39	25
VCCO_3	VCC For BANK_3 Output Driver	Power	38	12
VCCO_4	VCC For BANK_4 Output Driver	Power	32	5
VCCO_5	VCC For BANK_5 Output Driver	Power	17	4
VCCO_6	VCC For BANK_6 Output Driver	Power	11	
VCCO_7	VCC For BANK_7 Output Driver	Power	10	
VCCO_8	VCC For BANK_8 Output Driver	Power	4	
VCCO_9	VCC For BANK_9 Output Driver	Power	3	
GNDO_0	GND For BANK_0 Output Driver	GND	49	36
GNDO_1	GND For BANK_1 Output Driver	GND	42	29
GNDO_2	GND For BANK_2 Output Driver	GND		28
GNDO_3	GND For BANK_3 Output Driver	GND	35	9
GNDO_4	GND For BANK_4 Output Driver	GND		8
GNDO_5	GND For BANK_5 Output Driver	GND	14	1
GNDO_6	GND For BANK_6 Output Driver	GND		
GNDO_7	GND For BANK_7 Output Driver	GND	7	
GNDO_8	GND For BANK_8 Output Driver	GND		
GNDO_9	GND For BANK_9 Output Driver	GND	64	
BANK_0P	Bank_0 Clock Output Driver Positive	Output	48	35
BANK_0N	Bank_0 Clock Output Driver Negative	Output	47	34
BANK_1P	Bank_1 Clock Output Driver Positive	Output	44	31
BANK_1N	Bank_1 Clock Output Driver Negative	Output	43	30
BANK_2P	Bank_2 Clock Output Driver Positive	Output	41	27
BANK_2N	Bank_2 Clock Output Driver Negative	Output	40	26
BANK_3P	Bank_3 Clock Output Driver Positive	Output	37	10
BANK_3N	Bank_3 Clock Output Driver Negative	Output	36	11
BANK_4P	Bank_4 Clock Output Driver Positive	Output	34	6
BANK_4N	Bank_4 Clock Output Driver Negative	Output	33	7
BANK_5P	Bank_5 Clock Output Driver Positive	Output	15	2
BANK_5N	Bank_5 Clock Output Driver Negative	Output	16	3
BANK_6P	Bank_6 Clock Output Driver Positive	Output	12	
BANK_6N	Bank_6 Clock Output Driver Negative	Output	13	
BANK_7P	Bank_7 Clock Output Driver Positive	Output	8	
BANK_7N	Bank_7 Clock Output Driver Negative	Output	9	
BANK_8P	Bank_8 Clock Output Driver Positive	Output	5	
BANK_8N	Bank_8 Clock Output Driver Negative	Output	6	
BANK_9P	Bank_9 Clock Output Driver Positive	Output	1	
BANK_9N	Bank_9 Clock Output Driver Negative	Output	2	
VCCA	Analog VCC for the PLL Circuitry	Power	28,30	23
GNDA	Analog GND for the PLL Circuitry	GND	18	13

Pin Descriptions – ispClock5410D, 5406D (Continued)

Pin Name	Description	Pin Type	Pin Number	
			ispClock5410D 64-Pin QFNS	ispClock5406D 48-Pin QFNS
VCCD	Digital Core VCC	Power	57,59	44
GNDD	Digital GND	GND	56	43
RREF	HCSL Reference Resistor Connection Pin	REF	31	24
REFAP	Clock Input Reference A, Positive	Input	21	16
REFAN	Clock Input Reference A, Negative	Input	20	15
REFBP	Clock Input Reference B, Positive	Input	24	19
REFBN	Clock Input Reference B, Negative	Input	23	18
FBKP	Clock Feedback, Positive	Input	27	22
FBKN	Clock Feedback, Negative	Input	26	21
REFA_VTT	Termination Voltage for Reference A Input	Power	19	14
REFB_VTT	Termination Voltage for Reference B Input	Power	22	17
FBK_VTT	Termination Voltage for Feedback Input	Power	25	20
$\overline{\text{RESET}}$	Reset PLL and All Digital Circuitry	Input	55	42
USER 0	User Configurable Input / Output 0	I/O	63	48
USER 1	User Configurable Input / Output 1	I/O	62	47
USER 2	User Configurable Input 2	Input	61	46
USER 3	User Configurable Input 3	Input	60	45
VCCJ	JTAG Interface VCC	Power	50	37
TDO	JTAG TDO Output	Output	51	38
TMS	JTAG TMS Input	Input	52	39
TCK	JTAG TCK Input	Input	53	40
TDI	JTAG TDI Input	Input	54	41
GNDD	Digital GND	GND	Die Pad	Die Pad

Detailed Pin Descriptions

VCCO_[0..9], GNDO_[0..9] – These pins provide power and ground for each of the output banks. In the case when an output bank is unused, its corresponding VCCO pin may be left unconnected or preferably should be tied to ground. ALL GNDO pins should be tied to ground regardless of whether the associated bank is used or not. When a bank is used, it should be individually bypassed with a capacitor in the range of 0.01 to 0.1µF as close to its VCCO and GNDO pins as is practical.

BANK_[0..9]A, BANK_[0..9]B – These pins provide clock output signals. The choice of output driver type (LVDS, SSTL, etc.) may be selected on a bank-by-bank basis. The output impedance and slew rate may be selected on an output-by-output basis.

VCCA, GNDA – These pins provide analog supply and ground for the ispClock5400D family's internal analog circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity, it is suggested that the supply to the VCCA pin be isolated from other circuitry with a ferrite bead.

VCCD, GNDD – These pins provide digital supply and ground for the ispClock5400D family's internal digital circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity it is suggested that the supply to the VCCD pins be isolated with ferrite beads.

VCCJ – This pin provides power and a reference voltage for use by the JTAG interface circuitry. It may be set to allow the ispClock5400D family devices to function in JTAG chains operating at voltages differing from VCCD.

REFAP, REFAN, REFBP, REFBN – These input pins provide the inputs for clock signals, and can accommodate either single ended or differential signal protocols. Connect unused pins to ground.

REFA_VTT, REFB_VTT – These pins are used to provide a termination voltage for the reference inputs when they are configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases. Leave unused pins open.

FBKP, FBKN – This input pin provides feedback sense of the output clock signal, and can accommodate any of the single-ended logic types. Connect unused pins to ground.

FBK_VTT – This pin is used to provide a termination voltage for the feedback input when it is configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases. Leave unused pins open.

TDO, TDI, TCK, TMS – These pins comprise the ispClock5400D device's JTAG interface. The signal levels for these pins are determined by the selection of the VCCJ voltage.

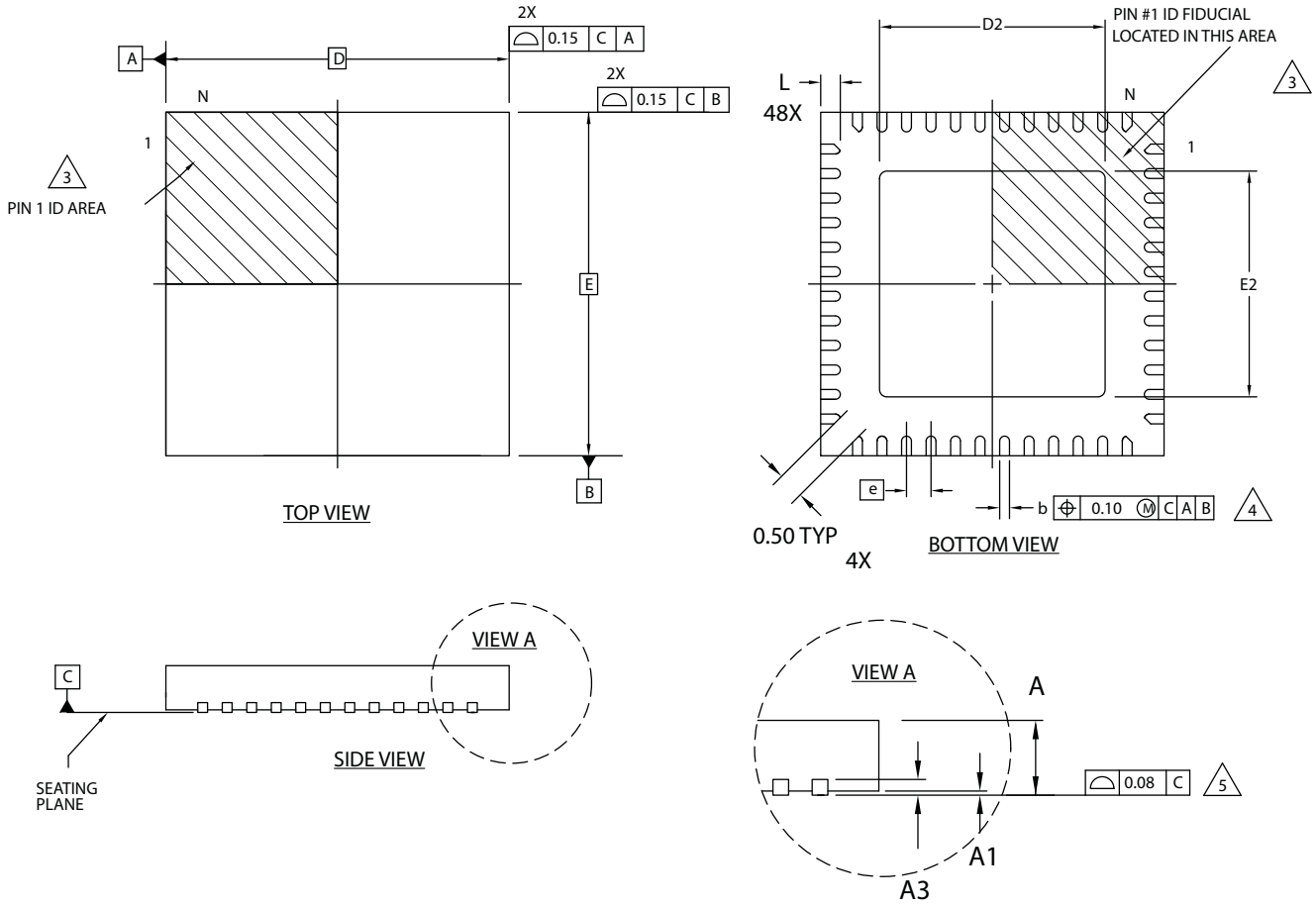
$\overline{\text{RESET}}$ – When this pin is pulled LOW, all on-board counters are reset, and lock is lost. If the $\overline{\text{RESET}}$ pin is not driven by an external logic it should be pulled up to V_{CCD} through a 10kΩ resistor.

NC – These pins have no internal connection. It is recommended that they be left unconnected.

RREF – Connect a 475 Ohm (1%) between this pin and VCCD when HCSL interface is used. Leave pin open when HCSL interface is not used.

Package Diagrams

48-Pin QFNS (Dimensions in Millimeters)



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

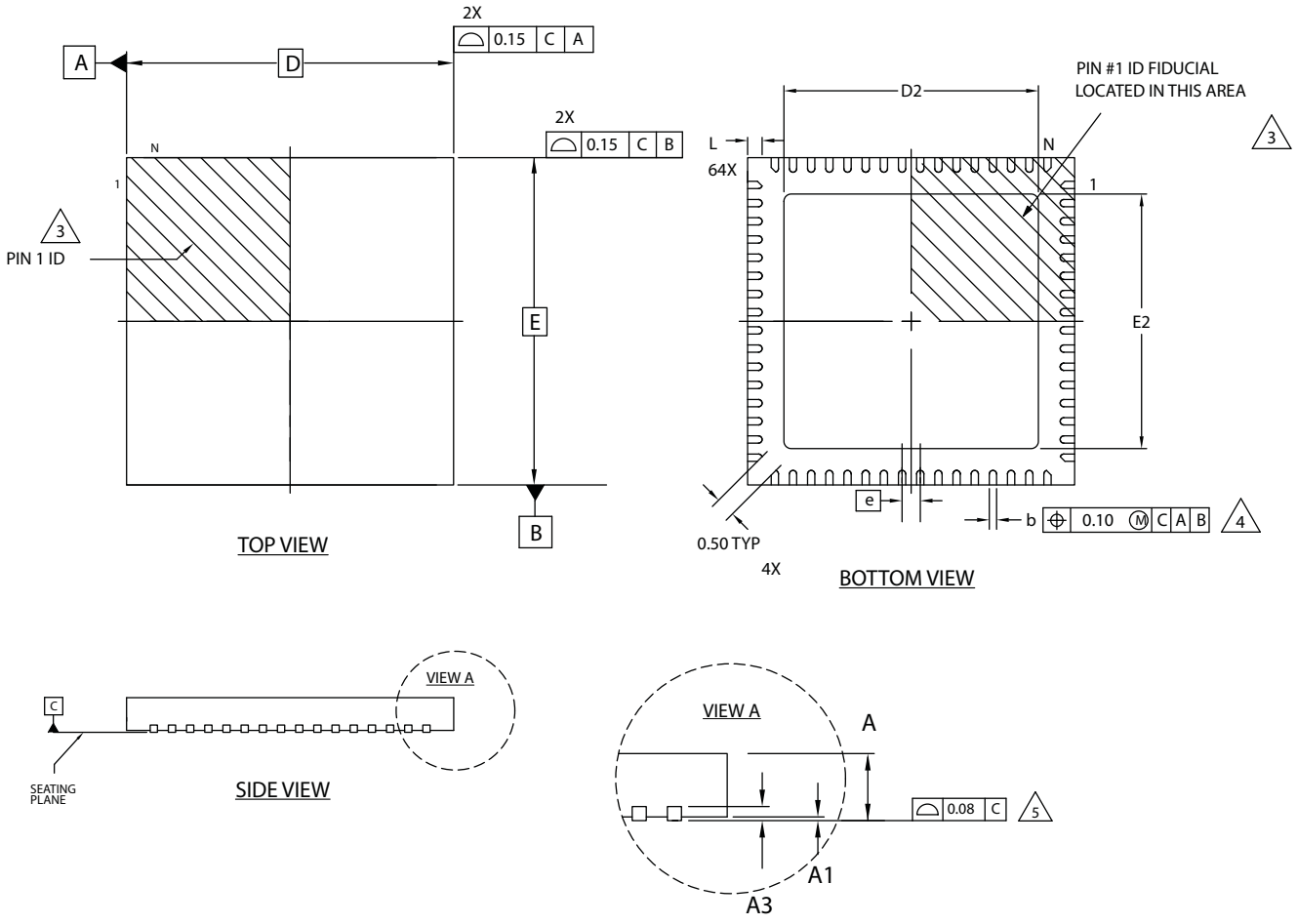
3 EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

4 DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.

5 APPLIES TO EXPOSED PORTION OF TERMINALS.

SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
D		7.0 BSC	
D2	3.00	-	5.80
E		7.0 BSC	
E2	3.00	-	5.80
b	0.18	0.24	0.30
e		0.50 BSC	
L	0.30	0.40	0.50

64-Pin QFNS (Dimensions in Millimeters)



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

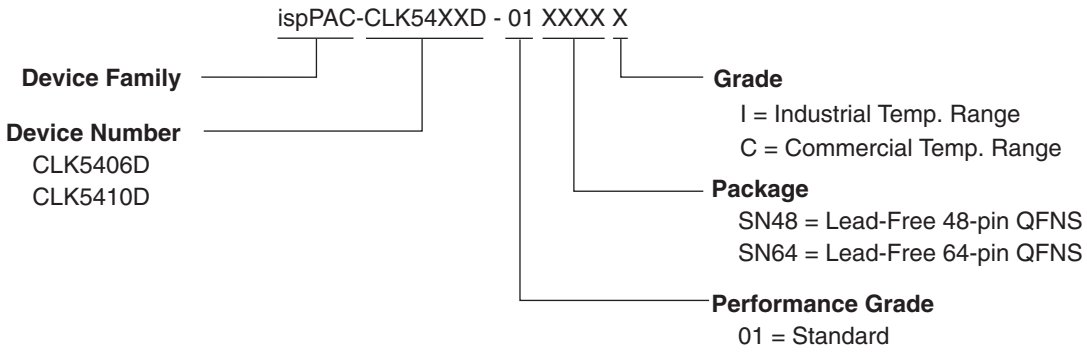
3 EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

4 DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.

5 APPLIES TO EXPOSED PORTION OF TERMINALS.

SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
D		9.0 BSC	
D2	5.00	-	7.50
E		9.0 BSC	
E2	5.00	-	7.50
b	0.18	0.24	0.30
e		0.50 BSC	
L	0.30	0.40	0.50

Part Number Description



Ordering Information

Lead-Free Packaging

Commercial

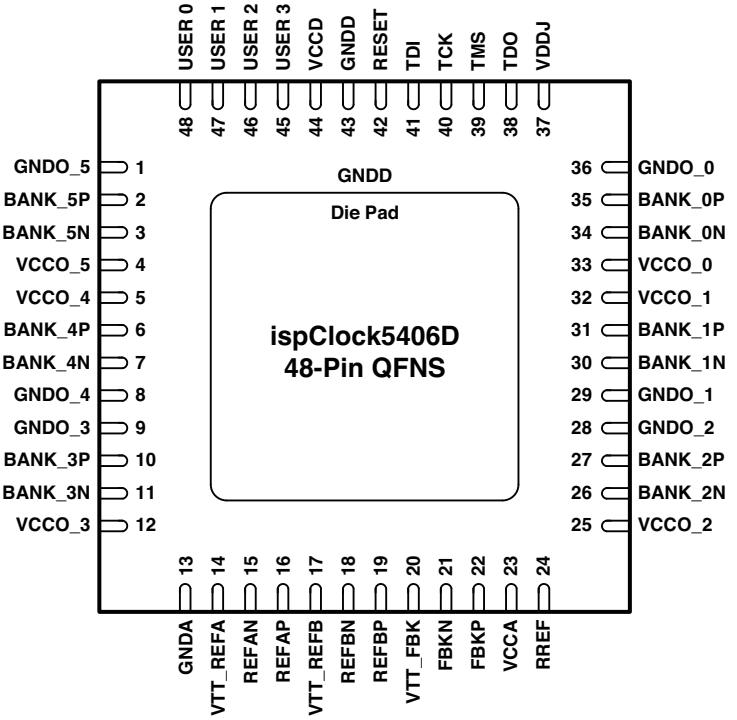
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5410D-01SN64C	10	3.3V	Lead-Free QFNS	64
ispPAC-CLK5406D-01SN48C	6	3.3V	Lead-Free QFNS	48

Industrial

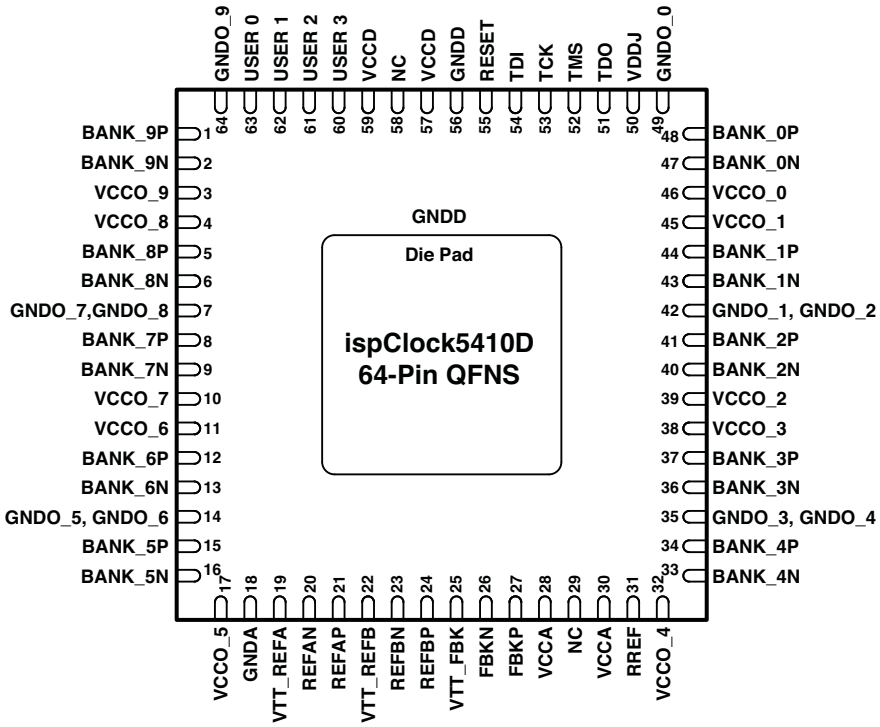
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5410D-01SN64I	10	3.3V	Lead-Free QFNS	64
ispPAC-CLK5406D-01SN48I	6	3.3V	Lead-Free QFNS	48

Package Options

ispClock5406D: 48-pin QFNS



ispClock5410D: 64-pin QFNS



Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-408-826-6002 (Outside North America)
e-mail: isppacs@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
February 2009	01.0	Initial release.
April 2009	01.1	Data sheet updated to preliminary status.
November 2009	01.2	Extended range of PLL operation.

ispClock™5300S Family

In-System Programmable, Zero-Delay Universal Fan-Out Buffer, Single-Ended

October 2007 Preliminary Data Sheet DS1010

Features

Four Operating Configurations

- Zero delay buffer
- Zero delay and non-zero delay buffer
- Dual non-zero delay buffer
- Non-zero delay buffer with output divider

8MHz to 267MHz Input/Output Operation

Low Output to Output Skew (<100ps)

Low Jitter Peak-to-Peak (< 70 ps)

Up to 20 Programmable Fan-out Buffers

- Programmable single-ended output standards and individual enable controls
  - LVTTL, LVCMOS, HSTL, eHSTL, SSTL
- Programmable output impedance
  - 40 to 70¾ in 5¾ increments
- Programmable slew rate
- Up to 10 banks with individual V_{CCO} and GND
  - 1.5V, 1.8V, 2.5V, 3.3V

Fully Integrated High-Performance PLL

- Programmable lock detect
- Three “Power of 2” output dividers (5-bit)
- Programmable on-chip loop filter
- Compatible with spread spectrum clocks
- Internal/external feedback

Precision Programmable Phase Adjustment (Skew) Per Output

- 8 settings; minimum step size 156ps
  - Locked to VCO frequency
- Up to +/- 5ns skew range
- Coarse and fine adjustment modes

Up to Three Clock Frequency Domains

Flexible Clock Reference and External Feedback Inputs

- Programmable single-ended or differential input reference standards
  - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, Differential SSTL
- Clock A/B selection multiplexer
- Programmable Feedback Standards
  - LVTTL, LVCMOS, SSTL, HSTL
- Programmable termination

All Inputs and Outputs are Hot Socket Compliant

Full JTAG Boundary Scan Test In-System Programming Support

Exceptional Power Supply Noise Immunity

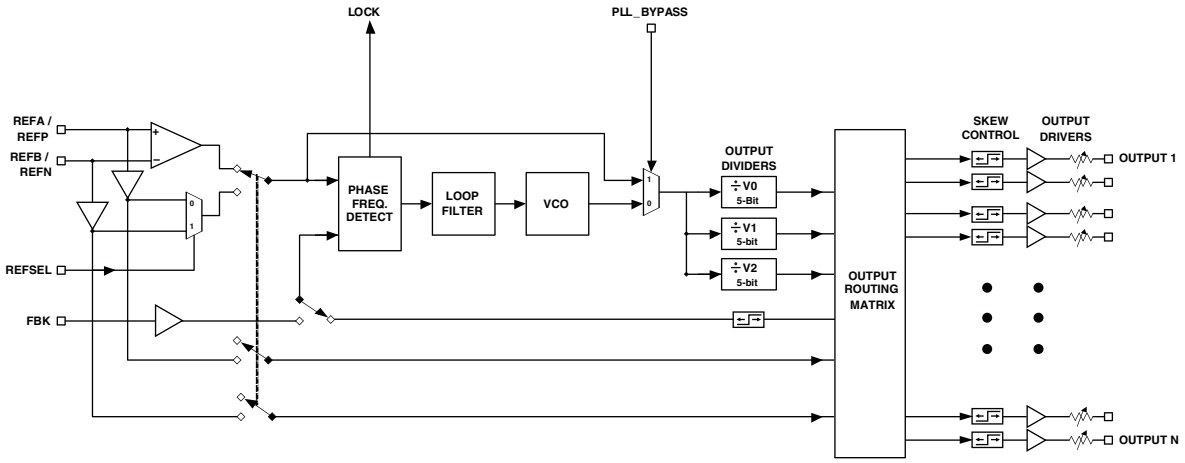
Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges

48-pin and 64-pin TQFP Packages

Applications

- Circuit board common clock distribution
- PLL-based frequency generation
- High fan-out clock buffer
- Zero-delay clock buffer

ispClock5300S Family Functional Diagram



General Description

The ispClock5300S is an in-system-programmable zero delay universal fan-out buffer for use in clock distribution applications. The ispClock5312S, the first member of the ispClock5300S family, provides up to 12 single-ended ultra low skew outputs. Each pair of outputs may be independently configured to support separate I/O standards (LVTTL, LVCMOS -3.3V, 2.5V, 1.8, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile E^{2}CMOS® memory.

The ispClock5300S devices provide extremely low propagation delay (zero-delay) from input to output using the on-chip low jitter high-performance PLL. A set of three programmable 5-bit counters can be used to generate three frequencies derived from the PLL clock. These counters are programmable in powers of 2 only (1, 2, 4, 8, 16, 32). The clock output from any of the V-dividers can then be routed to any clock output pin through the output routing matrix. The output routing matrix, in addition, also enables routing of reference clock inputs directly to any output.

The ispClock5300S device can be configured to operate in four modes: zero delay buffer mode, dual non-zero delay buffer mode, non-zero delay buffer mode with output dividers, and combined zero-delay and non-zero delay buffer mode.

The core functions of all members of the ispClock5300S family are identical. Table 3-1 summarizes the ispClock5300S device family.

Table 3-1. ispClock5300S Family

Device	Number of Programmable Clock Inputs	Number of Programmable Single-Ended Outputs
ispClock5320S	1 Differential, 2 Single-Ended	20
ispClock5316S	1 Differential, 2 Single-Ended	16
ispClock5312S	1 Differential, 2 Single-Ended	12
ispClock5308S	1 Differential, 2 Single-Ended	8
ispClock5304S	1 Differential, 2 Single-Ended	4

Figure 3-1. ispClock5304S Functional Block Diagram

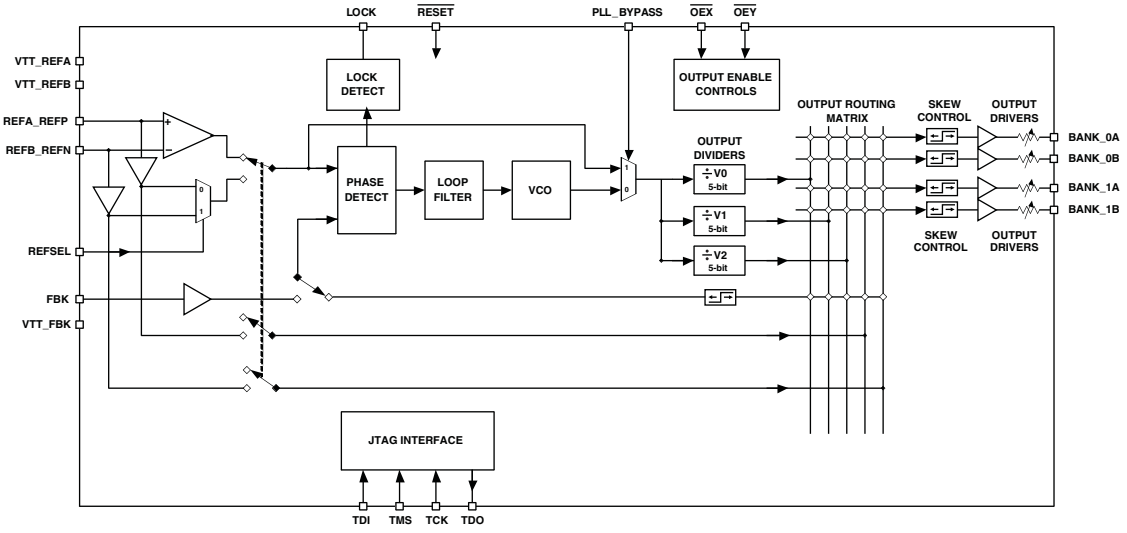


Figure 3-2. ispClock5308S Functional Block Diagram

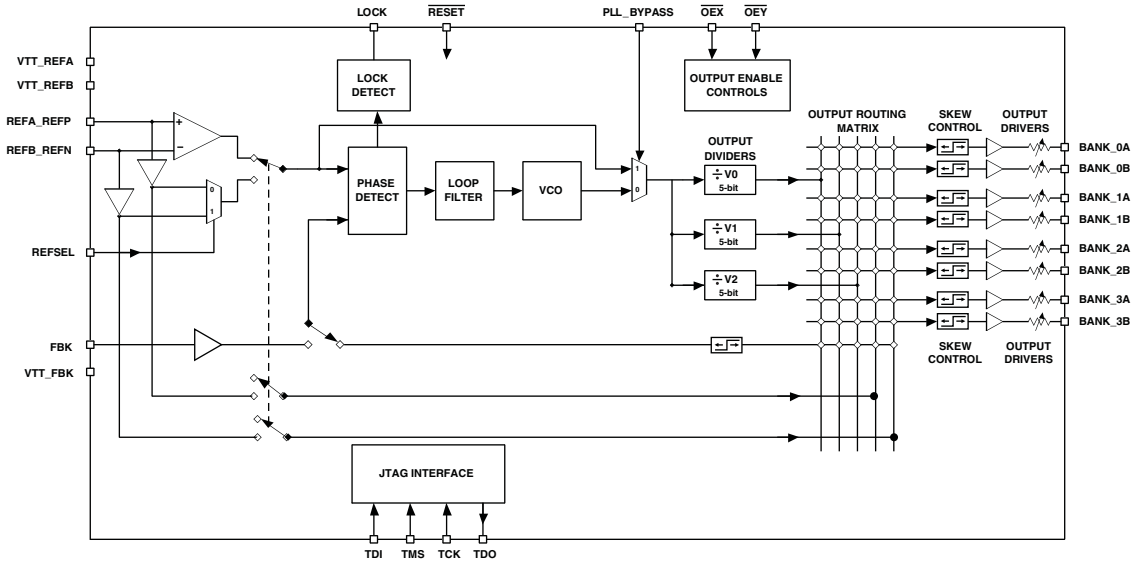


Figure 3-3. ispClock5312S Functional Block Diagram

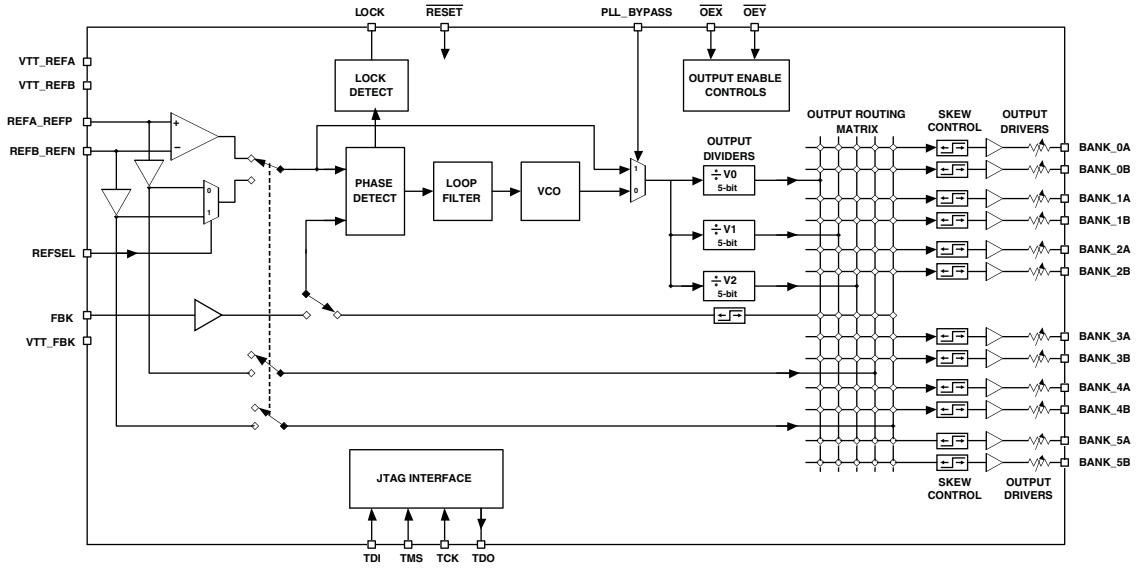


Figure 3-4. ispClock5316S Functional Block Diagram

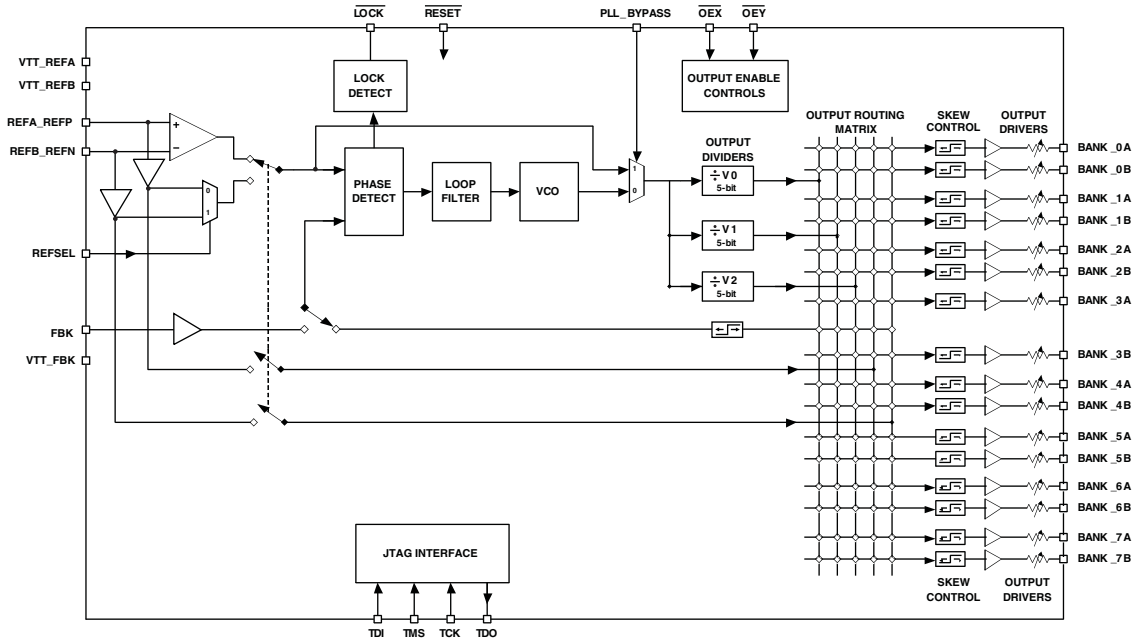
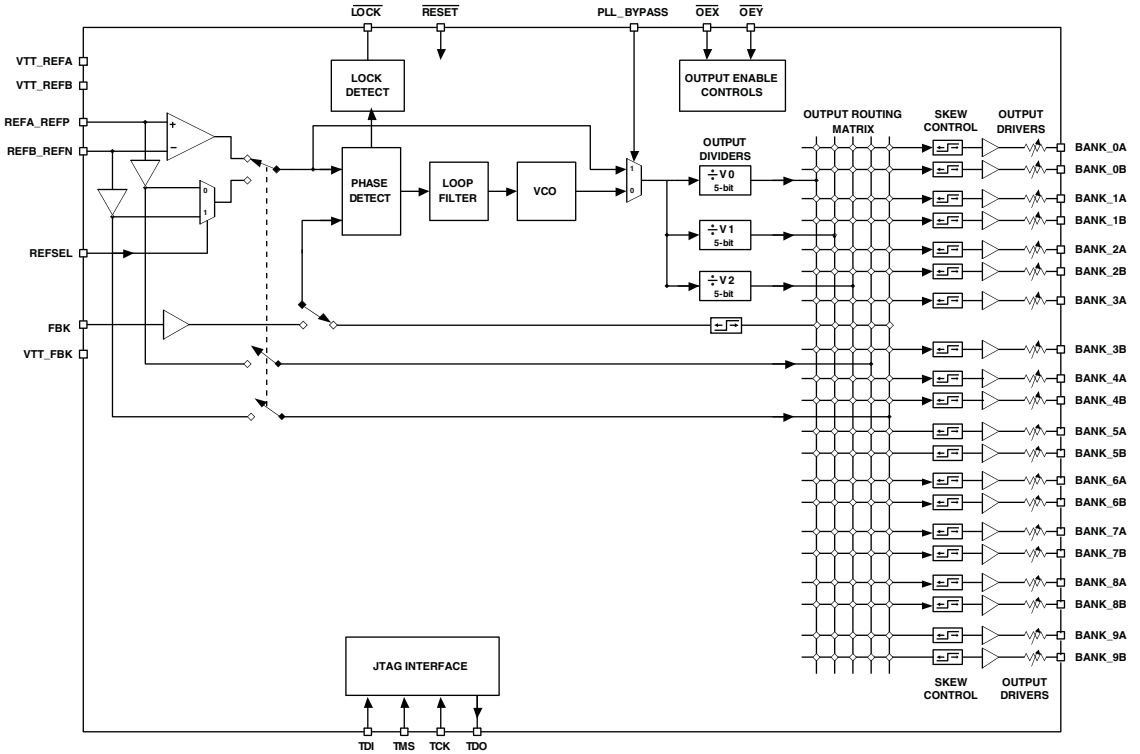


Figure 3-5. ispClock5320S Functional Block Diagram



Absolute Maximum Ratings

	ispClock5300S
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 130°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	ispClock5300S		Units
			Min.	Max.	
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		1.62	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	V_{CC} Turn-on Ramp Rate	All supply pins	—	0.33	V/µs
T_{JOP}	Operating Junction Temperature	Commercial	0	120	°C
		Industrial	-40	130	
T_A	Ambient Operating Temperature	Commercial	0	70[1]	°C
		Industrial	-40	85[1]	

1. Device power dissipation may also limit maximum ambient operating temperature.

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard	V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL	3.0	3.3	3.6	—	—	—	—	—	—
LVCMOS 1.8V	1.71	1.8	1.89	—	—	—	—	—	—
LVCMOS 2.5V	2.375	2.5	2.625	—	—	—	—	—	—
LVCMOS 3.3V	3.0	3.3	3.6	—	—	—	—	—	—
SSTL1.8	1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—
SSTL2 Class 1	2.375	2.5	2.625	1.15	1.25	1.35	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL3 Class 1	3.0	3.3	3.6	1.30	1.50	1.70	V_{REF} - 0.05	V_{REF}	V_{REF} + 0.05
HSTL Class 1	1.425	1.5	1.575	0.68	0.75	0.90	—	0.5 x V_{CCO}	—
eHSTL Class 1	1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—

Note: '—' denotes V_{REF} or V_{TT} not applicable to this logic standard

E²CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max.	Units
I_{CCD}	Core Supply Current[2]	f_{VCO} = 400MHz Feedback Output Active	110	150	mA
$I_{CCDADDER}$	Incremental I_{CCD} per Active Output	f_{OUT} = 267MHz		1.5	mA
I_{CCA}	Analog Supply Current[2]	f_{VCO} = 400MHz	5.5	7	mA
I_{CCO}	Output Driver Supply Current (per Bank)	V_{CCO} = 1.8V[1], LVCMOS, f_{OUT} = 267MHz	16	20	mA
		V_{CCO} = 2.5V[1], LVCMOS, f_{OUT} = 267MHz	21	27	mA
		V_{CCO} = 3.3V[1], LVCMOS, f_{OUT} = 267MHz	27	35	mA
I_{CCJ}	JTAG I/O Supply Current (static)	V_{CCJ} = 1.8V		300	µA
		V_{CCJ} = 2.5V		400	µA
		V_{CCJ} = 3.3V		400	µA

1. Supply current consumed by each bank, both outputs active, 5pF load.
2.All unused REFCLK and feedbacks connected to ground.

DC Electrical Characteristics – Single-Ended Logic

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
LVCMOS 1.8V	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
SSTL2 Class 1	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54[1]	V_{CCO} - 0.81[1]	7.6	-7.6
SSTL3 Class 1	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.9[1]	V_{CCO} - 1.3[1]	8	-8
HSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[2]	V_{CCO} - 0.4[2]	8	-8
eHSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[2]	V_{CCO} - 0.4[2]	8	-8

1. Specified for 40¾ internal series output termination.
2. Specified for Ý20¾ internal series output termination, fast slew rate setting.
3. For slower slew rate setting, I_{OH}, I_{OL} should be limited to 8mA.

DC Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage		V_{THD}/2		2.325	V
V_{THD}	Differential Input Threshold	V_{ICM} ð 2V	±100	—	—	mV
		2V < V_{ICM} < 2.325V	±150	—	—	mV
V_{IN}	Input Voltage		0	—	2.4	V

DC Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input Voltage High	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.17	—	V_{CCD} - 0.88	V
		V_{CCD} = 3.3V	2.14	—	2.42	
V_{IL}	Input Voltage Low	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.81	—	V_{CCD} - 1.48	V
		V_{CCD} = 3.3V	1.49	—	1.83	

Electrical Characteristics – Differential SSTL18

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Low-Logic Level Input Voltage				0.61	V
V_{IH}	Hi Logic Level Input Voltage		1.17			V
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} -175mV		V_{REF} +175mV	V

Electrical Characteristics – Differential SSTL2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.225	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.62		3.225	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} - 200 mV		V_{REF} + 200 mV	V

Electrical Characteristics – Differential HSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.325	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		3.325	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V

Electrical Characteristics – Differential eHSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.325	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		3.325	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	REFSEL, PLL_BYPASS	—	120	150	µA
		$\overline{OEX}$, $\overline{OEY}$, 2.5V CMOS Logic Standard	—	120	150	µA
		$\overline{OEX}$, $\overline{OEY}$, & 3.3V CMOS Logic Standard	—	200	400	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	8	10	pF
		Note 6	—	10	11	pF

1. Applies to clock reference inputs when termination 'open'.
2. Applies to TDI, TMS and $\overline{RESET}$ inputs.
3. Applies to REFSEL and PLL_BYPASS, $\overline{OEX}$, $\overline{OEY}$.
4. Applies to all logic types when in tristated mode.
5. Applies to $\overline{OEX}$, $\overline{OEY}$, TCK, $\overline{RESET}$ inputs.
6. Applies to REFA_REFP, REFB_REFN, FBK.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
t_{IOI} Input Adders[2]					
LVTTL_in	Using LVTTL Standard		0.00		ns
LVCMOS18_in	Using LVCMOS 1.8V Standard		0.10		ns
LVCMOS25_in	Using LVCMOS 2.5V Standard		0.00		ns
LVCMOS33_in	Using LVCMOS 3.3V Standard		0.00		ns
SSTL2_in	Using SSTL2 Standard		0.00		ns
SSTL3_in	Using SSTL3 Standard		0.00		ns
HSTL_in	Using HSTL Standard		1.15		ns
eHSTL_in	Using eHSTL Standard		1.10		ns
LVDS_in	Using LVDS Standard		0.60		ns
LVPECL_in	Using LVPECL Standard		0.60		ns
t_{IOO} Output Adders[1, 3]					
LVTTL_out	Output Configured as LVTTL Buffer		0.25		ns
LVCMOS18_out	Output Configured as LVCMOS 1.8V Buffer		0.25		ns
LVCMOS25_out	Output Configured as LVCMOS 2.5V Buffer		0.25		ns
LVCMOS33_out	Output Configured as LVCMOS 3.3V Buffer		0.25		ns
SSTL18_out	Output Configured as SSTL18 Buffer		0.00		ns
SSTL2_out	Output Configured as SSTL2 Buffer		0.00		ns
SSTL3_out	Output Configured as SSTL3 Buffer		0.00		ns
HSTL_out	Output Configured as HSTL Buffer		0.00		ns
eHSTL_out	Output Configured as eHSTL Buffer		0.00		ns
t_{IOS} Output Slew Rate Adders[1]					
Slew_1	Output Slew_1 (Fastest)	—	0.00	—	ps
Slew_2	Output Slew_2	—	475	—	ps
Slew_3	Output Slew_3	—	950	—	ps
Slew_4	Output Slew_4 (Slowest)	—	1900	—	ps

1. Measured under standard output load conditions – see Figures 3-6 and 3-7.
2. All input adders referenced to LVTTL.
3. All output adders referenced to SSTL/HSTL/eHSTL.

Output Rise and Fall Times – Typical Values[1, 2]

Output Type	Slew 1 (Fastest)		Slew 2		Slew 3		Slew 4 (Slowest)		Units
	t_R	t_F	t_R	t_F	t_R	t_F	t_R	t_F	
LVTTL	0.54	0.76	0.60	0.87	0.78	1.26	1.05	1.88	ns
LVCMOS 1.8V	0.75	0.69	0.88	0.78	0.83	1.11	1.20	1.68	ns
LVCMOS 2.5V	0.57	0.69	0.65	0.78	0.99	0.98	1.65	1.51	ns
LVCMOS 3.3V	0.55	0.77	0.60	0.87	0.78	1.26	1.05	1.88	ns
SSTL18	0.55	0.40	—	—	—	—	—	—	ns
SSTL2	0.50	0.40	—	—	—	—	—	—	ns
SSTL3	0.50	0.45	—	—	—	—	—	—	ns
HSTL	0.60	0.45	—	—	—	—	—	—	ns
eHSTL	0.55	0.40	—	—	—	—	—	—	ns

1. See Figures 3-6 and 3-7 for test conditions.
2. Measured between 20% and 80% points.

Output Test Loads

Figures 3-6 and 3-7 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 3-6. CMOS Termination Load

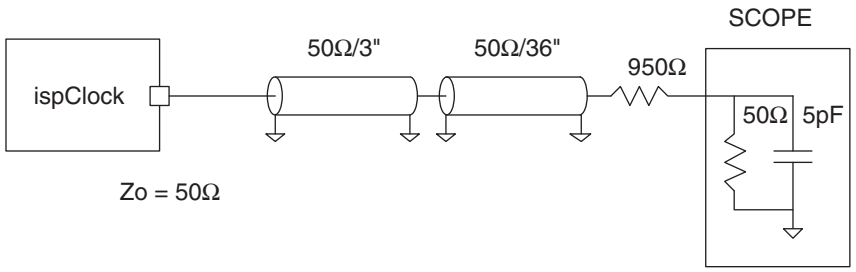
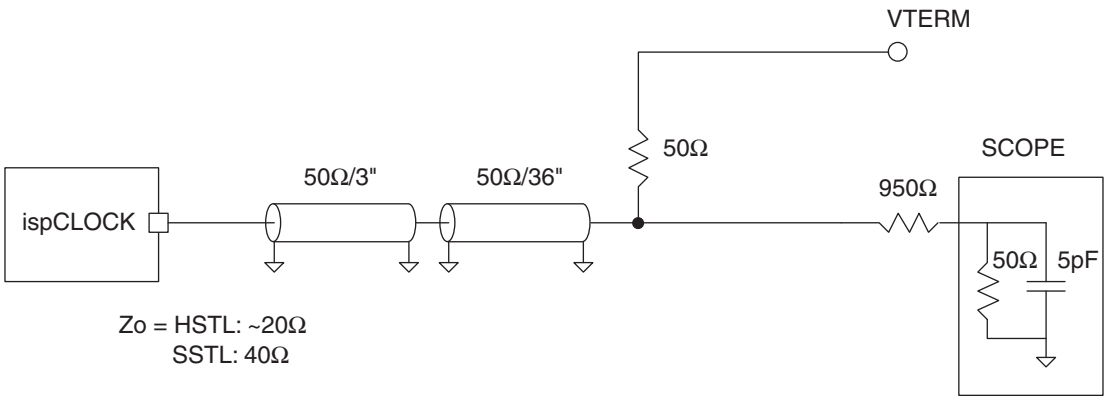


Figure 3-7. eHSTL/HSTL/SSTL Termination Load



Programmable Input and Output Termination Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input Resistance	Rin=40¾ setting	36	—	44	¾
		Rin=45¾ setting	40.5	—	49.5	
		Rin=50¾ setting	45	—	55	
		Rin=55¾ setting	49.5	—	60.5	
		Rin=60¾ setting	54	—	66	
		Rin=65¾ setting	59	—	71.5	
		Rin=70¾ setting	61	—	77	
R_{OUT}	Output Resistance	RoutÝ20¾ setting T_A = 25°C	—	14	—	¾
		RoutÝ40¾ setting T_A = 25°C	36	38	44	
		RoutÝ45¾ setting T_A = 25°C	41	45	51	
		RoutÝ50¾ setting T_A = 25°C	45	50	55	
		RoutÝ55¾ setting T_A = 25°C	50	55	61	
		RoutÝ60¾ setting T_A = 25°C	54	59	66	
		RoutÝ65¾ setting T_A = 25°C	59	65	71	
		RoutÝ70¾ setting T_A = 25°C	63	72	78	
R_{OUT_TEMPCO}	Output Resistor Temperature Coefficient		—	500	—	PPM/°C

Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{REF}, f_{FBK}	Reference and feedback input frequency range		8		267	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference and feedback input clock HIGH and LOW times		1.25			ns
t_{RINP}, t_{FINP}	Reference and feedback input rise and fall times	Measured between 20% and 80% levels			5	ns
f_{PFD}	Phase detector input frequency range		8		267	MHz
f_{VCO}	VCO operating frequency		160		400	MHz
V_{DIV}	Output divider range (Power of 2)		1		32	
f_{OUT}	Output frequency range[1]	Fine Skew Mode	5		267	MHz
		Coarse Skew Mode	2.5		200	MHz
t_{JIT} (cc)	Output adjacent-cycle jitter[5] (1000 cycle sample)	f_{PFD} Š 100MHz			70	ps (p-p)
t_{JIT} (per)	Output period jitter[5] (10000 cycle sample)	f_{PFD} Š 100MHz			9	ps (RMS)
$t_{JIT(\phi)}$	Reference clock to output jitter[5] (2000 cycle sample)	f_{PFD} Š 100MHz			50	ps (RMS)
$t\phi$	Static phase offset[4]	PFD input frequency Š100MHz[3]	-40		100	ps
$t\phi_{DYN}$	Dynamic phase offset	100MHz, Spread Spectrum Modulation index = 0.5%		2	8	ps
DC_{ERR}	Output duty cycle error	Output type LVCMOS 3.3V[2] f_{OUT} >100 MHz	47		53	%
$t_{PDBYPASS}$	Reference clock to output propagation delay	V=1		6.5		ns
t_{PD_FOB}	Reference to output propagation delay in Non-Zero Delay Buffer Mode	V=1	2.5	3.5	5	ns
t_{DELAY}	Reference to output delay with internal feedback mode[3]	V=1		500		ps
t_{LOCK}	PLL lock time	From Power-up event		150		µs
		From $\overline{\text{RESET}}$ event		15		µs
t_{RELOCK}	PLL relock time	To same reference frequency		15		µs
		To different frequency		150		µs
PSR	Power supply rejection, period jitter vs. power supply noise	$f_{IN} = f_{OUT}$ = 100MHz $V_{CCA} = V_{CCD} = V_{CCO}$ modulated with 100kHz sinusoidal stimulus		0.05		$\frac{ps(RMS)}{mV(p\text{-}p)}$

1. In PLL Bypass mode (PLL_BYPASS = HIGH), output will support frequencies down to 0Hz (divider chain is a fully static design).
2. See Figures 3-6 and 3-7 for output loads.
3. Input and outputs LVCMOS mode
4. Inserted feedback loop delay < 7ns
5. Measured with f_{OUT} = 100MHz, f_{VCO} = 400MHz, input and output interface set to LVCMOS.

Timing Specifications

Skew Matching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-output Skew	Between any two identically configured and loaded outputs regardless of bank.	—	—	100	ps

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKRANGE}$	Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 160 MHz	—	2.73	—	ns
		Fine Skew Mode, f_{VCO} = 400 MHz	—	1.09	—	
		Coarse Skew Mode, f_{VCO} = 160 MHz	—	5.46	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	2.19	—	
SK_{STEPS}	Skew Steps per Range		—	8	—	
t_{SKSTEP}	Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 160 MHz	—	390	—	ps
		Fine Skew Mode, f_{VCO} = 400 MHz	—	156	—	
		Coarse Skew Mode, f_{VCO} = 160 MHz	—	780	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	312	—	
t_{SKERR}	Skew Time Error[3]	Fine skew mode	—	30	—	ps
		Coarse skew mode	—	50	—	

1. Skew control range is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 7/(16 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 7/(8 \times f_{VCO})$.
2. Skew step size is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(16 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, $\overline{OEX}$ or $\overline{OEY}$ to Output Disabled/ Enabled		—	10	20	ns
t_{PLL_RSTW}	PLL $\overline{RESET}$ Pulse Width[1]		1	—	—	ms
t_{RSTW}	Logic $\overline{RESET}$ Pulse Width[2]		20	—	—	ns
RST_SLEW	Reset Signal Slew Rate		0.1			V/µs

1. Will completely reset PLL.
2. Will only reset digital logic.

Static Phase Offset vs. Reference Clock Logic Type

Symbol	Reference Clock Logic (REFA/REFB)	Feedback Input Logic (FBK)	Feedback Output Logic (BANK_xA/BANK_xB)	Min.	Max.	Units
$t_{(\phi)}$ – Static Phase Offset	LVCMOS 33	LVCMOS33	LVCMOS33	-40	100	ps
	LVCMOS 25	LVCMOS25	LVCMOS25	-70	80	ps
	LVCMOS 18	LVCMOS18	LVCMOS18	-80	80	ps
	SSTL3	SSTL3	SSTL3	-70	390	ps
	SSTL2	SSTL2	SSTL2	-70	340	ps
	HSTL(1.5V)	HSTL(1.5V)	HSTL(1.5V)	-100	360	ps
	eHSTL(1.8V)	eHSTL(1.8V)	eHSTL(1.8V)	-100	360	ps
	LVDS (2.5V)[1]	LVDS-Single Ended	LVCMOS25	140	530	ps
	LVPECL[1]	LVPECL-Single Ended	LVCMOS33	80	300	ps

1. The output clock to feedback can be skewed to center the static phase offset spread.

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_{H}	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

Timing Diagrams

Figure 3-8. Erase (User Erase or Erase All) Timing Diagram

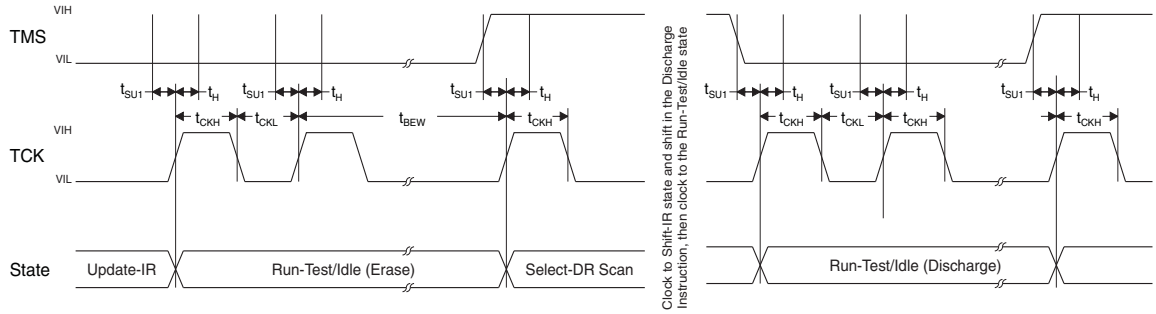


Figure 3-9. Programming Timing Diagram

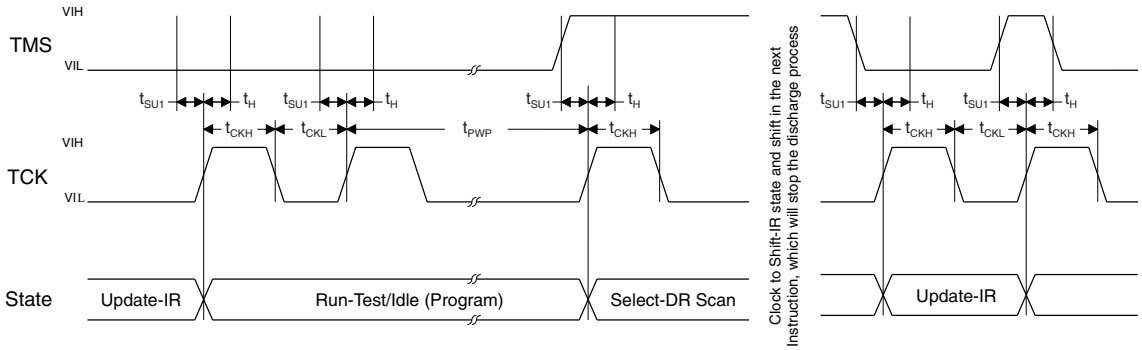


Figure 3-10. Verify Timing Diagram

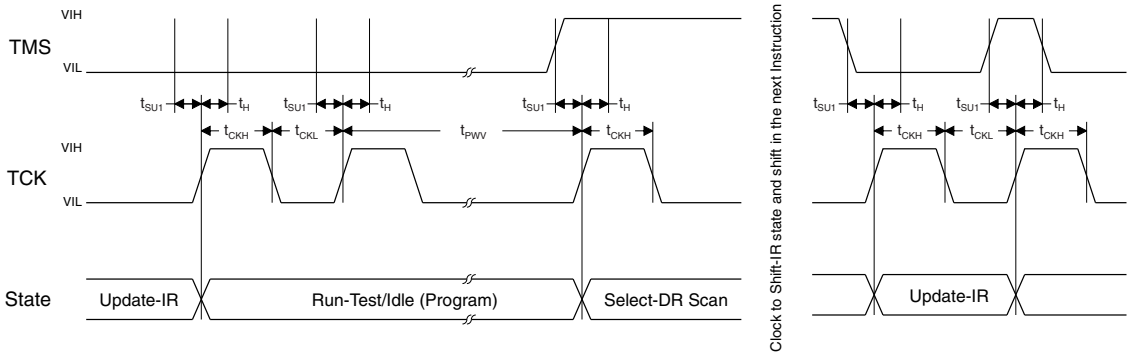
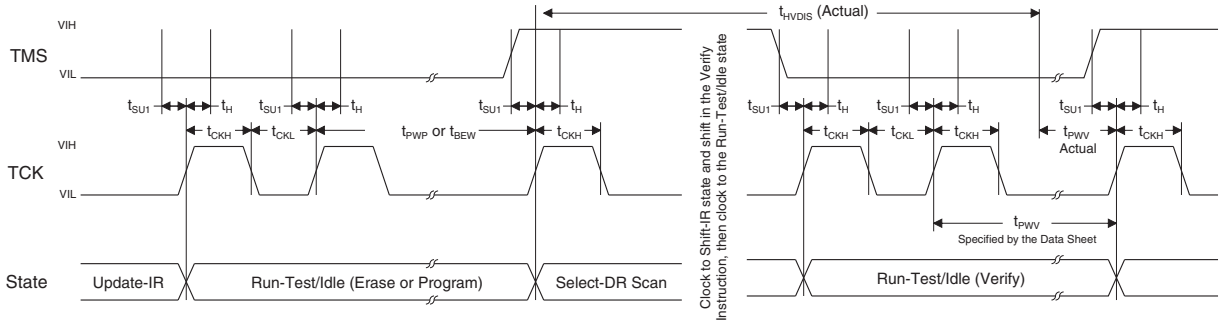
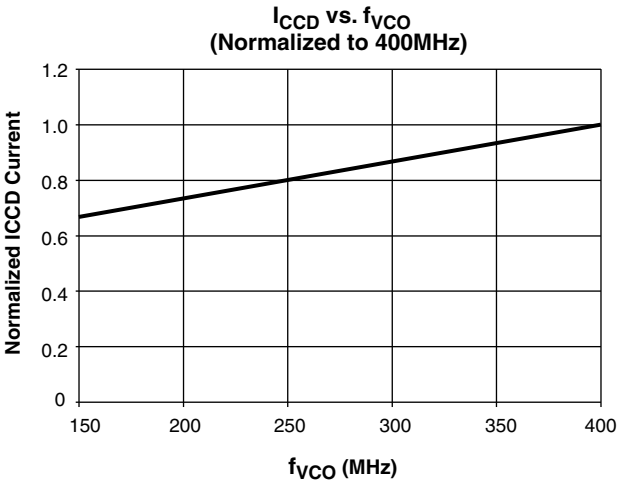
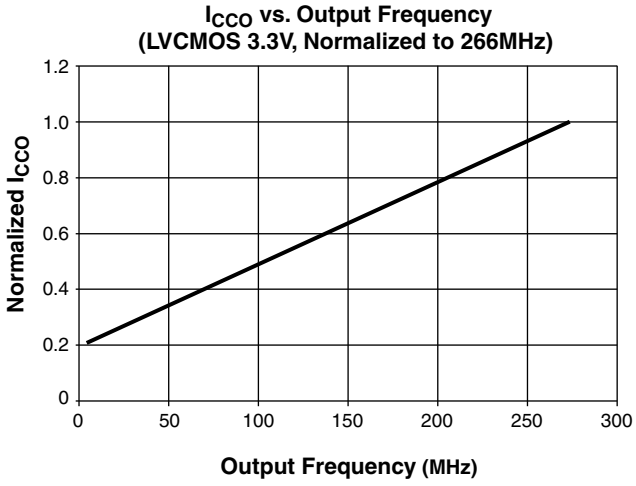


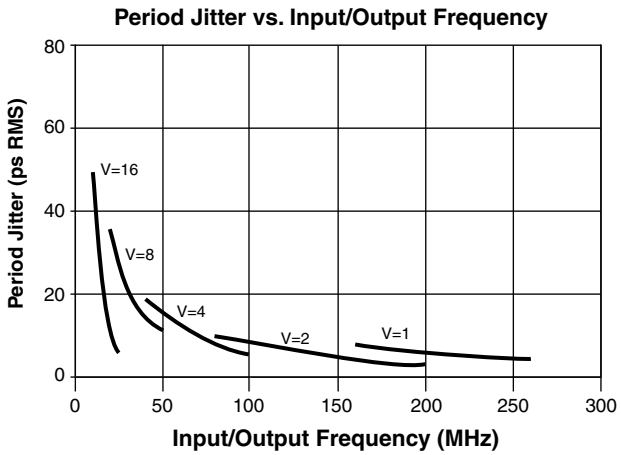
Figure 3-11. Discharge Timing Diagram

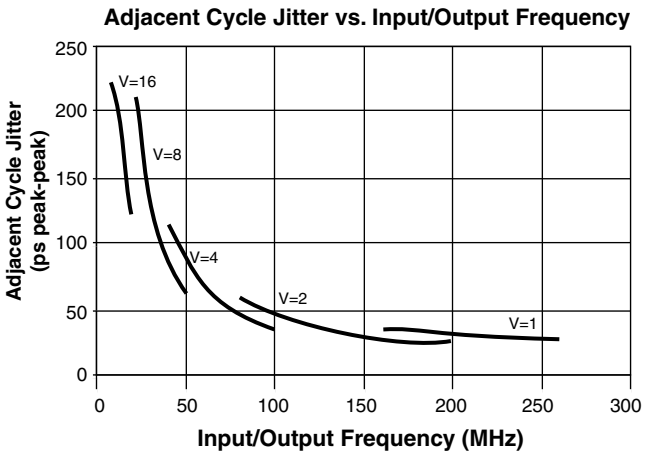


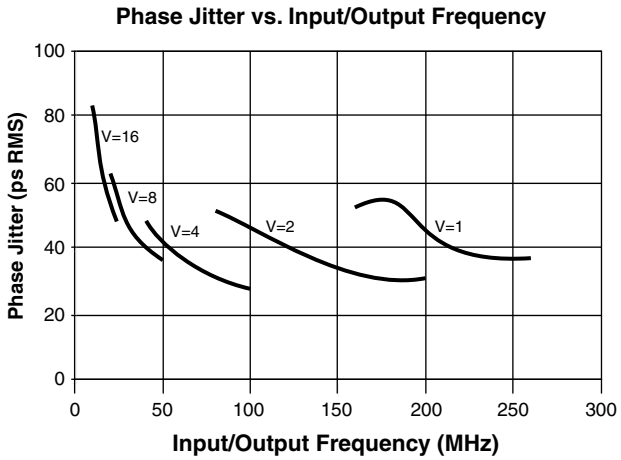
Typical Performance Characteristics











Detailed Description

PLL Subsystem

The ispClock5300S provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Additionally, a set of programmable feedback dividers (V[0, 1, 2]) is provided to support the synthesis of different output frequencies.

Phase/Frequency Detector
The ispClock5300S provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI,}$ $t_{CLOCKLO}$) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter.

A lock-detection feature is also associated with the PFD. When the ispClock5300S is in a LOCKED state, the LOCK output pin goes HIGH. The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 through 256.

When the lock condition is lost the LOCK signal will be de-asserted (Logic '0') immediately.

Loop Filter: The loop filter parameters for each profile are automatically selected by the PAC-Designer software depending on the following:

- Maximum VCO operating frequency

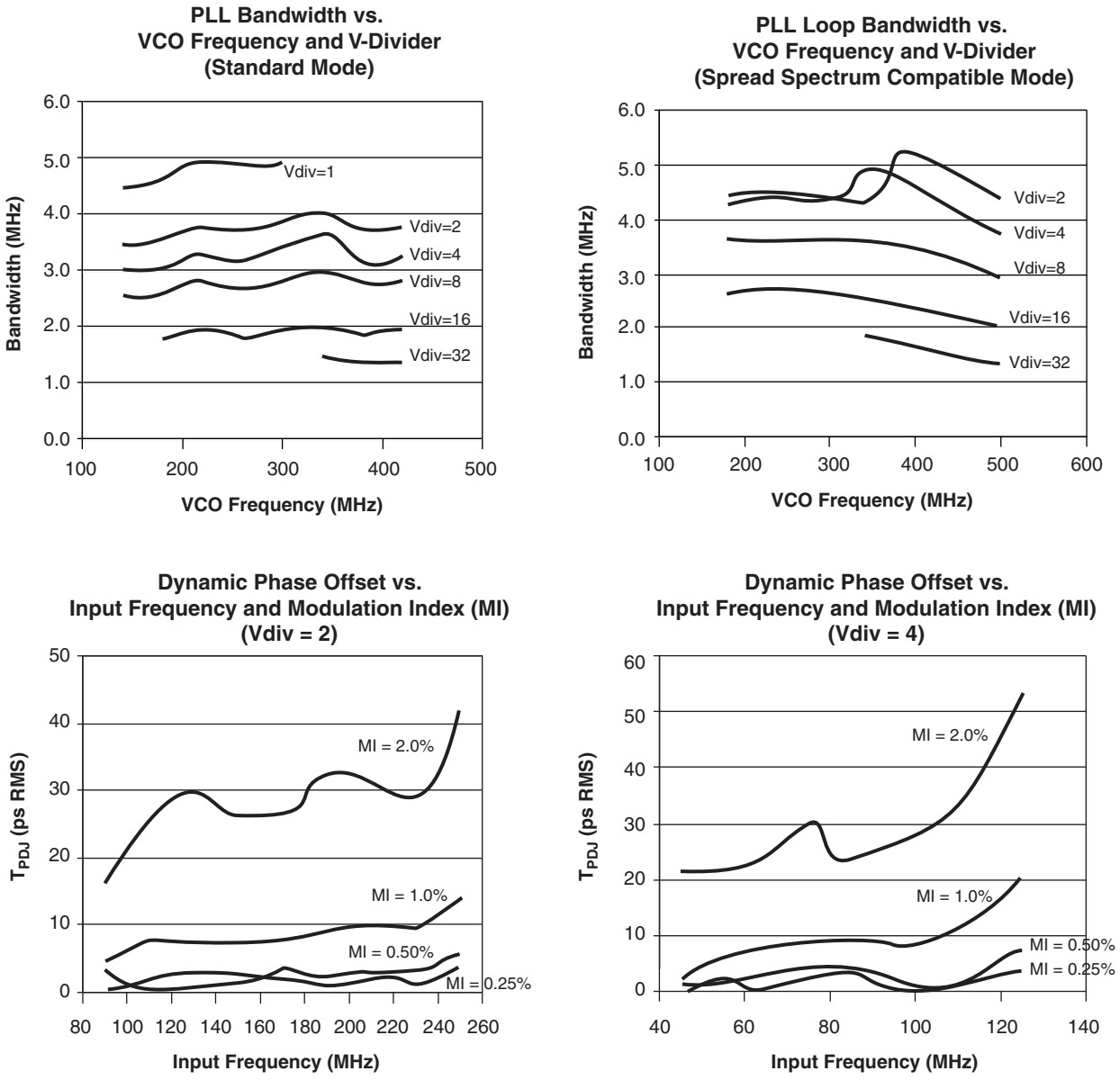
Spread Spectrum Support: The reference clock inputs of the ispClock5300S device are spread spectrum clock tolerant. The tolerance limits are:

- Center spread ±0.125% to ±2%
- Down spread -0.25% to 0.5%
- 30-33kHz modulation frequency

The ispClock5300S PLL has two modes of operation:

- Spread Spectrum setting turned on - Spread Spectrum modulation is transferred from input to output with minimal attenuation.
- Spread Spectrum setting turned off - Spread Spectrum modulation transfer from input to output is attenuated. The extent of attenuation depends on the VCO operating frequency and the feedback divider value.

Figure 3-12. PLL Loop Bandwidth vs. Feedback Divider Setting (Nominal)



VCO

The ispClock5300S provides an internal VCO which provides an output frequency ranging from 160MHz to 400MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to generate output clock skew as a function of the total VCO period. Using the VCO as the basis for controlling output skew allows for highly precise and consistent skew generation, both from device-to-device, as well as channel-to-channel within the same device.

Output V Dividers

The ispClock5300S incorporates a set of three 5-bit programmable Power of 2 dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input.

Each one of the three V dividers can be independently programmed to provide division ratios ranging from 1 to 32 in Power of 2 steps (1, 2, 4, 8, 16, 32).

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{V_{fbk}}{V_k} \quad (1)$$

where

f_k is the frequency of V divider k
f_{ref} is the input reference frequency
V_{fbk} is the setting of the V divider used to close the PLL feedback path
V_k is the output divider K

Note that because the feedback may be taken from any V divider, V_k and V_{fbk} may refer to the same divider.

Because the VCO has an operating frequency range spanning 160 MHz to 400 MHz, and the V dividers provide division ratios from 1 to 32, the ispClock5300S can generate output signals ranging from 2.5 MHz to 267 MHz.

PLL_BYPASS Mode
The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the reference clock is routed directly to the inputs of the V dividers. The output frequency for a given V divider (f_K) will be determined by

$$f_k = \frac{f_{REF}}{V_K} \quad (2)$$

When PLL_BYPASS mode is enabled, features such as lock detect and skew generation are unavailable and the output clock is inverted when V_K=1.

Internal/External Feedback Support

The PLL feedback path can be sourced internally or externally through an output pin. When the internal feedback path is selected, one can use all output pins for clock distribution. The programmable skew feature for the feedback path is available in both feedback modes.

Reference and External Feedback Inputs

The ispClock5300S provides configurable, internally-terminated inputs for both clock reference and feedback signals.

The reference clock inputs pins can be interfaced with either one differential input (REFP, REFN) or two single-ended (REFA, REFB) inputs with the active clock selection control through REFSEL pin. The following diagram shows the possible reference clock configurations. Note: When the reference clock inputs are configured as differential input, the REFSEL pin should be grounded.

Table 3-2. REFSEL Operation for ispClock5300S Programmed as Single-Ended Clock Inputs

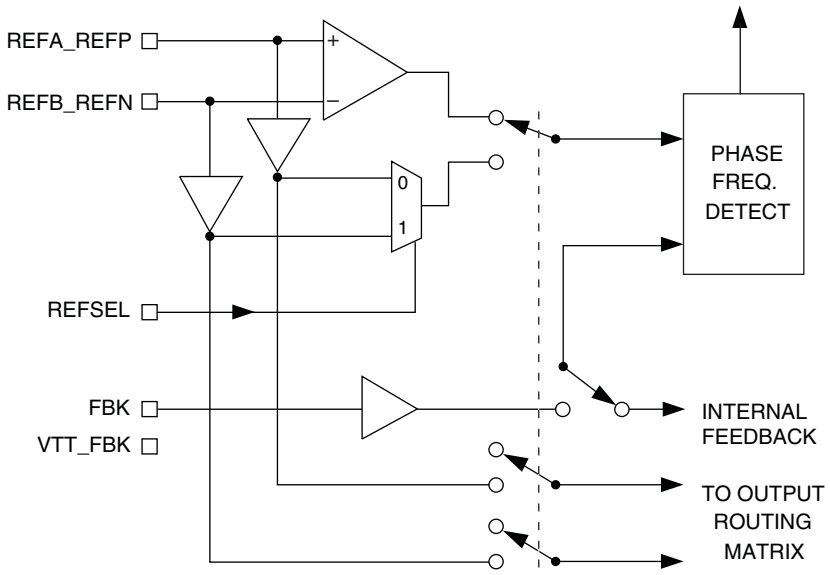
REFSEL	Selected Input
0	REFA
1	REFB

Supported input logic reference standards:

- LVTTL (3.3V)
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL

- eHSTL
- Differential SSTL1.8
- Differential SSTL2
- Differential SSTL3
- Differential HSTL
- LVDS
- LVPECL (differential, 3.3V)

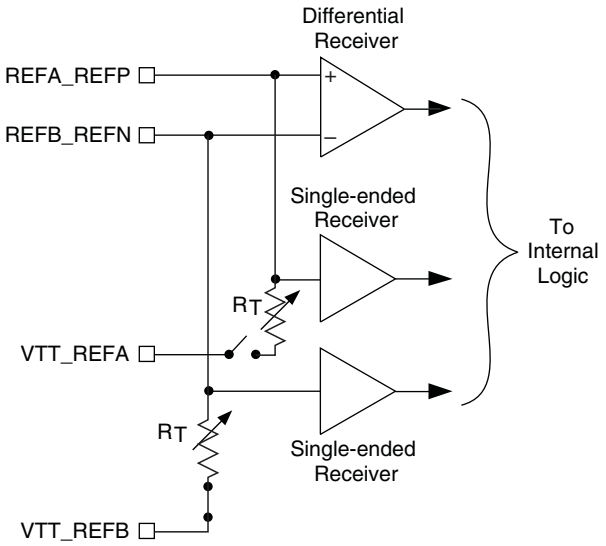
Figure 3-13. Reference and Feedback Input



Each input features internal programmable termination resistors as shown in Figure 3-14. The REFA and REFB inputs terminate to VTT_REFA and VTT_REFB respectively. In order to interface to differential clock input one should connect VTT_REFA and VTT_REFB pins together on circuit board and if necessary connect the common node to VTT supply.

The direct connection from REFA and REFB pins to the output routing matrix becomes unavailable when the REFA and REFB pins are configured as differential input pins.

Figure 3-14. Input Receiver Termination Configuration



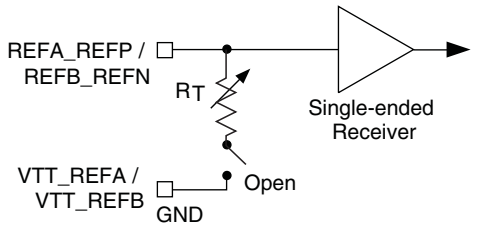
Feedback input is terminated to the VTT_FBK pin through a programmable resistor.

The following usage guidelines are suggested for interfacing to supported logic families.

LVTTL (3.3V), LVCMOS (1.8V, 2.5V, 3.3V)

The receiver should be set to LVCMOS or LVTTL mode, and the input signal can be connected to either the REFA or REFB pins. CMOS transmission lines are generally source terminated, so all termination resistors should be set to the OPEN state. Figure 3-15 shows the proper configuration. Please note that because switching thresholds are different for LVCMOS running at 1.8V, there is a separate configuration setting for this particular standard. Unused reference inputs and VTT pins should be grounded.

Figure 3-15. LVCMOS/LVTTL Input Receiver Configuration

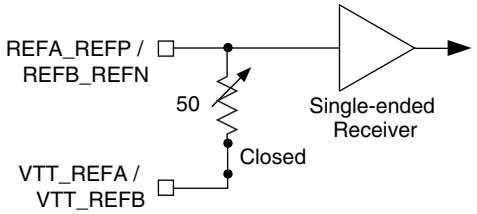


HSTL, eHSTL, SSTL2, SSTL3

The receiver should be set to HSTL/SSTL mode, and the input signal can be connected to the REFA or REFB terminal of the input pair and the associated VTT_REFA or VTT_REFB terminal should be tied to a VTT termination supply. The terminating resistor should be set to 50¾ and the engaging switch should be closed. Figure 3-16 shows an appropriate configuration. Refer to the "Recommended Operating Conditions - Supported Logic Standards" table in this data sheet for suitable values of V_{REF} and V_{TT}.

One important point to note is that the termination supplies must have low impedance and be able to both source and sink current without experiencing fluctuations. These requirements generally preclude the use of a resistive divider network, which has an impedance comparable to the resistors used, or of commodity-type linear voltage regulators, which can only source current. The best way to develop the necessary termination voltages is with a regulator specifically designed for this purpose. Because SSTL and HSTL logic is commonly used for high-performance memory busses, a suitable termination voltage supply is often already available in the system.

Figure 3-16. SSTL2, SSTL3, eHSTL, HSTL Receiver Configuration

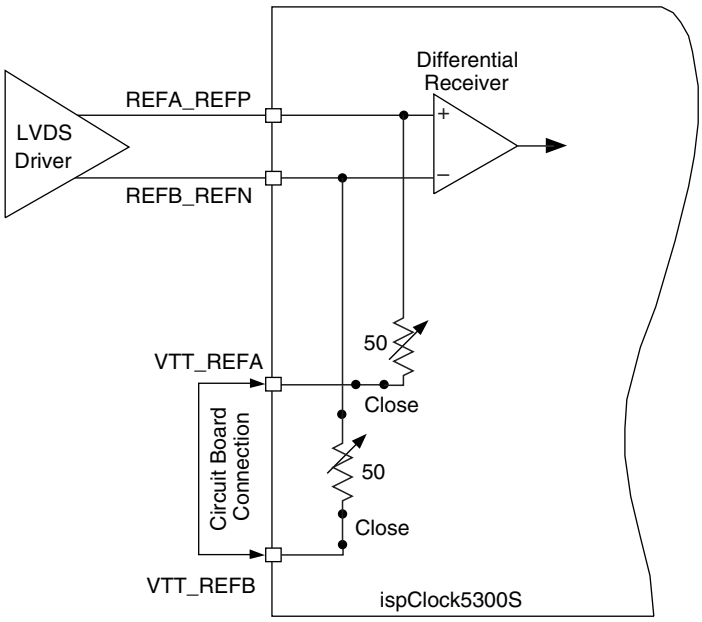


Differential LVPECL/LVDS

The receiver should be set to LVDS or LVPECL mode as required and both termination resistors should be engaged and set to 50¾. The VTT_REFA and VTT_REFB pins, however, should be connected. This creates a floating 100¾ differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 3-17.

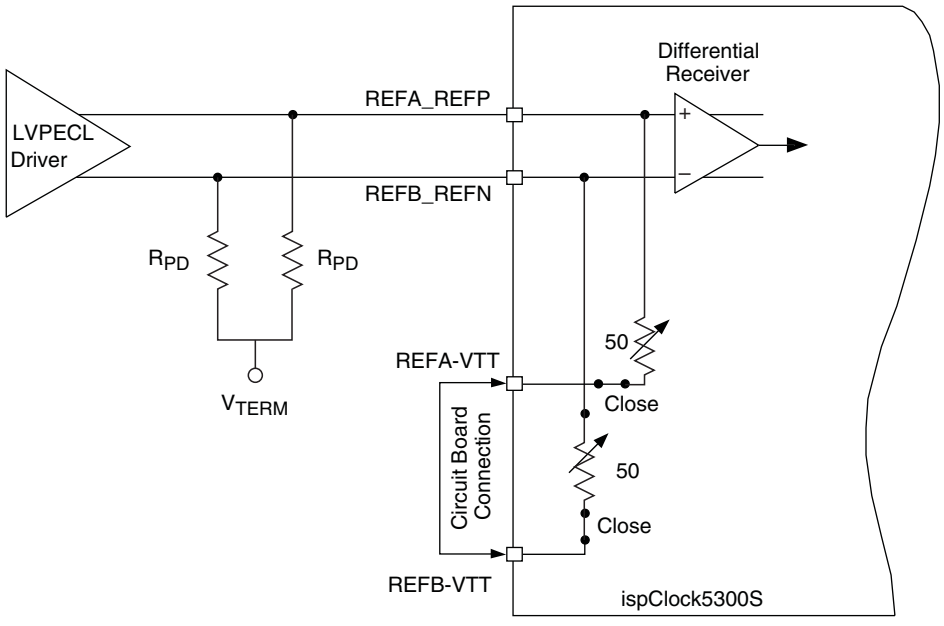
Note: the REFSEL pin should be grounded when the input receiver is configured as differential.

Figure 3-17. LVDS Input Receiver Configuration



Note that while a floating 100¾ resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. When interfacing to an LVPECL input signal, the ispClock5300S internal termination resistors should not be used for this pull-down function, as they may be damaged from excessive current. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 3-18)

Figure 3-18. LVPECL Input Receiver Configuration



Please note that while the above discussions specify using 50¾ termination impedances, the actual impedance required to properly terminate the transmission line and maintain good signal integrity may vary from this ideal. The

actual impedance required will be a function of the driver used to generate the signal and the transmission medium used (PCB traces, connectors and cabling). The ispClock5300S's ability to adjust input impedance over a range of 40¾ to 70¾ allows the user to adapt his circuit to non-ideal behaviors from the rest of the system without having to swap out components.

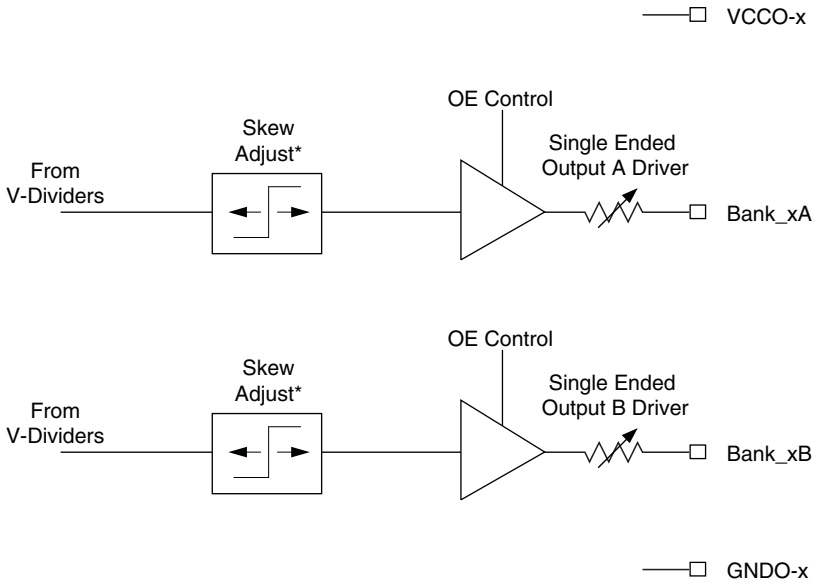
Output Drivers

The ispClock5300S provides multiple banks, with each bank supporting two high-speed clock outputs which are configurable and internally terminated. There are ten banks in the ispClock5320S, eight banks in the ispClock5316S, six banks in the ispClock5312S, four banks in the ispClock5308S and two banks in the ispClock5304S. Programmable internal source-series termination allows the ispClock5300S to be matched to transmission lines with impedances ranging from 40 to 70¾. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by external control lines. Additionally, each can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 3-19 shows a block diagram of a typical ispClock5300S output driver bank and associated skew control.

Because of the high edge rates which can be generated by the ispClock5300S clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respective output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GNDO pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 3-19. ispClock5300S Output Driver and Skew Control



*Skew Adjust Mechanism is applicable only to outputs connected to one of the three V-Dividers and when PLL is active (PLL-Bypass pin = 0). For all other conditions, Skew Adjust Mechanism is bypassed.

Each of the ispClock5300S's output driver banks can be configured to support the following logic outputs:

- LVTTL
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- eHSTL

To provide LVTTL, LVCMOS, SSTL2, SSTL3, HSTL and eHSTL outputs, the CMOS output drivers in each bank are enabled. These circuits provide logic outputs which swing from ground to the VCCO supply rail. The choice of VCCO to be supplied to a given bank is determined by the logic standard to which that bank is configured. Because each pair of outputs has its own VCCO supply pin, each bank can be independently configured to support a different logic standard. Note that the two outputs associated with a bank must necessarily be configured to the same logic standard. The source impedance of each of the two outputs in each bank may be independently set over a range of 40¾ to 70¾ in 5¾ steps. A low impedance option (Ý20¾) is also provided for cases where low source termination is desired on a given output.

Control of output slew rate is also provided in LVTTL, LVCMOS, SSTL2, SSTL3, HSTL and eHSTL output modes. Four output slew-rate settings are provided, as specified in the "Output Rise Times" and "Output Fall Times" tables in this data sheet.

Polarity control (true/inverted) is available for all output drivers. In the case of single-ended output standards, the polarity of each of the two output signals from each bank may be controlled independently.

Suggested Usage

Figure 3-20 shows a typical configuration for the ispClock5300S output driver when configured to drive an LVTTL or LVCMOS load. The ispClock5300S output impedance should be set to match the characteristic impedance of the transmission line being driven. The far end of the transmission line should be left open, with no termination resistors.

Figure 3-20. Configuration for LVTTL/LVCMOS Output Modes

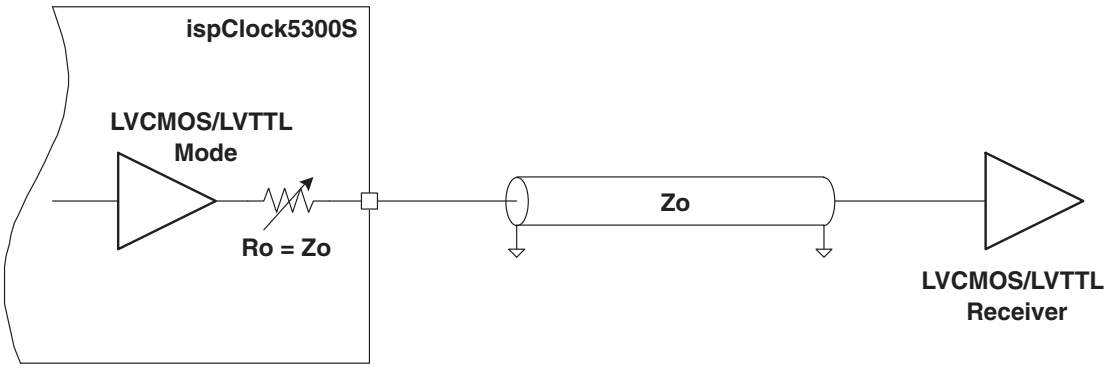
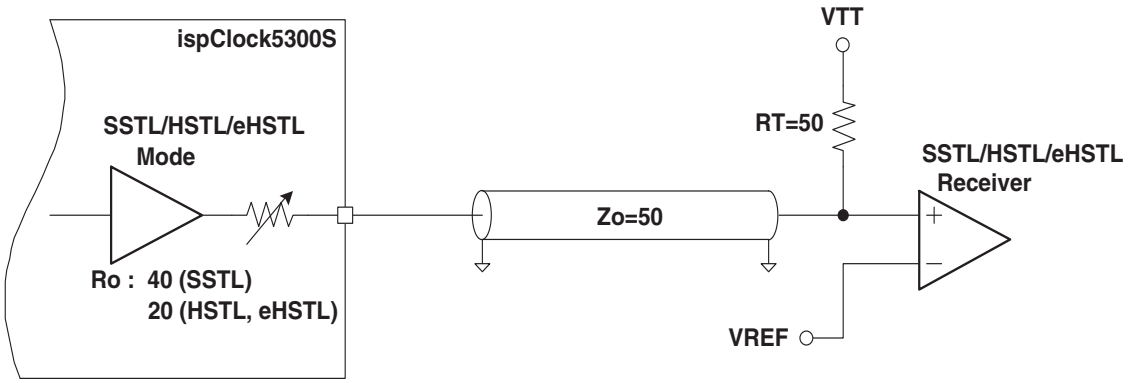


Figure 3-21 shows a typical configuration for the ispClock5300S output driver when configured to drive SSTL2, SSTL3, HSTL or eHSTL loads. The ispClock5300S output impedance should be set to 40¾ for driving SSTL2 or SSTL3 loads and to the Ý20¾ setting for driving HSTL and eHSTL. The far end of the transmission line must be terminated to an appropriate VTT voltage through a 50¾ resistor.

Figure 3-21. Configuration for SSTL2, SSTL3, and HSTL Output Modes



ispClock5300S Configurations

The ispClock5300S device can be configured to operate in four modes. They are:

- Zero Delay Buffer Mode
- Mixed Zero Delay and Non-Zero Delay Buffer Mode
- Non-Zero Delay Buffer mode 1
- Non-Zero Delay Buffer Mode 2

The output routing matrix of the ispClock5300S provides up to three independent any-to-any paths from inputs to outputs:

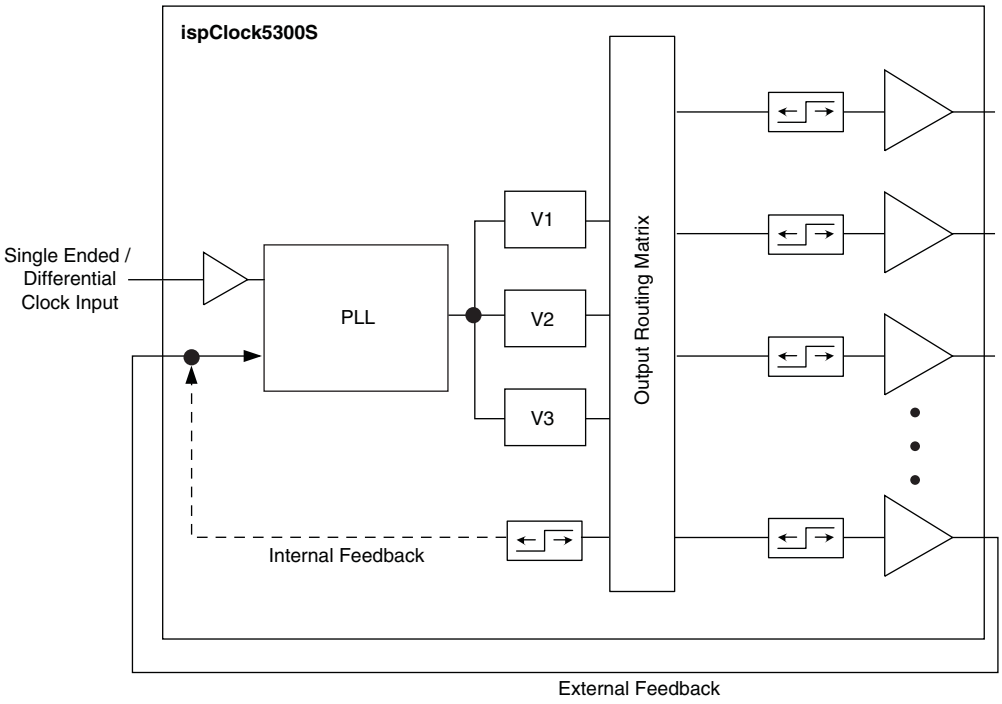
- From any V-Dividers to any output in ZDB mode or PLL Bypass modes
- From selected clock via REFSEL pin to any output (note single ended reference clock)
- From the other clock not selected by REFSEL pin to any output

Zero Delay Buffer Mode

Figure 3-22 shows the ispClock5300S device configured to operate in the Zero Delay Buffer mode. The Clock input can be single ended or differential. Two single ended clocks can be selected by the use of REFSEL pin and if the input is configured as a differential the REFSEL pin should be connected to GNDD. The input clock then drives the Phase frequency detector of the PLL. Up to 3 output clock frequencies can be generated from the input reference clock by the use of V-dividers at the output of PLL. Any V-divider output can be connected to any of the output pins. However, one of the V-dividers should be used in the feedback path to set the PLL operating frequency. The PLL can operate with internal or external feedback path.

In this mode, the skew control mechanism is active for all outputs.

Figure 3-22. ispClock5300S configured as Zero Delay Buffer Mode

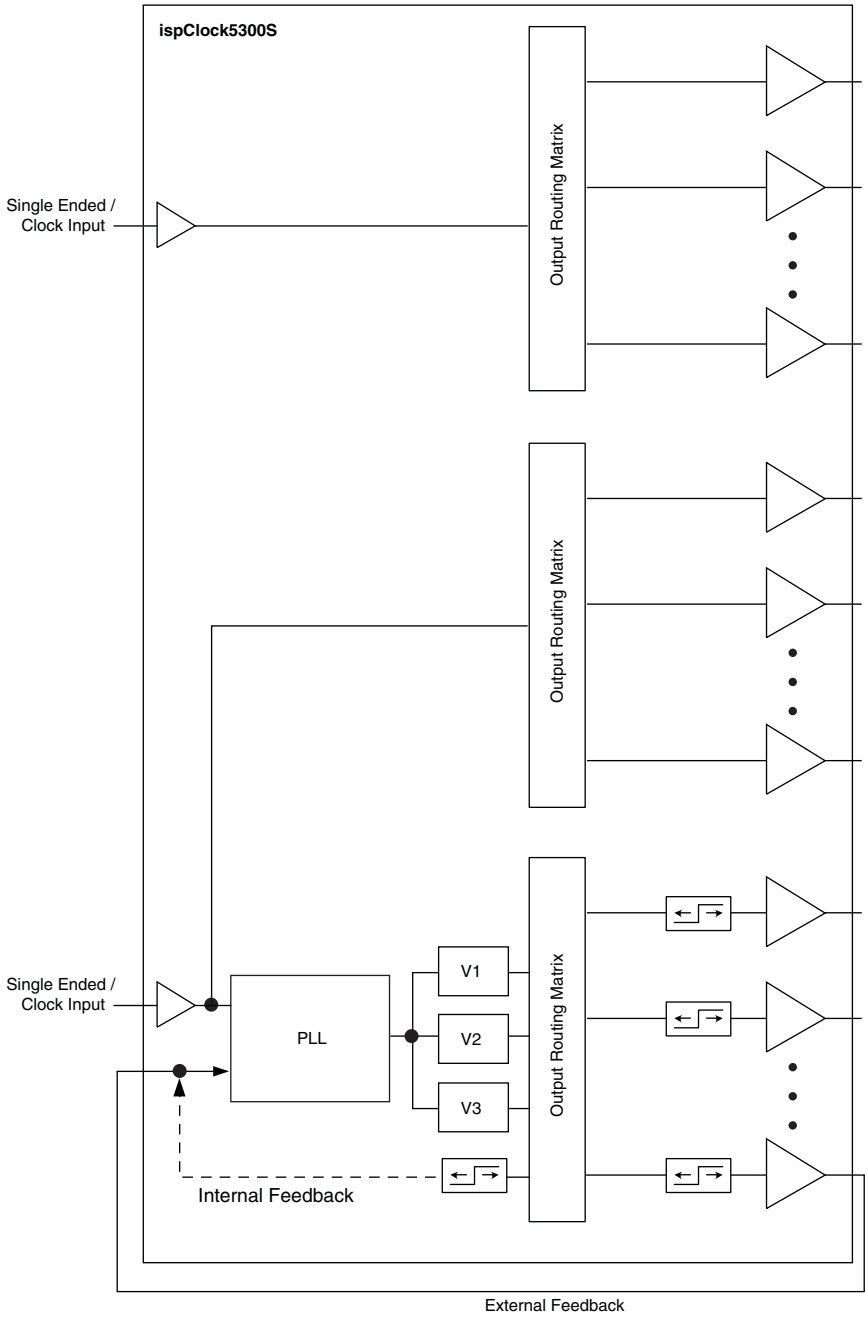


Mixed Zero Delay and Non-Zero Delay Buffer Mode

Figure 3-23 shows the operation of the ispClock5300S in Mixed Zero Delay and Non Zero Delay modes. In this mode the output switch matrix is configured to route non selected reference clock, selected reference clock, and the zero delay clock through the PLL.

The skew control mechanism is available only to clocks sourced from the PLL.

Figure 3-23. Mixed Zero Delay and Non Zero Delay Buffer Mode

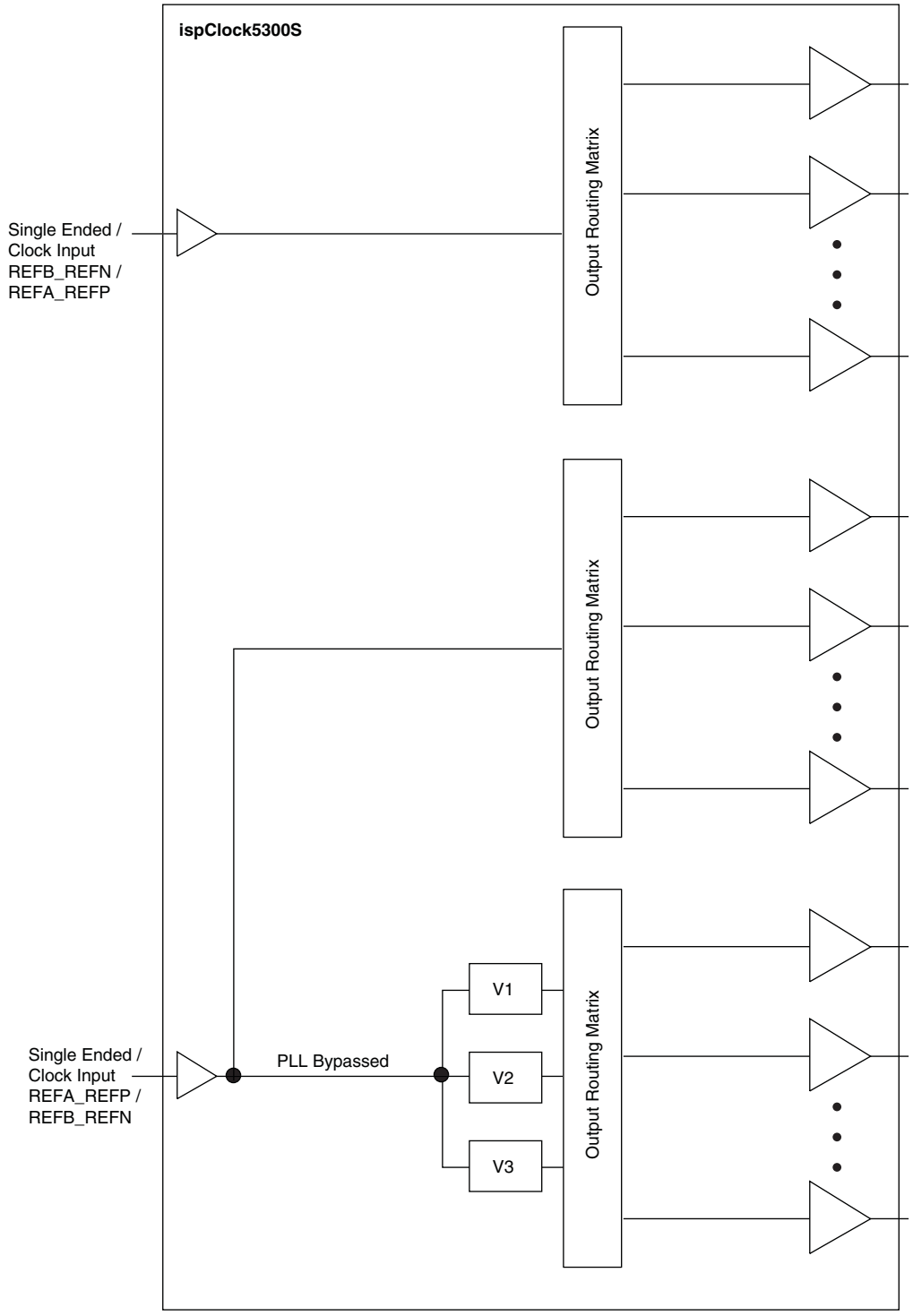


Non Zero Delay Buffer Mode 1

In the non zero delay buffer mode as shown in Figure 3-24 the output routing matrix completely bypasses the PLL. Each of the single ended input reference clocks can be routed to any number of available output clocks.

In this mode of operation there is no skew control.

Figure 3-24. Non Zero Delay Fan Out Buffer Mode 1



ispClock5300 Operating Configuration Summary

The following table summarizes the operating modes of the ispClock5300S.

Note:

- Whenever the input buffer is configured as differential input, the fan-out buffer paths become unavailable.
- Non-zero delay buffer for differential clock input is realized by using the PLL_BYPASS signal set to logical '1'.
- Output Skew control mechanism is available only to clock outputs sourced from PLL VCO.

Table 3-3. ispClock5300S Operating Modes

ispClock5300S Operating Mode	Reference Input Clocks	Skew Control	Output Clock Frequency Divider
Zero Delay Buffer Mode	Single Ended / Differential	Yes	Yes
Mixed Zero-Delay & Non-Zero Delay Buffer Mode	Single Ended Only	Only to Zero Delay Output Clocks	Only to Zero Delay Output Clocks
Non-Zero Delay Fan-out Buffer Mode 1	Single Ended Only	No	No
Non-Zero Delay Fan-out Buffer Mode 2	Single Ended / Differential	No	Only to Clocks Sourced From Bypassed PLL

Thermal Management

In applications where a majority of the ispClock5300S's outputs are active and operating at or near maximum output frequency, package thermal limitations may need to be considered to ensure a successful design. Thermal characteristics of the packages employed by Lattice Semiconductor may be found in the document *Thermal Management* which may be obtained at www.latticesemi.com.

The maximum current consumption of the digital and analog core circuitry for ispClock5312S is 150mA worst case (I_{CCD} + I_{CCA}), and each of the output banks may draw up to 16mA worst case (LVCMOS 3.60V, CL=5pF, f_{OUT}=100 MHz, both outputs in each bank enabled). This results in a total device dissipation:

$$P_{DMAX} = 3.60V \times (6 \times 16mA + 150mA) = 0.88W \quad (3)$$

With a maximum recommended operating junction temperature (T_{JOP}) of 130°C for an industrial grade device, the maximum allowable ambient temperature (T_{AMAX}) can be estimated as

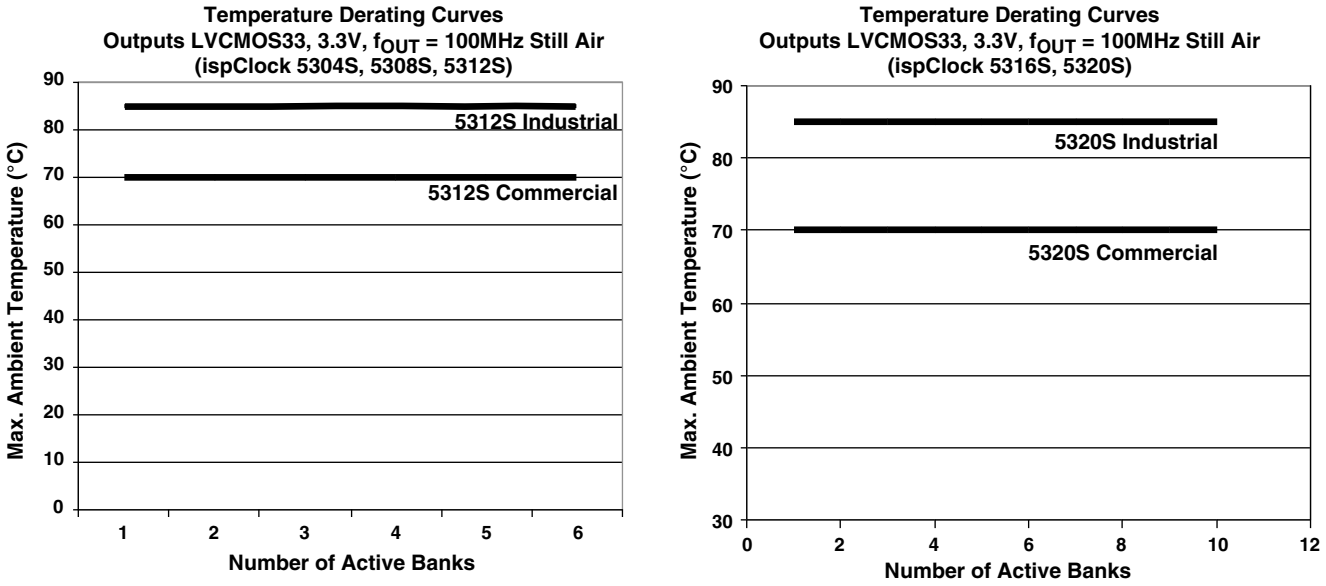
$$T_{AMAX} = T_{JOP} - PD_{MAX} \times \Theta_{JA} = 130°C - 0.88W \times 48°C/W = 85°C \quad (4)$$

where Θ_{JA} = 48°C/W for the 48 TQFP package in still air and Θ_{JA} = 42°C/W for the 64 TQFP package in still air.

The above analysis represents the worst-case scenario. Significant improvement in maximum ambient operating temperature can be realized with additional cooling. Providing a 200 LFM (Linear Feet per Minute) airflow reduces Θ_{JA} to 44°C/W for the 48 TQFP package.

While it is possible to perform detailed calculations to estimate the maximum ambient operating temperature from operating conditions, some simpler rule-of-thumb guidance can also be obtained through the derating curves shown in Figure 3-25 which shows the maximum ambient operating temperature permitted when operating a given number of output banks at the maximum output frequency.

Figure 3-25. Maximum Ambient Temperature vs. Number of Active Output Banks



Note that because of variations in circuit board mounting, construction, and layout, as well as convective and forced airflow present in a given design, actual die operating temperature is subject to considerable variation from that which may be theoretically predicted from package characteristics and device power dissipation.

Output Enable Controls ($\overline{OEX}$, $\overline{OEY}$)

The ispClock5300S family provides two output control pins for enabling and disabling clock outputs. In addition, the outputs can also be configured to be permanently enabled or permanently disabled.

Skew Control Units

Each of the ispClock5300S's clock outputs is supported by a skew control unit which allows the user to insert an individually programmable delay into each output signal. This feature is useful when it is necessary to de-skew clock signals to compensate for physical length variations among different PCB clock paths.

The ispClock5300S's skew adjustment feature provides exact and repeatable delays which exhibit extremely low channel-to-channel and device-to-device variation. This is achieved by deriving all skew timing from the VCO, which results in the skew increment being a linear function of the VCO period. For this reason, skews are defined in terms of 'unit delays', which may be programmed by the user over a range of 0 to 7. The ispClock5300S family also supports both 'fine' and 'coarse' skew modes. In fine skew mode, the unit skew ranges from 156ps to 390 ps, while in the coarse skew mode unit skew varies from 312ps to 780ps. The exact unit skew (TU) may be calculated from the VCO frequency (f_{vco}) by using the following expressions:

For fine skew mode, For coarse skew mode,

$$TU = \frac{1}{16f_{vco}} \qquad TU = \frac{1}{8f_{vco}} \tag{5}$$

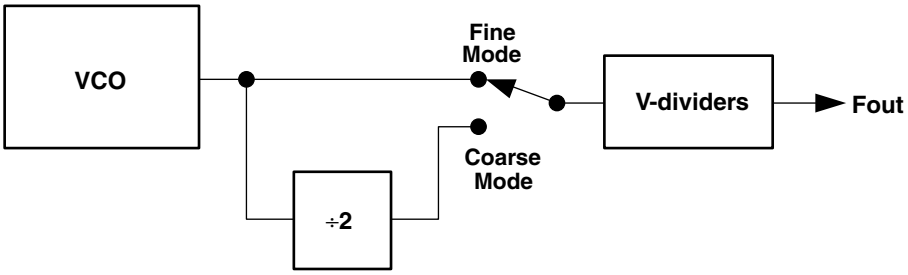
Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Coarse Skew Mode

The ispClock5300S family provides the user with the option of obtaining longer skew delays at the cost of reduced time resolution through the use of coarse skew mode. Coarse skew mode provides unit delays ranging from 312ps

(f_{VCO} = 400MHz) to 780ps (f_{VCO} = 160MHz), which is twice as long as those provided in fine skew mode. When coarse skew mode is selected, an additional divide-by-2 stage is effectively inserted between the VCO and the V-divider bank, as shown in Figure 3-26. When assigning divider settings in coarse skew mode, one must account for this additional divide-by-two so that the VCO still operates within its specified range (160-400MHz).

Figure 3-26. Additional Factor-of-2 Division in Coarse Mode



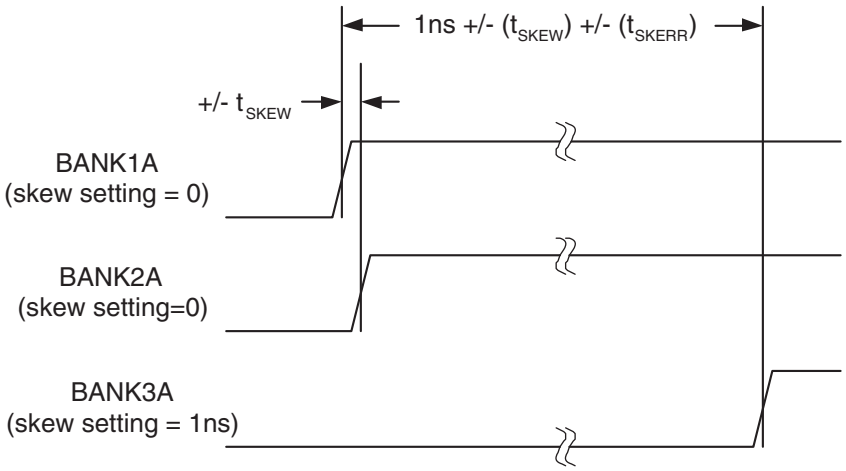
When one moves from fine skew mode to coarse skew mode with a given divider configuration, the VCO frequency will attempt to double to compensate for the additional divide-by-2 stage. Because the f_{VCO} range is not increased, however, one must modify the feedback path V-divider settings to bring f_{VCO} back into its specified operating range (160MHz to 400MHz). This can be accomplished by dividing all V-divider settings by two. All output frequencies will remain unchanged from what they were in fine mode.

Output Skew Matching and Accuracy

Understanding the various factors which relate to output skew is essential for realizing optimal skew performance in the ispClock5300S family of devices.

In the case where two outputs are identically configured, and driving identical loads, the maximum skew is defined by $t_{SKEW,}$ which is specified as a maximum of 100ps. In Figure 3-27 the Bank1A and BANK2A outputs show the skew error between two matched outputs.

Figure 3-27. Skew Matching Error Sources

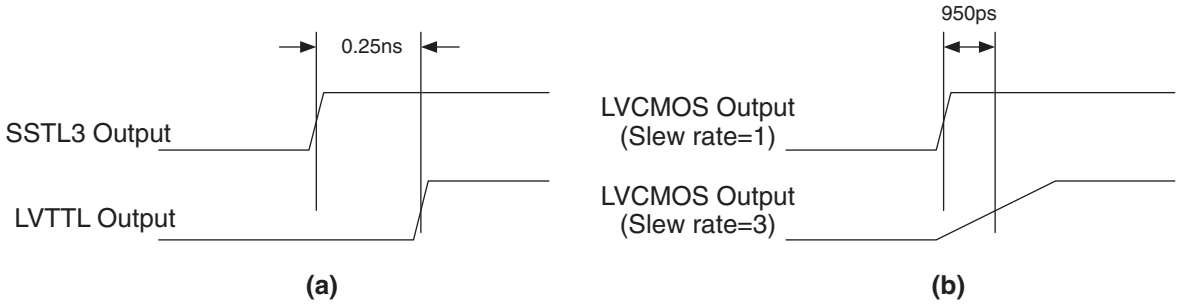


One can also program a user-defined skew between two outputs using the skew control units. Because the programmable skew is derived from the VCO frequency, as described in the previous section, the absolute skew is very accurate. The typical error for any non-zero skew setting is given by the t_{SKERR} specification. For example, if one is in fine skew mode with a VCO frequency of 250MHz, and selects a skew of 4TU, the realized skew will be 1ns, which will typically be accurate to within +/-30 ps. An example of error vs. skew setting can be found in the chart 'Typical Skew Error vs. Setting' in the typical performance characteristics section. Note that this parameter adds to output-to-output skew error only if the two outputs have *different* skew settings. The Bank1A and Bank3A

outputs in Figure 3-27 show how the various sources of skew error stack up in this case. Note that if two or more outputs are programmed to the same skew setting, then the contribution of the t_{SKERR} skew error term does not apply.

When outputs are configured or loaded differently, this also has an effect on skew matching. If an output is set to support a different logic type, this can be accounted for by using the t(ioo) output adders specified in the table 'Switching Characteristics'. That table specifies the additional skew added to an output using SSTL, HSTL, EHSTL as a base-line. For instance, if one output is specified as LVTTL, it has a delay adder relative to SSTL of 0.25ns. If another output is specified as SSTL3, then one would expect 0.25ns of additional skew between the two outputs due to this adder. This timing relationship is shown in Figure 3-28a.

Figure 3-28. Output Timing Adders for Logic Type (a) and Output Slew Rate (b)



By selecting the same feedback logic type and clock output, the output delay adders for the clock output are automatically compensated for. Similarly, a reference clock delay adder can be compensated for by selecting the same feedback input logic type and reference clock.

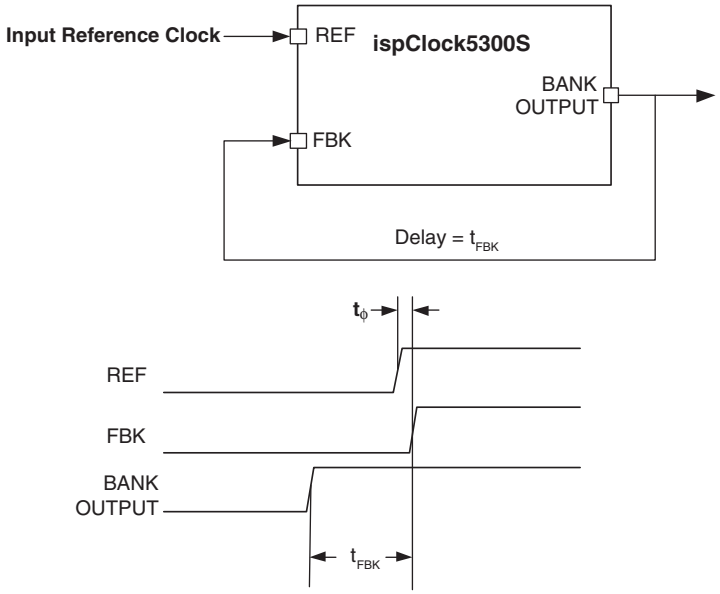
When the internal feedback mode is selected, however, one should add both input and output delay adders to t_{DELAY} specified in the Performance Characteristics PLL table to calculate the input-to-output delay.

Similarly, when one changes the slew rate of an output, the output slew rate adders (t_{IOS}) can be used to predict the resulting skew. In this case, the fastest slew setting (1) is used as the baseline against which other slews are measured. For example, in the case of outputs configured to the same logic type (e.g. LVCMOS 1.8V), if one output is set to the fastest slew rate (1, t_{IOS} = 0ps), and another set to slew rate 3 (t_{IOS} = 950ps), then one could expect 950ps of skew between the two outputs, as shown in Figure 3-28b.

Static Phase Offset and Input-Output Skew

The ispClock5300S's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. Using external feedback (Figure 3-29), the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase error. Note that any propagation delay (t_{FBK}) in the external feedback path drives the phase of the output signal *backwards* in time as measured at the output. For this reason, if zero input-to-output delays are required, the length of the signal path between the output pin and the feedback pin should be minimized.

Figure 3-29. External Feedback Mode and Timing Relationships



Other Features

RESET and Power-up Functions

To ensure proper PLL startup and synchronization of outputs, the ispClock5300S provides both internally generated and user-controllable external reset signals. An internal reset is generated whenever the device is powered up. An external reset may be applied by asserting a logic LOW at the $\overline{\text{RESET}}$ pin. Asserting $\overline{\text{RESET}}$ resets all internal dividers, and will cause the PLL to lose lock. On losing lock, the VCO frequency will begin dropping. The length of time required to regain lock is related to the length of time for which $\overline{\text{RESET}}$ was asserted.

When the ispClock5300S begins operating from initial power-on, the VCO starts running at a very low frequency (<100 MHz) which gradually increases as it approaches a locked condition. To prevent invalid outputs from being applied to the rest of the system, assert $\overline{\text{OEX}}$ or $\overline{\text{OEY}}$ high. This will result in the BANK outputs being held in a high-impedance state until the $\overline{\text{OEX}}$ or $\overline{\text{OEY}}$ pin is pulled LOW.

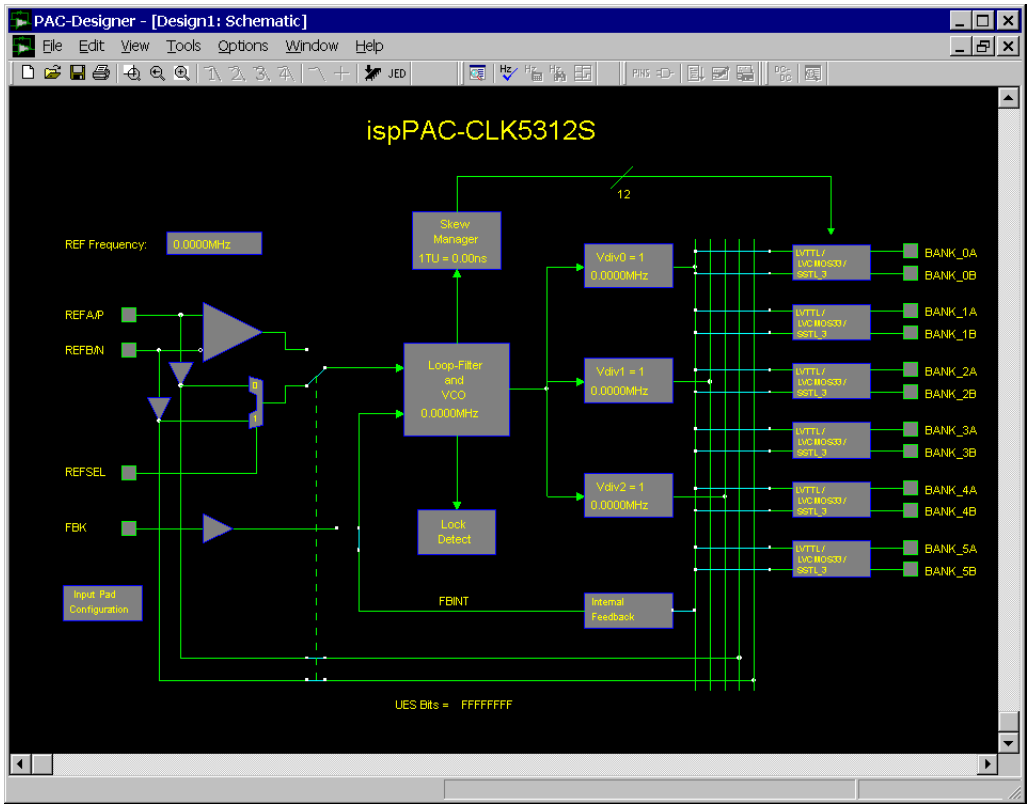
After in-system programming the device through the JTAG interface, the reset pin must be activated at least for a period of t_{PLL_RSTW} to reset the device.

If the $\overline{\text{RESET}}$ pin is not driven by an external logic it should be pulled up to V_{CCD} through a 10k¾ resistor.

Software-Based Design Environment

Designers can configure the ispClock5300S using Lattice's PAC-Designer software, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispClock5300S. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation. PAC-Designer is available for download from the Lattice web site at www.latticesemi.com. The PAC-Designer schematic window, shown in Figure 3-30 provides access to all configurable ispClock5300S elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved and downloaded to devices.

Figure 3-30. PAC-Designer Design Entry Screen



In-System Programming

The ispClock5300S is an In-System Programmable (ISP™) device. This is accomplished by integrating all E^2CMOS configuration control logic on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^2CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispClock5300S instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

A user electronic signature (UES) feature is included in the E^2CMOS memory of the ispClock5300S. This consists of 32 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Electronic Security

An electronic security “fuse” (ESF) bit is provided in every ispClock5300S device to prevent unauthorized readout of the E^2CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can not be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Production Programming Support

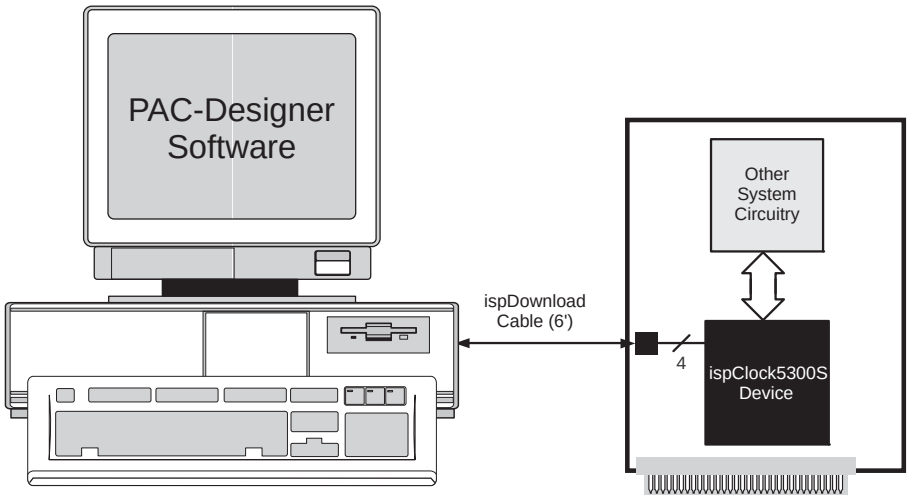
Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user’s specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

Evaluation Fixture

Included in the basic ispClock5300S Design Kit is an engineering prototype board that can be connected to the parallel port of a PC using a Lattice ispDOWNLOAD® cable. It demonstrates proper layout techniques for the ispClock5300S and can be used in real time to check circuit operation as part of the design process. Input and output connections (SMA connectors for all RF signals) are provided to aid in the evaluation of the ispClock5300S for a given application. (Figure 3-31).

Part Number	Description
PAC-SYSTEMCLK5312S	Complete system kit, evaluation board, ispDOWNLOAD cable and software.

Figure 3-31. Download from a PC



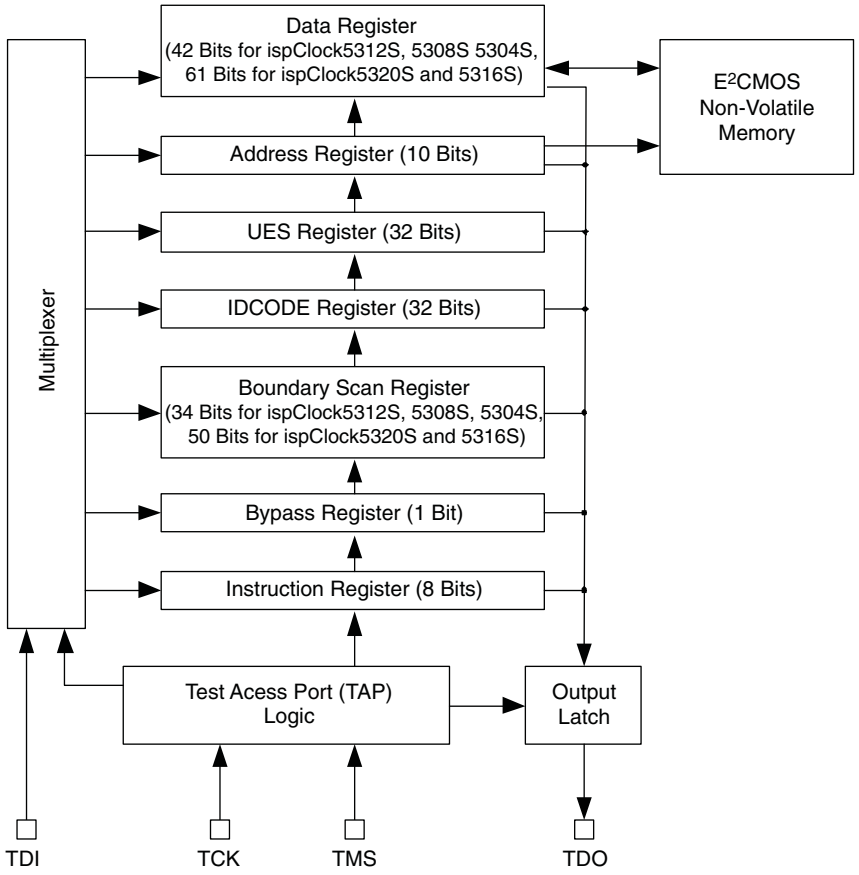
IEEE Standard 1149.1 Interface (JTAG)

Serial Port Programming Interface Communication with the ispClock5300S is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispClock5300S both as a serial programming interface, and for boundary scan test purposes. A brief description of the ispClock5300S JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990 (which now includes IEEE Std. 1149.1a-1993).

Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispClock5300S. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E^2CMOS cells. It is these non-volatile cells that store the configuration of the ispClock5300S. A set of instructions are defined that access all data registers and perform other internal control operations. For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. Figure 3-32 shows how the instruction and various data registers are organized in an ispClock5300S.

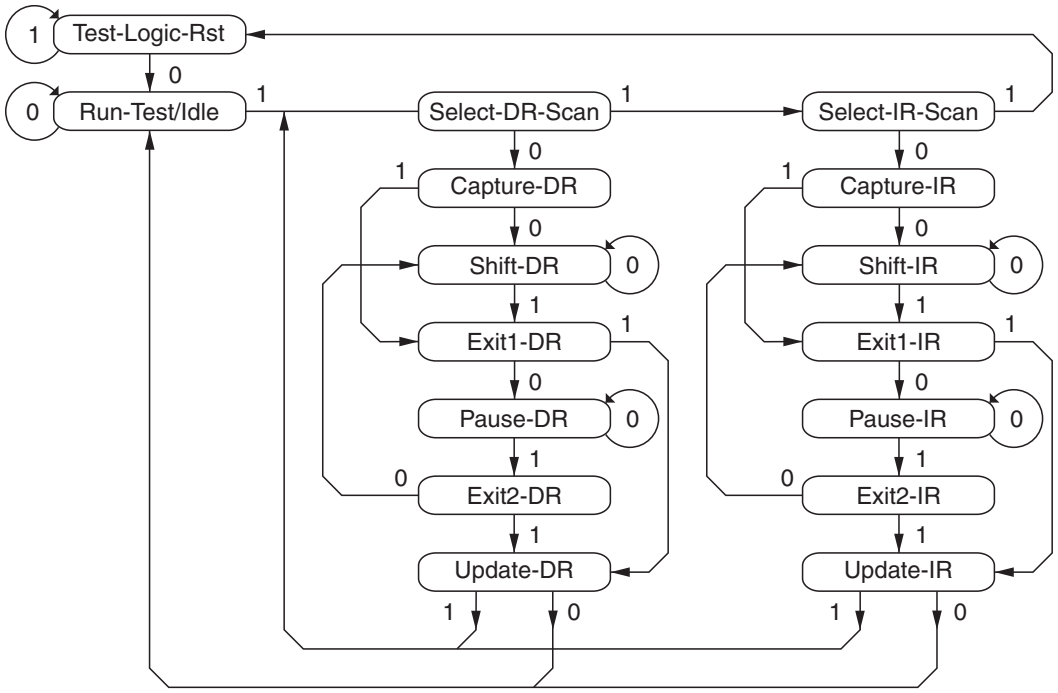
Figure 3-32. ispClock5300S TAP Registers



TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the TMS input as shown in Figure 3-33. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run- Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

Figure 3-33. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain. From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispClock5300S contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified.

For ispClock5300S, the instruction word length is eight bits. All ispClock5300S instructions available to users are shown in Table 3-4.

The following table lists the instructions supported by the ispClock5300S JTAG Test Access Port (TAP) controller:

Table 3-4. ispClock5300S TAP Instruction Table

Instruction	Code	Description
EXTEST	0000 0000	External Test.
ADDRESS_SHIFT	0000 0001	Address register (10 bits)
DATA_SHIFT	0000 0010	Address column data register (42 bits for ispClock5312S, 5308S and 5304S; 61 bits for ispClock5320S and 5316S)
BULK_ERASE	0000 0011	Bulk Erase
PROGRAM	0000 0111	Program column data register to E^2
PROGRAM_SECURITY	0000 1001	Program Electronic Security Fuse
VERIFY	0000 1010	Verify column
DISCHARGE	0001 0100	Fast VPP Discharge
PROGRAM_ENABLE	0001 0101	Enable Program Mode
IDCODE	0001 0110	Address Manufacturer ID code register (32 bits)
USERCODE	0001 0111	Read UES data from E^2 and addresses UES register (32 bits)
PROGRAM_USERCODE	0001 1010	Program UES register into E^2
PROGRAM_DISABLE	0001 1110	Disable Program Mode
HIGHZ	0001 1000	Force all outputs to High-Z state
SAMPLE/PRELOAD	0001 1100	Capture current state of pins to boundary scan register
CLAMP	0010 0000	Drive I/Os with boundary scan register
INTEST	0010 1100	Performs in-circuit functional testing of device.
ERASE DONE	0010 0100	Erases the ‘Done’ bit only
PROG_INCR	0010 0111	Program column data register to E^2 and auto-increment address register
VERIFY_INCR	0010 1010	Load column data register from E^2 and auto-increment address register
PROGRAM_DONE	0010 1111	Programs the ‘Done’ Bit
NOOP	0011 0000	Functions Similarly to CLAMP instruction
BYPASS	1xxx xxxx	Bypass - Connect TDO to TDI

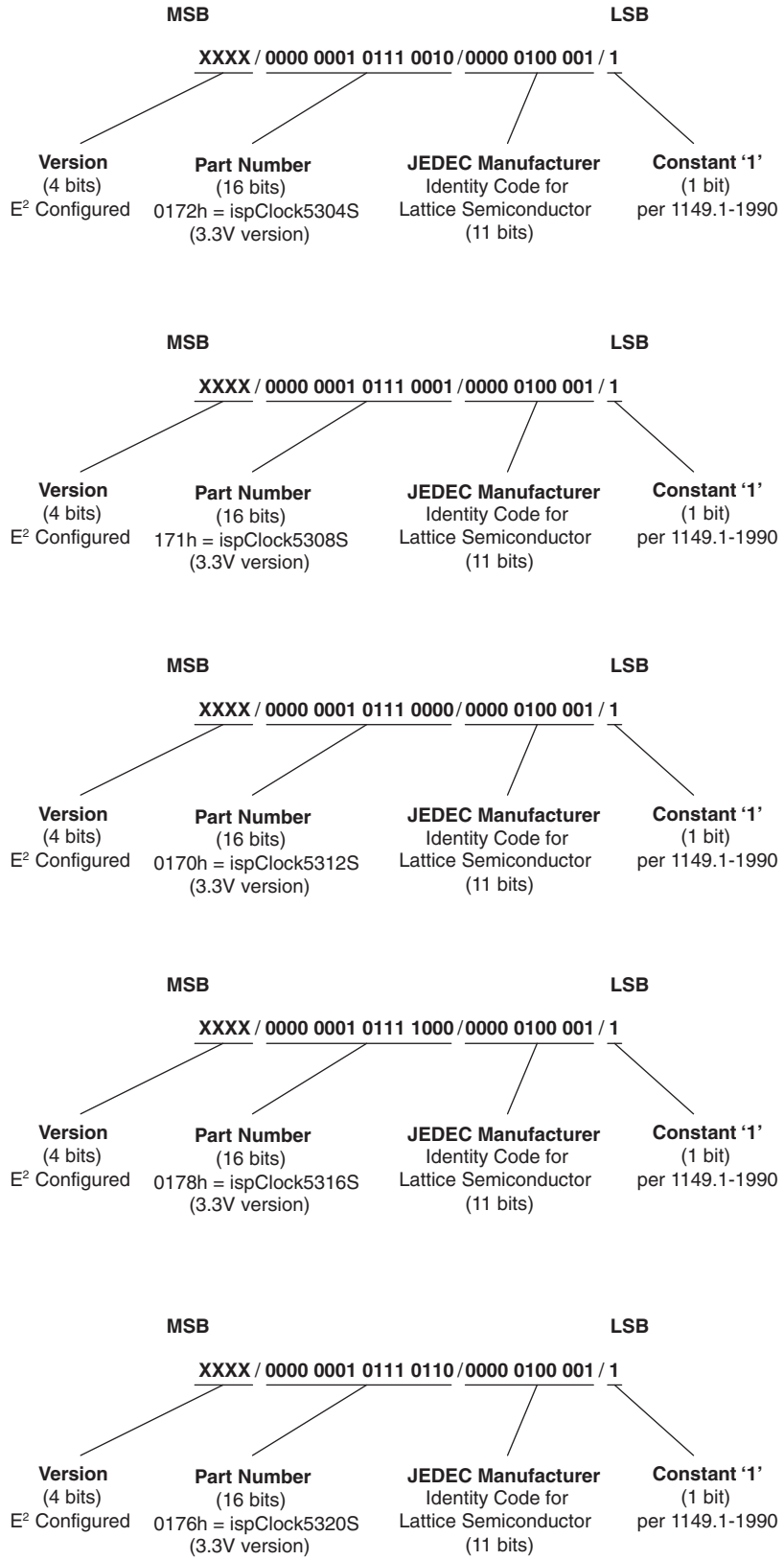
BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispClock5300S. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (111111).

The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The bit code for this instruction is defined by Lattice as shown in Table 3-4.

The **EXTEST** (external test) instruction is required and will place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispClock5300S and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device type and version code (Figure 3-34). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 3-4.

Figure 3-34. ispClock5300S Family ID Codes



In addition to the four instructions described above, there are 20 unique instructions specified by Lattice for the ispClock5300S. These instructions are primarily used to interface to the various user registers and the E^2CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device, including boundary scan operations. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 3-4.

PROGRAM_ENABLE – This instruction enables the ispClock5300S programming mode.

PROGRAM_DISABLE – This instruction disables the ispClock5300S programming mode.

BULK_ERASE – This instruction will erase all E^2CMOS bits in the device, including the UES data and electronic security fuse (ESF). A bulk erase instruction must be issued before reprogramming a device. The device must already be in programming mode for this instruction to execute.

ADDRESS_SHIFT – This instruction shifts address data into the address register (10 bits) in preparation for either a PROGRAM or VERIFY instruction.

DATA_SHIFT – This instruction shifts data into or out of the data register (43 bits for ispClock5312, 5308 and 5304; 61 bits for ispClock5320 and 5316), and is used with both the PROGRAM and VERIFY instructions.

PROGRAM – This instruction programs the contents of the data register to the E^2CMOS memory column pointed to by the address register. The device must already be in programming mode for this instruction to execute.

PROG_INCR – This instruction first programs the contents of the data register into E^2CMOS memory column pointed to by the address register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

PROGRAM_SECURITY – This instruction programs the electronic security fuse (ESF). This prevents data other than the ID code and UES strings from being read from the device. The electronic security fuse may only be reset by issuing a BULK_ERASE command. The device must already be in programming mode for this instruction to execute.

VERIFY – This instruction loads data from the E^2CMOS array into the column register. The data may then be shifted out. The device must already be in programming mode for this instruction to execute.

VERIFY_INCR – This instruction copies the E^2CMOS column pointed to by the address register into the data column register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispClock5300S for a read cycle.

PROGRAM_USERCODE – This instruction writes the contents of the UES register (32 bits) into E^2CMOS memory. The device must already be in programming mode for this instruction to execute.

USERCODE – This instruction both reads the UES string (32 bits) from E^2CMOS memory into the UES register and addresses the UES register so that this data may be shifted in and out.

HIGHZ – This instruction forces all outputs into a High-Z state.

CLAMP – This instruction drives I/O pins with the contents of the boundary scan register.

INTEST – This instruction performs in-circuit functional testing of the device.

ERASE_DONE – This instruction erases the ‘DONE’ bit only. This instruction is used to disable normal operation of the device while in programming mode until a valid configuration pattern has been programmed.

PROGRAM_DONE – This instruction programs the ‘DONE’ bit only. This instruction is used to enable normal device operation after programming is complete.

NOOP – This instruction behaves similarly to the CLAMP instruction.

Pin Descriptions – ispClock5304S, 5308S, 5312S

Pin Name	Description	Pin Type	Pin Number		
			ispClock5304S 48 TQFP	ispClock5308S 48 TQFP	ispClock5312S 48 TQFP
VCCO_0	Output Driver '0' VCC	Power	5	5	1
VCCO_1	Output Driver '1' VCC	Power	32	9	5
VCCO_2	Output Driver '2' VCC	Power	—	28	9
VCCO_3	Output Driver '3' VCC	Power	—	32	28
VCCO_4	Output Driver '4' VCC	Power	—	—	32
VCCO_5	Output Driver '5' VCC	Power	—	—	36
GNDO_0	Output Driver '0' Ground	GND	7	7	3
GNDO_1	Output Driver '1' Ground	GND	30	11	7
GNDO_2	Output Driver '2' Ground	GND	—	26	11
GNDO_3	Output Driver '3' Ground	GND	—	30	26
GNDO_4	Output Driver '4' Ground	GND	—	—	30
GNDO_5	Output Driver '5' Ground	GND	—	—	34
BANK_0A	Clock Output driver 0, 'A' output	Output	6	6	2
BANK_0B	Clock Output driver 0, 'B' output	Output	8	8	4
BANK_1A	Clock Output driver 1, 'A' output	Output	31	10	6
BANK_1B	Clock Output driver 1, 'B' output	Output	29	12	8
BANK_2A	Clock Output driver 2, 'A' output	Output	—	27	10
BANK_2B	Clock Output driver 2, 'B' output	Output	—	25	12
BANK_3A	Clock Output driver 3, 'A' output	Output	—	31	27
BANK_3B	Clock Output driver 3, 'B' output	Output	—	29	25
BANK_4A	Clock Output driver 4, 'A' output	Output	—	—	31
BANK_4B	Clock Output driver 4, 'B' output	Output	—	—	29
BANK_5A	Clock Output driver 5, 'A' output	Output	—	—	35
BANK_5B	Clock Output driver 5, 'B' output	Output	—	—	33
VCCA	Analog VCC for PLL circuitry	Power	46	46	46
GNDA	Analog Ground for PLL circuitry	GND	47	47	47
VCCD	Digital Core VCC	Power	21, 22	21, 22	21, 22
GNDD	Digital GND	GND	23, 24, 48	23, 24, 48	23, 24, 48
REFA_REFP	Clock Reference A/Positive Differential input[3]	Input	14	14	14
REFB_REFN	Clock Reference B/Negative Differential input[3]	Input	15	15	15
REFSEL	Clock Reference Select input (LVCMOS)	Input[1]	19	19	19
VTT_REFA	Termination voltage for reference input A	Power	13	13	13
FBK	Feedback Input[3]	Input	17	17	17
VTT_FBK	Termination voltage for feedback input	Power	18	18	18
VTT_REFB	Termination input for reference input B	Power	16	16	16
VCCJ	JTAG interface VCC	Power	41	41	41
TDO	JTAG TDO Output line	Output	37	37	37
TDI	JTAG TDI Input line	Input[2]	40	40	40
TCK	JTAG Clock Input	Input	39	39	39
TMS	JTAG Mode Select	Input[2]	38	38	38

Pin Descriptions – ispClock5304S, 5308S, 5312S (Continued)

Pin Name	Description	Pin Type	Pin Number		
			ispClock5304S 48 TQFP	ispClock5308S 48 TQFP	ispClock5312S 48 TQFP
LOCK	PLL Lock indicator, HIGH indicates PLL lock	Output	45	45	45
$\overline{OEX}$	Output Enable X	Input[1]	43	43	43
$\overline{OEY}$	Output Enable Y	Input[1]	42	42	42
PLL_BYPASS	PLL Bypass	Input[1]	44	44	44
$\overline{RESET}$	Reset PLL	Input[2]	20	20	20
NC	No internal connection	n/a	1, 2, 3, 4, 9, 10, 11, 12, 25, 26, 27, 28, 33, 34, 35, 36	1, 2, 3, 4, 33, 34, 35, 36	n/a

1. Internal pull-down resistor.
2. Internal pull-up resistor.
3. Must be connected to GNDD if this pin is not used.

Pin Descriptions – ispClock5316S, 5320S

Pin Name	Description	Pin Type	ispClock5316S 64 TQFP	ispClock5320S 64 TQFP
VCC_0	Output Driver '0' VCC	Power	63	63
VCC_1	Output Driver '1' VCC	Power	3	3
VCC_2	Output Driver '2' VCC	Power	7	7
VCC_3	Output Driver '3' VCC	Power	11	11
VCC_4	Output Driver '4' VCC	Power	38	17
VCC_5	Output Driver '5' VCC	Power	42	32
VCC_6	Output Driver '6' VCC	Power	46	38
VCC_7	Output Driver '7' VCC	Power	50	42
VCC_8	Output Driver '8' VCC	Power	—	46
VCC_9	Output Driver '9' VCC	Power	—	50
GND_0	Output Driver '0' GND	GND	64	64
GND_1	Output Driver '1' GND	GND	6	6
GND_2	Output Driver '2' GND	GND	10	10
GND_3	Output Driver '3' GND	GND	14	14
GND_4	Output Driver '4' GND	GND	35	18
GND_5	Output Driver '5' GND	GND	39	31
GND_6	Output Driver '6' GND	GND	43	35
GND_7	Output Driver '7' GND	GND	49	39
GND_8	Output Driver '8' GND	GND	—	43
GND_9	Output Driver '9' GND	GND	—	49
BANK_0A	Clock Output Driver 0, 'A' output	Output	1	1
BANK_0B	Clock Output Driver 0, 'B' output	Output	2	2
BANK_1A	Clock Output Driver 1, 'A' output	Output	4	4
BANK_1B	Clock Output Driver 1, 'B' output	Output	5	5
BANK_2A	Clock Output Driver 2, 'A' output	Output	8	8
BANK_2B	Clock Output Driver 2, 'B' output	Output	9	9
BANK_3A	Clock Output Driver 3, 'A' output	Output	12	12
BANK_3B	Clock Output Driver 3, 'B' output	Output	13	13
BANK_4A	Clock Output Driver 4, 'A' output	Output	37	15
BANK_4B	Clock Output Driver 4, 'B' output	Output	36	16
BANK_5A	Clock Output Driver 5, 'A' output	Output	41	34
BANK_5B	Clock Output Driver 5, 'B' output	Output	40	33
BANK_6A	Clock Output Driver 6, 'A' output	Output	45	37
BANK_6B	Clock Output Driver 6, 'B' output	Output	44	36
BANK_7A	Clock Output Driver 7, 'A' output	Output	48	41
BANK_7B	Clock Output Driver 7, 'B' output	Output	47	40
BANK_8A	Clock Output Driver 8, 'A' output	Output	—	45
BANK_8B	Clock Output Driver 8, 'B' output	Output	—	44
BANK_9A	Clock Output Driver 9, 'A' output	Output	—	48
BANK_9B	Clock Output Driver 9, 'B' output	Output	—	47
VCCA	Analog VCC for PLL Circuitry	Power	60	60
GNDA	Analog Ground for PLL circuitry	GND	61	61
VCCD	Digital Core VCC	Power	27, 28	27, 28

Pin Descriptions – ispClock5316S, 5320S (Continued)

Pin Name	Description	Pin Type	ispClock5316S 64 TQFP	ispClock5320S 64 TQFP
GNDD	Digital GND	GND	18, 29, 30, 31, 62	29, 30, 62
REFA_REFP	Clock Reference A/ Positive Differential Input[3]	Input	20	20
REFB_REFN	Clock Reference B/ Negative Differential Input[3]	Input	21	21
REFSEL	Clock Reference Select input (LVCMOS)	Input	25	25
VTT_REFA	Termination voltage for reference input A	Power	19	19
FBK	Feedback input[3]	Input	23	23
VTT_FBK	Termination voltage for feedback input	Power	24	24
VTT_REFB	Termination voltage for reference input B	Power	22	22
VCCJ	JTAG Interface VCC	Power	55	55
TDO	JTAG TDO output	Output	51	51
TDI	JTAG TDI input	Input[2]	54	54
TCK	JTAG Clock input	Input	53	53
TMS	JTAG Mode select	Input[2]	52	52
LOCK	PLL Lock indicator, HIGH indicates PLL Lock	Output	59	59
$\overline{\text{OEX}}$	Output enable X	Input[1]	57	57
$\overline{\text{OEY}}$	Output enable Y	Input[1]	56	56
PLL_BYPASS	PLL Bypass	Input[1]	58	58
$\overline{\text{RESET}}$	Reset PLL	Input[2]	26	26
NC	No internal connection	N/A	15, 16, 17, 32, 33, 34	—

1. Internal pull-down resistor.
2. Internal pull-up resistor.
3. Must be connected to GNDD if not used.

Detailed Pin Descriptions

VCCO_[0..9], GNDO_[0..9] – These pins provide power and ground for each of the output banks. In the case when an output bank is unused, its corresponding VCCO pin may be left unconnected or preferably should be tied to ground. ALL GNDO pins should be tied to ground regardless of whether the associated bank is used or not. When a bank is used, it should be individually bypassed with a capacitor in the range of 0.01 to 0.1µF as close to its VCCO and GNDO pins as is practical.

BANK_[0..9]A, BANK_[0..9]B – These pins provide clock output signals. The choice of output driver type (CMOS, SSTL, etc.) may be selected on a bank-by-bank basis. The output impedance and slew rate may be selected on an output-by-output basis.

VCCA, GNDA – These pins provide analog supply and ground for the ispClock5300S family's internal analog circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity, it is suggested that the supply to the VCCA pin be isolated from other circuitry with a ferrite bead.

VCCD, GNDD – These pins provide digital supply and ground for the ispClock5300S family's internal digital circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity it is suggested that the supply to the VCCD pins be isolated with ferrite beads.

VCCJ – This pin provides power and a reference voltage for use by the JTAG interface circuitry. It may be set to allow the ispClock5300S family devices to function in JTAG chains operating at voltages differing from VCCD.

REFA_REFP, REFB_REFN – These input pins provide the inputs for clock signals, and can accommodate either single ended or differential signal protocols.

REFSEL – This input pin is used to select which clock input pair (REFA or REB) is selected for use as the reference input. When REFSEL=0, REFA is used, and when REFSEL=1, REFB is used.

VTT_REFA, VTT_REFB – These pins are used to provide a termination voltage for the reference inputs when they are configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases.

FBK – This input pin provides feedback sense of the output clock signal, and can accommodate any of the single-ended logic types.

VTT_FBK – This pin is used to provide a termination voltage for the feedback input when it is configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases.

TDO, TDI, TCK, TMS – These pins comprise the ispClock5300S device's JTAG interface. The signal levels for these pins are determined by the selection of the VCCJ voltage.

LOCK – This output pin indicates that the device's PLL is in a locked condition when it goes HIGH.

$\overline{\text{OEX}}$, $\overline{\text{OEY}}$ – These pins are used to enable the outputs or put them into a high-impedance condition. Each output may be set so that it is always on, always off, enabled by $\overline{\text{OEX}}$ or enabled by $\overline{\text{OEY}}$.

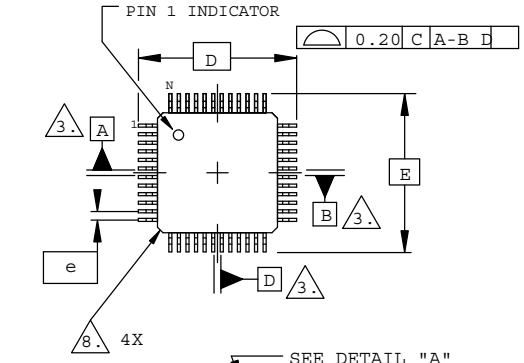
PLL_BYPASS – When this pin is pulled LOW, the V-dividers are driven from the output of the device's VCO, and the device behaves as a phase-locked loop. When this pin is pulled HIGH, the V-dividers are driven directly from a selected reference input, and the PLL functions are effectively bypassed.

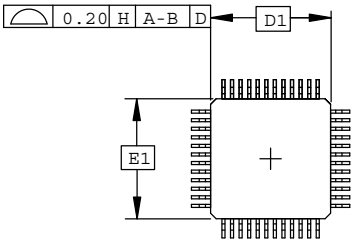
$\overline{\text{RESET}}$ – When this pin is pulled LOW, all on-board counters are reset, and lock is lost. If the $\overline{\text{RESET}}$ pin is not driven by an external logic it should be pulled up to V_{CCD} through a 10k¾ resistor.

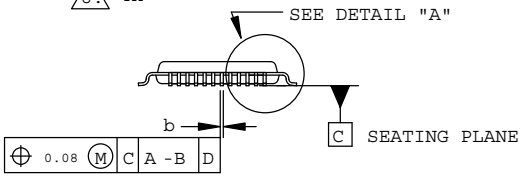
NC – These pins have no internal connection. It is recommended that they be left unconnected.

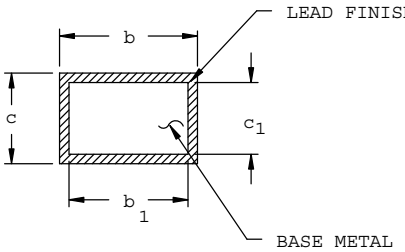
Package Diagrams

48-Pin TQFP (Dimensions in Millimeters)

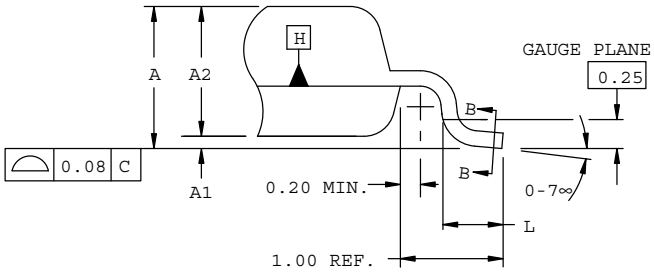








SECTION B - B



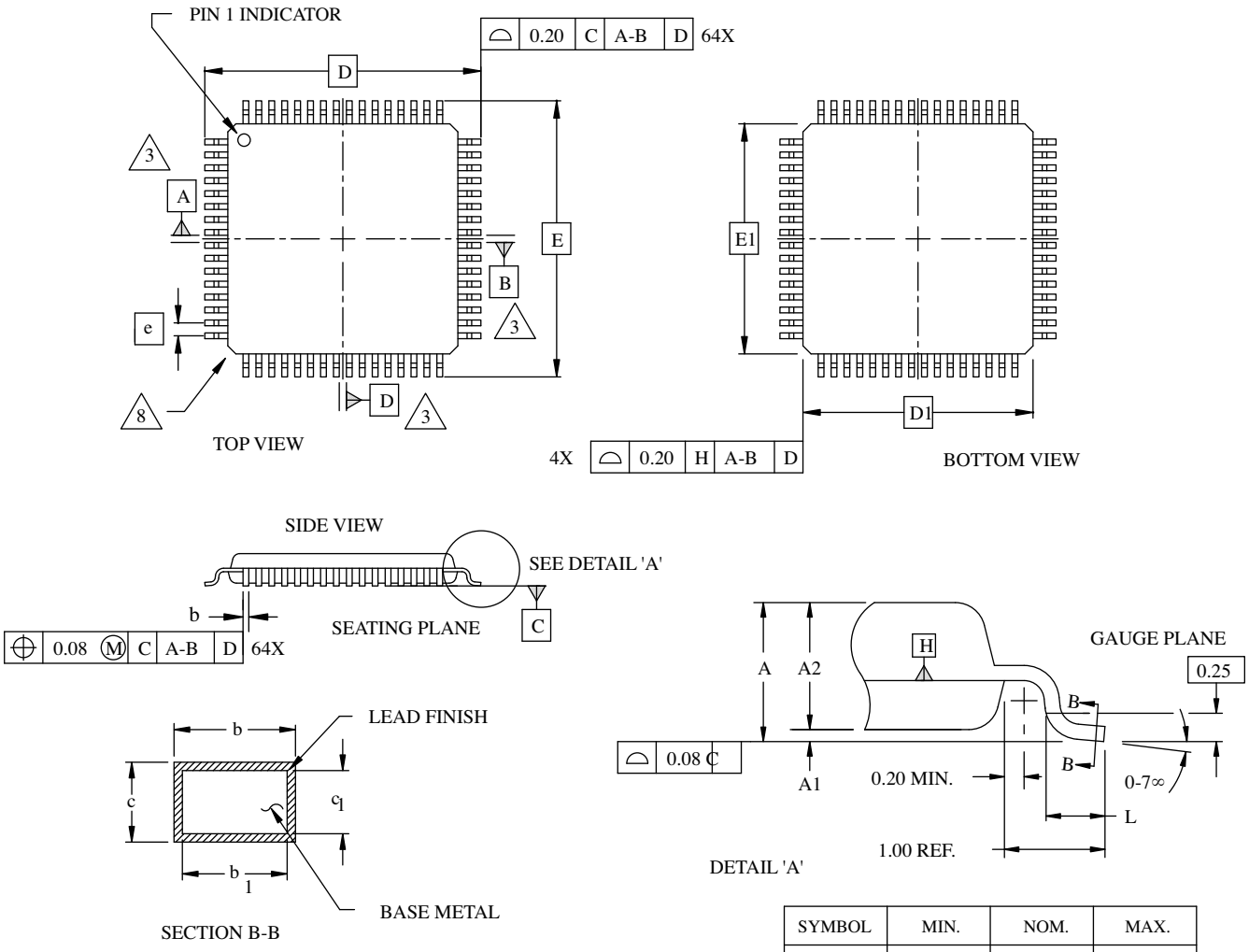
DETAIL "A"

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
5. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MM.
6. SECTION B-B: THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.
7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		9.00 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
N		48	
e		0.50 BSC	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.13	0.16

64-Pin TQFP (Dimensions in Millimeters)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
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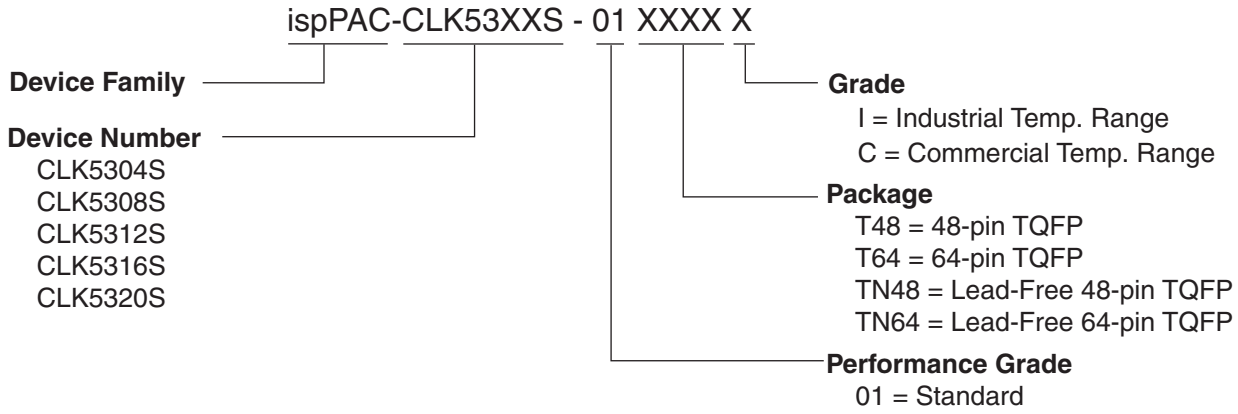
   THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.
7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
L	0.45	0.60	0.75
N		64	
e		0.50 BSC	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	-	0.16

Part Number Description



Ordering Information

Conventional Packaging

Commercial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5320S-01T64C	20	3.3V	TQFP	64
ispPAC-CLK5316S-01T64C	16	3.3V	TQFP	64
ispPAC-CLK5312S-01T48C	12	3.3V	TQFP	48
ispPAC-CLK5308S-01T48C	8	3.3V	TQFP	48
ispPAC-CLK5304S-01T48C	4	3.3V	TQFP	48

Industrial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5320S-01T64I	20	3.3V	TQFP	64
ispPAC-CLK5316S-01T64I	16	3.3V	TQFP	64
ispPAC-CLK5312S-01T48I	12	3.3V	TQFP	48
ispPAC-CLK5308S-01T48I	8	3.3V	TQFP	48
ispPAC-CLK5304S-01T48I	4	3.3V	TQFP	48

Lead-Free Packaging

Commercial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5320S-01TN64C	20	3.3V	Lead-Free TQFP	64
ispPAC-CLK5316S-01TN64C	16	3.3V	Lead-Free TQFP	64
ispPAC-CLK5312S-01TN48C	12	3.3V	Lead-Free TQFP	48
ispPAC-CLK5308S-01TN48C	8	3.3V	Lead-Free TQFP	48
ispPAC-CLK5304S-01TN48C	4	3.3V	Lead-Free TQFP	48

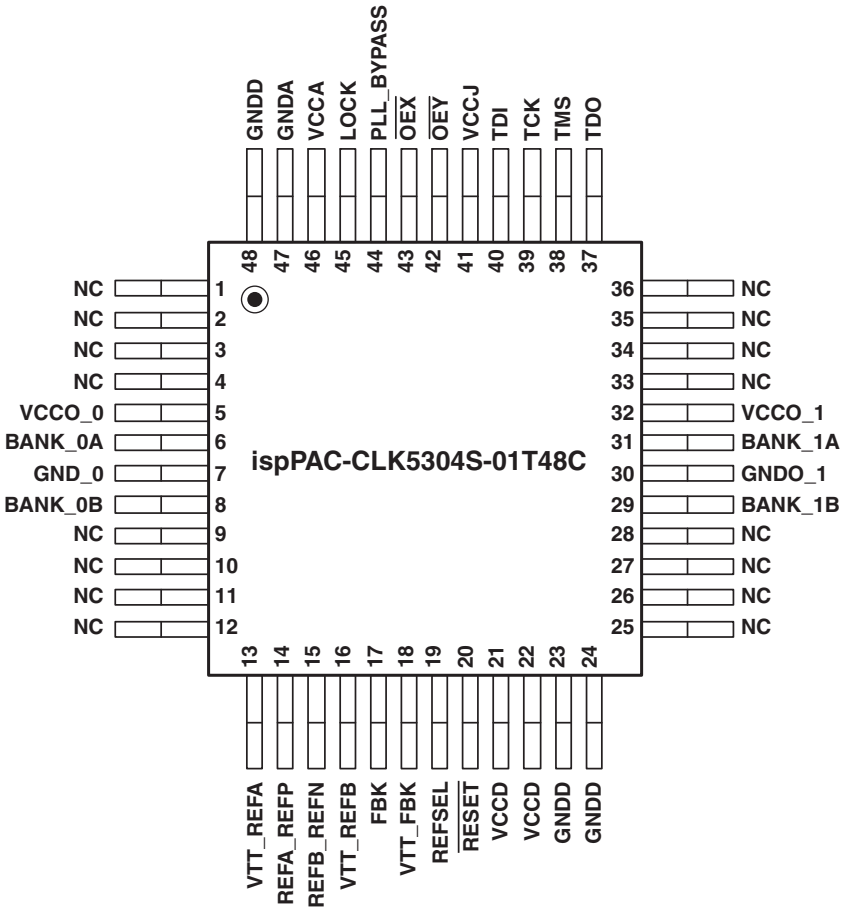
Lead-Free Packaging (Cont.)

Industrial

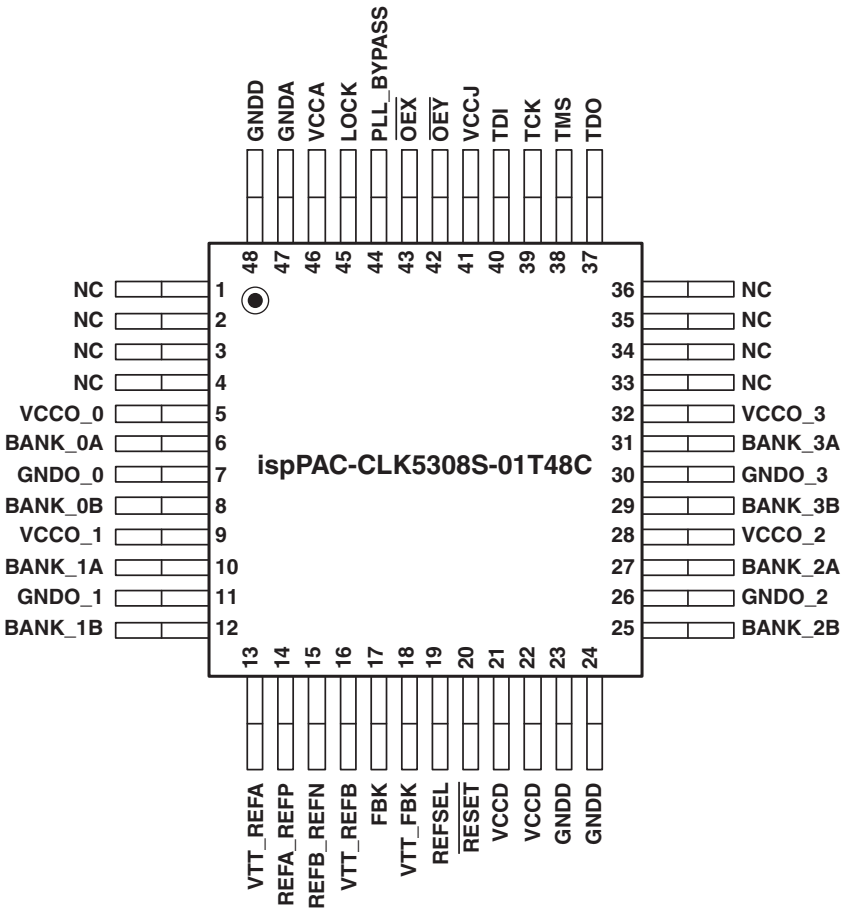
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5320S-01TN64I	20	3.3V	Lead-Free TQFP	64
ispPAC-CLK5316S-01TN64I	16	3.3V	Lead-Free TQFP	64
ispPAC-CLK5312S-01TN48I	12	3.3V	Lead-Free TQFP	48
ispPAC-CLK5308S-01TN48I	8	3.3V	Lead-Free TQFP	48
ispPAC-CLK5304S-01TN48I	4	3.3V	Lead-Free TQFP	48

Package Options

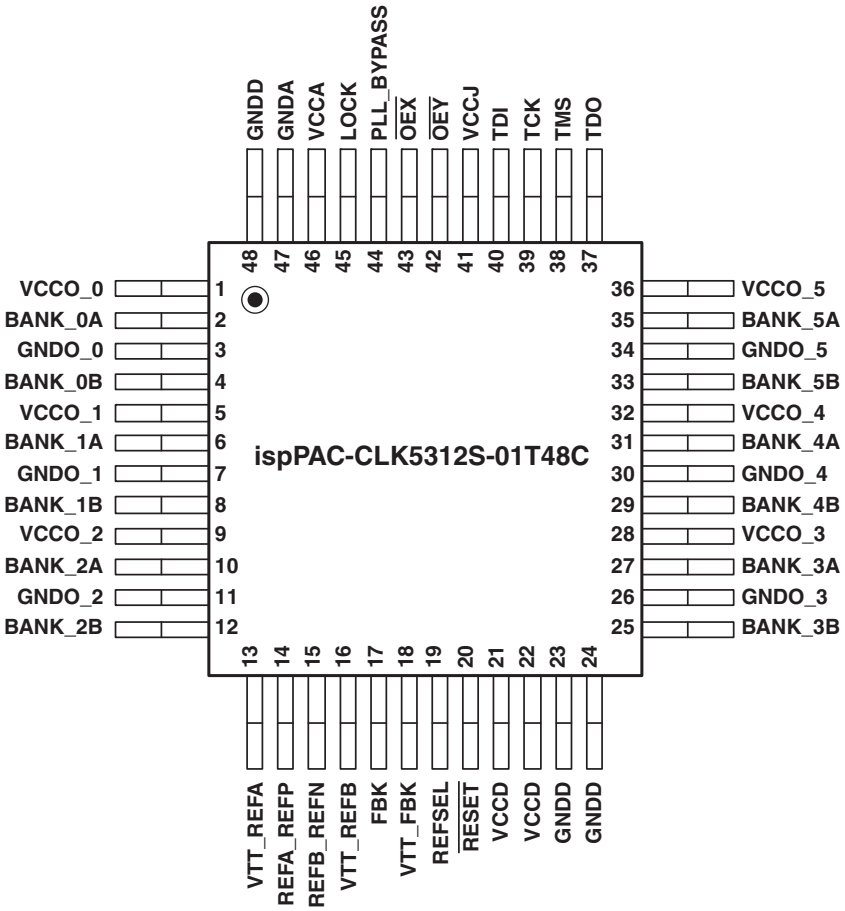
ispClock5304S: 48-pin TQFP



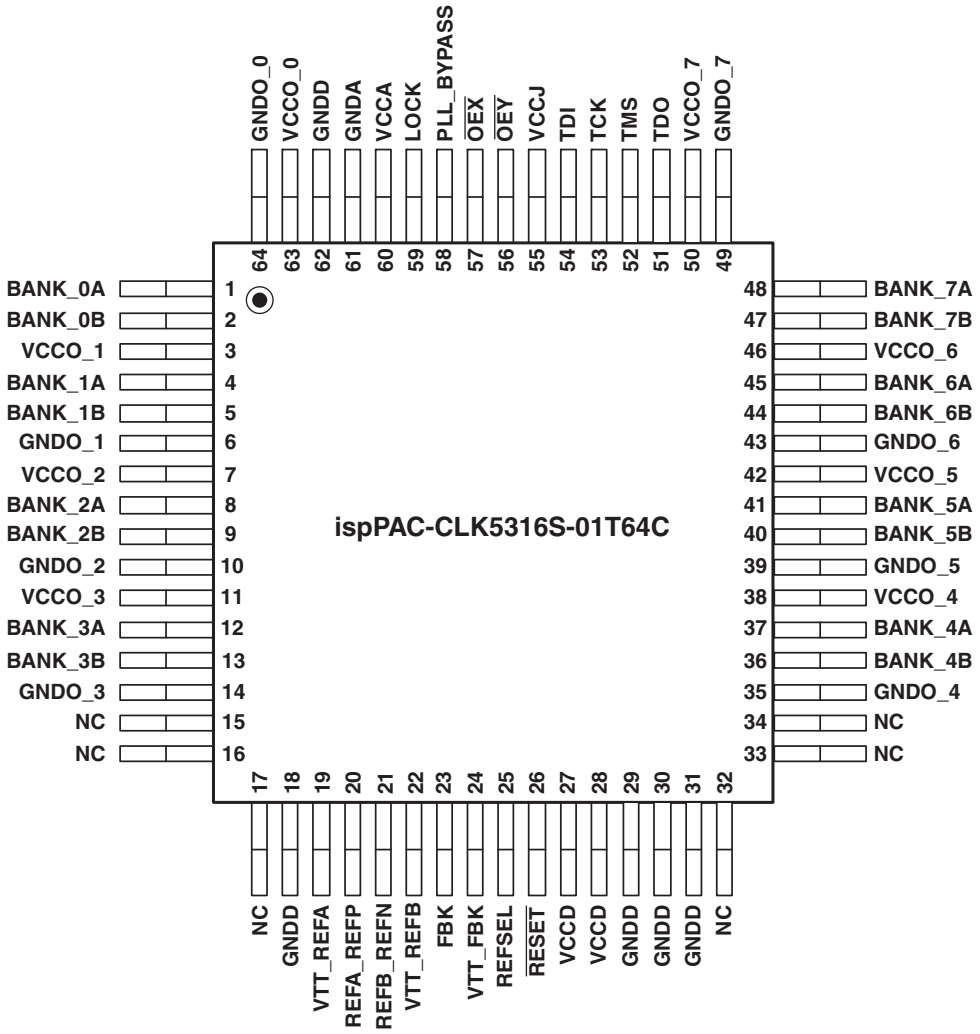
ispClock5308S: 48-pin TQFP



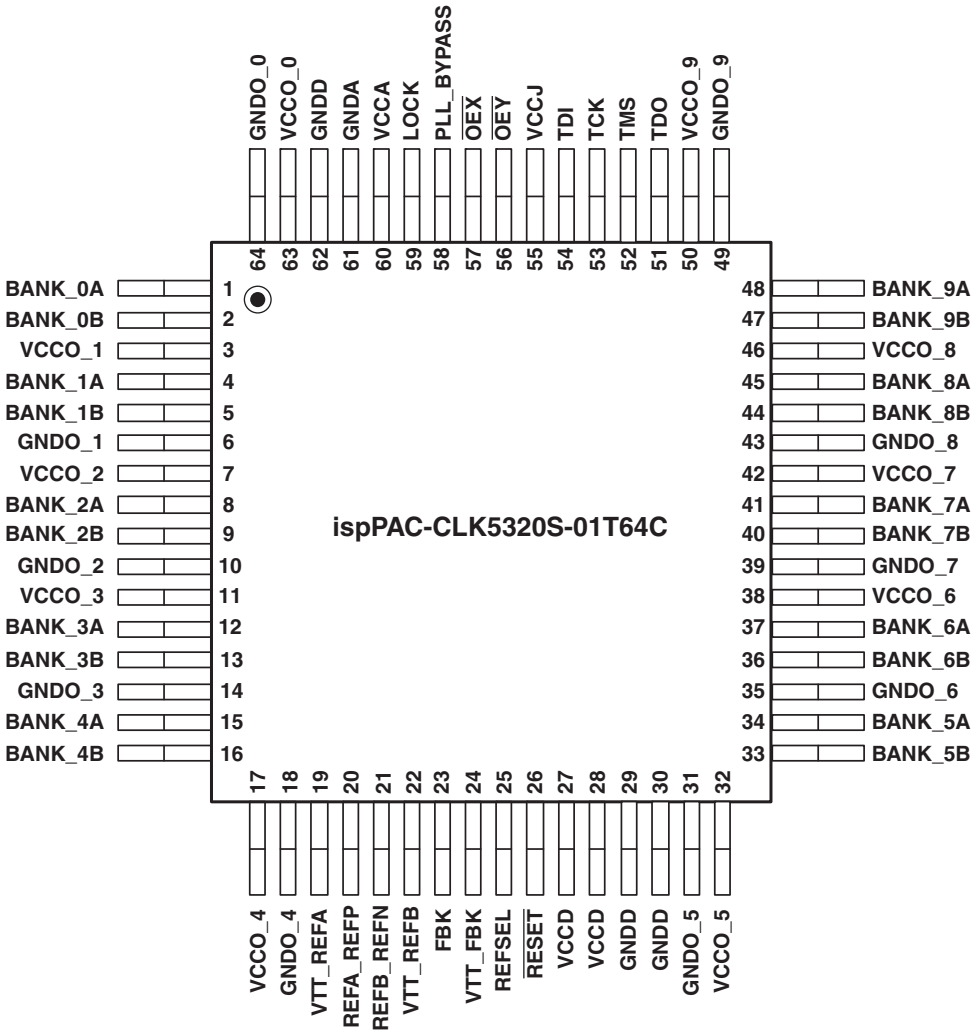
ispClock5312S: 48-pin TQFP



ispClock5316S: 64-pin TQFP



ispClock5320S: 64-pin TQFP



Technical Support Assistance

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e-mail: isppacs@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2006	01.0	Initial release.
May 2006	01.1	Performance Characteristics-PLL table - Correction to min. output frequency, f_{OUT} in Fine Skew Mode. Min frequency = 5MHz.
		Programmable Skew table - Correction to number of skew steps (from 16 to 8).
		Programmable Skew table - Correction to Skew control range.
		Output V Dividers section - Added explanation to V-divider settings as Power of 2 Settings (1, 2, 4, 8, 16, 32).
June 2006	01.2	Added Reset Signal Slew Rate specification to Control Functions table.
		Modified pin descriptions in Pin Descriptions table to reflect changes to pin 48 from NC to GNDD.
		Modified package diagrams to reflect the pin 48 changes from NC to GNDD.
		Modified RESET pin description to include pull-up resistor when not driven.
October 2006	01.3	Included references to ispClock5316S and ispClock5320S devices.
		Added typical performance graphs.
October 2007	01.4	Updated Boundary Scan Register information in ispClock5300S TAP Registers diagram.
		Added support for the Internal Feedback mode of operation.

Section II. ispClock Family Application Notes & User's Guide

Using a Low-Cost CMOS Oscillator as a Reference Clock for SERDES Applications

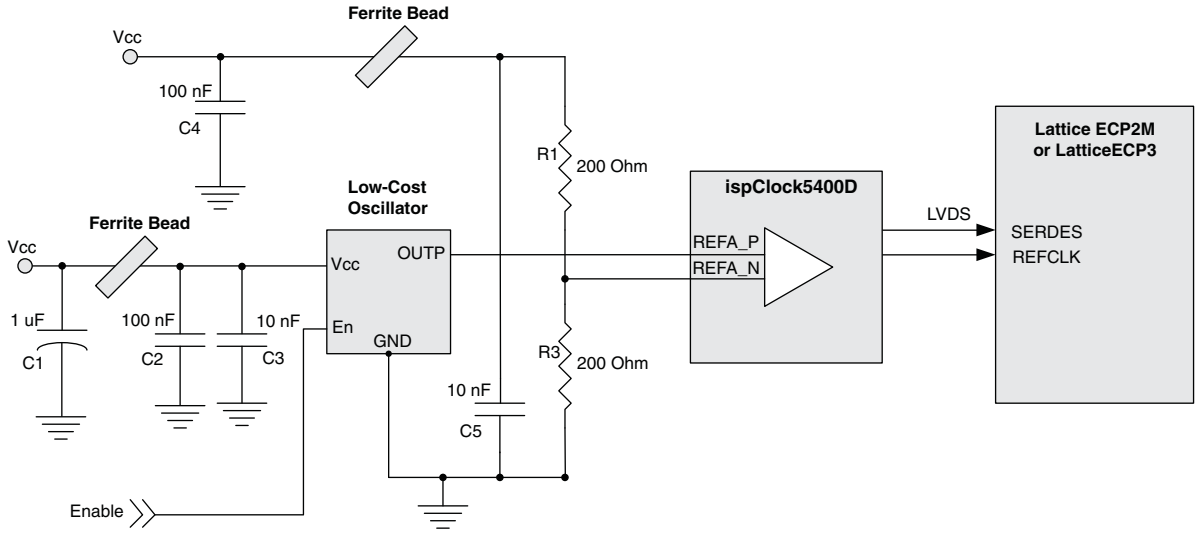
February 2009 **Application Note AN6080**

The Lattice ispClock™5400D family integrates a CleanClock™ PLL and a FlexiClock™ Output block. The CleanClock PLL provides an ultra-low-jitter clock source to a set of four V-dividers. The FlexiClock output block receives the clock output from these V-dividers through an output switch matrix and distributes them to the output pin using a programmable logic interface. There are two members in the ispClock5400D family, the ispClock54010D (10-output FlexiClock block) and the ispClock5406D (6-output FlexiClock block). Each of the outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, SSTL, HSTL, MLVDS, HCSL) and output frequency.

Typically, expensive oscillators with LVDS or LVPECL interface are used as a reference clock for FPGA SERDES interface applications. The ispClock5400D device provides ultra-low-jitter differential clock outputs that can be used to drive both the general purpose clocks and the SERDES reference clocks for FPGAs. The inputs of the ispClock can also be connected to a low cost CMOS oscillator. This application note will show how to interface a low-cost CMOS interface oscillator to the ispClock5400D and present some of its design considerations.

The FPGA SERDES reference clocks usually require lower jitter than many low-cost oscillator sources can provide. In order to keep the jitter output of the ispClock5400D device low, it is important to use good design practices when interfacing with a low cost oscillator with CMOS interface. Figure 4-1 shows an example circuit for interfacing a low cost CMOS interface oscillator to the ispClock5400D device.

Figure 4-1. Interfacing a Low-Cost CMOS Interface Oscillator to the FPGA SERDES Reference Clock



When designing the board for this system there are some important considerations to take into account.

1. The oscillator and ispClock5400D devices should be mounted close to each other to reduce the possibility of picking up noise on the system which will show up as jitter on the input to the ispClock5400D device.
2. The ground signal on the voltage divider circuit should be connected to the ground of the oscillator and located physically close to both devices. This circuit is used to insure that any noise that is picked up will show up as common mode noise and hence not add to the signal amplitude which would appear as jitter to the ispClock5400D.

3. Bypass capacitors should be used on the voltage divider circuit to provide additional noise rejection capability.

4. The use of a ferrite bead inductor is recommended on the power supply to the oscillator and also the voltage divider circuit as shown in Figure 4-1.

Technical Support Assistance

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Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
February 2009	01.0	Initial release.

ispClock5620A Evaluation Board: ispPAC-CLK5620A-EV1

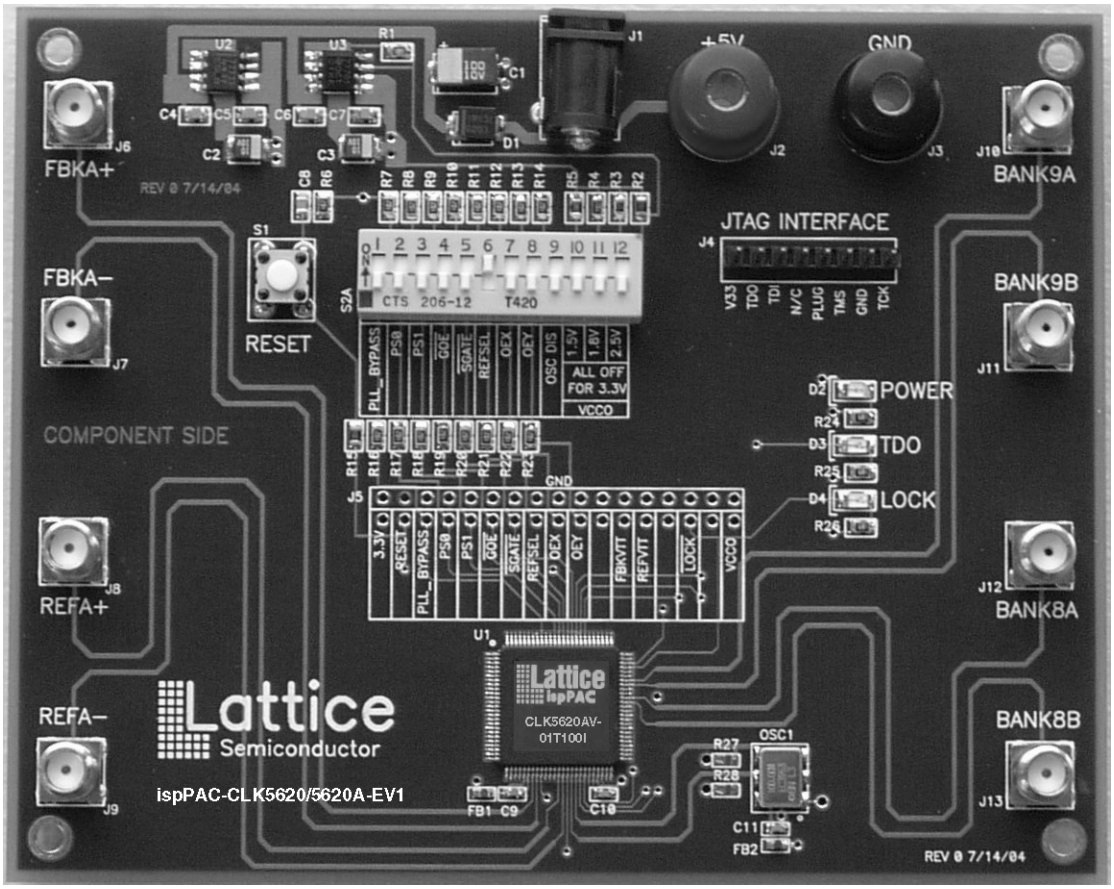
March 2007 Application Note AN6072

Introduction

The Lattice Semiconductor ispClock™5620A In-System-Programmable Analog Circuit allows designers to implement clock distribution networks supporting multiple, synchronized output frequencies using a single integrated circuit.

By integrating a Phase-Locked Loop (PLL) along with multiple output dividers, the ispClock5620A can derive up to five separate output frequencies from a single input reference frequency. To facilitate the implementation of wide-fanout clock trees, the ispClock5620A provides up to 20 single-ended outputs or 10 differential outputs, organized as ten banks of two. Each output bank may be independently programmed to support different logic standards and operating options. Additionally, each single-ended output or differential output may be skew-adjusted to compensate for the effects of propagation delay along the PCB traces used in the distribution network. All configuration data is stored internally in E^{2}CMOS® non-volatile memory. Programming a configuration is accomplished through an industry-standard JTAG IEEE 1149.1 interface.

Figure 5-1. ispPAC-CLK5620A-EV1 Evaluation Board



ispPAC-CLK5620A-EV1 Evaluation Board

The ispPAC-CLK5620A-EV1 evaluation board (Figure 5-1) allows the designer to quickly configure and evaluate the ispClock5620A on a fully assembled printed-circuit board. The four-layer board supports a 100-pin TQFP pack-

age, a header for user I/O and a JTAG programming cable connector. SMA connectors are installed to provide high-signal integrity access to selected high-speed I/O signals. JTAG programming signals can be generated by using an ispDOWNLOAD® programming cable connected between the evaluation board and a PC's parallel (printer) port. All user-programmable features of the ispPAC-CLK5620A can be easily configured using Lattice Semiconductor's PAC-Designer® software.

Programming Interface

Lattice Semiconductor's ispDOWNLOAD cable can be used to program the ispClock5620A which is provided on the evaluation board. This cable plugs into a PC-compatible's parallel port connector, and includes active buffer circuitry inside its DB-25 connector housing. The other end of the ispDOWNLOAD cable terminates in an 8-pin 0.100" pitch header connector which plugs directly into a mating connector provided on the ispPAC-CLK5620A-EV1 evaluation board.

Power Supply Considerations

The ispClock5620A operates with analog and digital core power supplies of 3.3V, while each output driver has a dedicated power supply pin which may be driven with supply voltage of 1.5V, 1.8V, 2.5V or 3.3V, depending on the logic standard which it has been configured to drive.

To simplify evaluation work, the ispPAC-CLK5620A-EV1 board was designed to operate from a single 4.5V-5.5V power supply, which may be brought in through either a pair of banana plugs (J2 and J3), or a standard 5mm power plug (J1 - center tip positive). The evaluation board provides two linear regulators to provide the appropriate operating voltages for the ispClock5620A. One of these regulators provides a fixed 3.3V for the analog and core functions, while the other regulator is dipswitch-programmable to provide 1.5V, 1.8V, 2.5V and 3.3V to power the BANK8 and BANK9 output drivers.

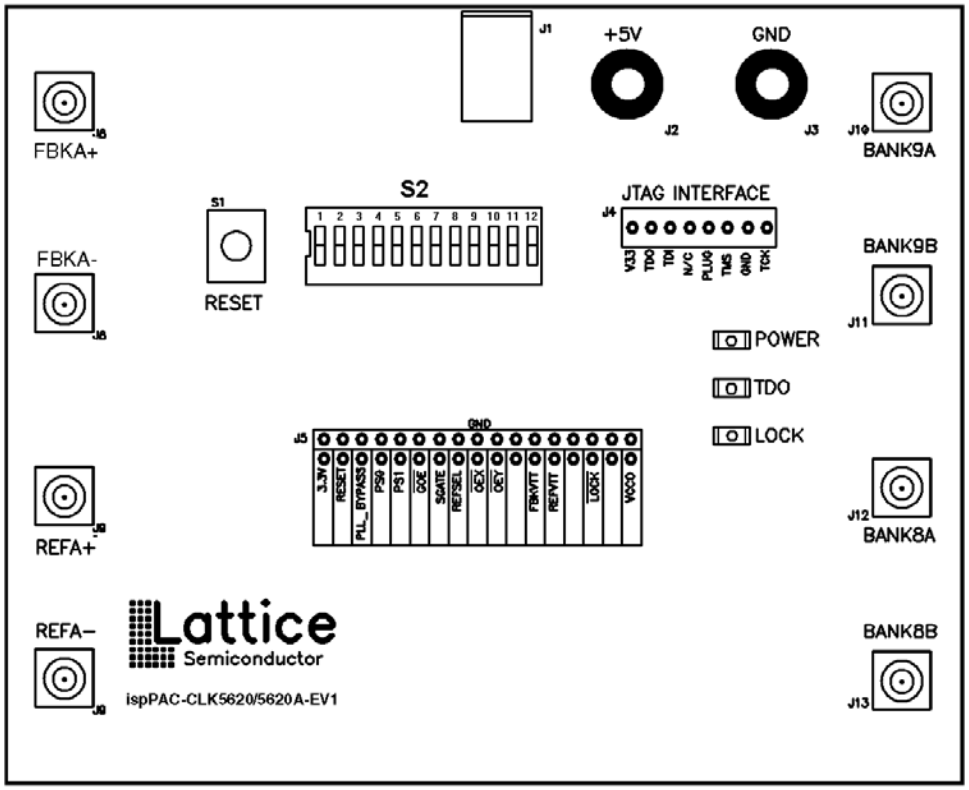
Input/Output Connections

Connectors are provided for key functions and test points on this evaluation board, as shown In Figure 5-2. Power may be supplied in one of two ways; either through two color coded (RED = +, BLACK = -) banana jacks in the upper right corner of the board or through a 5mm (center pin +) DC power connector (J1), The JTAG programming cable is connected to a keyed header (J4) in the upper right corner of the board.

Access to a subset of the ispClock5620A's I/O pins is available at J5, which is a 2x17 row of pads to which one may attach test probes or a ribbon-cable connector. At this point most of the device's non-RF control pins (except those required for the JTAG programming interface) are accessible.

SMA connectors are provided along the left and right edges of the board to support access to key high-speed I/O pins. Pairs of connectors are provided for the BANK8 and BANK9 outputs (J10-J13). Additional pairs of connectors are provided for REFA(+/-) clock reference inputs (J8, J9) and FBKA (+, -) external feedback inputs (J6, J7). On this evaluation board design the REFB(+/-) clock inputs are dedicated to supporting an on-board crystal oscillator. Because this board was designed to maintain high levels of signal integrity at the edge rates at which the ispClock5620A operates, it is strongly suggested that the user do not attempt to access any of the device's high-speed I/O except through the provided SMA connectors and supporting impedance-controlled printed-circuit traces.

Figure 5-2. I/O Connections, Controls and Indicators



Controls and Indicators

A 12-position dipswitch (S2) is provided on the evaluation board (Figure 5-2) for the purpose of setting device inputs and programming the VCCO power supply for the BANK8 and BANK9 outputs. The following table shows the options controlled by each switch:

Table 5-1. User Configuration Functions

Position	Function (when ON)
1	PLL_BYPASS
2	PS0
3	PS1
4	$\overline{\text{GOE}}$
5	SGATE
6	REFSEL
7	$\overline{\text{OEX}}$
8	$\overline{\text{OEY}}$
9	OSC DIS
10	BANK8 and BANK9 VCCO Programming
11	
12	

Each of the switch positions used to control logic inputs (positions 1-8) pulls its respective control signal HIGH when it is turned on. Each of these switch outputs is connected to the device through a 1K¾ resistor. This feature allows external CMOS logic control signals applied to the J5 header connector to over-ride the on-board switch settlings.

Switch position 9 (OSC DIS) is used to control the evaluation board's on-board clock oscillator. When this switch is set to the OFF position the on-board 100MHz oscillator is active and when it is the ON position it is disabled. Disabling the on-board oscillator is desirable when an external clock source is used as an input reference signal because doing so reduces the jitter measured at the board's output. Note that if the on-board source is selected (REFSEL switch = ON) the on-board clock must not be disabled.

Switch positions 10-12 are used to program the VCCO supply for output banks 8 and 9. When all of these switches are OFF, the default supply VCCO supply is 3.3V. The following table shows the switch configurations needed to develop standard supply voltages:

Table 5-2. VCCO Programming Switch (S2) Configurations

S2 Switch Position			
10	**11**	**12**	**VCCO**
OFF	OFF	OFF	3.3V
ON	OFF	OFF	1.5V
OFF	ON	OFF	1.8V
OFF	OFF	ON	2.5V

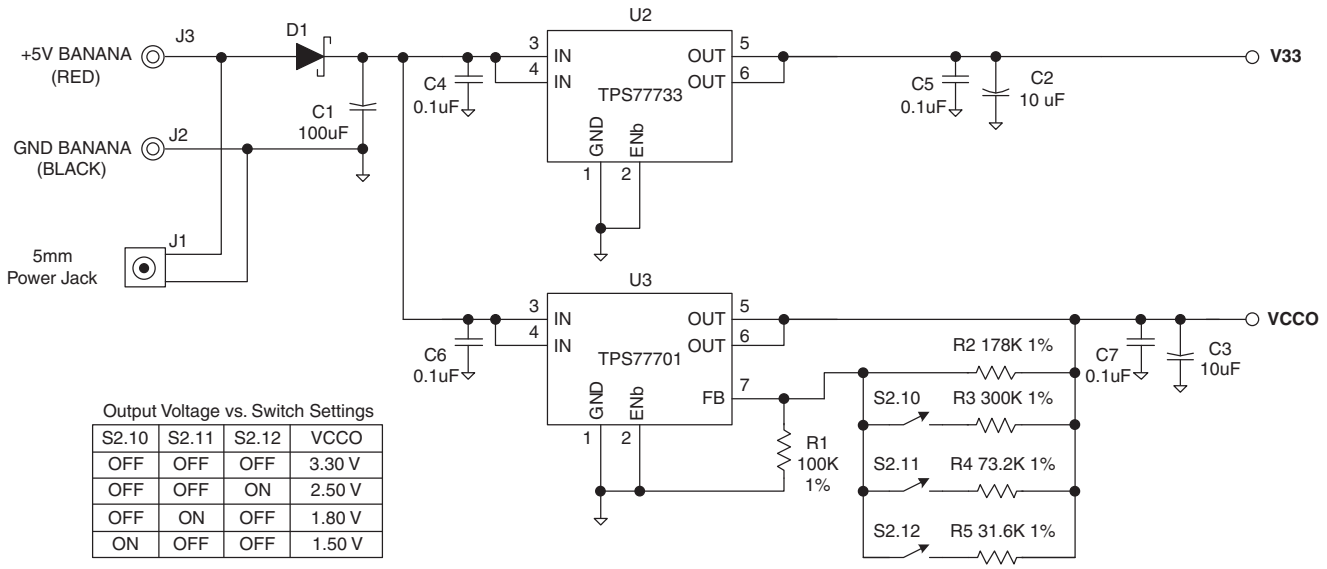
A reset switch (S1) is provided on the evaluation board which pulls the RESET input pin HIGH when it is depressed, re-initializing the ispClock5620A. After changing profiles or reprogramming the ispClock5620A it is necessary to reset the device to obtain a stable clock output.

Several LEDs are also provided on the evaluation board to indicate proper function and as aids to debugging. LED D2 (red) indicates that the on-board 3.3V supply is powered up. LED D3 (yellow) is connected to the ispClock5620A's TDO line, and will briefly flash when downloading, indicating that download data has made it to the device. Finally, when LED D4 (green) is lit, this indicates that the ispClock5620A's PLL is in a 'locked' state.

Schematics

The following three figures comprise the schematics for the ispPAC-CLK5620A-EV1 evaluation board. Figure 5-3 shows the on-board power-conditioning circuitry, Figure 5-4 shows the high-speed interconnects and on-board oscillator circuitry, while Figure 5-5 shows all the logic control signals and indicators.

Figure 5-3. On-Board Power Supplies



Output Voltage vs. Switch Settings

S2.10	S2.11	S2.12	VCCO
OFF	OFF	OFF	3.30 V
OFF	OFF	ON	2.50 V
OFF	ON	OFF	1.80 V
ON	OFF	OFF	1.50 V

Figure 5-4. Oscillator and High-Speed I/O

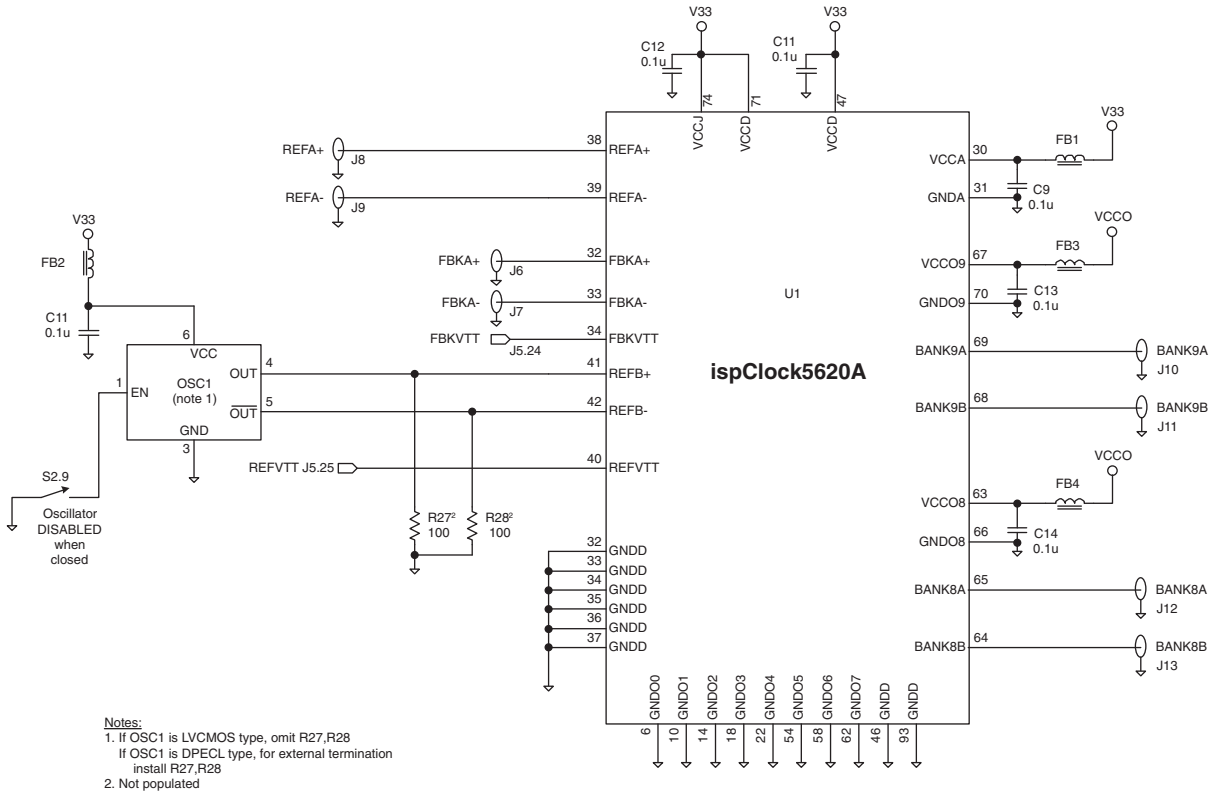
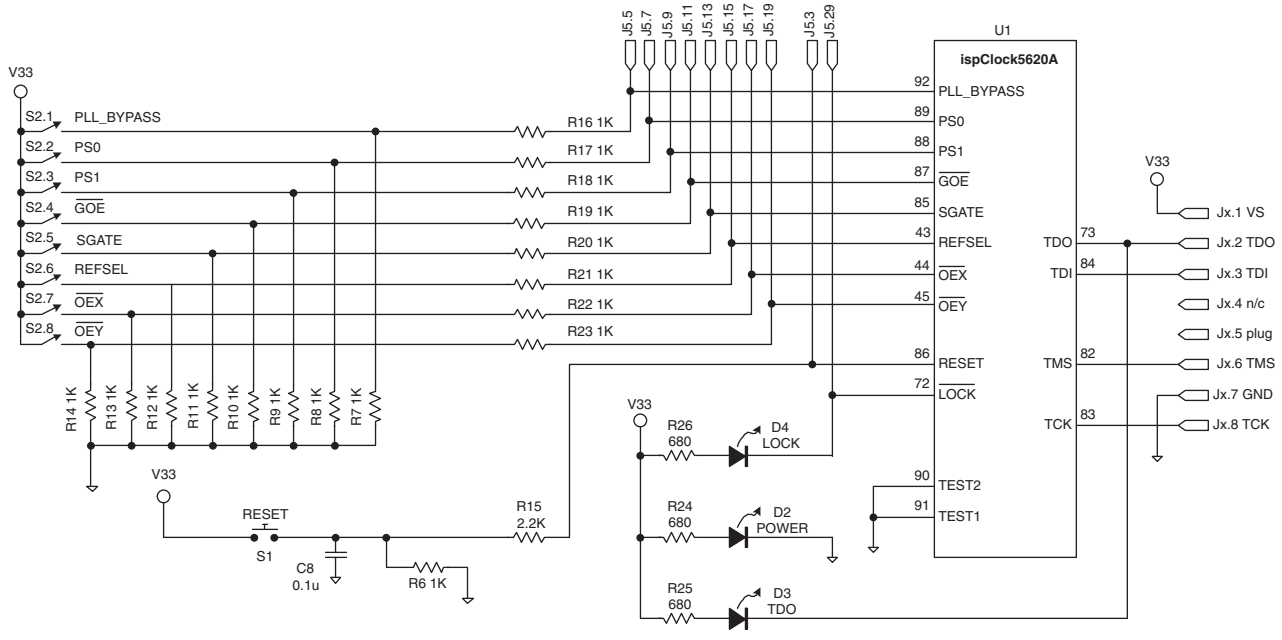


Figure 5-5. User Controls and Miscellaneous I/O



PCB Artwork

Figure 5-6. Silk Screen

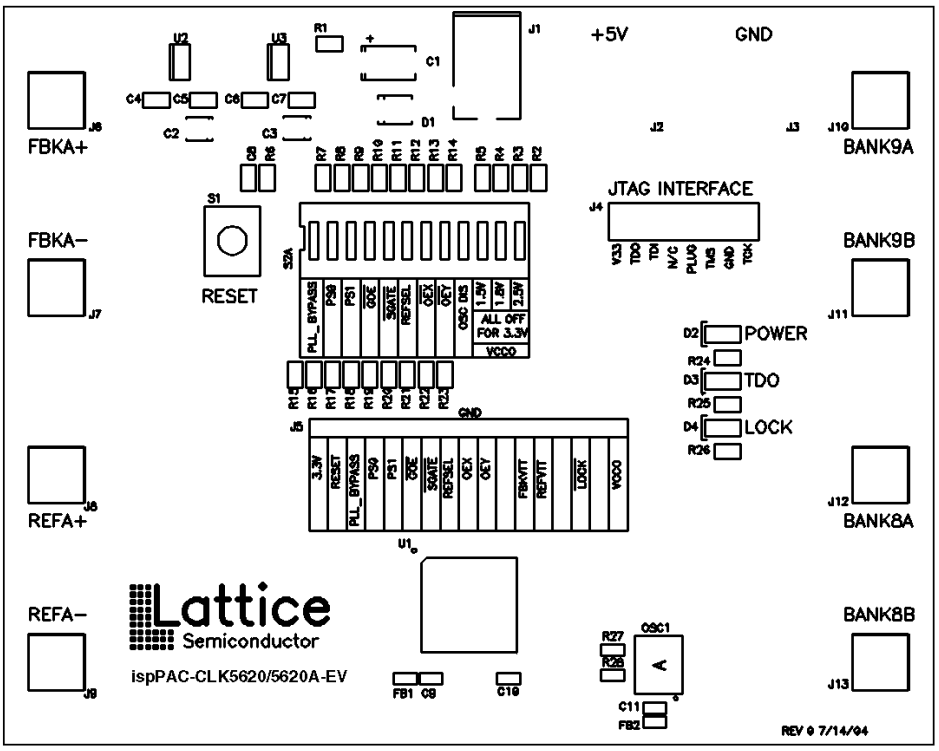


Figure 5-7. Component Side Copper (Layer 1)

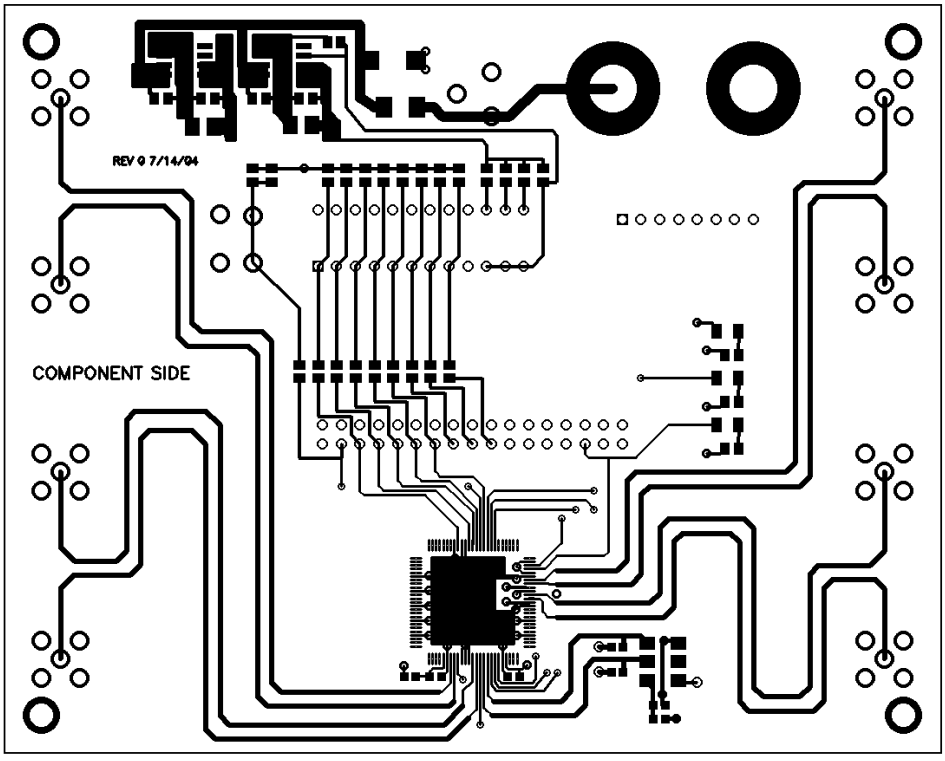


Figure 5-8. Ground Plane (Layer 2)

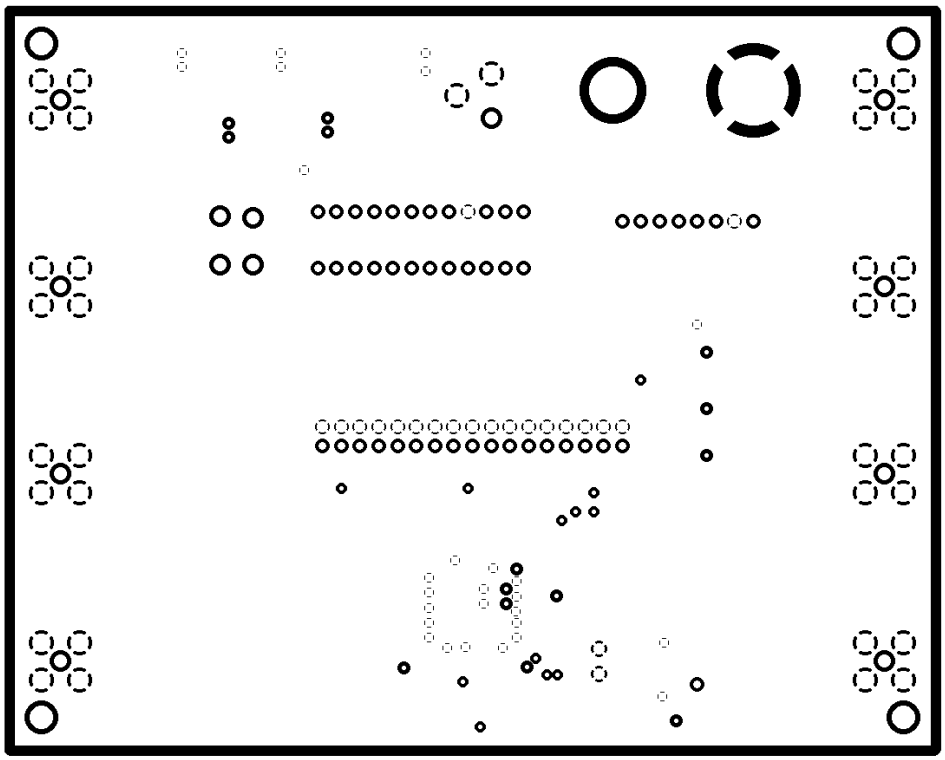


Figure 5-9. Power Plane (Layer 3)

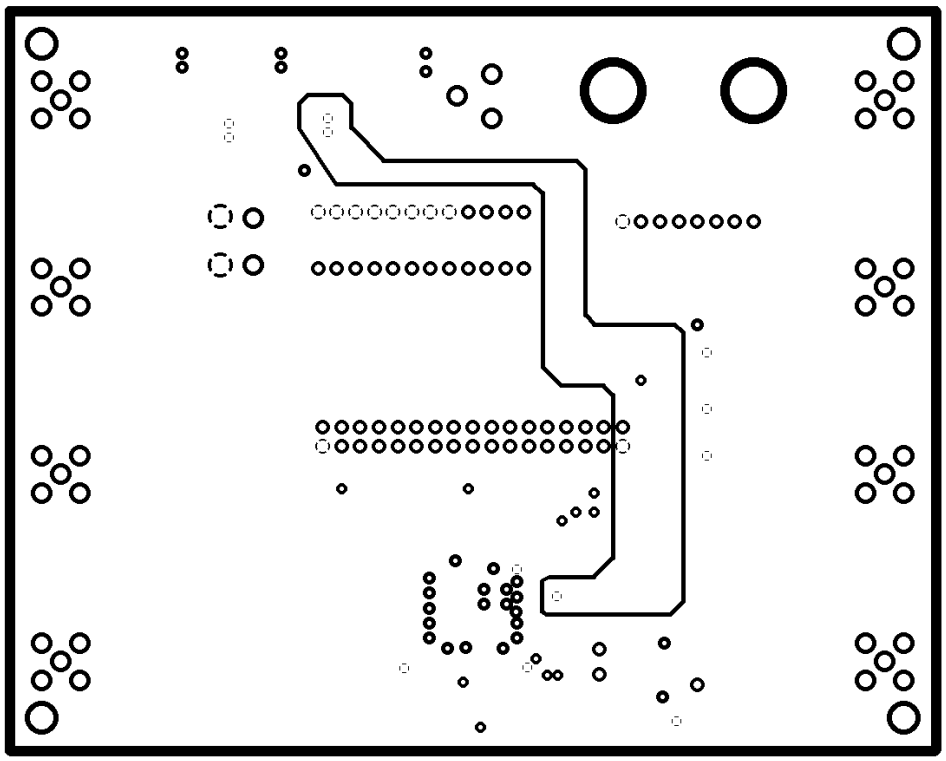
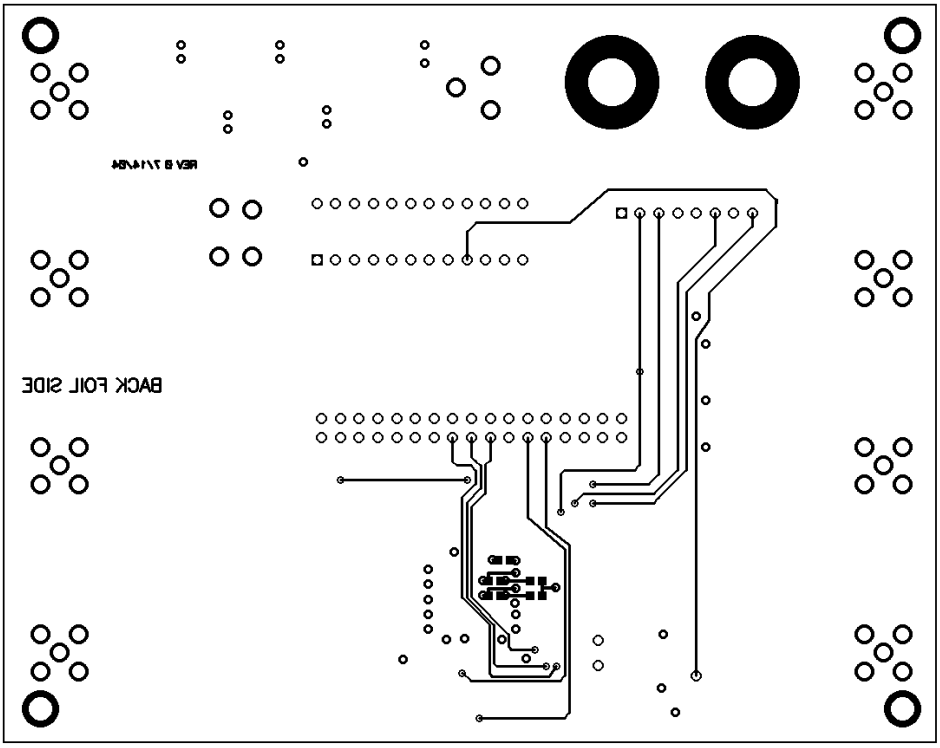


Figure 5-10. Solder-side Copper (Layer 4)



Component List

Quantity	Reference Designators	Description
1	n/a	ispPAC-CLK5620A-EV1 Printed Wiring Board
1	C1	100µF 10V tantalum capacitor, Panasonic ECS-T1AD107R
2	C2, C3	10µF 10V tantalum capacitor, Panasonic ECS-T1AX106R
5	C4, C5, C6, C7, C8	0.1µF 16V capacitor SMD0805, Panasonic ECJ-2VB1C104K
6	C9, C10, C11, C12, C13, C14	0.1µF 16V capacitor SMD0603, Panasonic ECJ-1VB1C104K
1	D1	Schottky rectifier, International Rectifier MRBS130LTR
1	D2	Red LED SMD1206, LiteOn LTST-C150KRKT
1	D3	Yellow LED SMD1206, LiteOn LTST-C150KYKT
1	D4	Green LED SMD1206, LiteOn LTST-C150KGKT
4	FB1, FB2, FB3, FB4	SMD0603 Ferrite Bead, Steward MI0603J600R-00
1	J1	DC Power Connector, CUI PJ-102BH
1	J2	Banana Jack Red, SPC Technologies 845-R
1	J3	Banana Jack Black, SPC Technologies 845-B
1	J4	8-Position Single-Row Header, Molex 22-28-4084
1	J5	34-position Dual Row Header (Not Populated), Molex 10-88-1341
8	J6, J7, J8, J9, J10, J11, J12, J13	SMA Connector, Amphenol 901-144-8RFX
1	R1	100k 1% SMD0805 Resistor, Yageo 9C08052A1003FKHFT
1	R2	178k 1% SMD0805 Resistor, Yageo 9C08052A1783FKHFT
1	R3	300k 1% SMD0805 Resistor, Yageo 9C08052A3003FKHFT
1	R4	73.2k 1% SMD0805 Resistor, Yageo 9C08052A7322FKHFT
1	R5	31.6k 1% SMD0805 Resistor, Yageo 9C08052A3162FKHFT
18	R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23	1K 5% SMD0805 Resistor, Yageo 9C08052A1001JLHFT
3	R24, R25, R26	680¾ 5% SMD0805 Resistor, Yageo 9C08052A6800JLHFT
2	R27[1], R28[1]	100¾ 1% SMD0603 Resistor, Panasonic ERJ-3EKF1000V
1	S1	Momentary Tactile Switch, Panasonic EVQPAD04M
1	S2	12-position dipswitch, CTS 206-12ST
1	U1	ispClock5620A (ispPAC-CLK5620AV-01T100I)
1	U2	3.3V fixed regulator SOIC8, Texas Instruments TPS77733D
1	U3	Adjustable regulator SOIC8, Texas Instruments TPS77701D
1	X1	100MHz LVCMOS Oscillator, ECS-3953M-1000-B
4	n/a	Rubber Feet, 3M SJ-5003

1. Install only for use with differential PECL oscillator.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ispClock5620A evaluation board with ispPAC-CLK5620VA-01T100I device and ispDOWNLOAD® Cable.	PAC-SYSCLK5620AV	

Revision History

Date	Version	Change Summary
January 2006	01.0	Initial release.
March 2007	01.1	Added Ordering Information section.

Technical Support Assistance

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ispClock5312S Evaluation Board

User's Guide

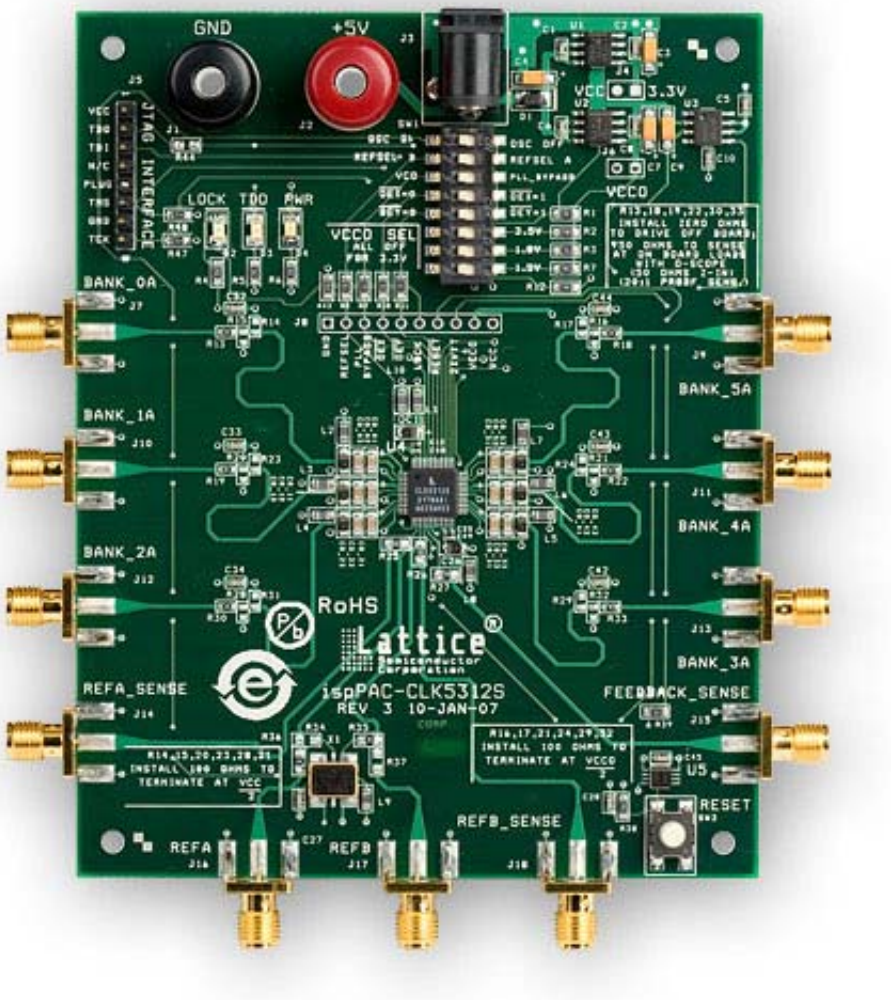
August 2007
Revision: EB32_01.0

Introduction

The family of ispClock™5300S devices from Lattice Semiconductor Corporation provide in-system-programmable zero delay universal fan-out buffers for use in clock distribution applications. Single-ended ultra low skew outputs are organized with two outputs per bank. Each pair of outputs may be independently configured to support separate I/O standards (LVTTL, LVCMOS -3.3V, 2.5V, 1.8, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on chip in non-volatile E^2CMOS® memory.

The ispClock5300S devices provide extremely low propagation delay (zero-delay) from input to output using the on-chip low jitter high-performance phase locked loop (PLL). A set of three programmable 5-bit counters can be used to generate three frequencies derived from the PLL clock. These counters are programmable in powers of 2 only (1, 2, 4, 8, 16, 32). The clock output from any of the V-dividers can then be routed to any clock output pair through the output routing matrix. The output routing matrix also enables routing of reference clock inputs directly to any output. For additional details, please refer to the ispPAC-CLK5300S Family Data Sheet.

Figure 6-1. ispClock5312S Evaluation Board



ispClock5312S Evaluation Board

The ispClock5312S is the first member of the ispClock5300S family with six output banks and thus has 12 single-ended ultra low skew outputs. The ispClock5312S evaluation board features this device with full support circuitry for power, programming, testing, and evaluation. The "A" output for each bank is supported with matched transmission lines, optional on-board termination, and SMA connections at the edge of the board to provide full flexibility in measurement and evaluation. Output 1B is hard-wired to the feedback input to complete the feedback loop of the PLL because, the ispClock5300S family of devices only supports external feedback. Each output bank has separate decoupling to isolate the outputs if they are configured for different frequencies. An on board 100 MHz oscillator with 3.3V CMOS output is connected to the REFB input of the ispClock5312S. The REFA input is connected to an SMA connector for testing with different input frequencies.

For a complete list of the various connections and interfaces used on the ispClock5312S evaluation board, please refer to the schematics in the appendix of this document.

Finally, the ispClock5312S evaluation board is 100% lead free and ROHS compliant as Lattice Semiconductor Corporation is sensitive to environmental issues.

Additional Resources

Additional resources relating to the ispClock5312S Evaluation Board are available on the Lattice web site. Go to: www.latticesemi/boards and navigate to "mixed signal boards" to find the appropriate link. Updates to this document can be found there, as well as sample programs and links to other related items.

PAC-Designer®

PAC-Designer is the software used to develop custom programs for the ispClock5312S device, generate programming files, and manage the download/programming of the device.

PAC-Designer is available for download from the Lattice web site at: www.latticesemi.com/pac-designer.

Programming Interface

JTAG programming is supported with the eight-pin connector J5 and either the USB download cable (HW-USBN-2A) or the parallel download cable (HW-DLN-3C). The Windows-based program PAC-Designer provides an intuitive interface for configuring the ispClock5312S and can be used to either directly program the evaluation board or to export a JEDEC file which can be used with ispVM® to program the evaluation board.

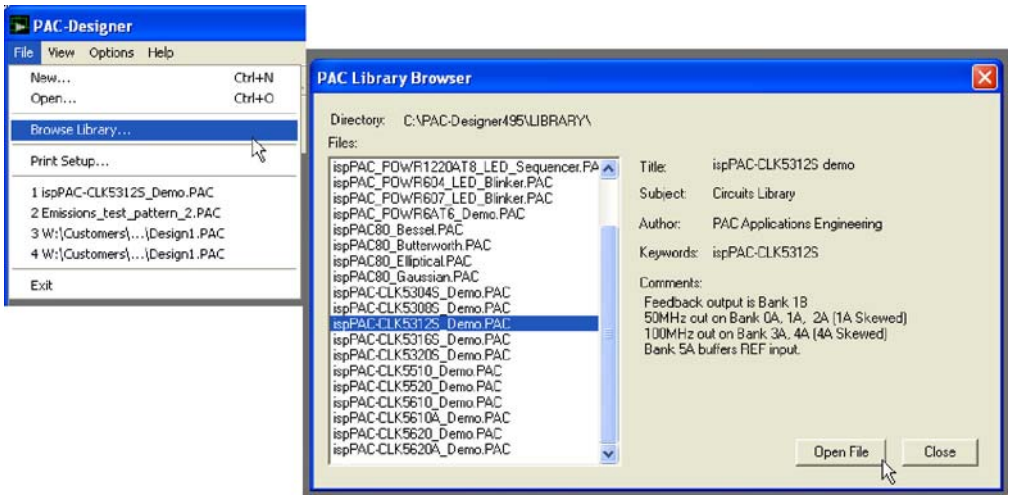
ispVM system is available for download from the Lattice web site at: www.latticesemi.com/ispvm.

Important Note: The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD® Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the ispClock5312S device and render the board inoperable.

Demo Configuration and Reprogramming

The ispClock5312S evaluation board is preprogrammed at the factory with a demonstration configuration. This demonstration configuration can be reprogrammed into the evaluation board from PAC-Designer by browsing the library files as shown in Figure 6-2.

Figure 6-2. Demonstration File in PAC-Designer's Library



Power Supply Considerations

All that is needed to power the ispClock5312S evaluation board is a 5V power supply capable of providing one ampere or more. The board can be powered either by a wall adapter with a 2.5mm coaxial power plug at J3 or from a bench supply with banana plugs at J1 and J2. Once onboard, the five volts is regulated (U1) to provide the 3.3V supply needed for VCCD, VCCA, VCCJ, and VCCO for banks zero, one, and two.

A second adjustable regulator (U2) provides the VCCO for banks three, four, and five and it is programmable using the on-board resistors and three of the DIP-switches of SW1. To bypass the on-board regulators, jumpers J4 and J6 can be cut on the bottom of the board to allow external supplies to power the ispClock5312S.

Input/Output Connections

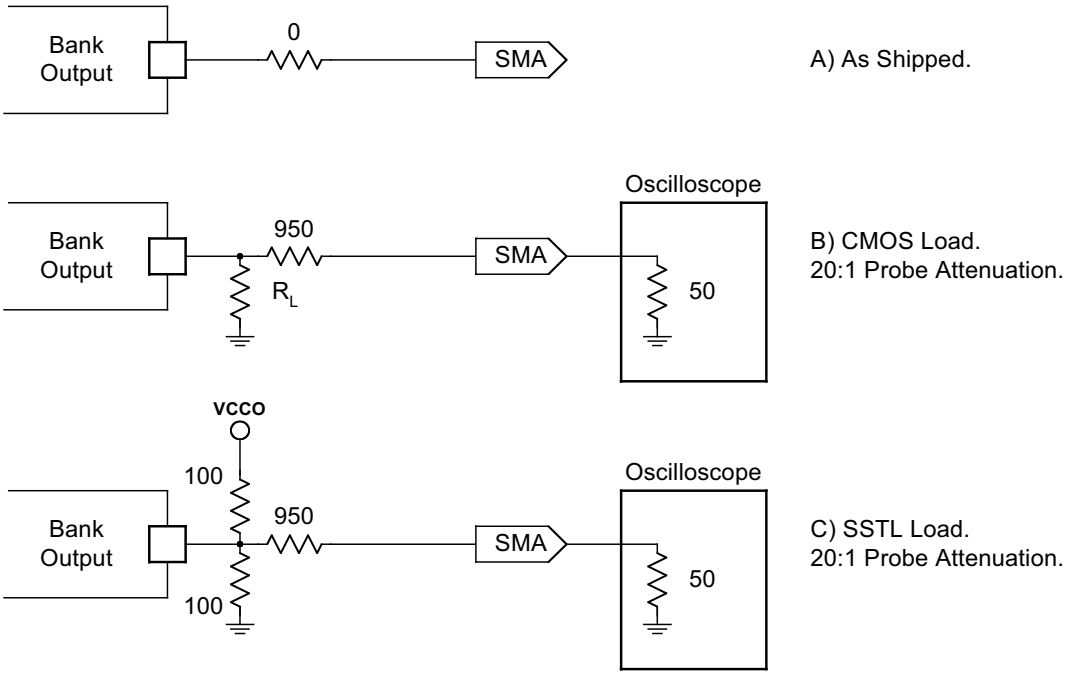
This board incorporates tapered transitions from the SMA connectors to the matched 50-ohms microstrip transmission lines. All of the output transmission lines are matched in length to the sense signals (REFA, REFB, and FEEDBACK) to support accurate timing measurements both for bank-to-bank and input to output. The header at J8 provides access to the essential control and monitor signals of the ispClock5312S such as REFSEL, PLL_BYPASS, OEX, OEY, LOCK, and RESET.

An off-board CMOS clock can be used by connecting to the REFA (J16) SMA connector. The ispClock5312S can also be driven from an external differential clock source by moving the zero-ohm resistor from the R35 location to the R37 location and connecting the clocks to both REFA and REFB inputs (J16 and J17). When an external clock source is used, switches 1 and 2 of DIP-switch SW1 should be in the left position (OSC OFF and REFSEL A).

On-Board Termination

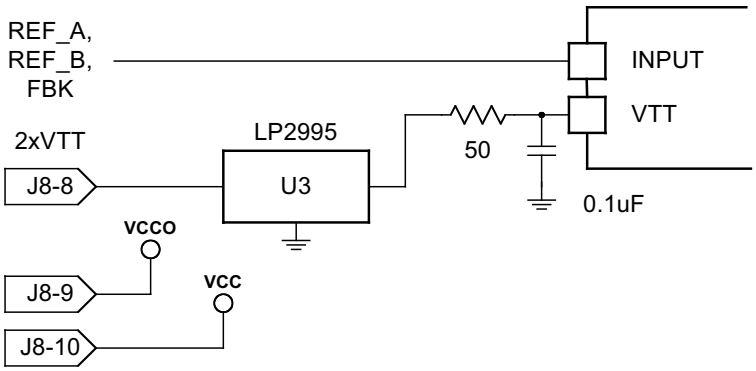
The ispClock5312S evaluation board is equipped with zero-ohm 0603 SMD resistors in series with the six outputs and their corresponding SMA connectors in order to drive an off-board CMOS loads. This is shown in Figure 3-A. However, these resistors can be replaced and additional resistors added to employ a variety of termination networks to match the desired output mode. In Figure 3-B the zero-ohm resistor is replaced with a 950-ohm sense resistor and a load resistor is added to ground. The input impedance of the oscilloscope provides a 20:1 probe attenuation. A small (5pF to 10pF) cap can be added on top of the load resistor to simulate a CMOS input. In Figure 3-C a divider network terminates the transmission line at 1/2 VCCO into a 50-ohm load and the 950-ohm resistor allows sensing by the oscilloscope with a 20:1 probe attenuation. A low value capacitor (5pF to 10pF) can be soldered on top of the 100-ohm resistor to ground to simulate an input to SSTL logic.

Figure 6-3. Onboard Output Termination Options



The ispClock5312S evaluation board also supports input termination for the reference clock inputs and the feedback input if they are configured as SSTL. For CMOS operation (default) nothing needs to be added to the board. For each SSTL input there is a set of pads on the backside of the board for a resistor and capacitor to terminate the input as close to the device as possible. In addition, for SSTL termination pin 8 of the header J8 needs to be connected to either pin 9 or 10 of the same header or connected off board to an adjustable supply to set the termination voltage. Note the voltage applied at pin 8 of J8 will be twice the termination voltage as U3 divides the input voltage in half, see Figure 4 and the schematic in the appendix for more details.

Figure 6-4. Optional Input Termination for SSTL



DIP Switch

To simplify the use of the ispClock5312S evaluation board an 8-position DIP switch (SW1) is provided for the more common adjustments. The switch can roughly be divided into four sections; reference oscillator control, PLL control, output enables, and VCCO control. Table 1 lists the switches and their respective functions. Note that for switch sections 6, 7, and 8 only one should be on at a time. The default setting with all the switches to the left (off) enables the onboard oscillator, selects that as the clock reference, and allows the PLL to lock to that frequency.

Table 6-1. DIP Switch Functions

Off (to the left)	SW1 - Section	ON (to the right)
Oscillator On	1	Oscillator Off
REFSEL = B	2	REFSEL = A
VCO Enabled	3	PLL-Bypass
OEX=0	4	OEX=1
OEY=0	5	OEY=1
VCCO = 3.3V	6	VCCO=2.5V
VCCO = 3.3V	7	VCCO=1.8V
VCCO = 3.3V	8	VCCO=1.5V

Measuring Zero Delay and Bank-to-Bank Skew

The transmission lines for the outputs are matched in length (and thus time) to the sense lines (FEEDBACK, REF_A, and REF_B). Thus, when matched SMA cables are used to connect the outputs to an oscilloscope the rising edges will be aligned as shown in Figure 5. Here the green trace (probe-2) displays the feedback as sensed by the on-board 950-ohm resistor (see the schematic) while the other traces illustrate the synchronization of the outputs. By double clicking the Skew Manager in PAC-Designer (see Figure 6), the skew between outputs is set to about 300ps. The ispClock5312S is then reprogrammed and the resulting measurement is shown in Figure 7. Note the feedback signal has been replaced with an output.

Figure 6-5. Outputs are Synchronized with the Feedback Input

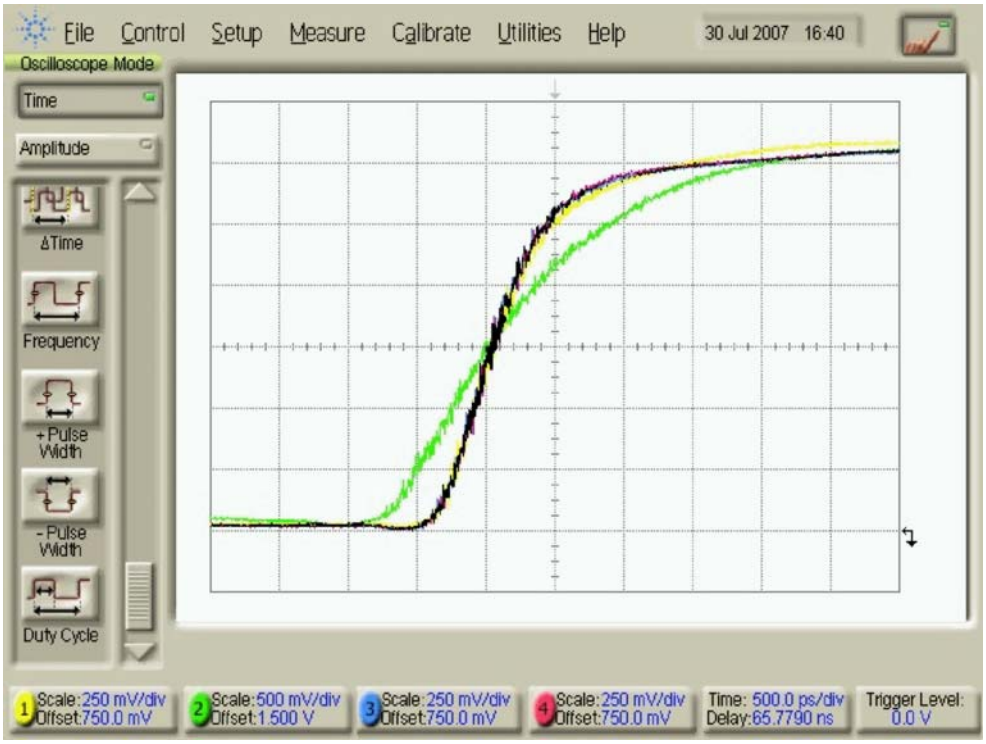


Figure 6-6. PAC-Designer Skew Manager and Settings Dialog

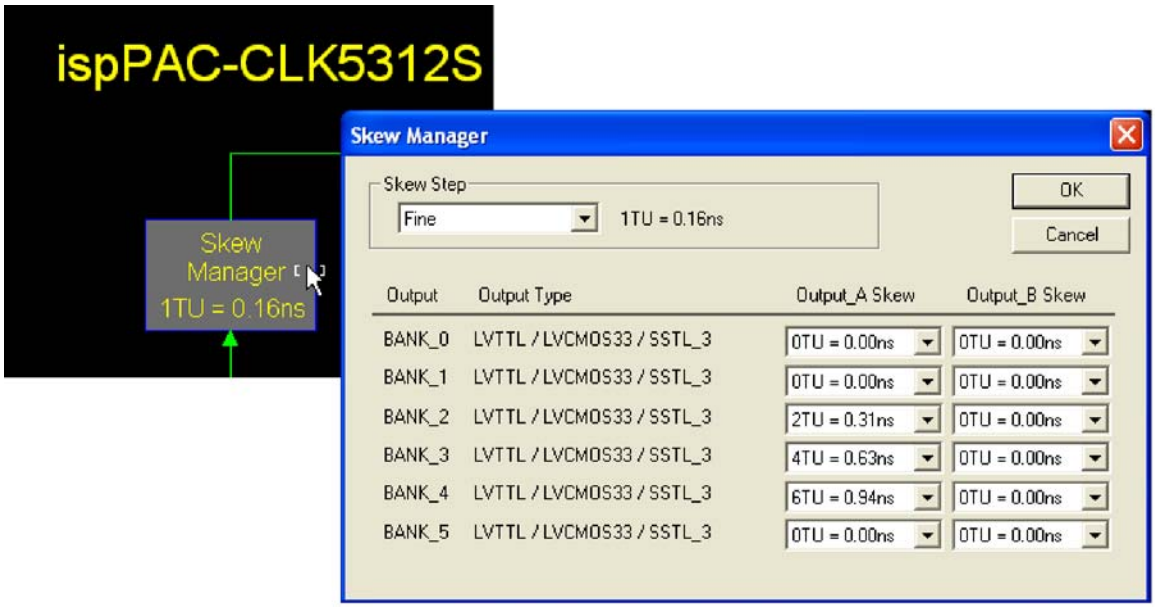
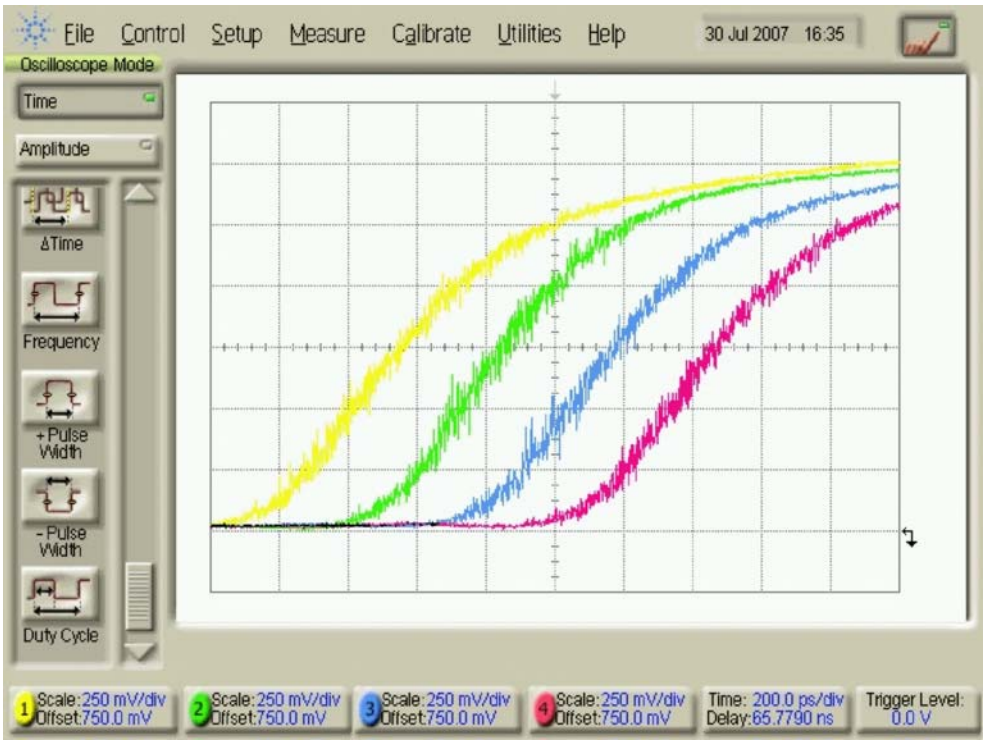


Figure 6-7. Outputs are Skewed 300ps



ispClock5312S Evaluation Board Bill of Materials

Quantity	Ref Des	Description	Manufacturer	Part Number
2	C12, 25	0.1uF SMD 0402 Ceramic Capacitor	Kemet	C0402C104K9PACTU
2	C48, 49	0.01uF SMD 0402 ceramic capacitor	Kemet	C0402C103K4RACTU
15	C1, 2, 5, 6, 8,10, 27, 28, 32, 33, 34, 42, 43, 44, 45	0.1uF SMD 0603 ceramic capacitor	Panasonic	ECJ-1VB1C104K
8	C11,26 CO_03, 13, 23, 33, 43, 53	6.8uF 6.3V SMD 0805 tantalum capacitor	Rohm	TCP0J685M8R
6	CO_01,11, 21, 31, 41, 51	330pF SMD 0805 ceramic capacitor	Kemet	C0805C331K5RACTU
6	CO_02, 12, 22, 32, 42, 52	3.3nF SMD 0805 ceramic capacitor	Kemet	C0805C332K5RACTU
4	C3, 4, 7, 9	10uF 10V SMD tantalum capacitor	AVX Corp.	TPSA106K010R0900
1	D1	Schottky diode SMD	ON Semi	MBR120VLSFT1G
1	D2	Blue LED SMD 1206	LiteOn	LTST-C150TBKT
1	D3	Red LED SMD 1206	LiteOn	LTST-C150KRKT
1	D4	Green LED SMD 1206	LiteOn	LTST-C150KGKT
1	J3	2.5mm DC power connector	CUI Inc.	PJ-102B
1	J2	Red banana jack	SPC Tech.	845-R
1	J1	Black banana jack	SPC Tech.	845-B
1	J5	8-position pin header	Molex	22-28-4084
11	J7,9,10-18	SMA Connector PCB End Launch	Johnson	142-0701-801
10	L1-L10	300 ohm Signal Ferrite SMD 0805	Stewart	LI0805G301R-10
1	X1	100 MHz Clock Source	ECS	ECS-3953M-1000BN
1	R1	178k 5% resistor SMD 0805	Yageo	RC0805FR-07178KL
1	R2	301k 5% resistor SMD 0805	Yageo	RC0805FR-07301KL
1	R3	73.2k 1% resistor SMD 0805	Yageo	RC0805FR-0773K2L
1	R7	31.6k 1% resistor SMD 0805	Yageo	RC0805FR-0731K6L
1	R12	100k 1% resistor SMD 0805	Yageo	RC0805FR-07100KL
3	R25,26,27	953 ohm 1% resistor SMD 0603	Yageo	RC0603FR-07953RL
2	R38, 43	10k 5% resistor SMD 0805	Yageo	RC0805JR-0710KL
8	R4, 5, 6, 8-11, 39	1k 5% resistor SMD 0805	Yageo	RC0805JR-071KL
2	R47,48	4.7k 5% resistor SMD 0805	Yageo	RC0805JR-074K7L
8	R13,18,19, 22, 30, 33, 35, 36	Zero-ohm resistor 5% SMD 0603	Yageo	RC0603JR-070RL
1	SW1	Slide Sw 8POS SMD	ITT Industries	SDA08H1SBD
1	SW2	Momentary Switch SMD	Panasonic	EVQ-QXT03W
1	U1	3.3V fixed regulator SMD 8SOIC	Texas Inst.	TPS77733D
1	U2	Adj LDO Regulator SMD 8SOIC	Texas Inst.	TPS77701D
1	U3	DDR Term Regulator SMD 8SOIC	National Semi.	LP2995M
1	U4	IspPAC-CLK5312S	Lattice	
1	U5	74LVC3G34 Triple Buffer 8-SSOP	Texas Inst.	SN74LVC3G34DCTR

References

- ispPAC-CLK5300S Family Data Sheet

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ispClock5312S Evaluation Board	PACCLK5312S-EVN	

Technical Support Assistance

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e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
August 2007	01.0	Initial release.

Appendix A. Schematic

Figure 6-8. ispClock5312S Inputs, JTAG, Core and PLL

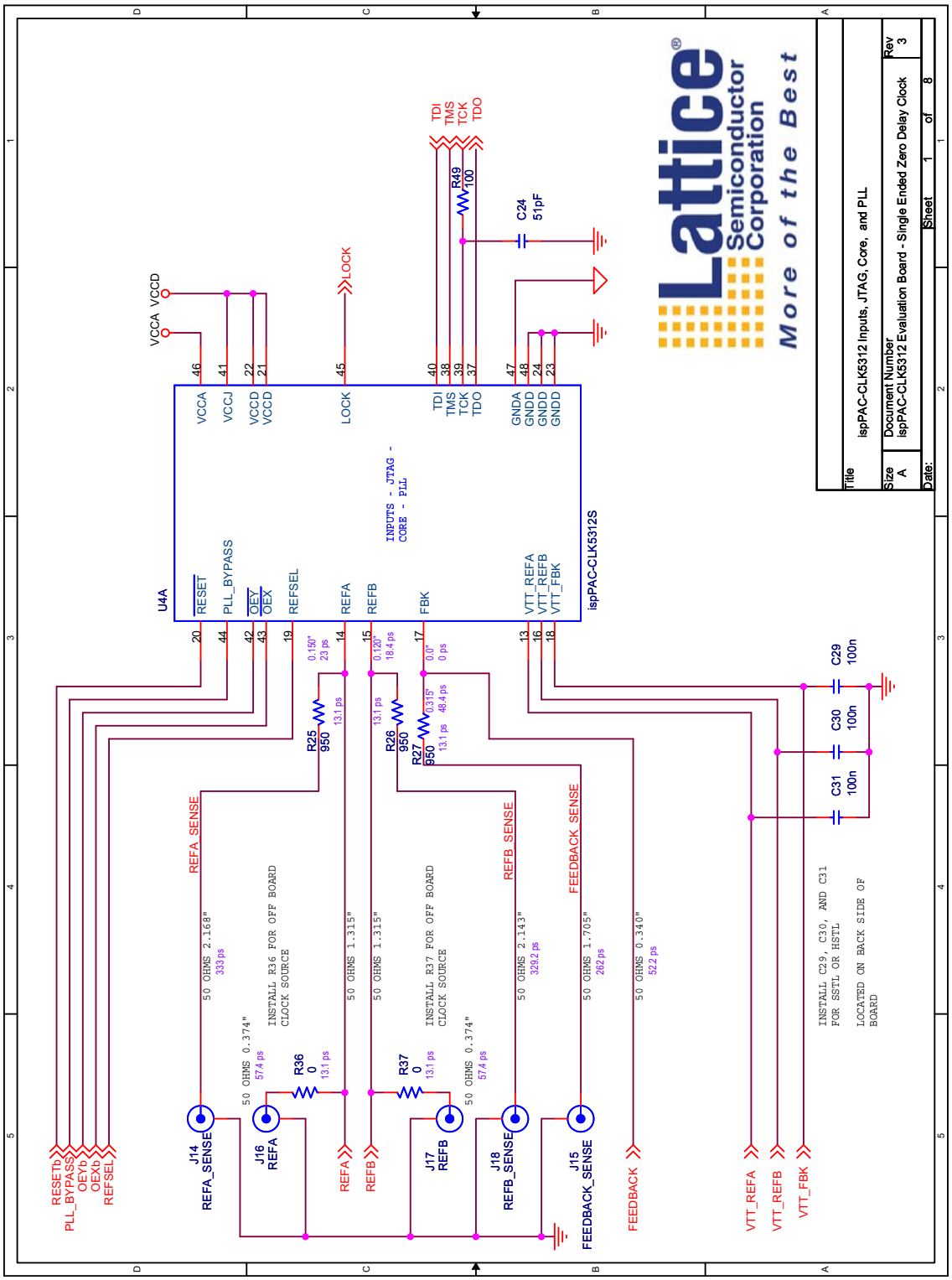


Figure 6-9. ispClock5312S Output Banks 0, 1 and 2

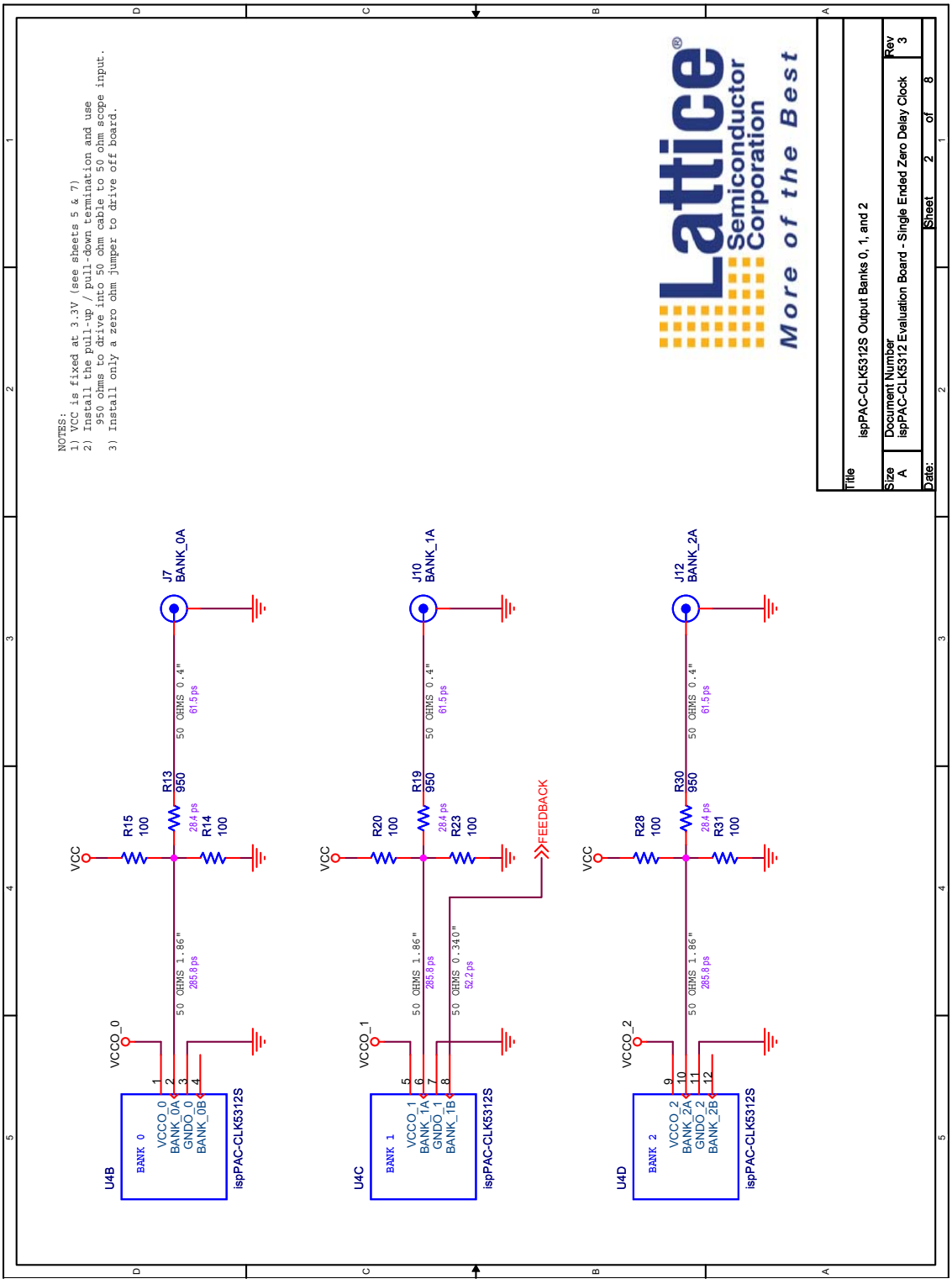


Figure 6-10. ispClock5312S Output Banks 3, 4 and 5

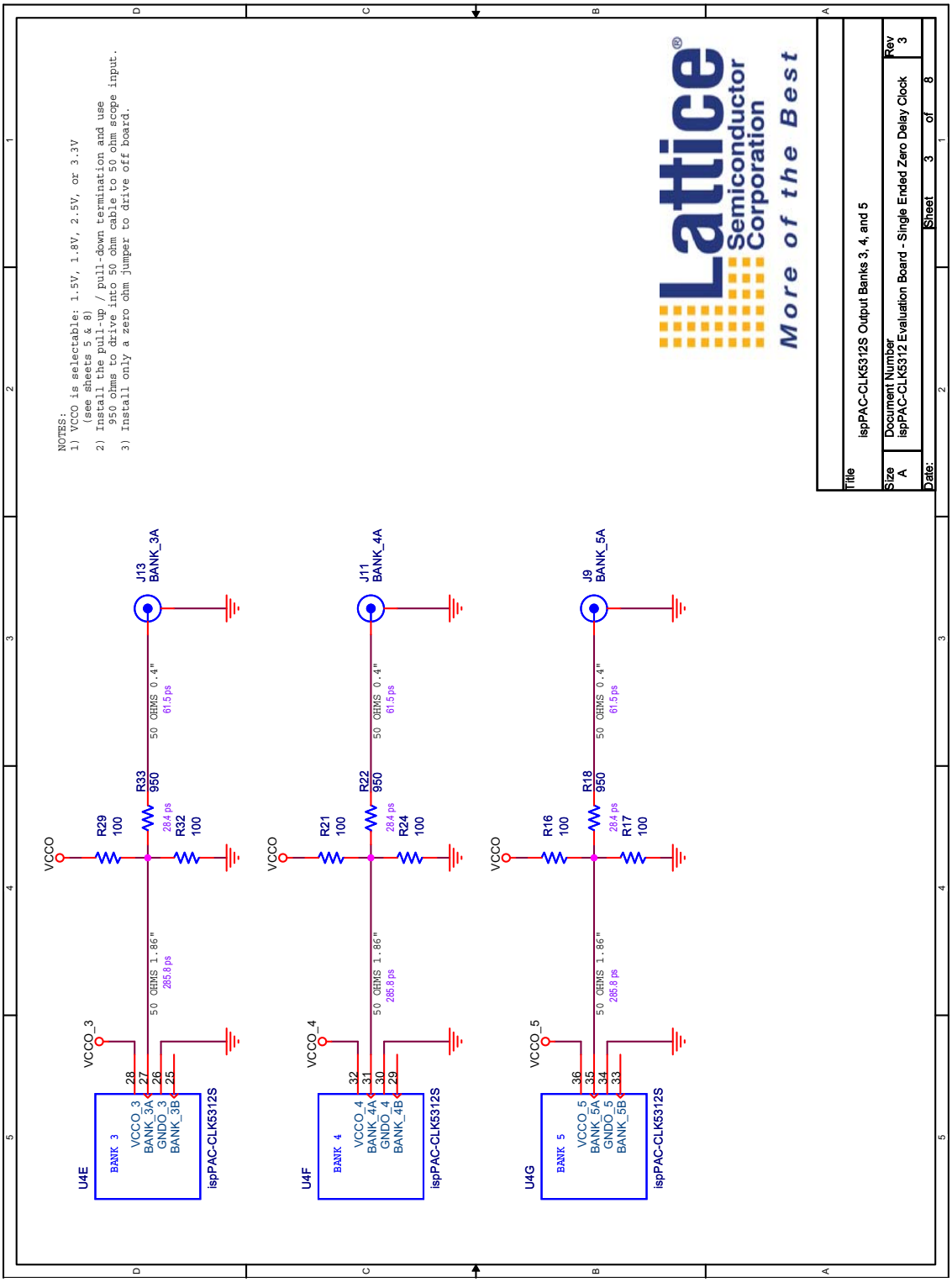


Figure 6-11. Connectors and Oscillator

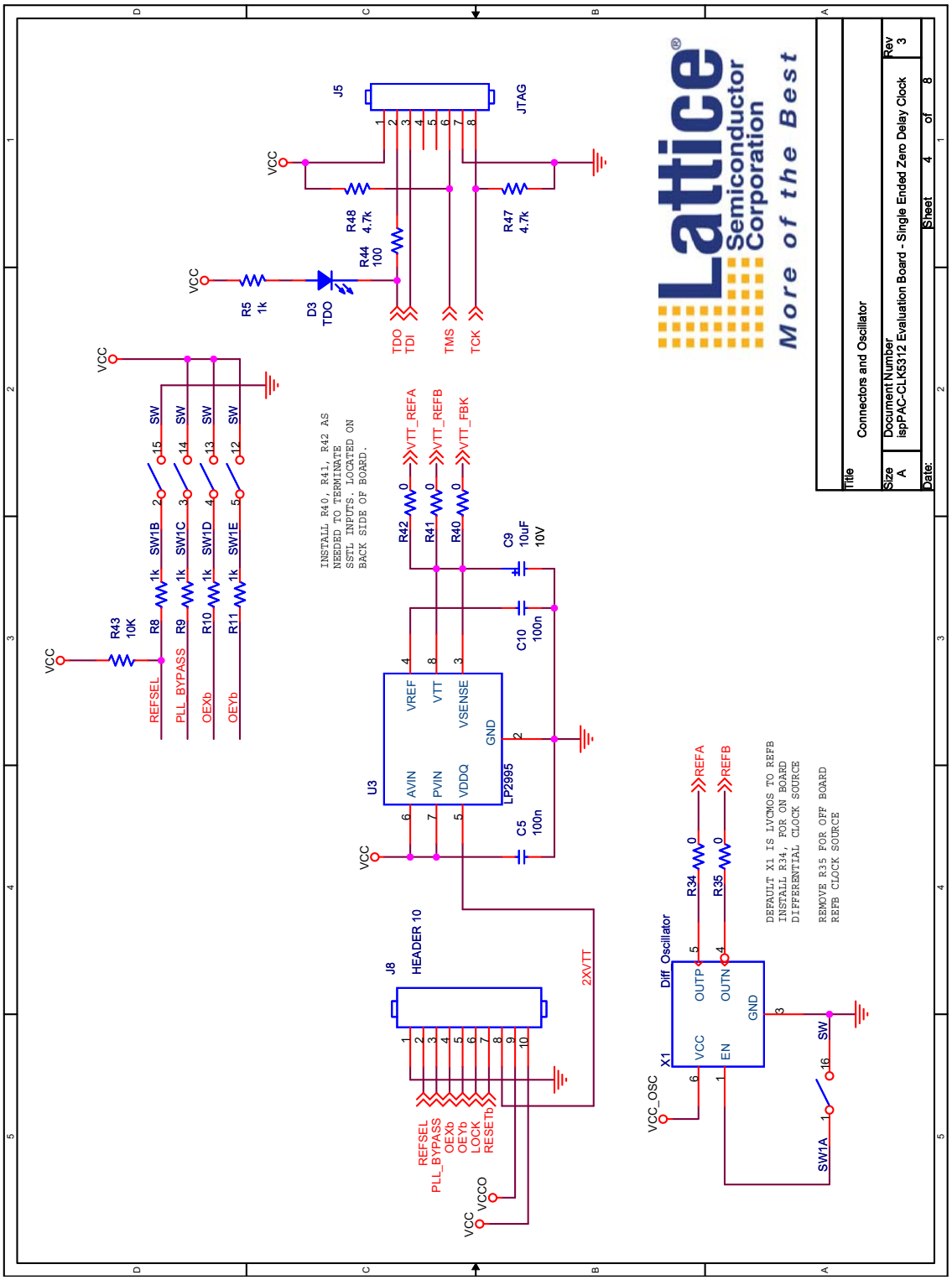


Figure 6-12. Power Supplies and LEDs

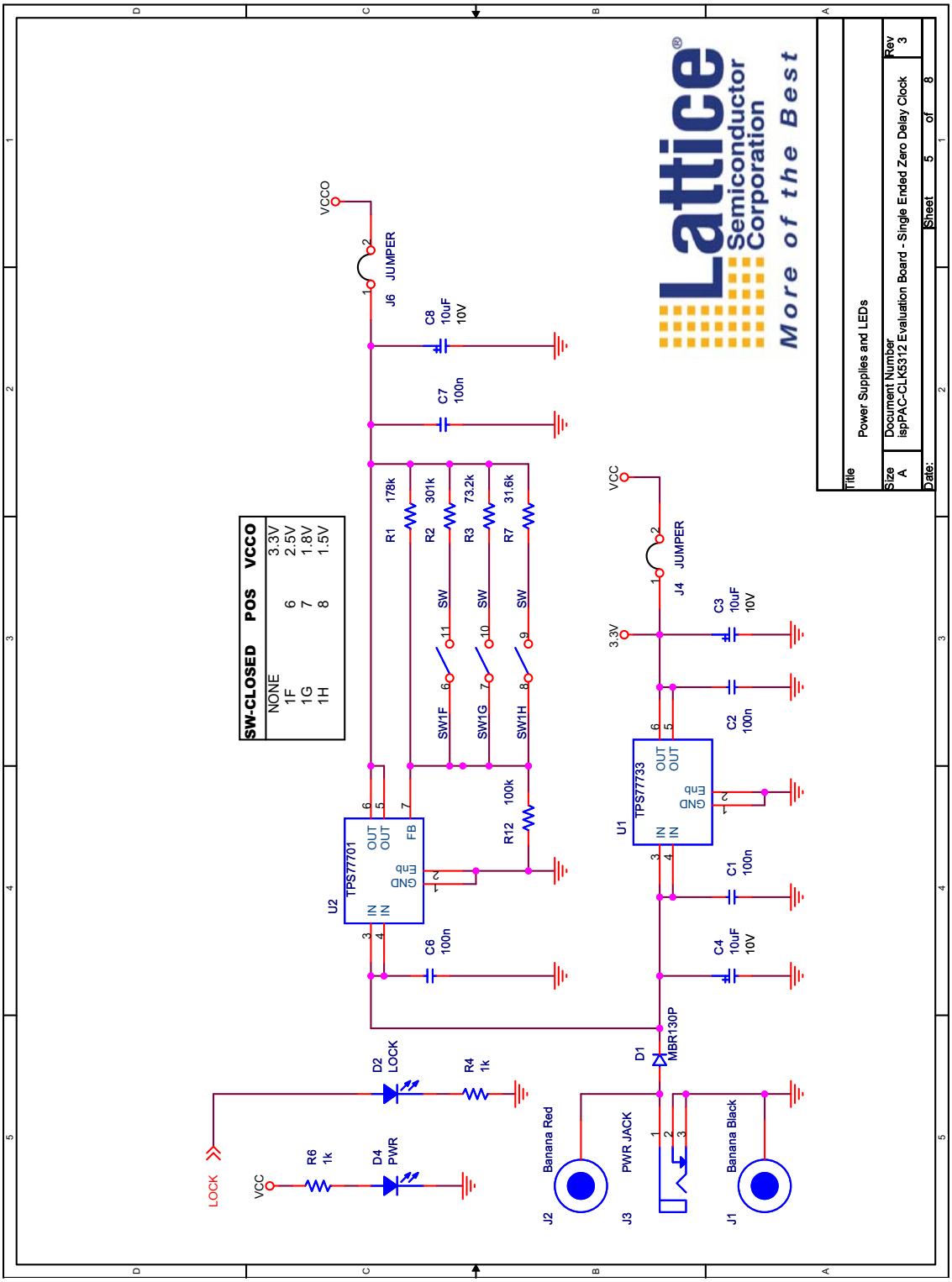


Figure 6-13. Power Supply Decoupling Networks and Reset Circuit

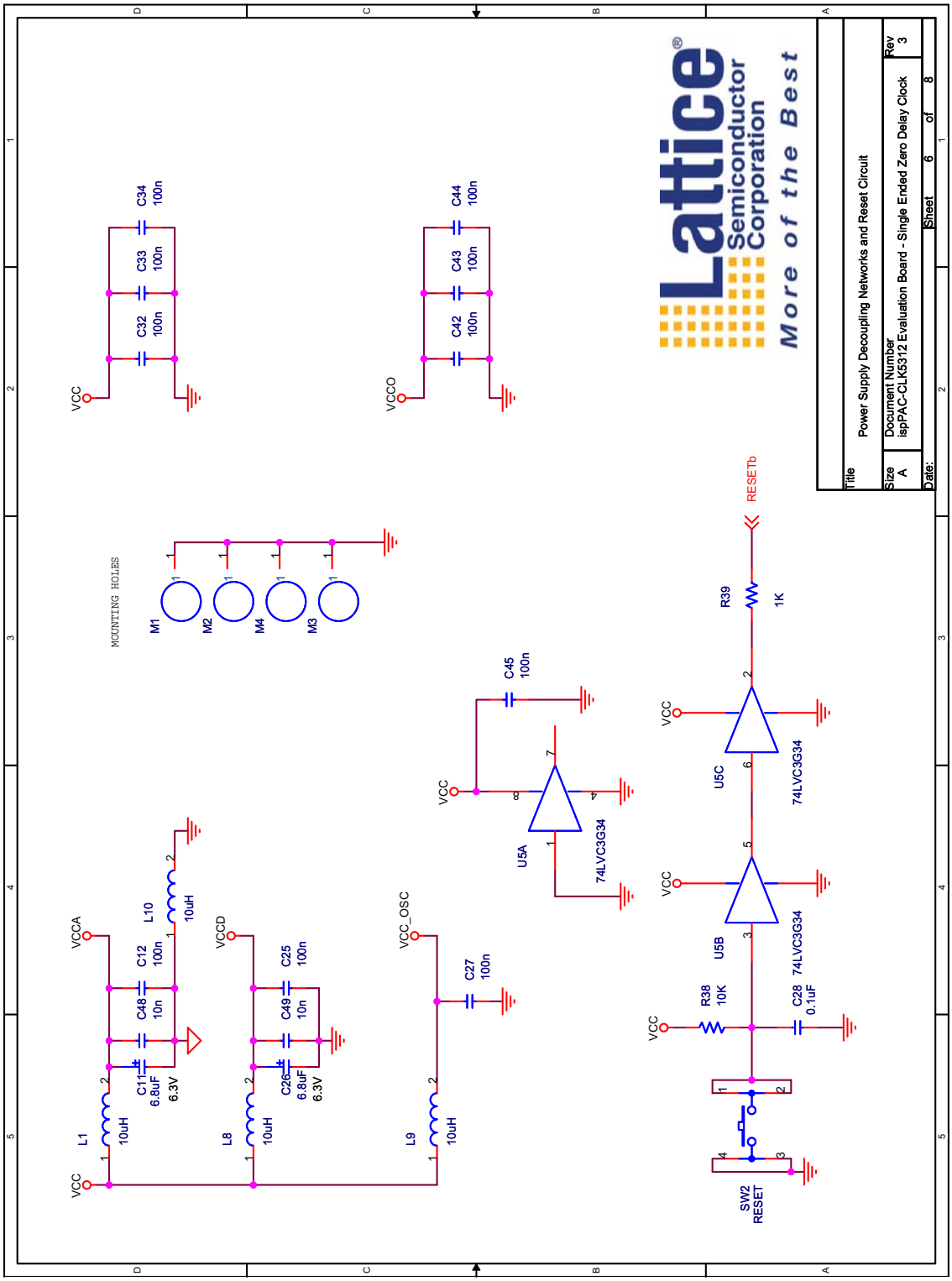


Figure 6-14. Banks 0, 1 and 2 Power Supply Decoupling Networks

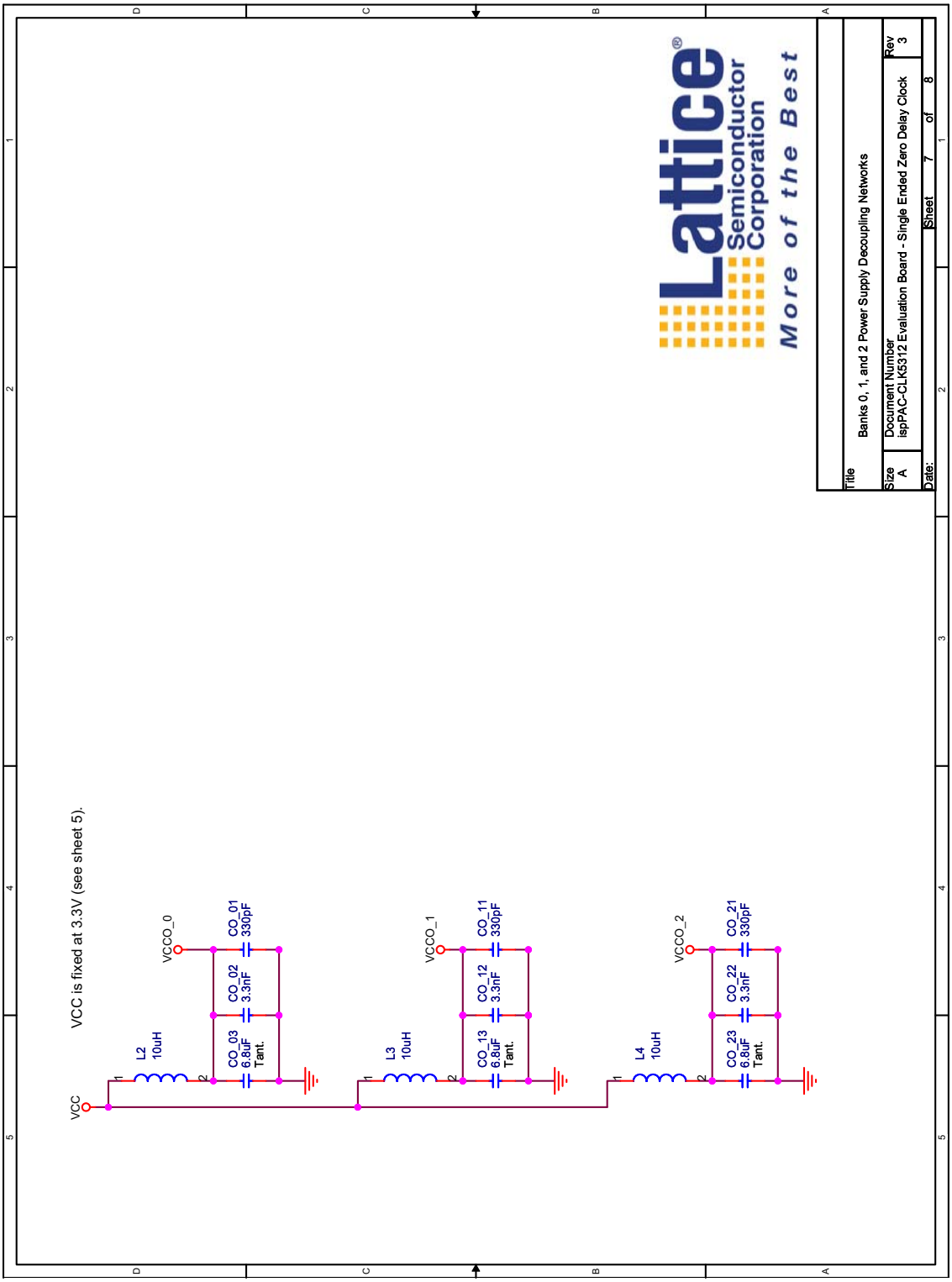
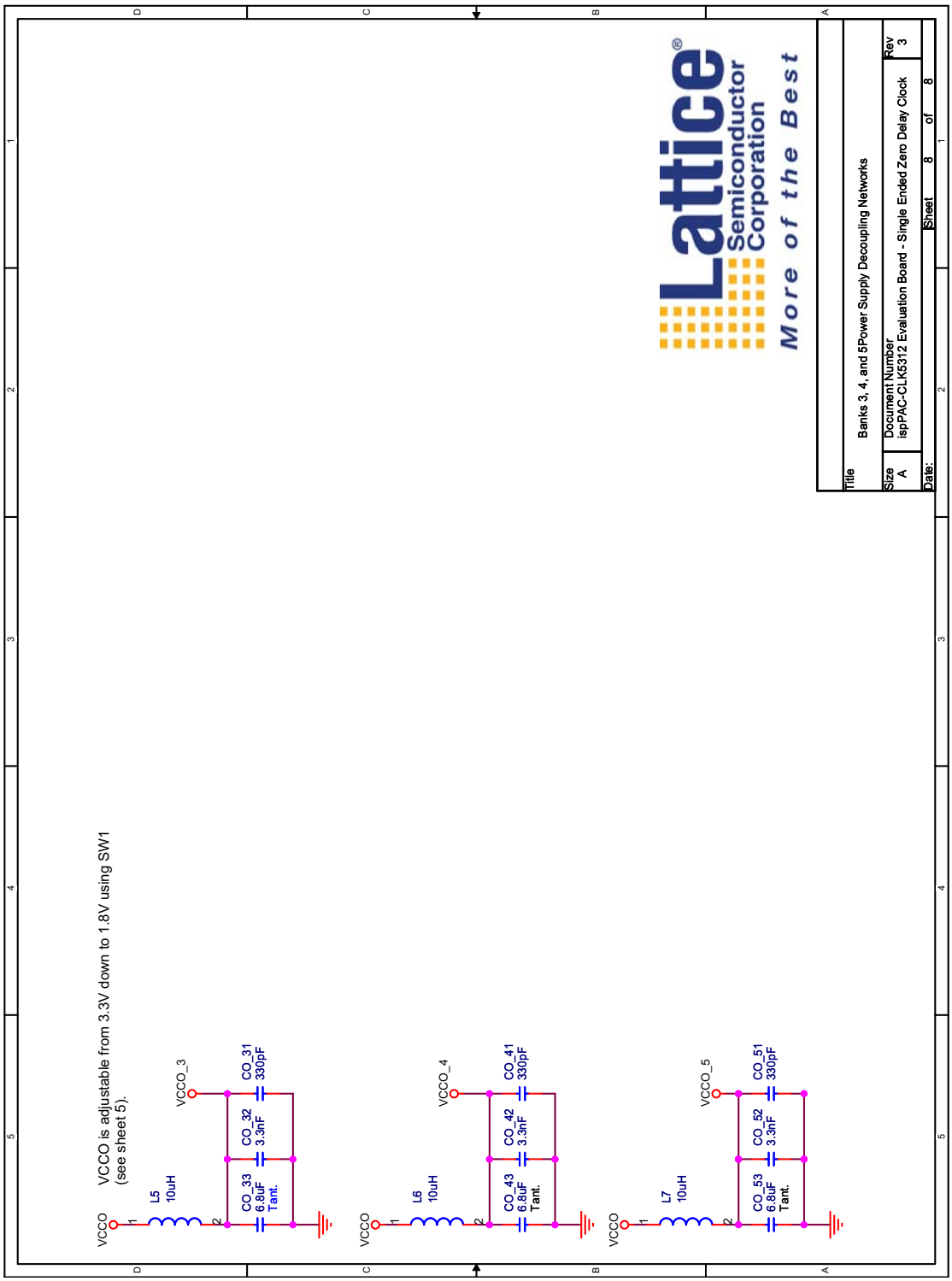


Figure 6-15. Banks 3, 4 and 5 Power Supply Decoupling Networks



Section III. ispClock Family Handbook Revision History

ispClock Family Handbook Revision History

Revision History

Date	Handbook Revison Number	Change Summary
April 2008	01.0	Initial release.
June 2008	01.1	ispClock5600A Family Data Sheet updated to version 01.4.
February 2009	01.2	Added ispClock5400D Family Data Sheet version 01.0.
		Added AN6080 version 01.0.
April 2009	01.3	ispClock5400D Family Data Sheet updated to version 01.1.
November 2009	01.4	ispClock5400D Family Data Sheet updated to version 01.2.

Note: For detailed revision changes, please refer to the revision history for each document.