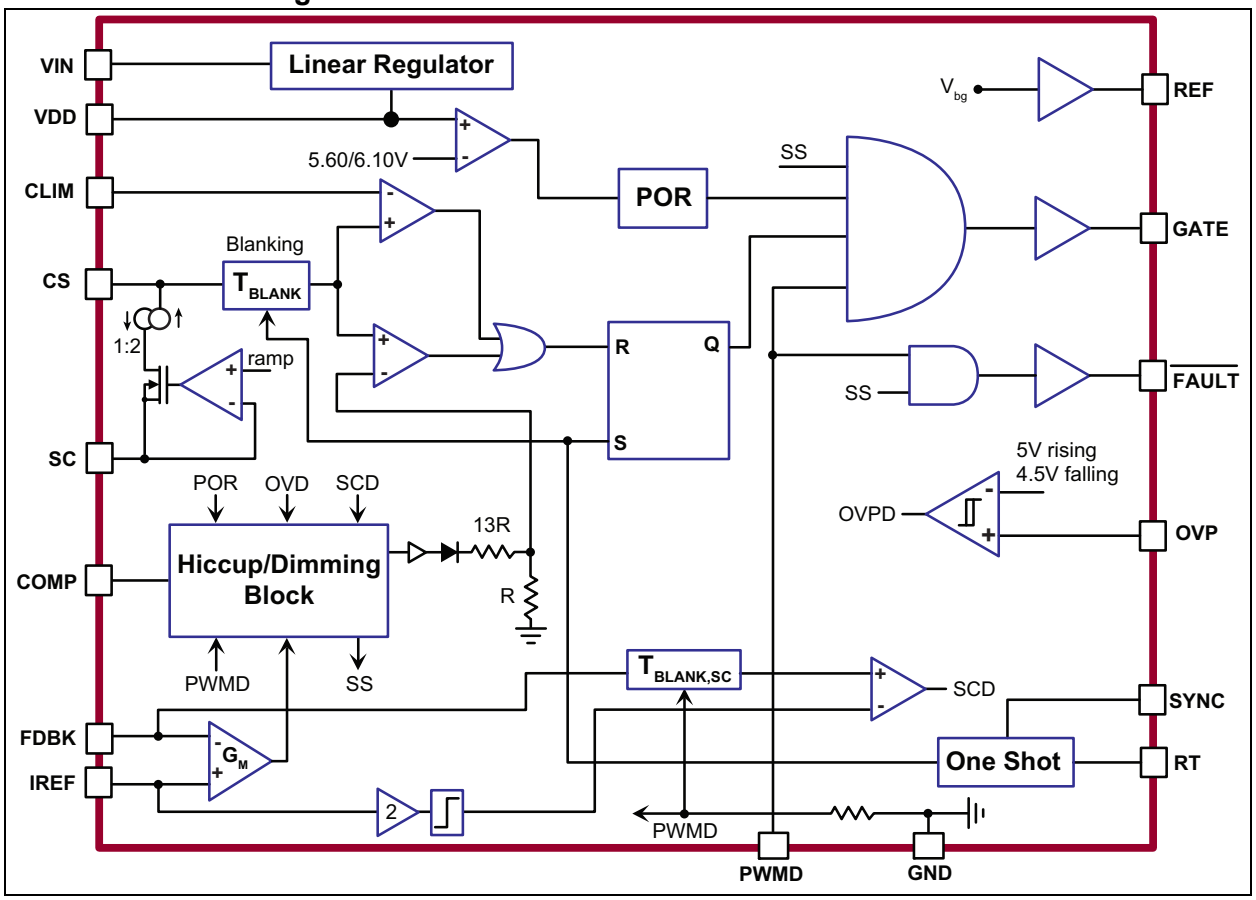
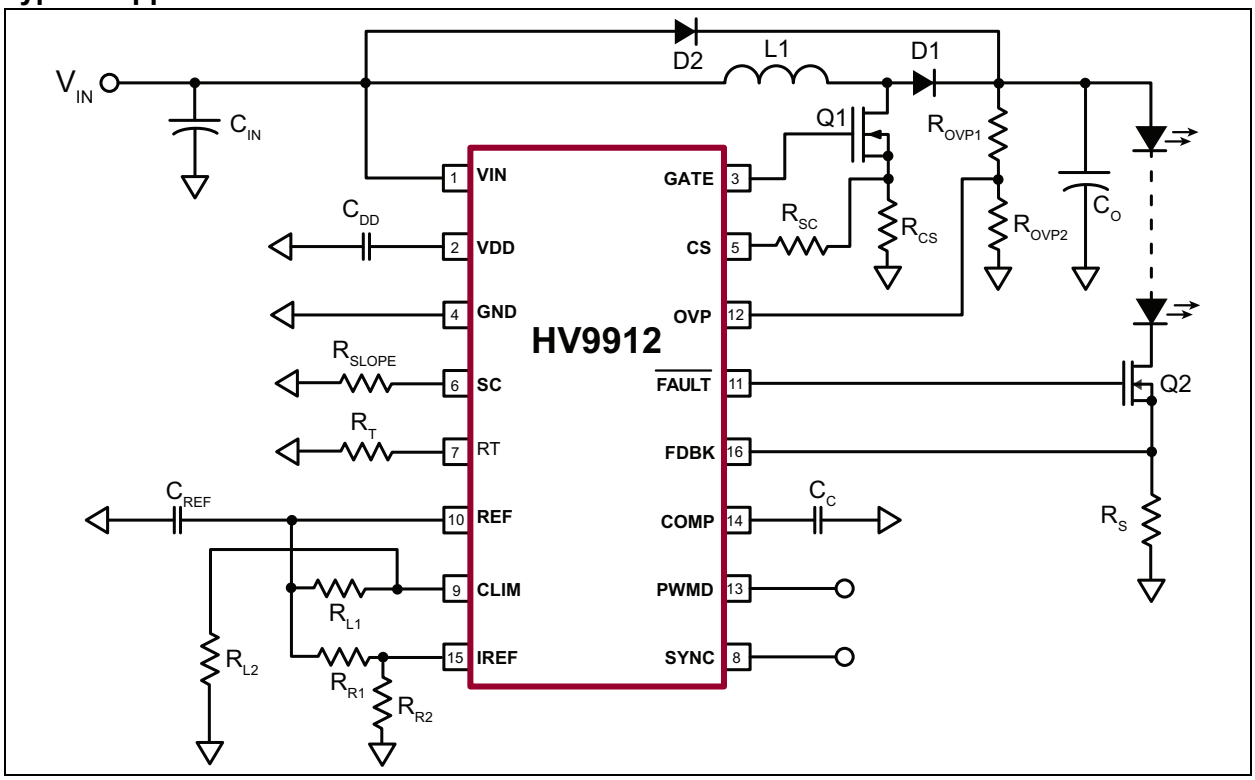
Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} to GND ..... –0.5 to +100V
V_{DD} to GND ..... –0.3V to +13.5V
CS to GND ..... –0.3V to V_{DD}+0.3V
PWMD to GND ..... –0.3V to V_{DD}+0.3V
GATE to GND ..... –0.3V to V_{DD}+0.3V
All Other Pins to GND ..... –0.3V to V_{DD}+0.3V
Continuous Power Dissipation (T_A= +25°C) ..... 1200 mW
Operating Junction Temperature Range ..... –40°C to +125°C
Storage Temperature Range ..... –65°C to +150°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C and V_{IN} = 12V unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
INPUT						
Input DC Supply Voltage Range	V_{INDC}	**Note 1**	—	90	V	DC input voltage (**Note 2**)
Shutdown Mode Supply Current	I_{INSD}	—	—	1.5	mA	PWMD connected to GND (**Note 2**)
INTERNAL REGULATOR						
Internally Regulated Voltage	V_{DD}	7.25	7.75	8.25	V	V_{IN} = 9V–90V; PWMD connected to GND (**Note 2**)
V_{DD} Undervoltage Lockout Threshold	$UVLO_{RISE}$	6.5	—	7	V	V_{DD} rising
V_{DD} Undervoltage Lockout Hysteresis	$UVLO_{HYST}$	—	500	—	mV	V_{DD} falling
REFERENCE						
REF Pin Voltage	V_{REF}	1.225	1.25	1.285	V	REF bypassed with a 0.1 µF capacitor to GND; I_{REF} = 0; PWMD = GND; 0°C < T_A < +85°C
		1.225	1.25	1.29		REF bypassed with a 0.1 µF capacitor to GND; I_{REF} = 0; PWMD = GND; –40°C < T_A < 125°C
Line Regulation of Reference Voltage	$V_{REFLINE}$	0	—	20	mV	REF bypassed with a 0.1 µF capacitor to GND; I_{REF} = 0; V_{DD} = 7.25V–12V; PWMD = GND

Note 1: See **Section 3.3 "Minimum Input Voltage at VIN Pin"** for the minimum input voltage.
2: The specifications which apply over the full operating temperature range at –40°C < T_A < +85°C are guaranteed by design and characterization.
3: For design guidance only

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: T_A = 25°C and V_{IN} = 12V unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Load Regulation of Reference Voltage	$V_{REFLOAD}$	0	—	10	mV	REF bypassed with a 0.1 µF capacitor to GND; I_{REF} = 0 µA–500 µA; PWMD = GND
PWM DIMMING						
PWMD Input Low Voltage	$V_{PWMD(LO)}$	—	—	0.8	V	**Note 2**
PWMD Input High Voltage	$V_{PWMD(HI)}$	2	—	—	V	**Note 2**
PWMD Pull-down Resistance	R_{PWMD}	50	100	150	kΩ	V_{PWMD} = 5V
GATE						
GATE Short-circuit Current	I_{SOURCE}	0.2	—	—	A	V_{GATE} = 0V
GATE Sinking Current	I_{SINK}	0.4	—	—	A	V_{GATE} = V_{DD}
GATE Output Rise Time	T_{RISE}	—	50	85	ns	C_{GATE} = 1 nF
GATE Output Fall Time	T_{FALL}	—	25	45	ns	C_{GATE} = 1 nF
OVERVOLTAGE PROTECTION						
Overvoltage Rising Trip Point	$V_{OVP,RISING}$	4.75	5	5.25	V	OVP rising
Overvoltage Hysteresis	$V_{OVP,HYST}$	—	0.5	—	V	OVP falling
CURRENT SENSE						
Leading Edge Blanking	T_{BLANK}	100	—	280	ns	0°C < T_A < +85°C
		100	—	330		–40°C < T_A < +125°C
Delay to Output of C_{OMP} Comparator	T_{DELAY1}	—	—	200	ns	COMP = V_{DD}; C_{LIM} = REF; C_{SENSE} = 0 mV to 600 mV (step up)
Delay to Output of C_{LIMIT} Comparator	T_{DELAY2}	—	—	200	ns	COMP = V_{DD}; C_{LIM} = 300 mV; C_{SENSE} = 0 mV to 400 mV (step up)
Comparator Offset Voltage	V_{OFFSET}	–10	—	10	mV	
INTERNAL TRANSCONDUCTANCE OPAMP						
Gain Bandwidth Product	GBW	—	1	—	MHz	75 pF capacitance at OP pin **(Note 3)**
Open-loop DC Gain	A_V	60	—	—	dB	Output open
Input Common Mode Range	V_{CM}	–0.3	—	3	V	**Note 3**
Output Voltage Range	V_O	0.7	—	6.75	V	**Note 3**
Transconductance	g_M	450	550	650	µA/V	
Input Offset Voltage	V_{OFFSET}	–5	—	5	mV	
Input Bias Current	I_{BIAS}	—	0.5	1	nA	**Note 3**
OSCILLATOR						
Oscillator Frequency	f_{OSC1}	99	106	118	kHz	R_T = 500 kΩ **(Note 2)**
	f_{OSC2}	510	580	650	kHz	R_T = 96 kΩ **(Note 2)**
Maximum Duty Cycle	D_{MAX}	87	—	93	%	

Note 1: See **Section 3.3 "Minimum Input Voltage at VIN Pin"** for the minimum input voltage.

2: The specifications which apply over the full operating temperature range at –40°C < T_A < +85°C are guaranteed by design and characterization.

3: For design guidance only

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: T_A = 25°C and V_{IN} = 12V unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
SYNC Input High	V_{SYNCH}	2	—	—	V	
SYNC Input Low	V_{SYNCL}	—	—	0.8	V	
SYNC Output Current	$I_{OUTSYNC}$	—	18	—	µA	
OUTPUT SHORT-CIRCUIT						
Gain for Short-circuit Comparator	G_{SC}	1.9	2	2.1	V	
Minimum Output Voltage of the Gain Stage	V_{OMIN}	0.125	—	0.25	V	0°C < T_A < +85°C; I_{REF} = GND
		0.125	—	0.26		–40°C < T_A < +125°C; I_{REF} = GND
Propagation Time for Short-circuit Detection	T_{OFF}	—	—	250	ns	PWMD = V_{DD}; I_{REF} = 400 mA; FDBK step from 0 mV to 900 mV; $\overline{FAULT}$ goes from high to low
Fault Output Rise Time	$T_{RISE,FAULT}$	—	—	300	ns	330 pF capacitor at $\overline{FAULT}$ pin
Fault Output Fall Time	$T_{FALL,FAULT}$	—	—	300	ns	330 pF capacitor at $\overline{FAULT}$ pin
Blanking Time	$T_{BLANK,SC}$	480	—	900	ns	
Current Source at COMP Pin used for Hiccup Mode Protection	I_{HICCUP}	—	5	—	µA	
SLOPE COMPENSATION						
Current Sourced Out of SC Pin	I_{SLOPE}	0	—	100	µA	**Note 2**
Internal Current Mirror Ratio	G_{SLOPE}	1.8	2	2.26		I_{SLOPE} = 50 µA; R_{SC} = 1 kΩ

Note 1: See **Section 3.3 "Minimum Input Voltage at VIN Pin"** for the minimum input voltage.

2: The specifications which apply over the full operating temperature range at –40°C < T_A < +85°C are guaranteed by design and characterization.

3: For design guidance only

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
TEMPERATURE RANGES						
Operating Junction Temperature	T_J	–40	—	+125	°C	
Storage Temperature	Ts	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
16-lead SOIC	θ_{JA}	—	83	—	°C/W	

2.0 PIN DESCRIPTION

Table 2-1 shows the pin description details of HV9912.

TABLE 2-1: PIN DESCRIPTION TABLE

Pin Number	Name	Description
1	VIN	This pin is the input of a 90V high-voltage regulator.
2	VDD	This is a power supply pin for all internal circuits. It must be bypassed with a low-ESR capacitor to GND (at least 0.1 µF).
3	GATE	This pin is the output gate driver for an external N-channel power MOSFET.
4	GND	This is the ground return for all the low-power analog internal circuitry. This pin must be connected to the return path from the input.
5	CS	This pin is used to sense the source current of the external power FET. It includes a built-in 100 ns (minimum) blanking time.
6	SC	This pin is used to set the slope compensation.
7	RT	This pin sets the frequency of the power circuit. A resistor between RT and GND will program the circuit in Constant Frequency mode.
8	SYNC	This I/O pin may be connected to the SYNC pin of other HV9912 circuits and will cause the oscillators to lock to the highest frequency oscillator.
9	CLIM	This pin provides a programmable input current limit for the converter. The current limit can be set using a resistor divider from the REF pin.
10	REF	This pin provides 2% accurate reference voltage. It must be bypassed with a 0.01 µF–0.1 µF capacitor to GND.
11	$\overline{\text{FAULT}}$	This pin is pulled to ground when there is an Output Short-circuit condition or Output Overvoltage condition. This pin can be used to drive an external MOSFET (in the case of boost converters) to disconnect the load from the source.
12	OVP	This pin provides the overvoltage protection for the converter. When the voltage at this pin exceeds 5V, the GATE output of the HV9912 is turned off, and the $\overline{\text{FAULT}}$ goes low. The IC will turn on when the voltage at the pin goes below 4.5V.
13	PWMD	When this pin is pulled to GND (or left open), switching of the HV9912 is disabled. When an external TTL high level is applied to it, switching will resume.
14	COMP	Stable Closed-loop control can be accomplished by connecting a compensation network between COMP and GND. This capacitor also controls the hiccup time.
15	IREF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the REF pin.
16	FDBK	This pin provides output current feedback to the HV9912 by using a current sense resistor.

3.0 DETAILED DESCRIPTION

3.1 Power Topology

The HV9912 is a Switch-mode converter LED driver designed to control a Continuous Conduction mode buck or boost in a Constant Frequency or Constant Off-time mode. The IC includes an internal linear regulator, which operates from input voltages up to 90V, eliminating the need for an external power supply for the IC. The IC includes features typically required in LED drivers, such as open LED protection, output short-circuit protection, linear and PWM dimming, programmable input current limiting and accurate control of the LED current. A high-current gate drive output enables the controller to be used in high-power converters.

The HV9912 is an enhanced version of the HV9911 with hysteretic overvoltage protection and Hiccup mode short-circuit protection. The IC includes a blanking network controlled by the PWMD input to prevent the short-circuit protection from triggering prematurely during PWM dimming due to the parasitic capacitance of the LED string. It also allows the I_{REF} pin to be pulled all the way down to GND without triggering the short-circuit protection. It is a pin-compatible replacement for the HV9911.

3.2 Linear Regulator

The HV9912 can be powered directly from its V_{IN} pin that withstands a voltage of up to 90V. When a voltage is applied to the V_{IN} pin, the HV9912 tries to maintain a constant 7.75V (typical) at the V_{DD} pin. The regulator also has a built-in undervoltage lockout which shuts off the IC if the voltage at the V_{DD} pin falls below the UVLO threshold.

The V_{DD} pin must be bypassed by a low-ESR capacitor (≥0.1 µF) to provide a low-impedance path for the high-frequency current of the output gate driver.

The input current drawn from the V_{IN} pin is the sum of the 1.5 mA current drawn by the internal circuit and the current drawn by the gate driver, which in turn depends on the switching frequency and the gate charge of the external FET. See Equation 3-1.

EQUATION 3-1:

$$I_{IN} = 1.5mA + (Q_G \bullet f_S)$$

In the above equation, f_S is the switching frequency, and Q_G is the external FET's gate charge, which can be obtained from the data sheet of the FET.

3.3 Minimum Input Voltage at V_{IN} Pin

The minimum input voltage at which the converter will start and stop depends on the minimum voltage drop required for the linear regulator. The internal linear regulator will control the voltage at the V_{DD} pin when V_{IN} is between 9V and 90V. However, when V_{IN} is less than 9V, the converter will still function as long as V_{DD} is greater than the undervoltage lockout. Thus, the converter might be able to start at input voltages lower than 9V. The start/stop voltages at the V_{IN} pin can be determined using the minimum voltage drop across the linear regulator as a function of the current drawn. This data is shown in Figure 3-1 for ambient temperatures of 25°C and 85°C.

Assume an ambient temperature of 85°C. Provided that the IC is driving a 15 nC gate charge FET at 200 kHz, the total input current is estimated to be 4.5 mA when Equation 3-1 is used. At this input current, the minimum voltage drop from Figure 3-1 would be around V_{DROP} = 1.25V. However, before the IC starts switching, the current drawn would have been 1.5 mA. At this current level, the voltage drop would be approximately V_{DROP1} = 0.3V. Thus, the start/stop V_{IN} voltages could be computed as demonstrated in Equation 3-2 and Equation 3-3 below:

EQUATION 3-2:

$$\begin{aligned} V_{IN(START)} &= UVLO_{MAX} + V_{DROP1} \\ &= 7V + 0.3V \\ &= 7.3V \end{aligned}$$

EQUATION 3-3:

$$\begin{aligned} V_{IN(STOP)} &= UVLO_{MAX} - \Delta UVLO + V_{DROP} \\ &= 7V - 0.5V + 1.25V \\ &= 7.75V \end{aligned}$$

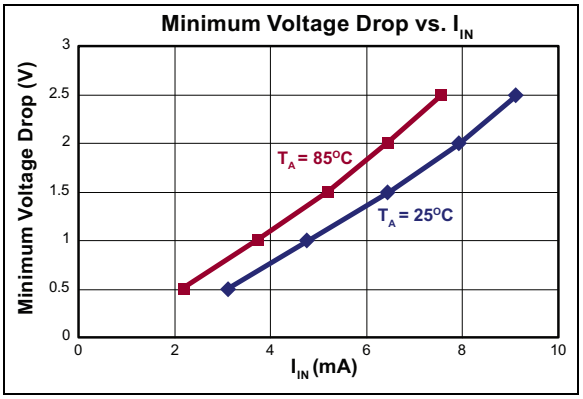


FIGURE 3-1: *Headroom vs. Input Current.*

In this case, the gate driver draws too much current and $V_{INSTART}$ is less than V_{INSTOP}. When this happens, the IC will oscillate between ON and OFF if the input

voltage is between the start and stop voltages. Therefore, it is recommended that the input voltage be kept higher than V_{INSTOP}.

3.4 Reference

HV9912 includes a 2% accurate 1.25V reference, which can be used as the reference for the output current as well as to set the switch current limit. The reference is buffered so that it can deliver a maximum of 500 µA external current to drive the external circuitry. The reference should be bypassed with at least a 10 nF low-ESR capacitor.

Note:	To avoid abnormal Startup conditions, the bypass capacitor at the REF pin should not exceed 0.1 µF.

3.5 Oscillator

Connecting the resistor between R_T and GND will program the time period.

In both cases, resistor R_T sets the current, which charges an internal oscillator capacitor. The capacitor voltage ramps up linearly. When the voltage increases beyond the internal set voltage, a comparator triggers the set input of the internal SR flip-flop. This starts the next switching cycle. The time period of the oscillator can be computed as shown in Equation 3-4.

EQUATION 3-4:

$$T_S \approx R_T \bullet 18pF$$

3.6 Synchronization

The SYNC pin is an input/output (I/O) port to a fault-tolerant peer-to-peer and/or master clock synchronization circuit. For synchronization, the SYNC pins of multiple HV9912-based converters can be connected together and may also be connected to the open drain output of a master clock. When connected in this manner, the oscillators will lock to the device with the highest operating frequency. When synchronizing multiple ICs, it is recommended that the same timing resistor (corresponding to the switching frequency) be used in all the HV9912 circuits.

On rare occasions, given the length of the connecting lines for the SYNC pins, a resistor between SYNC and GND may be required to damp any ringing due to parasitic capacitances. It is recommended that the resistor chosen be greater than 300 kΩ.

When synchronized in this manner, a permanent High or Low condition on the SYNC pin will result in a loss of synchronization, but the HV9912-based converters will continue to operate at their individually set operating frequencies. Since loss of synchronization will not result in total system failure, the SYNC pin is considered fault tolerant.

3.7 Slope Compensation

For Continuous Conduction mode converters operating in the Constant Frequency mode, slope compensation becomes necessary to ensure stability of the Peak Current mode controller if the operating duty cycle is greater than 50%. Choosing a slope compensation which is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

Slope compensation can be programmed by two resistors R_{SLOPE} and R_{SC}. Assuming a down slope of DS (A/µs) for the inductor current, the slope compensation resistors can be computed as illustrated in Equation 3-5.

EQUATION 3-5:

$$R_{SC} = \frac{R_{SLOPE} \bullet DS \bullet 10^6 \bullet T_S \bullet R_{CS}}{10}$$

Where R_{CS} is the current sense resistor which senses the switching FET current

Note:	The maximum current that can be sourced out of the SC pin is 100 µA. This limits the minimum value of the R_{SLOPE} resistor to 25 kΩ. If the equation for slope compensation produces a R_{SLOPE} less than this value, then R_{SC} would have to be reduced accordingly. It is recommended that R_{SLOPE} be chosen within the range of 25 kΩ to 50 kΩ.

3.8 Current Sense

The current sense input of the HV9912 includes a built-in 100 ns (minimum) blanking time to prevent spurious turn-off due to the initial current spike when the FET turns on.

The HV9912 includes two high-speed comparators—one is used during normal operation and the other is used to limit the maximum input current during Input Undervoltage or Overload conditions.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pin by a factor of 15. This stepped-down voltage is given to one of the comparators as the current reference. The reference to the other comparator, which acts to limit the maximum inductor current, is given externally.

It is recommended that the sense resistor R_{CS} be chosen so as to provide about 250 mV current sense signal.

3.9 Current Limit

Current limit has to be set by a resistor divider from the 1.25V reference available on the IC. Assuming a maximum operating inductor current I_{pk} (including ripple current), the maximum voltage at the C_{LIM} pin can be set as shown in Equation 3-6.

EQUATION 3-6:

$$V_{CLIM} \geq 1.2 \bullet I_{PK} \bullet R_{CS} + (5 \bullet R_{CS} / R_{SLOPE}) \bullet 0.9$$

Note that this equation assumes a current limit at 120% of the maximum input current. Also, if V_{CLIM} is greater than 450 mV, the saturation of the internal opamp will determine the limit on the input current rather than the C_{LIM} pin. In such a case, the sense resistor R_{CS} should be reduced until V_{CLIM} reduces below 550 mV.

It is recommended that no capacitor be connected between C_{LIM} and GND.

3.10 Internal 1 MHz Transconductance Amplifier

HV9912 includes a built-in 1 MHz transconductance amplifier with tri-state output, which can be used to close the feedback loop. The output current sense signal is connected to the FDBK pin and the current reference is connected to the I_{REF} pin.

The output of the opamp is controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the opamp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage on the integrating capacitor will force the converter into Steady state almost instantaneously.

The output of the opamp is buffered and connected to the current sense comparator using a 15:1 divider. The buffer helps to prevent the integrator capacitor from discharging during the PWM Dimming state.

3.11 PWM Dimming

PWM dimming can be achieved by driving the PWMD pin with a TTL-compatible square wave source. The PWM signal is connected internally to three different nodes—the transconductance amplifier, the $\overline{\text{FAULT}}$ output and the GATE output.

When the PWMD signal is high, the GATE and $\overline{\text{FAULT}}$ pins are enabled and the transconductance opamp's output is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Therefore the integrating capacitor maintains the voltage across it. The GATE is disabled, so the converter stops switching and the $\overline{\text{FAULT}}$ pin goes low, turning off the disconnect switch.

The output capacitor of the converter determines the converter's PWM dimming response because the capacitor has to get charged and discharged whenever the PWMD signal goes high or low. In the case of a buck converter, since the inductor current is continuous, a very small capacitor is used across the LEDs. This minimizes the effect of the capacitor on the converter's PWM dimming response. However, in the case of a boost converter, the output current is discontinuous, and a very large output capacitor is required to reduce the ripple in the LED current. Thus, this capacitor will have a significant impact on the PWM dimming response. By turning off the disconnect switch when PWMD goes low, the output capacitor is prevented from being discharged. This dramatically improves the boost converter's PWM dimming response.

Note:	In case of Continuous Conduction mode boost converters, disconnecting the capacitor might cause a sudden spike in the capacitor voltage as the energy in the inductor is dumped into the capacitor. This increase in the capacitor voltage might cause the OVP comparator to trip if the OVP point is set too close to the maximum operating voltage. Thus, either the capacitor has to be larger to absorb this energy without increasing the capacitor voltage significantly or the OVP set point has to be increased.

3.12 False Triggering of the Short-Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string causes a spike in the output current when the disconnect FET is turned on. With the HV9911, this parasitic spike in the output current makes the IC falsely detect an Overcurrent condition and shut down. To prevent this false shutdown, an R-C filter is used at the FDBK pin to filter this spike.

To prevent false triggering in the HV9912, there is a built-in 500 ns blanking network for the short-circuit comparator, which eliminates the need for the external R-C low-pass filter. This blanking network is activated when the PWMD input goes high. Thus, the short-circuit comparator will not see the spike in the LED current during the PWM Dimming turn-on transition. Once the blanking timer is completed, the short-circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short-circuit will depend on the condition of the PWMD input.

If the output short-circuit exists before the PWMD signal goes high, the total detection can be computed as shown in Equation 3-7:

EQUATION 3-7:

$$t_{detect} = t_{blank,SC(max)} + t_{delay(max)} \approx 900 + 250 \approx 1150ns(max)$$

If the short-circuit occurs when the PWMD signal is already high, the time to detect is determined through Equation 3-8:

EQUATION 3-8:

$$t_{detect1} = t_{delay(max)} \approx 250ns(max)$$

3.13 Hiccup Timer

HV9912 reuses the compensation network on the COMP pin to create a timer which is activated upon startup or when a detected Fault has been cleared. When a Fault is detected (either open-circuit or short-circuit) or upon startup, the COMP pin is disconnected from the g_M amplifier and the GATE and $\overline{FAULT}$ pins are pulled low, disabling the LED driver. When the Fault has cleared, a 5 µA current source is activated which pulls the COMP network up to 5V. Once the voltage at the COMP network reaches 5V, the 5 µA sourcing current is disconnected and a 5 µA sinking current is activated which pulls the COMP pin low. When the voltage at the COMP pin reaches 1V, the sinking current is disconnected and the g_M amplifier is reconnected to the COMP pin. The $\overline{FAULT}$ pin goes high and the GATE pin would be allowed to switch. The closed-loop control then takes over the control of the LED current.

3.14 Startup Condition

The startup waveforms are shown in Figure 3-2.

Assuming a pole-zero R-C network at the COMP pin (series combination of R_Z and C_Z in parallel with C_C), the start-up delay time can be approximately computed as shown in Equation 3-9.

EQUATION 3-9:

$$t_{delay} \approx t_{POR} + (C_C + C_Z) \bullet \frac{9V}{5\mu A}$$

This equation assumes that the voltage drop across R_Z can be neglected compared to the voltage swing at the COMP pin, which is true in most cases (R_Z < 100 kΩ). The POR time (t_{POR}) for the HV9912 is 10 µs.

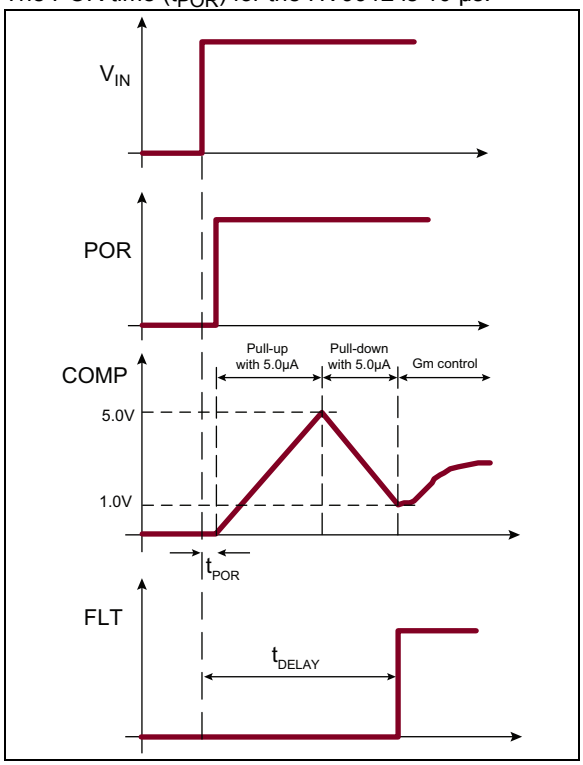


FIGURE 3-2: *Waveforms during Startup.*

3.15 Fault Condition

In the case of a Fault condition (either open-circuit or short-circuit), the same sequence is repeated, and the only difference is that the COMP pin voltage does not start from zero but from its Steady-state condition.

3.16 Short-Circuit Protection

When a Short-circuit condition is detected (output current becomes higher than twice the Steady-state current), the GATE and $\overline{FAULT}$ outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the Short-circuit condition disappears. At this time, the hiccup timer is started. (See Figure 3-3.) Once the timing is complete, the converter attempts to restart. If the Fault condition still persists, the converter shuts down and goes through the cycle again. If the Fault condition is cleared due to a momentary output short, the converter will start regulating the output current normally. This allows the LED driver to recover from accidental shorts without having to reset the IC.

The hiccup time will depend on the Steady-state voltage of the COMP pin (V_{COMP}). This is typically in the range of 3V–4V. The hiccup time can be approximately computed with Equation 3-10.

EQUATION 3-10:

$$t_{HICCUP} \approx (C_C + C_Z) \bullet \frac{9V - V_{COMP}}{5\mu A}$$

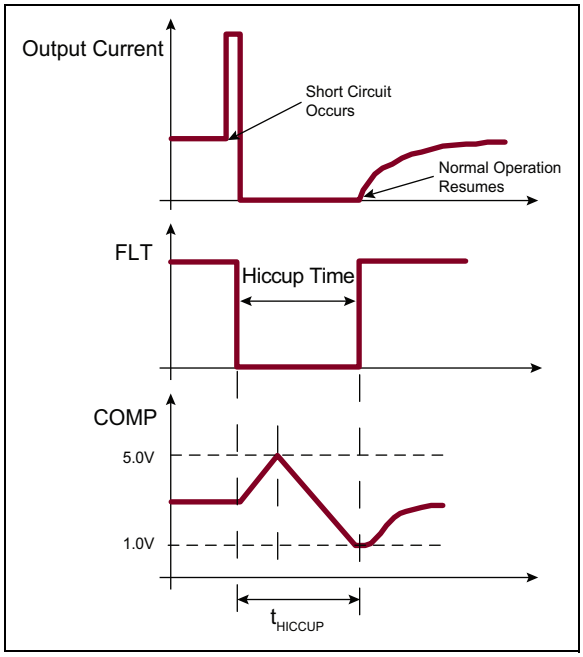


FIGURE 3-3: *Short-circuit Protection.*

3.17 Overvoltage Protection

The HV9912 provides hysteretic overvoltage protection, allowing the IC to recover in case the LED load is disconnected momentarily.

When the load is disconnected in a boost converter, the output voltage rises as the output capacitor starts charging. When the output voltage reaches the OVP rising threshold, the HV9912 detects an Overvoltage condition and turns off the converter. The converter is turned back on only when the output voltage falls below the falling OVP threshold, which is 10% lower than the rising threshold. This time is mostly dictated by the R-C time constant of the output capacitor C_O and the resistor network used to sense overvoltage (R_{OVP1} + R_{OVP2}). In case of a persistent Open-circuit condition, this cycle keeps repeating, maintaining the output voltage within a 10% band.

In most designs, the lower threshold voltage of the overvoltage protection is more than the LED string voltage when the converter is turned on. Thus, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED string voltage will cause a spike in the output current when the $\overline{FAULT}$ signal goes high. This causes a short-circuit to be detected and the HV9912 will go into short-circuit protection. This continues until the output voltage becomes lower than the LED string voltage, at which point no Fault will be detected and the normal operation of the circuit will commence. (See Figure 3-4.)

The various delay times can be determined as shown in Equation 3-11, Equation 3-12 and Equation 3-13:

EQUATION 3-11:

$$t_{RC} \approx 0.1 \bullet (R_{OVP1} + R_{OVP2}) \bullet C_O$$

EQUATION 3-12:

$$t_{HICCUP1} \approx (C_C + C_Z) \bullet \frac{9V - V_{COMP}}{5\mu A}$$

EQUATION 3-13:

$$t_{HICCUP2-n} \approx (C_C + C_Z) \bullet \frac{9V}{5\mu A}$$

Note: The number of hiccup cycles might be more than two.

3.18 Linear Dimming

Linear dimming can be achieved by varying the voltage at the I_{REF} pin because the output current is proportional to the voltage at the pin. This can be done either by using a potentiometer from the I_{REF} pin or applying an external voltage source to the pin.

In the HV9911, due to the offset voltage of the short-circuit comparator as well as the non-linearity of the X2 gain stage, pulling the I_{REF} pin very close to GND will cause the internal short-circuit comparator to trigger and shut down the IC.

To overcome this in the HV9912, the minimum output of the gain stage is limited to 125 ~ 250mV, allowing the I_{REF} pin to be pulled all the way to 0V without triggering the short-circuit comparator.

Note: Since this control IC is a Peak Current mode controller, pulling the I_{REF} pin to zero will not cause the LED current to become zero. The converter will still be operating at its minimum on time, causing a very small current to flow through the LEDs. To get zero LED current, the PWMD input has to be pulled to GND.

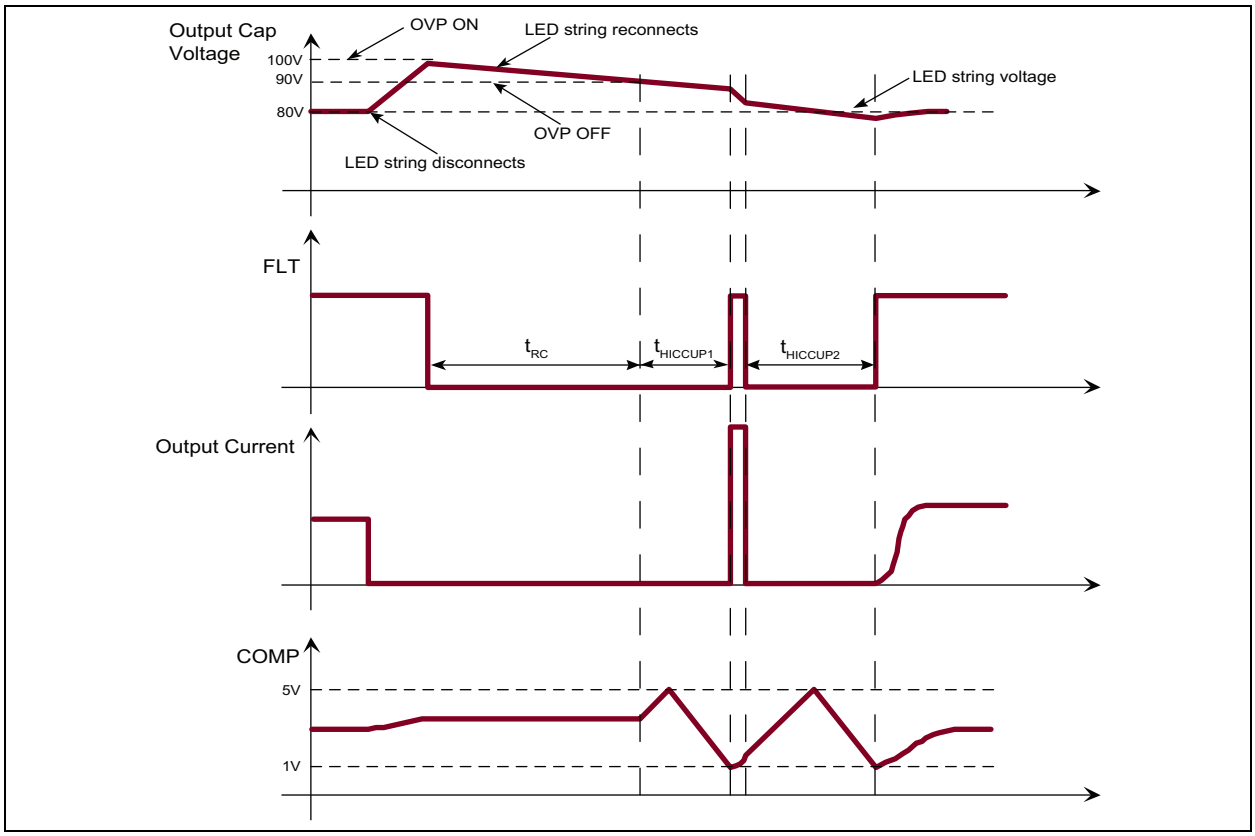
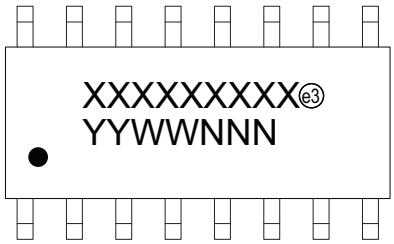


FIGURE 3-4: *Open-circuit Protection.*

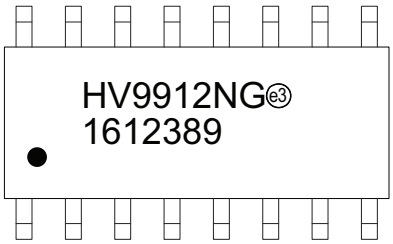
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

16-lead SOIC



Example

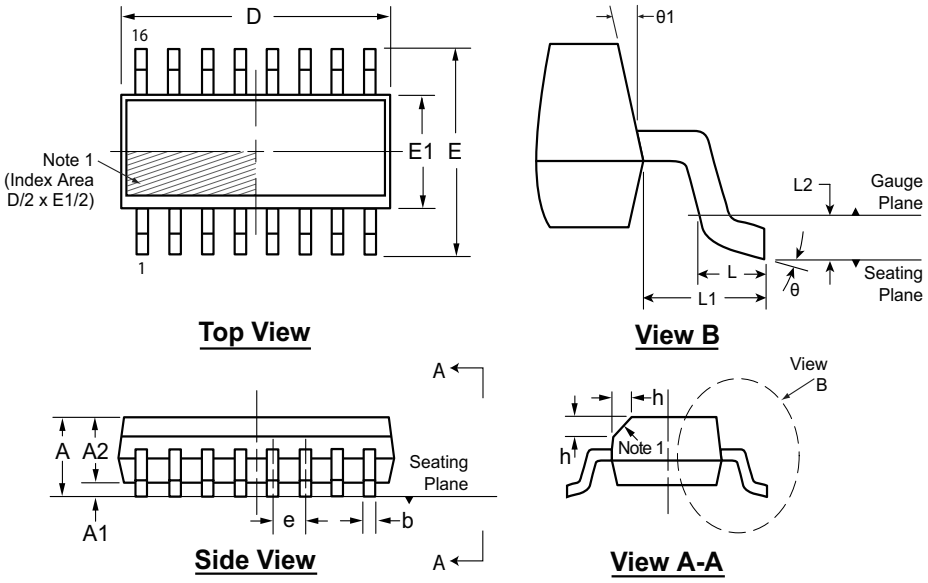


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (July 2016)

- Converted Supertex Doc# DSFP-HV9912 to Microchip DS20005583A.
- Made minor text changes throughout the document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9912	=	Switch-Mode LED Driver IC with High Current Accuracy and Hiccup Mode Protection
Package:	NG	=	16-lead SOIC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	45/Tube for an NG Package
	M901	=	2600/Reel for an NG Package
	M934	=	2600/Reel for an NG Package

Note: For media types M901 and M934, the base quantity for tape and reel was standardized to 2600/reel. Both options will result in delivery of the same number of parts/reel.

Examples:

a) HV9912NG-G: Switch-Mode LED Driver IC with High Current Accuracy and Hiccup Mode Protection, 16-lead SOIC Package, 45/Tube

b) HV9912NG-G-M901: Switch-Mode LED Driver IC with High Current Accuracy and Hiccup Mode Protection, 16-lead SOIC Package, 2600/Reel

c) HV9912NG-G-M934: Switch-Mode LED Driver IC with High Current Accuracy and Hiccup Mode Protection, 16-lead SOIC Package, 2600/Reel

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