ON Semiconductor®

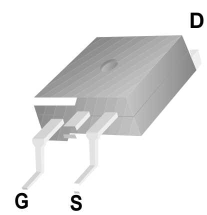
# FCB20N60-F085

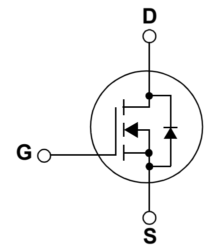
## N-Channel MOSFET

### 600V, 20A, 198mΩ

### Features

- Typ $r_{DS(on)}$ = 173mΩ at $V_{GS}$ = 10V, $I_D$ = 20A
- Typ $Q_{g(tot)}$ = 72nC at $V_{GS}$ = 10V, $I_D$ = 20A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101




### Description

SuperFET[TM] is ON Semiconductor's proprietary new generation of high voltage MOSFETs utilizing an advanced charge balance mechanism for outstanding low on-resistance and

lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.

Consequently, SuperFET is suitable for various automotive DC/DC power conversion.

### Applications

- Automotive On Board Charger
- Automotive DC/DC converter for HEV

### MOSFET Maximum Ratings $T_J$ = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | 600 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±30 | V |
| $I_D$ | Drain Current - Continuous ($V_{GS}$=10) (Note 1) | $T_C$ = 25°C | 20 | A |
| | Pulsed Drain Current | $T_C$ = 25°C | See Figure4 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | (Note 2) | 480 | mJ |
| $P_D$ | Power Dissipation | | 341 | W |
| | Derate above 25°C | | 2.3 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | | -55 to + 150 | °C |
| $R_{\theta JC}$ | Thermal Resistance Junction to Case | | 0.44 | °C/W |
| $R_{\theta JA}$ | Maximum Thermal Resistance Junction to Ambient | (Note 3) | 43 | °C/W |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FCB20N60 | FCB20N60-F085 | TO-263AB | 330mm | 24mm | 800 units |

Notes:
1: Current is limited by bondwire configuration.
2: Starting $T_J$ = 25°C, L = 15mH, $I_{AS}$ = 8A, $V_{DD}$ = 100V during inductor charging and $V_{DD}$ = 0V during time in avalanche
3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 $in^2$ pad of 2oz copper.


September-2017, Rev. 3

Publication Order Number:
FCB20N60-F085/D

## Electrical Characteristics $T_J$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|

### Off Characteristics

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $B_{VDSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250μA, $V_{GS}$ = 0V | | 600 | - | - | V |
| $I_{DSS}$ | Drain to Source Leakage Current | $V_{DS}$=600V, | $T_J$ = 25°C | - | - | 1 | μA |
| | | $V_{GS}$ = 0V | $T_J$ = 150°C(Note 4) | - | - | 1 | mA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±30V | | - | - | ±100 | nA |

### On Characteristics

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | | 3.0 | 4.0 | 5.0 | V |
| $r_{DS(on)}$ | Drain to Source On Resistance | $I_D$ = 20A, | $T_J$ = 25°C | - | 173 | 198 | mΩ |
| | | $V_{GS}$= 10V | $T_J$ = 150°C(Note 4) | - | 471 | 570 | mΩ |

### Dynamic Characteristics

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1MHz | | - | 2710 | 3080 | pF |
| $C_{oss}$ | Output Capacitance | | | - | 1350 | 1665 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | - | 86 | 150 | pF |
| $R_g$ | Gate Resistance | f = 1MHz | | - | 1 | - | Ω |
| $Q_{g(ToT)}$ | Total Gate Charge at 10V | $V_{GS}$ = 0 to 10V | $V_{DD}$ = 300V, $I_D$ = 20A | - | 72 | 102 | nC |
| $Q_{g(th)}$ | Threshold Gate Charge | $V_{GS}$ = 0 to 2V | | - | 5 | 8.6 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | - | 15 | - | nC |
| $Q_{gd}$ | Gate to Drain "Miller" Charge | | | - | 31 | - | nC |

### Switching Characteristics

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-On Time | $V_{DD}$ = 300V, $I_D$ = 20A, $V_{GS}$ = 10V, $R_G$ = 25Ω | - | - | 166 | ns |
| $t_{d(on)}$ | Turn-On Delay Time | | - | 44 | - | ns |
| $t_r$ | Rise Time | | - | 60 | - | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 208 | - | ns |
| $t_f$ | Fall Time | | - | 43 | - | ns |
| $t_{off}$ | Turn-Off Time | | - | - | 400 | ns |

### Drain-Source Diode Characteristics

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Source to Drain Diode Voltage | $I_{SD}$ = 20A, $V_{GS}$ = 0V | - | - | 1.4 | V |
| $T_{rr}$ | Reverse Recovery Time | $I_F$ = 20A, $dI_{SD}/dt$ = 100A/μs, $V_{DD}$=480V | - | 486 | 632 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 10 | 13 | μC |

**Notes:**

4: The maximum value is specified by design at $T_J$ = 150°C. Product is not tested to this condition in production.

## Typical Characteristics

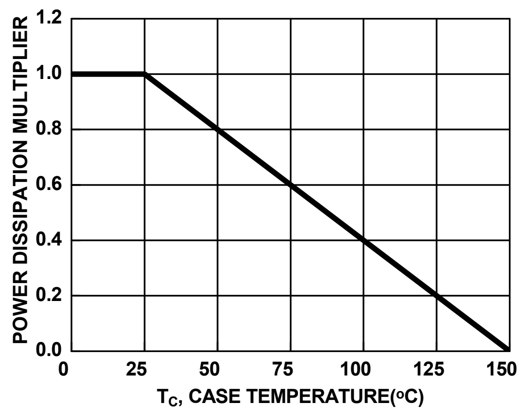



Figure 1. Normalized Power Dissipation vs Case Temperature

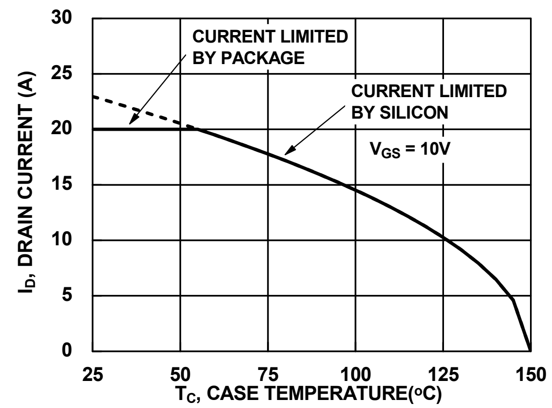



Figure 2. Maximum Continuous Drain Current vs Case Temperature

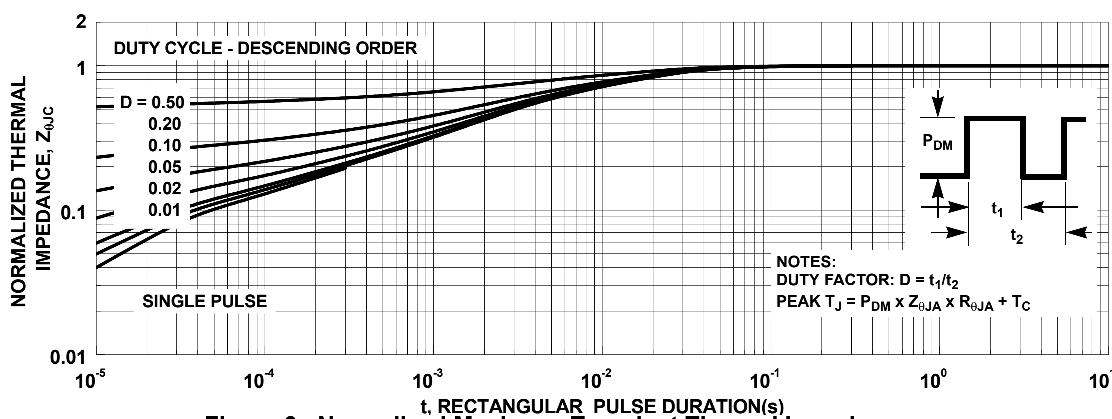



Figure 3. Normalized Maximum Transient Thermal Impedance

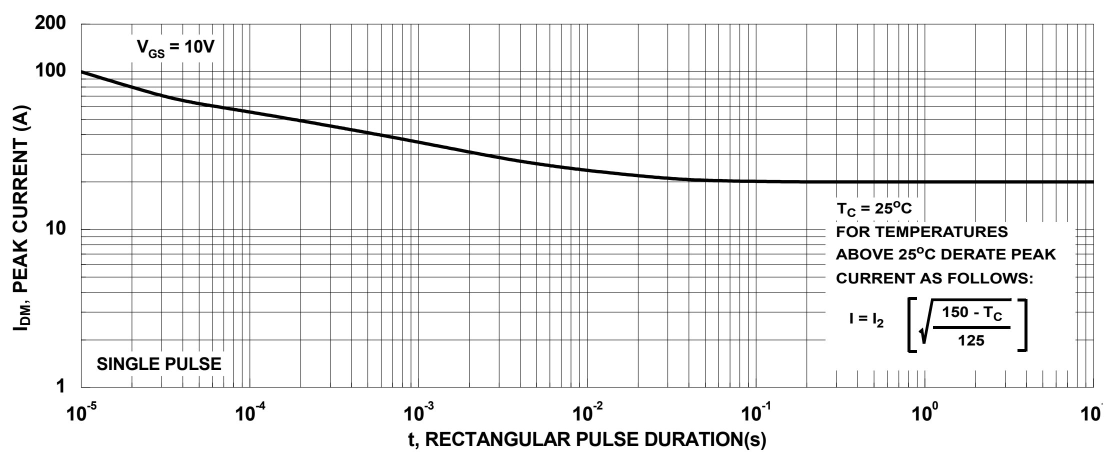



Figure 4. Peak Current Capability

## Typical Characteristics

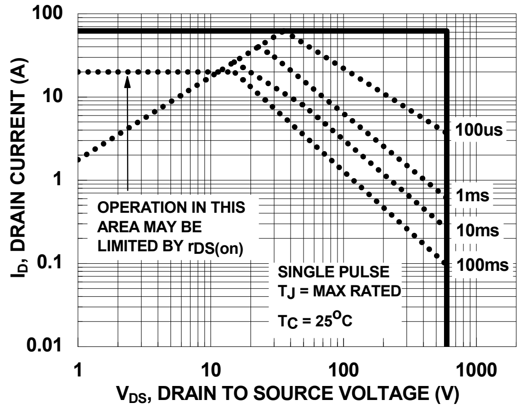



Figure 5. Forward Bias Safe Operating Area

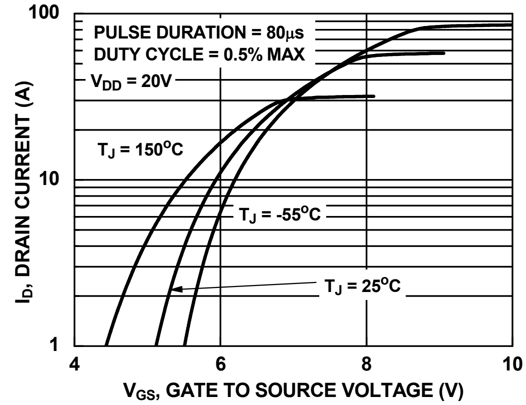



Figure 6. Transfer Characteristics

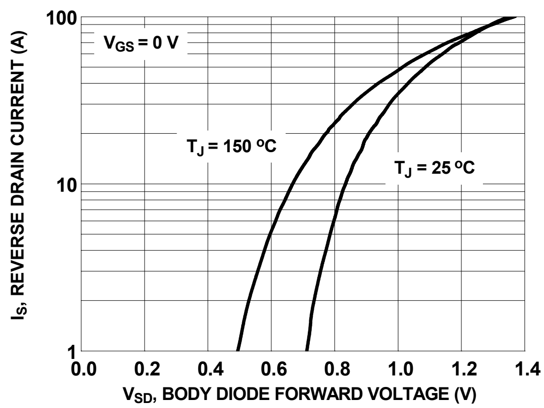



Figure 7. Forward Diode Characteristics

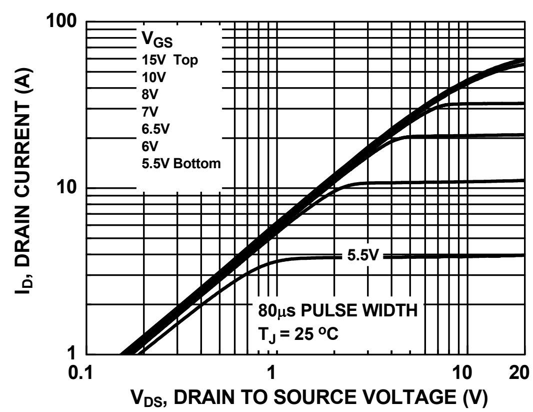



Figure 8. Saturation Characteristics

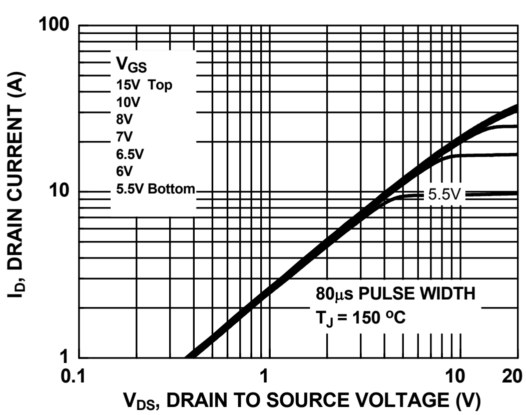



Figure 9. Saturation Characteristics

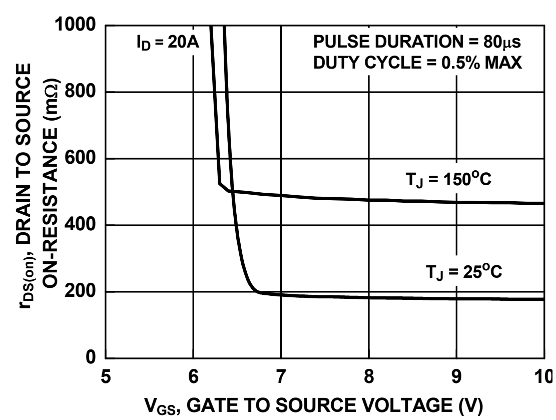



Figure 10. Rdson vs Gate Voltage

## Typical Characteristics

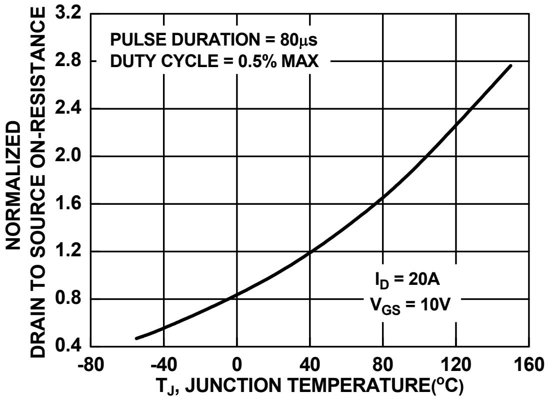



**Figure 11. Normalized Rdson vs Junction Temperature**

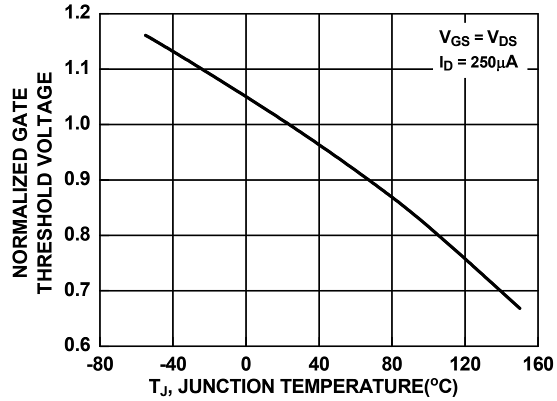



**Figure 12. Normalized Gate Threshold Voltage vs Temperature**

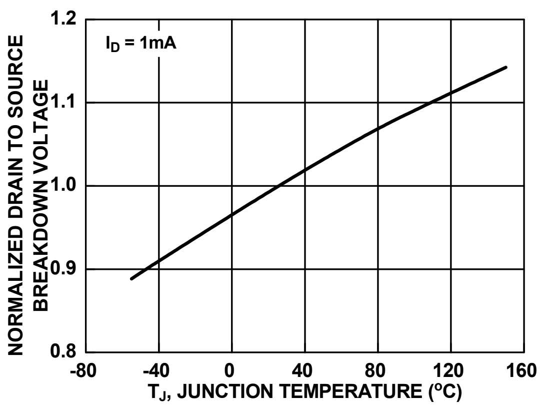



**Figure 13. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**

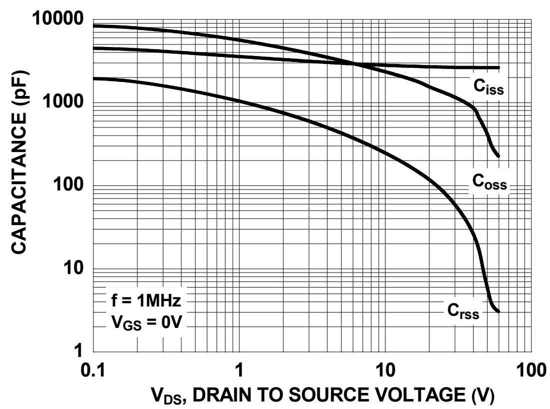



**Figure 14. Capacitance vs Drain to Source Voltage**

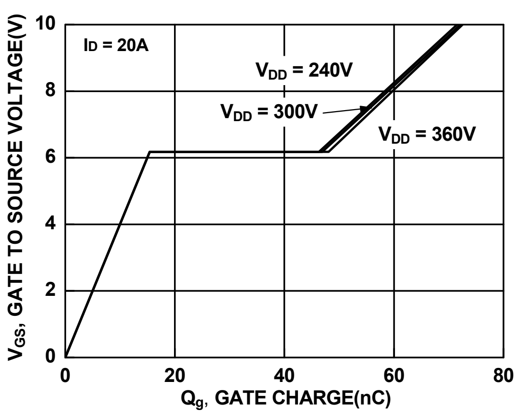



**Figure 15. Gate Charge vs Gate to Source Voltage**

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