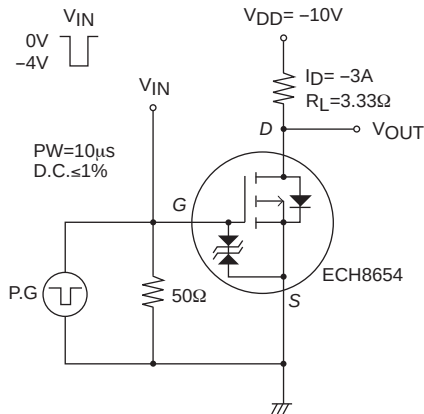


Electrical Characteristics at Ta=25°C

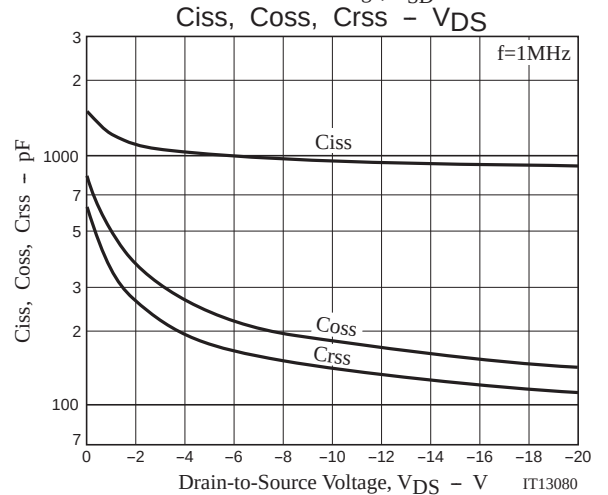
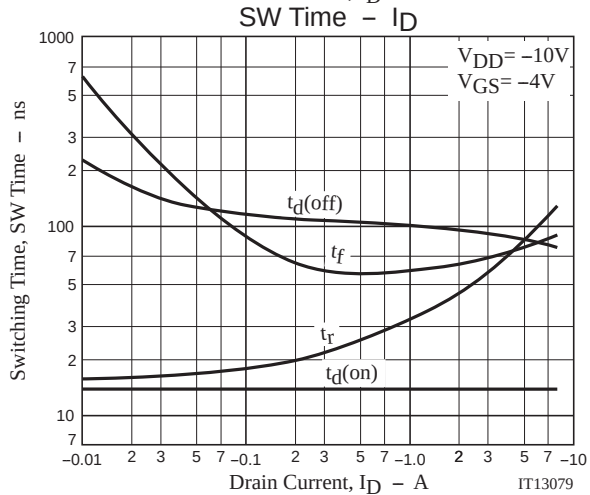
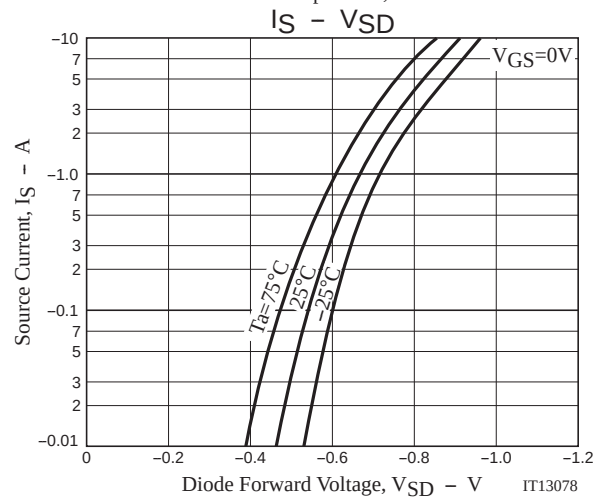
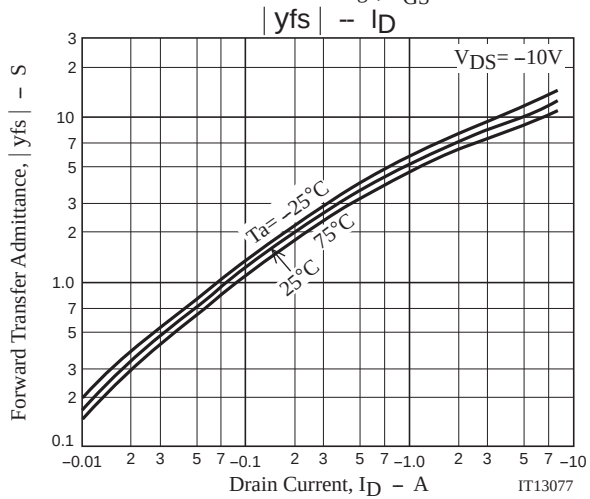
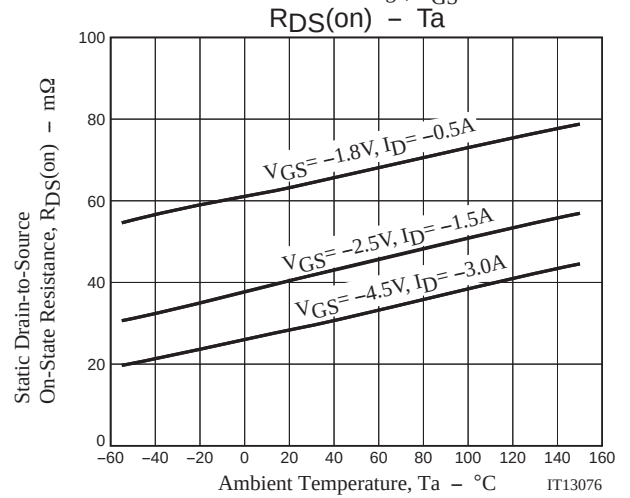
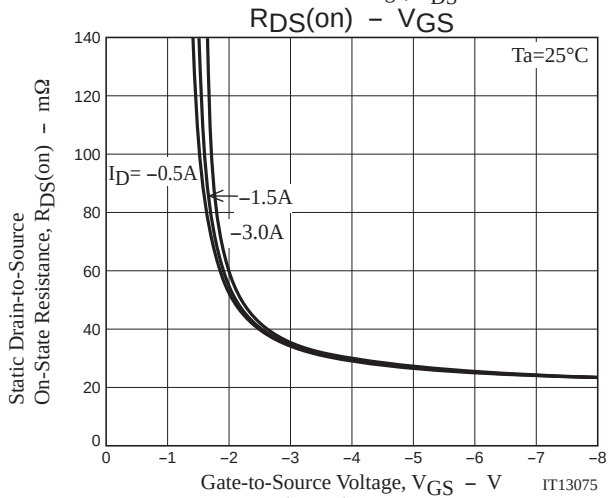
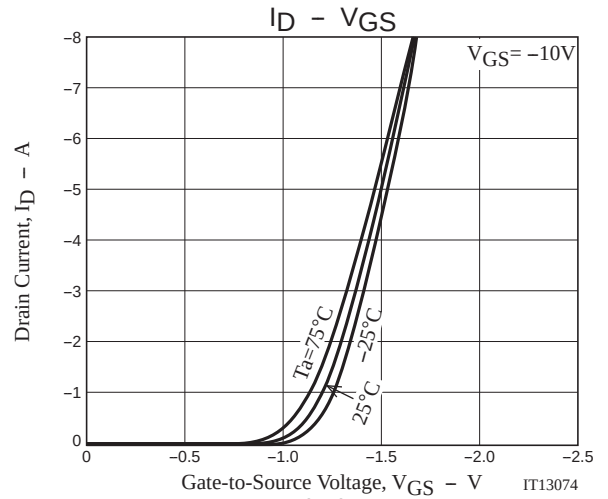
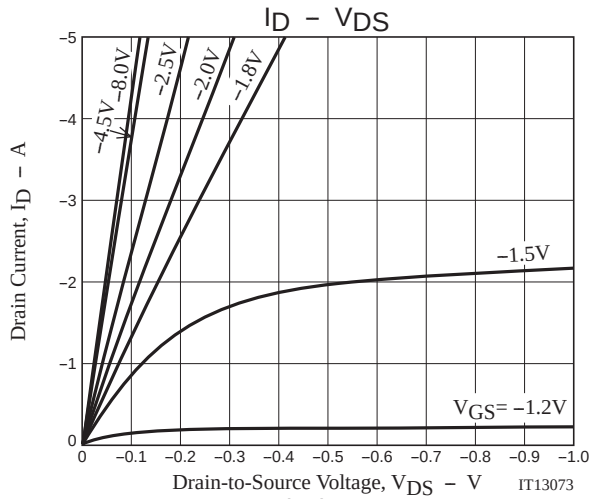
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = -1mA, V_{GS} = 0V$	-20			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$			-1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 8V, V_{DS} = 0V$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = -10V, I_D = -1mA$	-0.4		-1.3	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10V, I_D = -3A$	4.9	8.3		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D = -3A, V_{GS} = -4.5V$		29	38	m Ω
	$R_{DS(on)2}$	$I_D = -1.5A, V_{GS} = -2.5V$		41	58	m Ω
	$R_{DS(on)3}$	$I_D = -0.5A, V_{GS} = -1.8V$		64	98	m Ω
Input Capacitance	C_{iss}	$V_{DS} = -10V, f = 1MHz$		960		pF
Output Capacitance	C_{oss}			180		pF
Reverse Transfer Capacitance	C_{rss}			140		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		14		ns
Rise Time	t_r			55		ns
Turn-OFF Delay Time	$t_{d(off)}$			92		ns
Fall Time	t_f			68		ns
Total Gate Charge	Q_g	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -5A$		11		nC
Gate-to-Source Charge	Q_{gs}			2.0		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			2.8		nC
Diode Forward Voltage	V_{SD}	$I_S = -5A, V_{GS} = 0V$		-0.82	-1.2	V

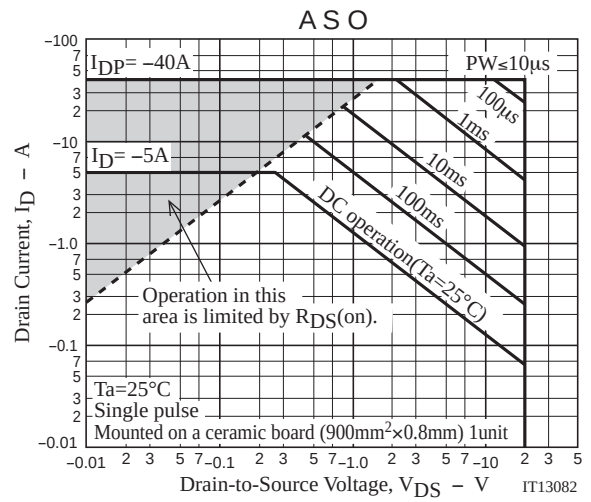
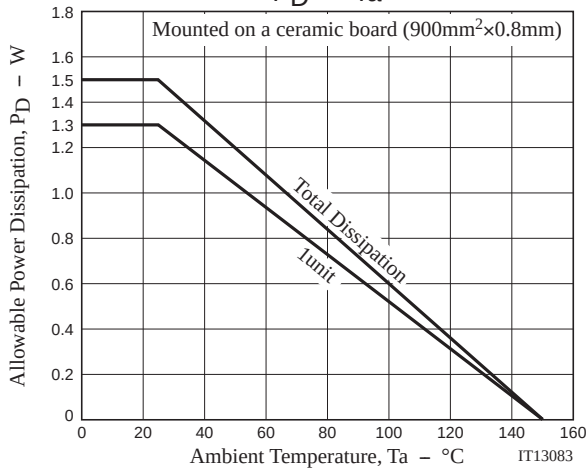
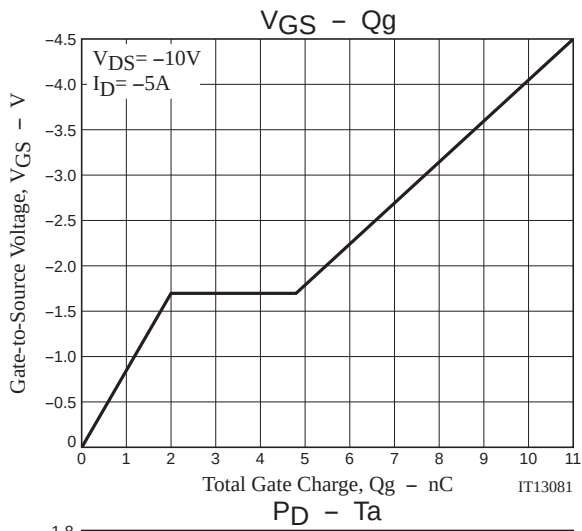
Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
ECH8654-TL-H	ECH8	3,000pcs./reel	Pb Free and Halogen Free





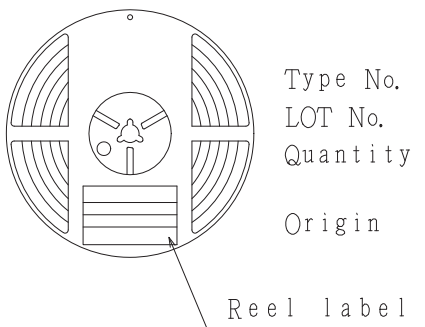
Embossed Taping Specification

ECH8654-TL-H

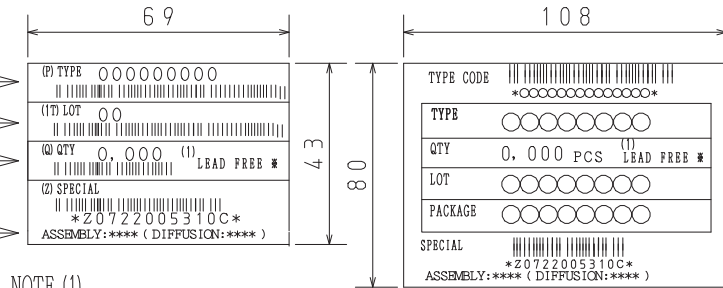
1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
ECH8	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Packing method



Reel label, Inner box label
(unit:mm)



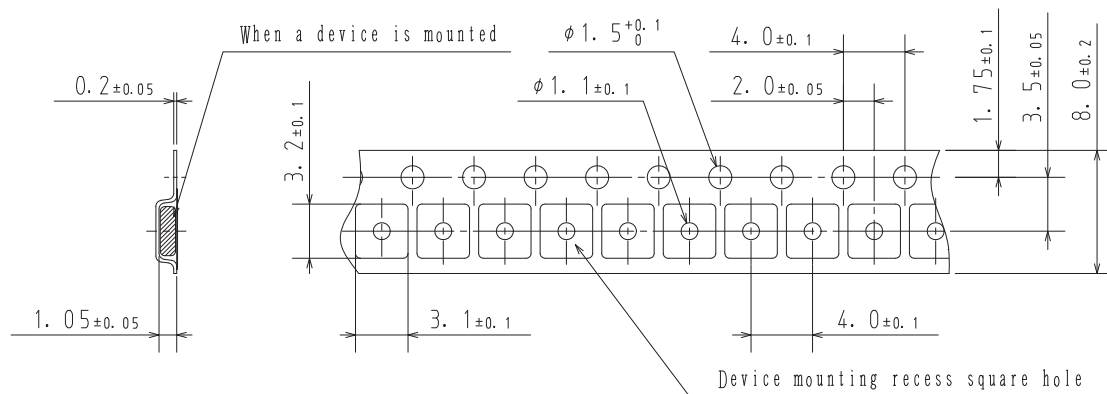
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

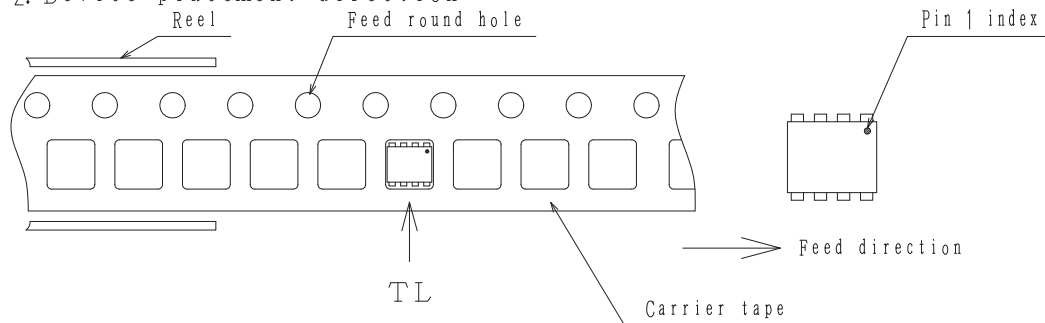
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)

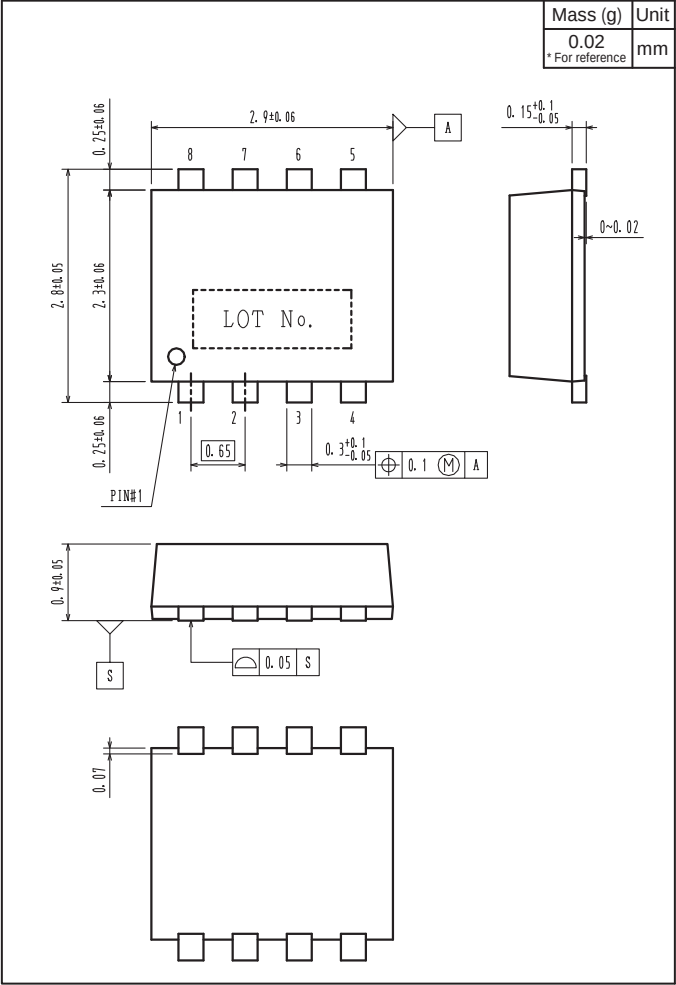


2-2. Device placement direction

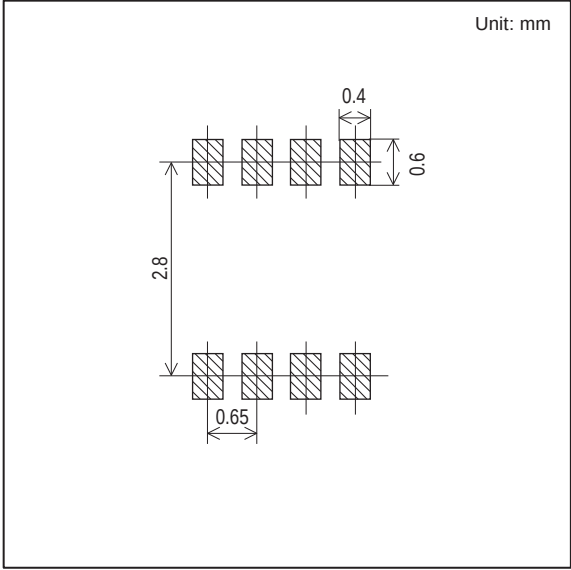


Those with pin 1 index on the feed hole side.....TL

Outline Drawing
ECH8654-TL-H



Land Pattern Example



Note on usage : Since the ECH8654 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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