ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD}, V_{IN} Relative to V_{SS}	-0.3V to +12V
Voltage Range on Any Pin Relative to V_{SS}	-0.3V to +6.0V
Continuous Sink Current, DQ, PIO	20mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CHARACTERISTICS

(V_{DD} = 2.5V to 10V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	+2.5		+10	V
V_{IN} Voltage Range		(Note 1)	-0.3		V_{DD} + 0.3	V
DQ, PIO Voltage Range		(Note 1)	-0.3		+5.5	V
VB Output Voltage	V_{VB}	V_{DD} > 3.0V, I_{VB} = 500µA, (Note 1)	2.5	2.8	3.1	V
OVD Voltage Range		(Note 1)	-0.3		V_{VB} + 0.3	V

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 10V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACTIVE Current	I_{ACTIVE}	I_{VB} = 0		70	95	µA
SLEEP Mode Current	I_{SLEEP}	T_A > +50°C, I_{VB} = 0			10	µA
		I_{VB} = 0, (Note 5)		3	5	
Input Logic-High:DQ, PIO	V_{IH}	(Note 1)	1.5			V
Input Logic-Low: DQ, PIO	V_{IL}	(Note 1)			0.6	V
Output Logic-Low: DQ, PIO	V_{OL}	I_{OL} = 4mA (Note 1)			0.4	V
Pulldown Current: DQ, PIO	I_{PD}	V_{DQ}, V_{PIO} = 0.4V		0.2		µA
Input Logic-High: OVD	V_{IH}	(Note 1)	V_{VB} - 0.2			V
Input Logic-Low: OVD	V_{IL}	(Note 1)			V_{SS} + 0.2	V
V_{IN} Input Resistance	R_{IN}		15			MΩ
DQ Capacitance	C_{DQ}	(Note 4)		50		pF
DQ SLEEP Timeout	t_{SLEEP}	DQ < V_{IL}	1.5	2	2.5	s
Undervoltage SLEEP Threshold	V_{SLEEP}	UVTH = 1, (Note 1)	4.8	4.9	5.0	V
		UVTH = 0, (Note 1)	2.40	2.45	2.50	

ELECTRICAL CHARACTERISTICS: TEMPERATURE, VOLTAGE, CURRENT

(V_{DD} = 2.5V to 10V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Resolution	T_{LSB}			0.125		°C
Temperature Error	T_{ERR}				±3	°C
Voltage Resolution	V_{LSB}			9.76		mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Full-Scale	V_{FS}		0		9.9902	V
Voltage Error	V_{ERR}				±100	mV
Current Resolution	I_{LSB}			1.56		µV
Current Full-Scale	I_{FS}				±51.2	mV
Current Gain Error	I_{GERR}	(Note 2)			±1	% Full-Scale
Current Offset Error	I_{OERR}	0°C ≤ T_A ≤ +70°C, (Note 4)	- 7.82		+ 12.5	µV
Accumulated Current Offset	q_{OERR}	0°C ≤ T_A ≤ +70°C, V_{SNS} = V_{SS} (Notes 3, 4)	- 188		+ 0	µVhr/day
Timebase Error	t_{ERR}	T_A = +25°C, V_{DD} = 7.6V			±1	%
					±2	

ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE, STANDARD

(V_{DD} = 2.5V to 10V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}		60		120	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		60		120	µs
Write-1 Low Time	t_{LOW1}		1		15	µs
Read Data Valid	t_{RDV}				15	µs
Reset Time High	t_{RSTH}		480			µs
Reset Time Low	t_{RSTL}		480		960	µs
Presence Detect High	t_{PDH}		15		60	µs
Presence Detect Low	t_{PDL}		60		240	µs

ELECTRICAL CHARACTERISTICS: 1-Wire INTERFACE, OVERDRIVE

(V_{DD} = 2.5V to 10V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}		6		16	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		6		16	µs
Write-1 Low Time	t_{LOW1}		1		2	µs
Read Data Valid	t_{RDV}				2	µs
Reset-Time High	t_{RSTH}		48			µs
Reset-Time Low	t_{RSTL}		48		80	µs
Presence-Detect High	t_{PDH}		2		6	µs
Presence-Detect Low	t_{PDL}		8		24	µs

EEPROM RELIABILITY SPECIFICATION

(V_{DD} = 2.5V to 10V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

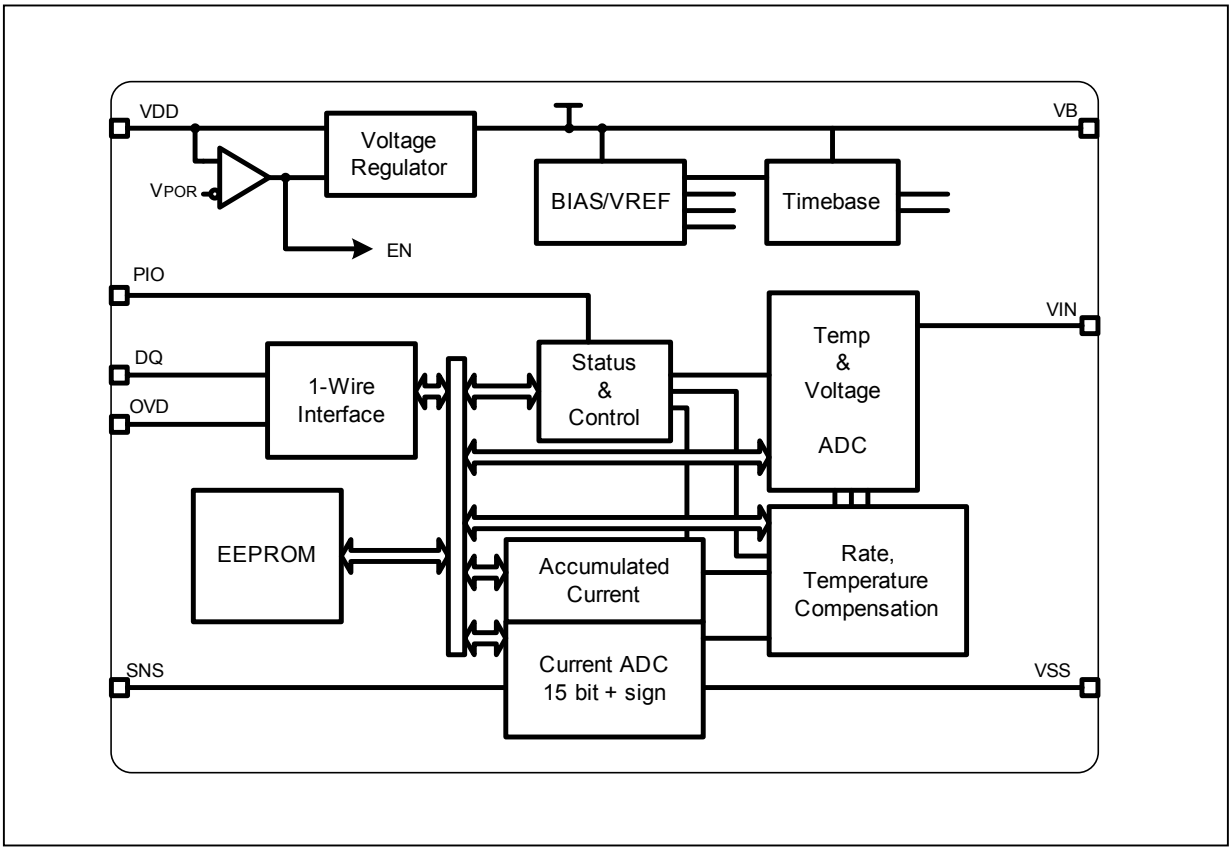
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Copy Time	t_{EEC}				15	ms
EEPROM Copy Endurance	N_{EEC}	T_A = +50°C	50,000			cycles

Note 1: All voltages are referenced to V_{SS}.
Note 2: Factory calibrated accuracy. Higher accuracy can be achieved by in-system calibration by the user.
Note 3: Accumulation Bias register set to 00h. Current Offset Bias register set to 00h. NBEN bit = 0.
Note 4: Parameters guaranteed by design.
Note 5: Internal voltage regulator active.

PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP	TDFN-EP		
1	1	VB	**Internal Supply**. Bypass to V_{SS} with a 0.1µF capacitor.
2	2, 3	V_{SS}	**Device Ground.** Connect directly to the negative terminal of the cell stack. Connect the sense resistor between V_{SS} and SNS.
3	4	V_{IN}	**Voltage Sense Input.** The voltage of the battery pack is monitored through this input pin with respect to the V_{SS} pin.
4	5	V_{DD}	**Power-Supply Input.** Connect to the positive terminal of the battery pack through a decoupling network.
5	6	DQ	**Data Input/Output**. 1-Wire data line. Open-drain output driver. Connect this pin to the DATA terminal of the battery pack. This pin has a weak internal pulldown (I_{PD}) for sensing pack disconnection from host or charger.
6	7	OVD	**1-Wire Bus Speed Control.** Input logic level selects the speed of the 1-Wire bus. Logic 1 selects overdrive (OVD) and logic 0 selects standard timing (STD). On a multidrop bus, all devices must operate at the same speed.
—	8	N.C.	**No Connection**
7	9	SNS	**Sense Resistor Connection.** Connect to the negative terminal of the battery pack. Connect the sense resistor between V_{SS} and SNS.
8	10	PIO	**Programmable I/O Pin.** Can be configured as input or output to monitor or control user-defined external circuitry. Output driver is open drain. This pin has a weak internal pulldown (I_{PD}).
—	EP	EP	**Exposed Pad.** Connect to V_{SS} or leave floating.

Figure 1. Block Diagram



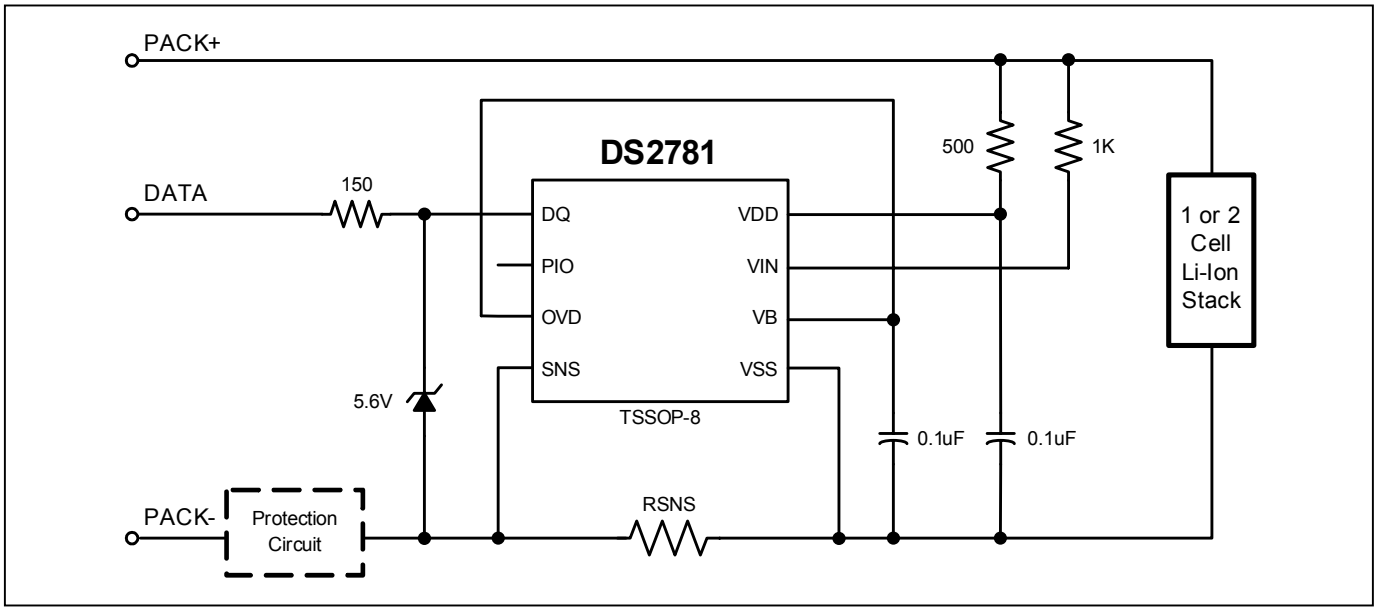
DETAILED DESCRIPTION

The DS2781 operates directly from 2.5V to 10V and supports single or dual cell Lithium-ion battery packs. Nonvolatile storage is provided for cell compensation and application parameters. Host side development of fuel-gauging algorithms is eliminated. On-chip algorithms and convenient status reporting of operating conditions reduce the serial polling required of the host processor.

Additionally, 16 bytes of EEPROM memory are made available for the exclusive use of the host system and/or pack manufacturer. The additional EEPROM memory can be used to facilitate battery lot and date tracking and non-volatile storage of system or battery usage statistics.

A Maxim 1-Wire interface provides serial communication at the standard 16kbps or overdrive 140kbps speeds allows access to data registers, control registers and user memory. A unique, factory programmed 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC) assures that no two parts are alike and enables absolute traceability. The Maxim 1-Wire interface on the DS2781 supports multidrop capability so that multiple slave devices may be addressed with a single pin.

Figure 2. Typical Operating Circuit



POWER MODES

The DS2781 has two power modes: ACTIVE and SLEEP. On initial power up, the DS2781 defaults to ACTIVE mode. While in ACTIVE mode, the DS2781 is fully functional with measurements and capacity estimation continuously updated.

In SLEEP mode, the DS2781 conserves power by disabling measurement and capacity estimation functions, but preserves register contents. SLEEP mode is entered under two different conditions. An enable bit makes entry into SLEEP optional for each condition. The first condition in which SLEEP is entered is a bus low condition. The Power Mode (PMOD) bit must be set to enter SLEEP when a bus low condition occurs. (PMOD = 1 AND BUS_LOW). A bus low condition, where the DQ pin is low for t_{SLEEP} (2s nominal), is used to detect a pack disconnection or system shutdown in which the bus pull-up voltage, V_{PULLUP}, is not present. PMOD type SLEEP assumes that no charge or discharge current will flow and therefore coulomb counting is not necessary. A system with PMOD SLEEP enabled must ensure that a stand-alone or cradle charger includes a pull-up on DQ. The DS2781 transitions from PMOD SLEEP to ACTIVE mode when DQ is pulled high, as would happen when a battery is inserted into a system.

The second condition to enter SLEEP is an under voltage condition (measured on V_{IN}). When the Under Voltage Enable (UVEN) bit is set, the DS2781 will transition to SLEEP if the VIN voltage is less than V_{SLEEP} (Selectable 2.45 or 4.9V). The bus must be in a static state, that is with DQ either high or low for t_{SLEEP}. UVEN SLEEP reduces battery drain due to the DS2781 to prevent over discharge. The DS2781 transitions from UVEN SLEEP to ACTIVE mode when DQ changes logic state. The bus master should initiate communication when charging of a depleted battery begins to ensure that the DS2781 enters ACTIVE mode from UVEN SLEEP.

NOTE: *PMOD and UVEN SLEEP features must be disabled when a battery is charged on an external charger that does not connect to the DQ pin. PMOD SLEEP can be used if the charger pulls DQ high. UVEN SLEEP can be used if the charger toggles DQ. The DS2781 remains in SLEEP and therefore does not measure or accumulate current when a battery is charged on a charger that failures properly drive DQ.*

INITIATING COMMUNICATION IN SLEEP

When beginning communication with a DS2781 in PMOD SLEEP, DQ must be pulled up first and then a 1-Wire Reset pulse must be issued by the master. In UVEN SLEEP, the procedure depends on the state of DQ when UVEN SLEEP was entered. If DQ was low, DQ must be pulled up and then a 1-Wire Reset pulse must be issued by the master as with PMOD SLEEP. If DQ was high when UVEN SLEEP was entered, then the DS2781 is prepared to receive a 1-Wire reset from the master. In the first two cases with DQ low during SLEEP, the DS2781 *does not respond* to the first rising edge of DQ with a presence pulse.

VOLTAGE MEASUREMENT

Battery voltage is measured at the V_{IN} input with respect to V_{SS} over a range of 0V to 9.9902V, with a resolution of 9.76mV. The result is updated every 440ms and placed in the VOLTAGE register in two's complement form. Voltages above the maximum register value are reported at the maximum value; voltages below the minimum register value are reported at the minimum value. The format of the voltage register is shown in Figure 3.

Figure 3. Voltage Register Format

VOLT Read Only

MSB—Address 0Ch							
S	2^9	2^8	2^7	2^6	2^5	2^4	2^3
MSb							LSb

LSB—Address 0Dh							
2^2	2^1	2^0	X	X	X	X	X
MSb							LSb

"S": sign bit(s), "X": reserved

Units: 9.76mV

TEMPERATURE MEASUREMENT

The DS2781 uses an integrated temperature sensor to measure battery temperature with a resolution of 0.125°C. Temperature measurements are updated every 440ms and placed in the temperature register in two's complement form. The format of the temperature register is shown in Figure 4.

Figure 4. Temperature Register Format

TEMP Read Only

MSB—Address 0Ah							
S	2^9	2^8	2^7	2^6	2^5	2^4	2^3
MSb							LSb

LSB—Address 0Bh							
2^2	2^1	2^0	X	X	X	X	X
MSb							LSb

"S": sign bit(s), "X": reserved

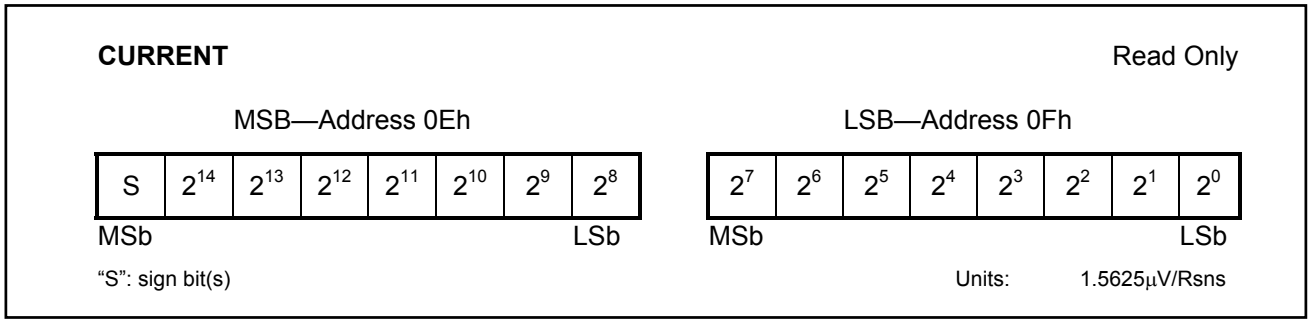
Units: 0.125°C

CURRENT MEASUREMENT

In the ACTIVE mode of operation, the DS2781 continually measures the current flow into and out of the battery by measuring the voltage drop across a low-value current-sense resistor, R_{SNS}. The voltage-sense range between SNS and V_{SS} is ±51.2mV. The input linearly converts peak signal amplitudes up to 102.4mV as long as the continuous signal level (average over the conversion cycle period) does not exceed ±51.2mV. The ADC samples the input differentially at 18.6kHz and updates the Current register at the completion of each conversion cycle.

The Current register is updated every 3.515s with the current conversion result in two's complement form. Charge currents above the maximum register value are reported at the maximum value (7FFFh = +51.2mV). Discharge currents below the minimum register value are reported at the minimum value (8000h = -51.2mV).

Figure 5. Current Register Format



CURRENT RESOLUTION (1 LSB)				
V_{SS} - V_{SNS}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
1.5625µV	78.13µA	104.2µA	156.3µA	312.5µA

CURRENT OFFSET CORRECTION

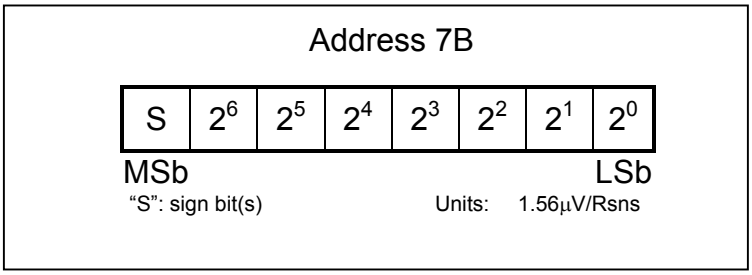
Every 1024th conversion, the ADC measures its input offset to facilitate offset correction. Offset correction occurs approximately once per hour. The resulting correction factor is applied to the subsequent 1023 measurements. During the offset correction conversion, the ADC does not measure the sense resistor signal. A maximum error of 1/1024 in the accumulated current register (ACR) is possible; however, to reduce the error, the current measurement made just prior to the offset conversion is displayed in the current register and is substituted for the dropped current measurement in the current accumulation process. This results in an accumulated current error due to offset correction of less than 1/1024.

CURRENT OFFSET BIAS

The Current Offset Bias (COB) register allows a programmable offset value to be added to raw current measurements. The result of the raw current measurement plus COB is displayed as the current measurement result in the CURRENT register, and is used for current accumulation. COB can be used to correct for a static offset error, or can be used to intentionally skew the current results and therefore the current accumulation.

Read and write access is allowed to COB. Whenever the COB is written, the new value is applied to all subsequent current measurements. COB can be programmed in 1.56µV steps to any value between +198.1µV and -199.7µV. The COB value is stored as a two's complement value in volatile memory, and must be initialized through the interface on power-up.

Figure 6. Current Offset Bias Register Format



CURRENT MEASUREMENT CALIBRATION

The DS2781's current measurement gain can be adjusted through the RSGAIN register, which is factory-calibrated to meet the data sheet specified accuracy. RSGAIN is user accessible and can be reprogrammed after module or pack manufacture to improve the current measurement accuracy. Adjusting RSGAIN can correct for variation in an external sense resistor's nominal value, and allows the use of low-cost, non-precision current sense resistors. RSGAIN is an 11 bit value stored in 2 bytes of the Parameter EEPROM Memory Block. The RSGAIN value adjusts the gain from 0 to 1.999 in steps of 0.001 (precisely 2^{-10}). The user must program RSGAIN cautiously to ensure accurate current measurement. When shipped, the same unique factory gain calibration value is stored in RSGAIN and in a read only location, FSGAIN (B0h and B1h).The original factory gain value can be restored to the device at any time by writing the value of FSGAIN back into RSGAIN.

SENSE RESISTOR TEMPERATURE COMPENSATION

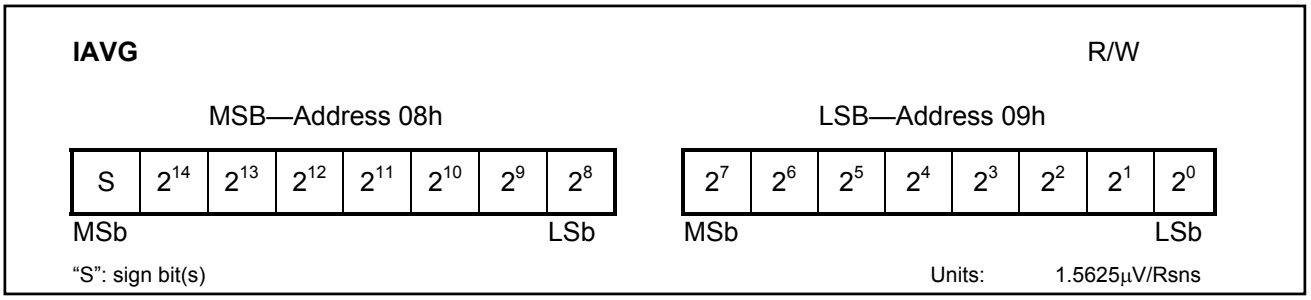
The DS2781 is capable of temperature compensating the current sense resistor to correct for variation in a sense resistor's value over temperature. The DS2781 is factory programmed with the sense resistor temperature coefficient, RSTC, set to zero, which turns off the temperature compensation function. RSTC is user accessible and can be reprogrammed after module or pack manufacture to improve the current accuracy when using a high temperature coefficient current-sense resistor. RSTC is an 8-bit value stored in the Parameter EEPROM Memory Block. The RSTC value sets the temperature coefficient from 0 to +7782ppm/ºC in steps of 30.5ppm/ºC. The user must program RSTC cautiously to ensure accurate current measurement.

Temperature compensation adjustments are made when the Temperature register crosses 0.5°C boundaries. The temperature compensation is most effective with the resistor placed as close as possible to the V_{SS} terminal to optimize thermal coupling of the resistor to the on-chip temperature sensor. If the current shunt is constructed with a copper PCB trace, run the trace under the DS2781 package if possible.

AVERAGE CURRENT MEASUREMENT

The Average Current register reports an average current level over the preceding 28 seconds. The register value is updated every 28s in two's complement form, and is the average of the 8 preceding Current register updates. The format of the Average Current register is shown in Figure 7. Charge currents above the maximum register value are reported at the maximum value (7FFFh = +51.2mV). Discharge currents below the minimum register value are reported at the minimum value (8000h = -51.2mV).

Figure 7. Average Current Register Format



CURRENT ACCUMULATION

Current measurements are internally summed, or accumulated, at the completion of each conversion period with the results displayed in the Accumulated Current Register (ACR). The accuracy of the ACR is dependent on both the current measurement and the conversion time base. The ACR has a range of 0 to 409.6mVh with an LSb of 6.25µVh. Additional read-only registers (ACRL) hold fractional results of each accumulation to avoid truncation errors. Accumulation of charge current above the maximum register value is reported at the maximum register value (7FFFh); conversely, accumulation of discharge current below the minimum register value is reported at the minimum value (8000h).

Read and write access is allowed to the ACR. The ACR must be written MSByte first then LSByte. Whenever the ACR is written, the fractional accumulation result bits are cleared. The write must be completed within 3.515s (one ACR register update period). A write to the ACR forces the ADC to perform an offset correction conversion and

update the internal offset correction factor. Current measurement and accumulation begins with the second conversion following a write to the ACR. Writing ACR clears the fractional values in ACRL. The Format of the ACR register is shown in Figure 8, and the format of ACRL is shown in Figure 9.

In order to preserve the ACR value in case of power loss, the ACR value is backed up to EEPROM. The ACR value is recovered from EEPROM on power-up. See the Memory Map in Table 2 for specific address location and backup frequency.

Figure 8. Accumulated Current Register Format, ACR

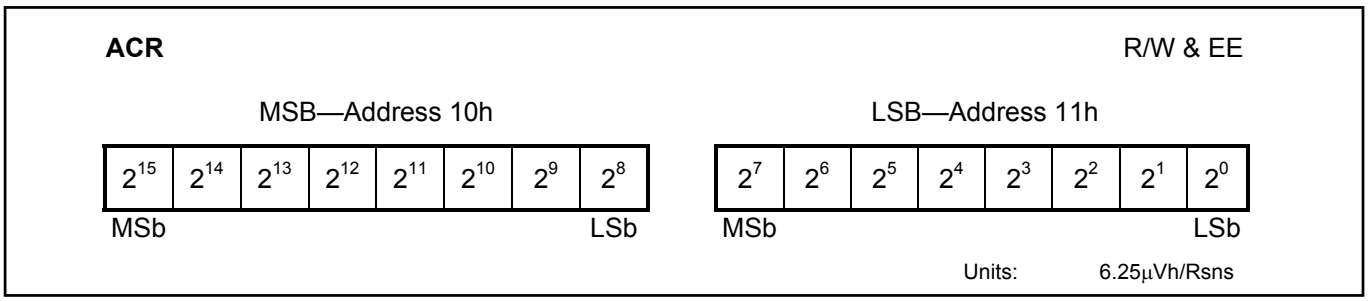
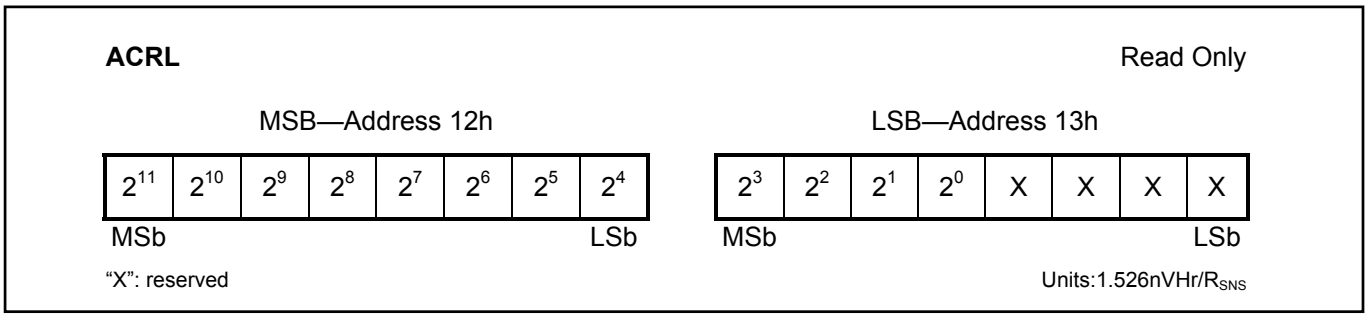


Figure 9. Fractional/Low Accumulated Current Register Format, ACRL



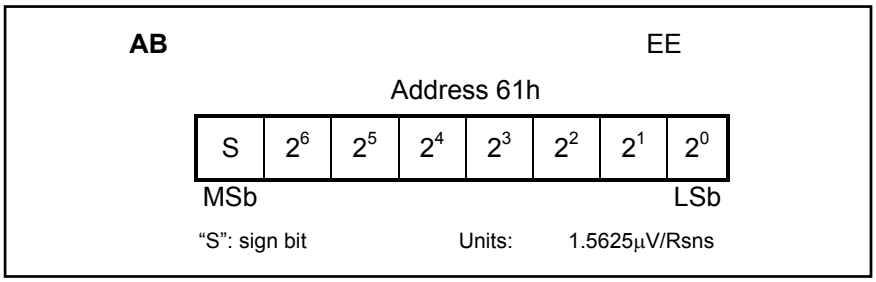
ACR LSb				
V_{SS} - V_{SNS}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
6.25μVh	312.5μAh	416.7μAh	625μAh	1.250mAh

ACR RANGE				
V_{SS} - V_{SNS}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
409.6mVh	20.48Ah	27.30Ah	40.96Ah	81.92Ah

ACCUMULATION BIAS

The Accumulation Bias register (AB) allows an arbitrary bias to be introduced into the current-accumulation process. The AB can be used to account for currents that do not flow through the sense resistor, estimate currents too small to measure, estimate battery self-discharge or correct for static offset of the individual DS2781 device. The AB register allows a user programmed constant positive or negative polarity bias to be included in the current accumulation process. The user-programmed two's complement value, with bit weighting the same as the current register, is added to the ACR once per current conversion cycle. The AB value is loaded on power-up from EEPROM memory. The format of the AB register is shown in Figure 10.

Figure 10. Accumulation Bias Register Formats



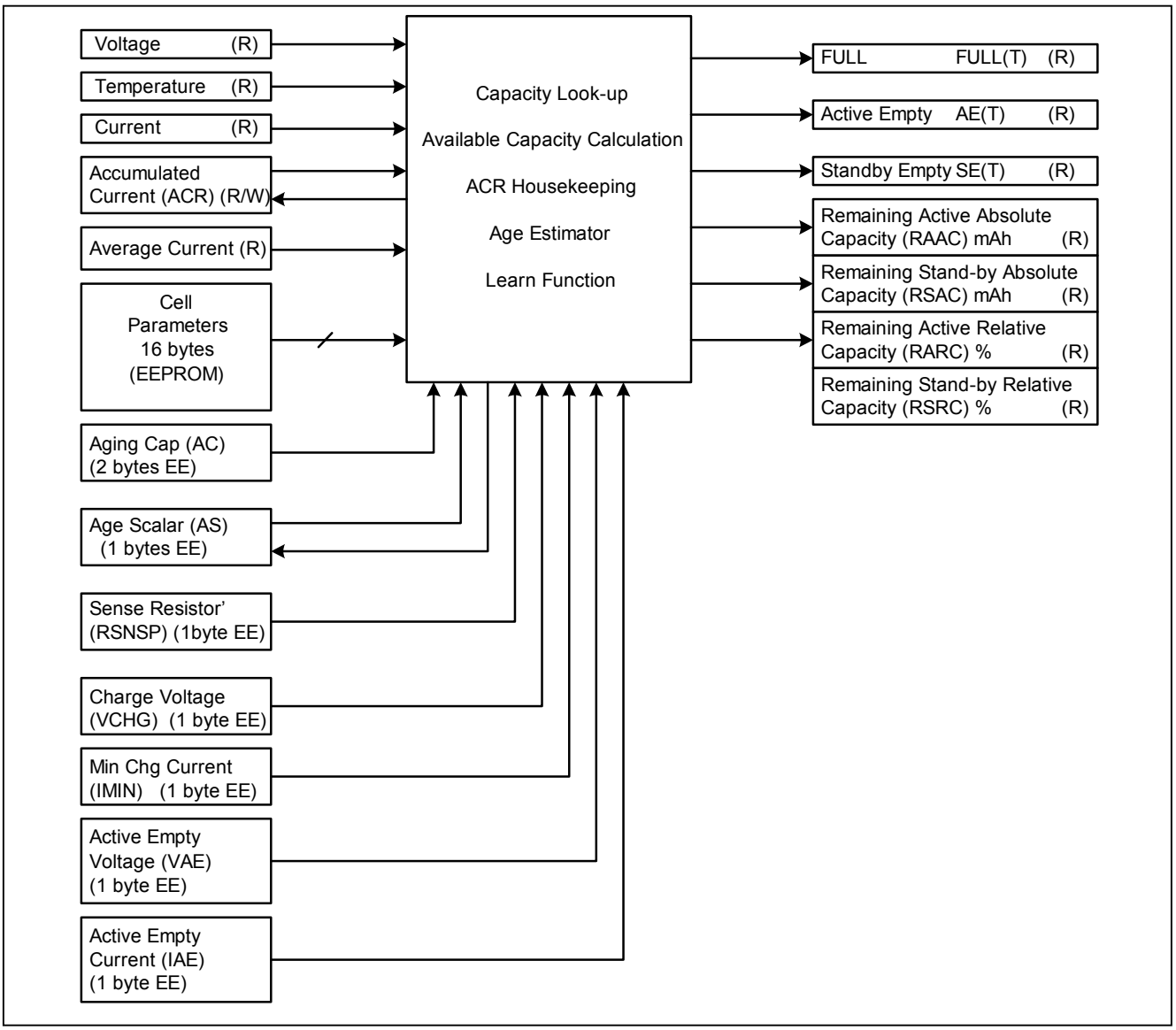
CURRENT BLANKING

The Current Blanking feature modifies current measurement result prior to being accumulated in the ACR. Current Blanking occurs conditionally when a current measurement (raw current + COB) falls in one of two defined ranges. The first range prevents charge currents less than 100µV from being accumulated. The second range prevents discharge currents less than 25µV in magnitude from being accumulated. Charge current blanking is always performed, however, discharge current blanking must be enabled by setting the NBEN bit in the Control register. See the register description for additional information.

CAPACITY ESTIMATION ALGORITHM

Remaining capacity estimation uses real-time measured values and stored parameters describing the cell stack characteristics and application operating limits. The following diagram describes the algorithm inputs and outputs.

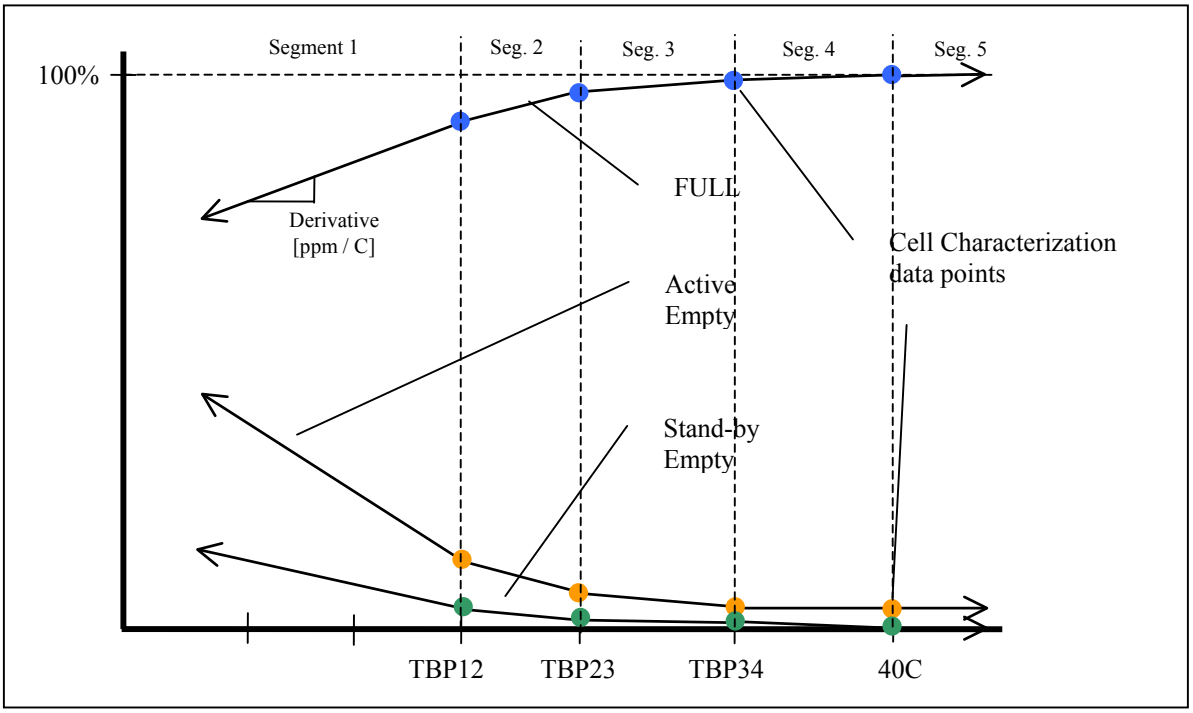
Figure 11. Top-Level Algorithm Diagram



MODELING CELL STACK CHARACTERISTICS

In order to achieve reasonable accuracy in estimating remaining capacity, the cell stack performance characteristics over temperature, load current and charge termination point must be considered. Since the behavior of Li-ion cells is non-linear, these characteristics must be included in the capacity estimation to achieve an acceptable level of accuracy in the capacity estimation. The FuelPack™ method used in the DS2781 is described in general in Application Note AN131: *Lithium-Ion Cell Fuel Gauging with Dallas Semiconductor Battery Monitor ICs*. To facilitate efficient implementation in hardware, a modified version of the method outlined in AN131 is used to store cell characteristics in the DS2781. Full and empty points are retrieved in a look-up process which re-traces piece-wise linear model consisting of three model curves named Full, Active Empty and Stand-by Empty. Each model curve is constructed with 5 line segments, numbered 1 through 5. Above +40°C, the segment 5 model curves extend infinitely with zero slope, approximating the nearly flat change in capacity of Li-Ion cells at temperatures above +40°C. Segment 4 of each model curves originates at +40°C on its upper end and extends downward in temperature to the junction with segment 3. Segment 3 joins with segment 2, which in turn joins with segment 1. Segment 1 of each model curve extends from the junction with segment 2 to infinitely colder temperatures. Segment slopes are stored as µVh ppm change per ºC. The three junctions or breakpoints that join the segments (labeled TBP12, TBP23 and TBP34 in figure 12) are programmable in +1°C increments from -128°C to +40°C. They are stored in two's complement format in locations 0x7C, 0x7D, and 0x7E, respectively. The slope or derivative for segments 1, 2, 3, and 4 are also programmable. One the lower (cold) end of each model curve, segment 1 extends from breakpoint TBP12 to infinitely to colder temperatures.

Figure 12. Cell Model Example Diagram



Full: The Full curve defines how the full point of a given cell stack depends on temperature for a given charge termination. The charge termination method used in the application is used to determine the table values. The DS2781 reconstructs the Full line from cell characteristic table values to determine the Full capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments. Full values are stored as ppm change per ºC. For example if a cell had a nominal capacity of 1051mAh at 40ºC, a full value of 1031mAh at 18ºC (TBP34) and 1009mAh at 0ºC (TBP23), the slope for segment 3 would be:

((1031mAh – 1009mAh) / (1051mAh / 1M)) / (18ºC - 0ºC) = 1163ppm/ºC

1 LSB of the slope registers equals 61ppm so the Full Segment 3 Slope register (location 0x6Dh) would be programmed with a value of 0x13h. Each slope register has a dynamic range 0ppm to 15555ppm.

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Active Empty: The Active Empty curve defines the temperature variation in the empty point of the discharge profile based on a high level load current (one that is sustained during a high power operating mode) and the minimum voltage required for system operation. This load current is programmed as the Active Empty current (IAE), and should be a 3.5s average value to correspond to values read from the Current register, and the specified minimum voltage, or Active Empty voltage (VAE) should be a 250ms average to correspond to values read from the Voltage register. The DS2781 reconstructs the Active Empty line from cell characteristic table values to determine the Active Empty capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments. Active Empty segment slopes are stored the same as described for the Full segments above.

Standby Empty: The Standby Empty curve defines the temperature variation in the empty point in the discharge defined by the application standby current and the minimum voltage required for standby operation. Standby Empty represents the point that the battery can no longer support a subset of the full application operation, such as memory data retention or organizer functions on a wireless handset. Standby Empty segment slopes are stored the same as described for the Full segments above.

The standby load current and voltage are used for determining the cell characteristics but are not programmed into the DS2781. The DS2781 reconstructs the Standby Empty line from cell characteristic table values to determine the Standby Empty capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

CELL STACK MODEL CONSTRUCTION

The model is constructed with all points normalized to the fully charged state at +40°C. Initial values, the +40°C Full value in mVh units and the +40°C Active Empty value as a fraction of the +40°C Full are stored in the cell parameter EEPROM block. Standby Empty at +40°C is by definition zero and therefore no storage is required. The slopes (derivatives) of the 4 segments for each model curve are also stored in the cell parameter EEPROM block along with the break point temperatures of each segment. An example of data stored in this manner is shown in Table 1.

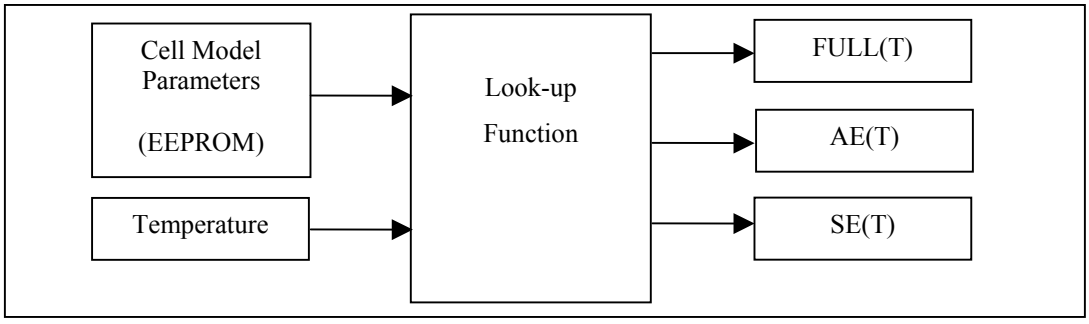
Table 1. Example Cell Characterization Table (Normalized to +40°C)

Manufacturers Rated Cell Capacity: 1000mAh		
Charge Voltage: 8.4V	**Charge Current: 500mA**	**Termination Current: 50mA**
Active Empty (V, I): 6.0V, 300mA	**Standby Empty (V, I): 6.0V, 4mA**	
Sense Resistor: 0.020Ω		

	TBP12	TBP23	TBP34
Segment Break Points	**-12ºC**	**0ºC**	**18ºC**

	+40°C Nominal [mAh]	Seg. 1 ppm/°C	Seg. 2 ppm/°C	Seg. 3 ppm/°C	Seg. 4 ppm/°C
Full	**1051**	**3601**	**3113**	**1163**	**854**
Active Empty		**2380**	**1099**	**671**	**305**
Standby Empty		**1404**	**427**	**244**	**183**

Figure 13. Lookup Function Diagram



APPLICATION PARAMETERS

In addition to cell model characteristics, several application parameters are needed to detect the full and empty points, as well as calculate results in mAh units.

Sense Resistor Prime (RSNSP): RSNSP stores the value of the sense resistor for use in computing the absolute capacity results. The value is stored as a 1-byte conductance value with units of mhos. RSNSP supports resistor values of 1Ω to 3.922mΩ. RSNSP is located in the Parameter EEPROM block.

Charge Voltage (VCHG): VCHG stores the charge voltage threshold used to detect a fully charged state. The value is stored as a 1-byte voltage with units of 39.04mV and can range from 0V to 9.956V. VCHG should be set marginally less than the cell stack voltage at the end of the charge cycle to ensure reliable charge termination detection. VCHG is located in the Parameter EEPROM block.

Minimum Charge Current (IMIN): IMIN stores the charge current threshold used to detect a fully charged state. The value is stored as a 1-byte value with units of 50µV and can range from 0 to 12.75mV. Assuming RSNS = 20mΩ, IMIN can be programmed from 0mA to 637.5mA in 2.5mA steps. IMIN should be set marginally greater than the charge current at the end of the charge cycle to ensure reliable charge termination detection. IMIN is located in the Parameter EEPROM block.

Active Empty Voltage (VAE): VAE stores the voltage threshold used to detect the Active Empty point. The value is stored in 1-byte with units of 39.04mV and can range from 0V to 9.956V. VAE is located in the Parameter EEPROM block. See the *Modeling Cell Stack Characteristics* section for more information.

Active Empty Current (IAE): IAE stores the discharge current threshold used to detect the Active Empty point. The unsigned value represents the magnitude of the discharge current and is stored in 1-byte with units of 200µV and can range from 0 to 51.2mV. Assuming RSNS = 20mΩ, IAE can be programmed from 0mA to 2550mA in 10mA steps. IAE is located in the Parameter EEPROM block. See the *Modeling Cell Stack Characteristics* section for more information.

Aging Capacity (AC): AC stores the rated battery capacity used in estimating the decrease in battery capacity that occurs in normal use. The value is stored in 2-bytes in the same units as the ACR (6.25µVh). Setting AC to the manufacturer's rated capacity sets the aging rate to approximately 2.4% per 100 cycles of equivalent full capacity discharges. Partial discharge cycles are added to form equivalent full capacity discharges. The default estimation results in 88% capacity after 500 equivalent cycles. The estimated aging rate can be adjusted by setting AC to a different value than the cell manufacturer's rating. Setting AC to a lower value, accelerates the estimated aging. Setting AC to a higher value, retards the estimated aging. AC is located in the Parameter EEPROM block.

Age Scalar (AS): AS adjusts the capacity estimation results downward to compensate for cell aging. AS is a 1-byte value that represents values between 49.2% and 100%. The lsb is weighted at 0.78% (precisely 2^{-7}). A value of 100% (128 decimal or 80h) represents an un-aged battery. A value of 95% is recommended as the starting AS value at the time of pack manufacture to allow learning a larger capacity on batteries that have an initial capacity greater than the nominal capacity programmed in the cell characteristic table. AS is modified by the cycle count based age estimation introduced above and by the capacity Learn function. The host system has read and write access to AS, however caution should exercised when writing AS to ensure that the cumulative aging estimate is not overwritten with an incorrect value. Usually, writing AS by the host is not necessary because AS is automatically saved to EEPROM on a periodic basis by the DS2781. (See the *Memory* section for details.) The EEPROM stored value of AS is recalled on power-up.

CAPACITY ESTIMATION UTILITY FUNCTIONS

Aging Estimation

As discussed above, the AS register value is adjusted occasionally based on cumulative discharge. As the ACR register decrements during each discharge cycle, an internal counter is incremented until equal to 32 times AC. AS is then decremented by one, resulting in a decrease in the scaled full battery capacity of 0.78%. Refer to the AC register description above for recommendations on customizing the age estimation rate.

Learn Function

Since Li+ cells exhibit charge efficiencies near unity, the charge delivered to a Li+ cell from a known empty point to a known full point is a dependable measure of the cell capacity. A continuous charge from empty to full results in a "learn cycle". First, the Active Empty point must be detected. The Learn Flag (*LEARNF*) is set at this point. Then, once charging starts, the charge must continue uninterrupted until the battery is charged to full. Upon detecting full, *LEARNF* is cleared, the Charge to Full (*CHGTF*) flag is set and the Age Scalar (AS) is adjusted according to the learned capacity of the cell stack.

ACR Housekeeping

The ACR register value is adjusted occasionally to maintain the coulomb count within the model curve boundaries. When the battery is charged to full (*CHGTF* set), the ACR is set equal to the age scaled full lookup value at the present temperature. If a learn cycle is in progress, correction of the ACR value occurs after the age scalar (AS) is updated.

When an empty condition is detected (*AEF* or *LEARNF* set), the ACR adjustment is conditional. If *AEF* is set and *LEARNF* is not, then the Active Empty Point was not detected and the battery is likely below the Active Empty capacity of the model. The ACR is set to the Active Empty model value only if it is greater than the Active Empty model value. If *LEARNF* is set, then the battery is at the Active Empty Point and the ACR is set to the Active Empty model value.

Full Detect

Full detection occurs when the Voltage (VOLT) readings remain continuously above the VCHG threshold for the period between two Average Current (IAVG) readings, where both IAVG readings are below IMIN. The two consecutive IAVG readings must also be positive and non-zero. This ensures that removing the battery from the charger does not result in a false detection of full. Full Detect sets the Charge to Full (*CHGTF*) bit in the Status register.

Active Empty Point Detect

Active Empty Point detection occurs when the Voltage register drops below the VAE threshold and the two previous Current readings are above IAE. This captures the event of the battery reaching the Active Empty point. Note that the two previous Current readings must be negative and greater in magnitude than IAE, that is, a larger discharge current than specified by the IAE threshold. Qualifying the Voltage level with the discharge rate ensures that the Active Empty point is not detected at loads much lighter than those used to construct the model. Also, Active Empty must not be detected when a deep discharge at a very light load is followed by a load greater than IAE. Either case would cause a learn cycle on the following charge to full to include part of the Standby capacity in the measurement of the Active capacity. Active Empty detection sets the Learn Flag (*LEARNF*) bit in the Status register.

RESULT REGISTERS

The DS2781 processes measurement and cell characteristics on a 440ms interval and yields seven result registers. The result registers are sufficient for direct display to the user in most applications. The host system can produce customized values for system use, or user display by combining measurement, result and User EEPROM values.

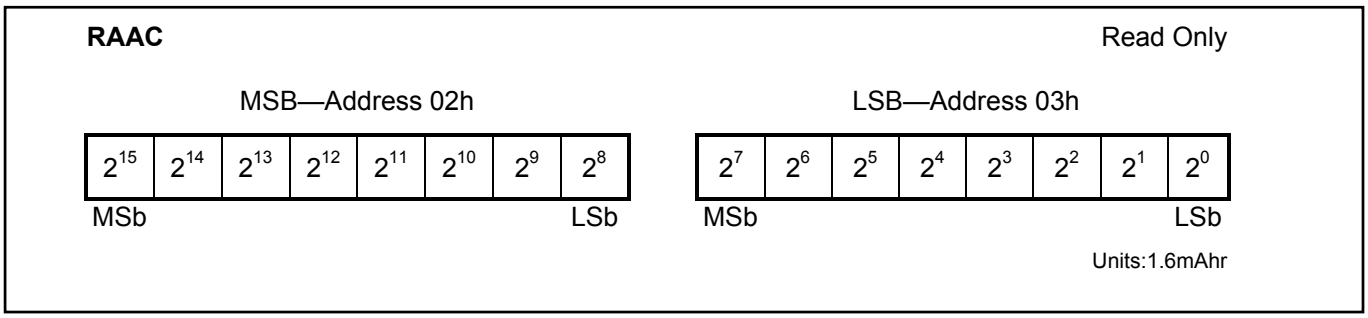
FULL(T) [ ]: The Full capacity of the battery at the present temperature is reported normalized to the 40°C Full value. This 15-bit value reflects the cell stack model Full value at the given temperature. FULL(T) reports values between 100% and 50% with a resolution of 61ppm (precisely 2^{-14}). Though the register format permits values greater than 100%, the register value is clamped to a maximum value of 100%.

Active Empty, AE(T) [ ]: The Active Empty capacity of the battery at the present temperature is reported normalized to the 40°C Full value. This 13-bit value reflects the cell stack model Active Empty at the given temperature. AE(T) reports values between 0% and 49.8% with a resolution of 61ppm (precisely 2^{-14}).

Standby Empty, SE(T) [ ]: The Standby Empty capacity of the battery at the present temperature is reported normalized to the 40°C Full value. This 13-bit value reflects the cell stack model Standby Empty value at the current temperature. SE(T) reports values between 0% and 49.8% with a resolution of 61ppm (precisely 2^{-14}).

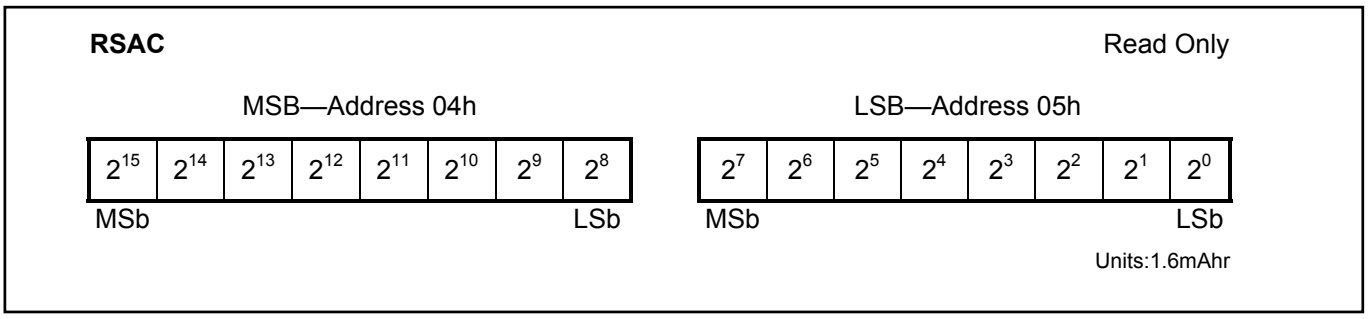
Remaining Active Absolute Capacity (RAAC) [mAh]: RAAC reports the capacity available under the current temperature conditions at the Active Empty discharge rate (IAE) to the Active Empty point in absolute units of milli-amp-hours. RAAC is 16 bits. See Figure 14.

Figure 14. Remaining Active Absolute Capacity Register Format



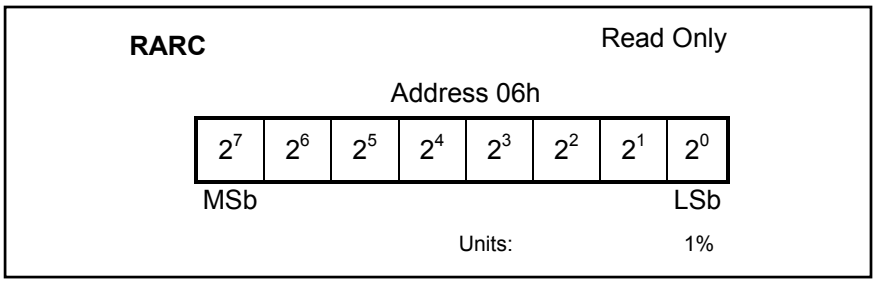
Remaining Standby Absolute Capacity (RSAC) [mAh]: RSAC reports the capacity available under the current temperature conditions at the Standby Empty discharge rate (ISE) to the Standby Empty point capacity in absolute units of milli-amp-hours. RSAC is 16 bits. See Figure 15.

Figure 15. Remaining Standby Absolute Capacity Register Format



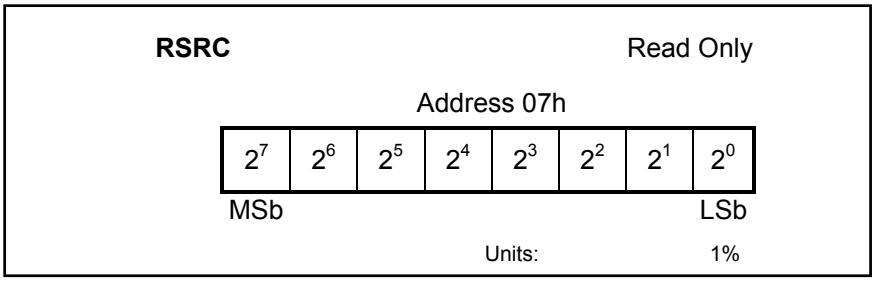
Remaining Active Relative Capacity (RARC) [%]: RARC reports the capacity available under the current temperature conditions at the Active Empty discharge rate (IAE) to the Active Empty point in relative units of percent. RARC is 8 bits. See Figure 16.

Figure 16. Remaining Active Relative Capacity Register Format



Remaining Standby Relative Capacity (RSRC) [%]: RSRC reports the capacity available under the current temperature conditions at the Standby Empty discharge rate (ISE) to the Standby Empty point capacity in relative units of percent. RSRC is 8 bits. See Figure 17.

Figure 17. Remaining Standby Relative Capacity Register Format



Calculation of Results

RAAC [mAh] = (ACR[mVh] - AE(T) * FULL40[mVh]) * RSNSP [mhos]

RSAC [mAh] = (ACR[mVh] - SE(T) * FULL40[mVh]) * RSNSP [mhos]

RARC [%] = 100% * (ACR[mVh] - AE(T) * FULL40[mVh]) /
{(AS * FULL(T) - AE(T)) * FULL40[mVh]}

RSRC [%] = 100%* (ACR[mVh] - SE(T) * FULL40[mVh]) /
{(AS * FULL(T) - SE(T)) * FULL40[mVh]}

STATUS REGISTER

The STATUS register contains bits that report the device status. The bits can be set internally by the DS2781. The CHGTF, AEF, SEF, LEARNF and VER bits are read only bits that can be cleared by hardware. The UVF and PORF bits can only be cleared via the 1-Wire interface.

Figure 18. Status Register Format

ADDRESS	01h		BIT DEFINITION
FIELD	**BIT**	**FORMAT**	**ALLOWABLE VALUES**
CHGTF	7	Read Only	Charge Termination Flag Set to 1 when: (VOLT > VCHG) AND (0 < IAVG < IMIN) continuously for a period between two IAVG register updates (28s to 56s). Cleared to 0 when: RARC < 90%
AEF	6	Read Only	Active Empty Flag Set to 1 when: VOLT < VAE Cleared to 0 when: RARC > 5%
SEF	5	Read Only	Standby Empty Flag Set to 1 when: RSRC < 10% Cleared to 0 when: RSRC > 15%
LEARNF	4	Read Only	Learn Flag—When set to 1, a charge cycle can be used to learn battery capacity. Set to 1 when: (VOLT falls from above VAE to below VAE) AND (CURRENT > IAE) Cleared to 0 when: (CHGTF = 1) OR (CURRENT < 0) OR (ACR = 0 **) OR (ACR written or recalled from EEPROM) OR (SLEEP Entered)
Reserved	3	Read Only	Undefined
UVF	2	Read / Write *	Undervoltage Flag Set to 1 when: VOLT < V_{SLEEP} Cleared to 0 by: User
PORF	1	Read / Write *	Power-On Reset Flag—Useful for reset detection, see text below. Set to 1 upon Power-Up by hardware. Cleared to 0 by: User
Reserved	0	Read Only	Undefined

* - This bit can be set by the DS2781, and may only be cleared through the 1-Wire interface.
** - LEARNF is only cleared if ACR reaches 0 after VOLT < VAE.

CONTROL REGISTER

All CONTROL register bits are read and write accessible. The CONTROL register is recalled from Parameter EEPROM memory at power-up. Register bit values can be modified in shadow RAM after power-up. Shadow RAM values can be saved as the power up default values by using the Copy Data command.

Figure 19. Control Register Format

ADDRESS 60h			BIT DEFINITION
FIELD	**BIT**	**FORMAT**	**ALLOWABLE VALUES**
NBEN	7	Read/Write	Negative Blanking Enable 0: Allows negative current readings to always be accumulated 1: Enables blanking of negative current readings up to -25µV
UVEN	6	Read/Write	Under Voltage SLEEP Enable 0: Disables transition to SLEEP mode based on V_{IN} voltage 1: Enables transition to SLEEP mode if, $V_{IN} < V_{SLEEP}$ AND DQ stable at either logic level for t_{SLEEP}
PMOD	5	Read/Write	Power Mode Enable 0: Disables transition to SLEEP mode based on DQ logic state 1: Enables transition to SLEEP mode if DQ at a logic-low for t_{SLEEP}
RNAOP	4	Read/Write	Read Net Address Opcode 0: Read Net Address Command = 33h 1: Read Net Address Command = 39h
UVTH	3	Read/Write	Under Voltage Threshold Select 0: Selects an Under Voltage Sleep threshold of 2.45V 1: Selects an Under Voltage Sleep threshold of 4.9V
Reserved	0:2	—	Undefined

SPECIAL FEATURE REGISTER

All Special Feature Register bits are read and write accessible, with default values specified in each bit definition.

Figure 20. Special Feature Register Format

ADDRESS 15h			BIT DEFINITION
FIELD	**BIT**	**FORMAT**	**ALLOWABLE VALUES**
Reserved	1:7	—	Undefined
PIOSC	0	Read/Write	PIO Sense and Control Read values 0: PIO pin ≤ Vil 1: PIO pin ≥ Vih Write values 0: Activates PIO pin open-drain output driver, forcing the PIO pin low 1: Disables the output driver, allowing the PIO pin to be pulled high or used as an input Power-up and SLEEP mode default: 1 (PIO pin is hi-Z) Note: PIO pin has weak pulldown

EEPROM REGISTER

The EEPROM register provides access control of the EEPROM blocks. EEPROM blocks can be locked to prevent alteration of data within the block. Locking a block disables write access to the block. Once a block is locked, it cannot be unlocked. Read access to EEPROM blocks is unaffected by the lock/unlock status.

Figure 21. EEPROM Register Format

ADDRESS	1Fh		BIT DEFINITION
FIELD	**BIT**	**FORMAT**	**ALLOWABLE VALUES**
EEC	7	Read Only	EEPROM Copy Flag Set to 1 when: Copy Data command executed Cleared to 0 when: Copy Data command completes Note: While EEC = 1, writes to EEPROM addresses are ignored Power-up default: 0
LOCK	6	Read / Write to 1	EEPROM Lock Enable Host write to 1: Enables the Lock command. Host must issue Lock command as next command after writing Lock Enable bit to 1. Cleared to 0 when: Lock command completes or when Lock command not the command issued immediately following the Write command used to set the Lock Enable bit. Power-up default: 0
Reserved	2:6	—	Undefined
BL1	1	Read Only	EEPROM Block 1 Lock Flag (Parameter EEPROM 60h–7Fh) 0: EEPROM is not locked 1: EEPROM block is locked Factory default: 0
BL0	0	Read Only	EEPROM Block 0 Lock Flag (User EEPROM 20h–2Fh) 0: EEPROM is not locked 1: EEPROM block is locked Factory default: 0

MEMORY

The DS2781 has a 256 byte linear memory space with registers for instrumentation, status, and control, as well as EEPROM memory blocks to store parameters and user information. Byte addresses designated as “Reserved” return undefined data when read. Reserved bytes should not be written. Several byte registers are paired into two-byte registers in order to store 16-bit values. The most significant byte (MSB) of the 16 bit value is located at a even address and the least significant byte (LSB) is located at the next address (odd) byte. When the MSB of a two-byte register is read, the MSB and LSB are latched simultaneously and held for the duration of the Read Data command to prevent updates to the LSB during the read. This ensures synchronization between the two register bytes. For consistent results, always read the MSB and the LSB of a two-byte register during the same Read Data command sequence.

EEPROM memory consists of the non-volatile EEPROM cells overlaid with volatile shadow RAM. The Read Data and Write Data commands allow the 1-Wire interface to directly accesses only the shadow RAM. The Copy Data and Recall Data function commands transfer data between the shadow RAM and the EEPROM cells. In order to modify the data stored in the EEPROM cells, data must be written to the shadow RAM and then copied to the EEPROM. In order to verify the data stored in the EEPROM cells, the EEPROM data must be recalled to the shadow RAM and then read from the shadow RAM.

USER EEPROM

A 16 byte User EEPROM memory (block 0, addresses 20h–2Fh) provides non-volatile memory that is uncommitted to other DS2781 functions. Accessing the User EEPROM block does not affect the operation of the DS2781. User EEPROM is lockable, and once locked, write access is not allowed. The battery pack or host system manufacturer can program lot codes, date codes and other manufacturing, warranty, or diagnostic information and then lock it to safeguard the data. User EEPROM can also store parameters for charging to support different size batteries in a host device as well as auxiliary model data such as time to full charge estimation parameters.

PARAMETER EEPROM

Model data for the cells, as well as application operating parameters are stored in the Parameter EEPROM memory (block 1, addresses 60h–7Fh). The **ACR** (MSB and LSB) and **AS** registers are automatically saved to EEPROM when the **RARC** result crosses 4% boundaries. This allows the DS2781 to be located outside the protection FETs. In this manner, if a protection device is triggered, the DS2781 cannot lose more that 4% of charge or discharge data.

Table 2. Memory Map

ADDRESS (HEX)	DESCRIPTION	READ/WRITE
00	Reserved	R
01	**STATUS** - Status Register	R/W
02	**RAAC** - Remaining Active Absolute Capacity MSB	R
03	**RAAC** - Remaining Active Absolute Capacity LSB	R
04	**RSAC** - Remaining Standby Absolute Capacity MSB	R
05	**RSAC** - Remaining Standby Absolute Capacity LSB	R
06	**RARC** - Remaining Active Relative Capacity	R
07	**RSRC** - Remaining Standby Relative Capacity	R
08	**IAVG** - Average Current Register MSB	R
09	**IAVG** - Average Current Register LSB	R
0A	**TEMP** - Temperature Register MSB	R
0B	**TEMP** - Temperature Register LSB	R
0C	**VOLT** - Voltage Register MSB	R
0D	**VOLT** - Voltage Register LSB	R
0E	**CURRENT** - Current Register MSB	R
0F	**CURRENT** - Current Register LSB	R
10	**ACR** - Accumulated Current Register MSB	R/W*
11	**ACR** - Accumulated Current Register LSB	R/W *
12	**ACRL** – Low Accumulated Current Register MSB	R
13	**ACRL** – Low Accumulated Current Register LSB	R
14	**AS** - Age Scalar	R/W *
15	**SFR** - Special Feature Register	R/W
16	**FULL** - Full Capacity MSB	R
17	**FULL** - Full Capacity LSB	R
18	**AE** - Active Empty MSB	R
19	**AE** - Active Empty LSB	R
1A	**SE** - Standby Empty MSB	R
1B	**SE** - Standby Empty LSB	R
1C to 1E	Reserved	—
1F	**EEPROM** - EEPROM Register	R/W
20 to 2F	User EEPROM, Lockable, Block 0	R/W
30 to 5F	Reserved	—
60 to 7F	Parameter EEPROM, Lockable, Block 1	R/W
80 to AF	Reserved	—
B0 to B1	FSGAIN – Factory Gain Calibration Value	R
B2 to FF	Reserved	—

**Register value is automatically saved to EEPROM during ACTIVE mode operation and recalled from EEPROM on power-up.*

Table 3. Parameter EEPROM Memory Block 1

ADDRESS (HEX)	DESCRIPTION	ADDRESS (HEX)	DESCRIPTION
60	**CONTROL** - Control Register	70	AE Segment 4 Slope
61	**AB** - Accumulation Bias	71	AE Segment 3 Slope
62	**AC** - Aging Capacity MSB	72	AE Segment 2 Slope
63	**AC** - Aging Capacity LSB	73	AE Segment 1 Slope
64	**VCHG** - Charge Voltage	74	SE Segment 4 Slope
65	**IMIN** - Minimum Charge Current	75	SE Segment 3 Slope
66	**VAE** - Active Empty Voltage	76	SE Segment 2 Slope
67	**IAE** - Active Empty Current	77	SE Segment 1 Slope
68	Active Empty 40	78	**RSGAIN** - Sense Resistor Gain MSB
69	**RSNSP** - Sense Resistor Prime	79	**RSGAIN** - Sense Resistor Gain LSB
6A	Full 40 MSB	7A	**RSTC** - Sense Resistor Temp. Coeff.
6B	Full 40 LSB	7B	**COB** – Current Offset Bias
6C	Full Segment 4 Slope	7C	**TBP34**
6D	Full Segment 3 Slope	7D	**TBP23**
6E	Full Segment 2 Slope	7E	**TBP12**
6F	Full Segment 1 Slope	7F	Reserved

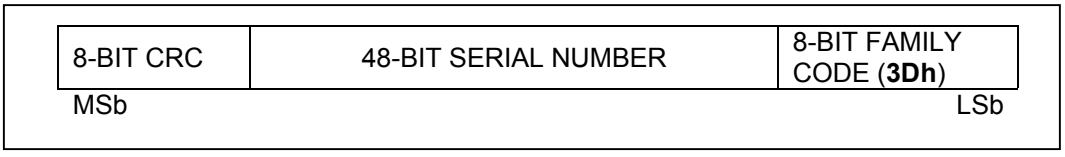
1-Wire BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. A multidrop bus is a 1-Wire bus with multiple slaves. A single-drop bus has only one slave device. In all instances, the DS2781 is a slave device. The bus master is typically a microprocessor in the host system. The discussion of this bus system consists of four topics: 64-bit net address, hardware configuration, transaction sequence, and 1-Wire signaling.

64-BIT NET ADDRESS

Each DS2781 has a unique, factory-programmed 1-Wire net address that is 64 bits in length. The first eight bits are the 1-Wire family code (**3Dh** for DS2781). The next 48 bits are a unique serial number. The last eight bits are a cyclic redundancy check (CRC) of the first 56 bits (see Figure 22). The 64-bit net address and the 1-Wire I/O circuitry built into the device enable the DS2781 to communicate through the 1-Wire protocol detailed in the *1-Wire Bus System* section.

Figure 22. 1-Wire Net Address Format



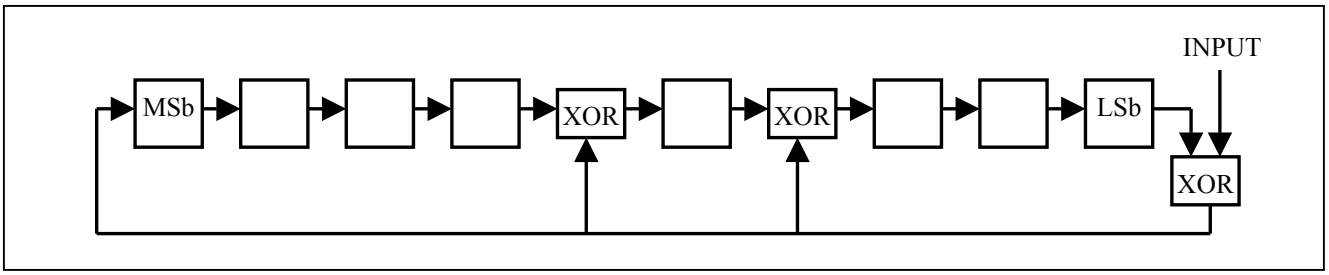
CRC GENERATION

The DS2781 has an 8-bit CRC stored in the most significant byte of its 1-Wire net address. To ensure error-free transmission of the address, the host system can compute a CRC value from the first 56 bits of the address and compare it to the CRC from the DS2781. The host system is responsible for verifying the CRC value and taking action as a result. The DS2781 does not compare CRC values and does not prevent a command sequence from proceeding as a result of a CRC mismatch. Proper use of the CRC can result in a communication channel with a very high level of integrity.

The CRC can be generated by the host using a circuit consisting of a shift register and XOR gates as shown in Figure 23, or it can be generated in software. Additional information about the 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products*.

In the circuit in Figure 23, the shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value.

Figure 23. 1-Wire CRC Generation Block Diagram



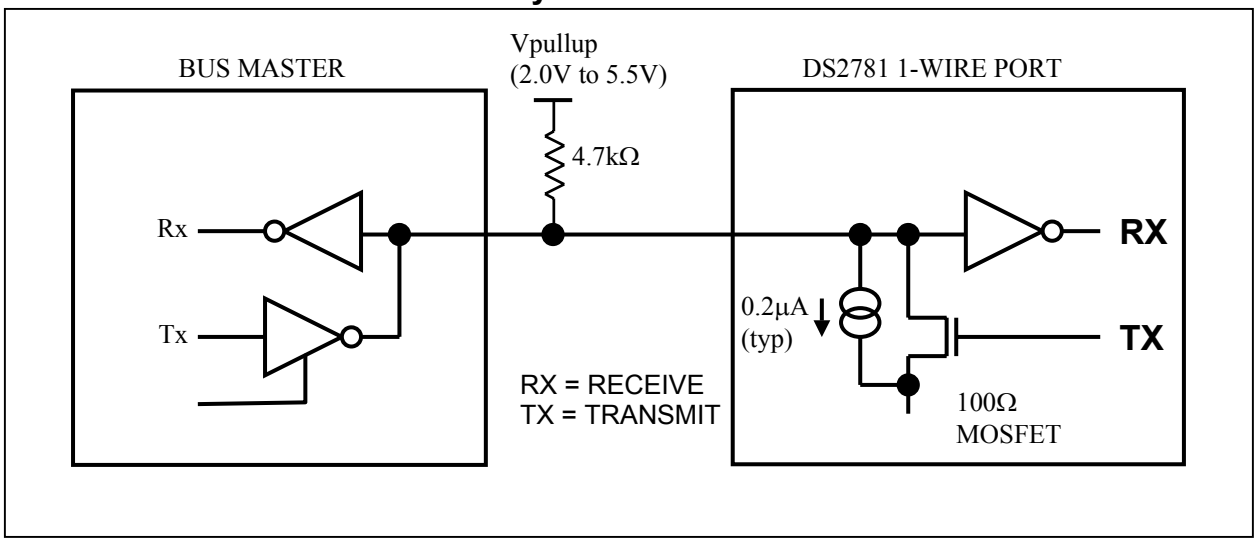
HARDWARE CONFIGURATION

Because the 1-Wire bus has only a single line, it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus with open-drain or tri-state output drivers. The DS2781 uses an open-drain output driver as part of the bidirectional interface circuitry shown in Figure 24. If a bidirectional pin is not available on the bus master, separate output and input pins can be connected together.

The 1-Wire bus must have a pullup resistor at the bus-master end of the bus. For short line lengths, the value of this resistor should be approximately 5kΩ. The idle state for the 1-Wire bus is high. If, for any reason, a bus transaction must be suspended, the bus must be left in the idle state to properly resume the transaction later. If the bus is left low for more than 120µs (16µs for overdrive speed), slave devices on the bus begin to interpret the low period as a reset pulse, effectively terminating the transaction.

The DS2781 can operate in two communication speed modes, standard and overdrive. The speed mode is determined by the input logic level of the OVD pin with a logic 0 selecting standard speed and a logic 1 selecting overdrive speed. The OVD pin must be at a stable logic level of 0 or 1 before initializing a transaction with a reset pulse. All 1-Wire devices on a multinode bus must operate at the same communication speed for proper operation. 1-Wire timing for both standard and overdrive speeds are listed in the *Electrical Characteristics: 1-Wire Interface* tables.

Figure 24. 1-Wire Bus Interface Circuitry



TRANSACTION SEQUENCE

The protocol for accessing the DS2781 through the 1-Wire port is as follows:

- Initialization
- Net Address Command
- Function Command
- Transaction/Data

The sections that follow describe each of these steps in detail.

All transactions of the 1-Wire bus begin with an initialization sequence consisting of a reset pulse transmitted by the bus master followed by a presence pulse simultaneously transmitted by the DS2781 and any other slaves on the bus. The presence pulse tells the bus master that one or more devices are on the bus and ready to operate. For more details, see the *1-Wire Signaling* section.

NET ADDRESS COMMANDS

Once the bus master has detected the presence of one or more slaves, it can issue one of the net address commands described in the following paragraphs. The name of each ROM command is followed by the 8-bit opcode for that command in square brackets. Figure 25 presents a transaction flowchart of the net address commands.

Read Net Address [33h or 39h]. This command allows the bus master to read the DS2781's 1-Wire net address. This command can only be used if there is a single slave on the bus. If more than one slave is present, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The RNAOP bit in the status register selects the opcode for this command, with RNAOP = 0 indicating 33h, and RNAOP = 1 indicating 39h.

Match Net Address [55h]. This command allows the bus master to specifically address one DS2781 on the 1-Wire bus. Only the addressed DS2781 responds to any subsequent function command. All other slave devices ignore the function command and wait for a reset pulse. This command can be used with one or more slave devices on the bus.

Skip Net Address [CCh]. This command saves time when there is only one DS2781 on the bus by allowing the bus master to issue a function command without specifying the address of the slave. If more than one slave device is present on the bus, a subsequent function command can cause a data collision when all slaves transmit data at the same time.

Search Net Address [F0h]. This command allows the bus master to use a process of elimination to identify the 1-Wire net addresses of all slave devices on the bus. The search process involves the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit location of the net address. After one complete pass through all 64 bits, the bus master knows the address of one device. The remaining devices can then be identified on additional iterations of the process. See Chapter 5 of the *Book of DS19xx iButton Standards* for a comprehensive discussion of a net address search, including an actual example (www.maxim-ic.com/ibuttonbook).

Resume [A5h]. This command increases data throughput in multidrop environments where the DS2781 needs to be accessed several times. Resume is similar to the Skip Net Address command in that the 64-bit net address does not have to be transmitted each time the DS2781 is accessed. After successfully executing a Match Net Address command or Search Net Address command, an internal flag is set in the DS2781. When the flag is set, the DS2781 can be repeatedly accessed through the Resume command function. Accessing another device on the bus clears the flag, thus preventing two or more devices from simultaneously responding to the Resume command function.

FUNCTION COMMANDS

After successfully completing one of the net address commands, the bus master can access the features of the DS2781 with any of the function commands described in the following paragraphs. The name of each function is followed by the 8-bit opcode for that command in square brackets. The function commands are summarized in Table 4.

Read Data [69h, XX]. This command reads data from the DS2781 starting at memory address XX. The LSb of the data in address XX is available to be read immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is received, the LSb of the data at address XX + 1 is available to be read immediately after the MSb of the data at address XX. If the bus master continues to read beyond address FFh, data is read starting at memory address 00 and the address is automatically incremented until a reset pulse occurs. Addresses labeled “Reserved” in the memory map contain undefined data values. The Read Data command can be terminated by the bus master with a reset pulse at any bit boundary. Reads from EEPROM block addresses return the data in the shadow RAM. A Recall Data command is required to transfer data from the EEPROM to the shadow. See the *Memory* section for more details.

Write Data [6Ch, XX]. This command writes data to the DS2781 starting at memory address XX. The LSb of the data to be stored at address XX can be written immediately after the MSb of address has been entered. Because the address is automatically incremented after the MSb of each byte is written, the LSb to be stored at address XX + 1 can be written immediately after the MSb to be stored at address XX. If the bus master continues to write beyond address FFh, the data starting at address 00 is overwritten. Writes to read-only addresses, reserved addresses and locked EEPROM blocks are ignored. Incomplete bytes are not written. Writes to unlocked EEPROM block addresses modify the shadow RAM. A Copy Data command is required to transfer data from the shadow to the EEPROM. See the *Memory* section for more details.

Copy Data [48h, XX]. This command copies the contents of the EEPROM shadow RAM to EEPROM cells for the EEPROM block containing address XX. Copy data commands that address locked blocks are ignored. While the copy data command is executing, the EEC bit in the EEPROM register is set to 1 and writes to EEPROM addresses are ignored. Reads and writes to non-EEPROM addresses can still occur while the copy is in progress. The copy data command takes t_{EEC} time to execute, starting on the next falling edge after the address is transmitted.

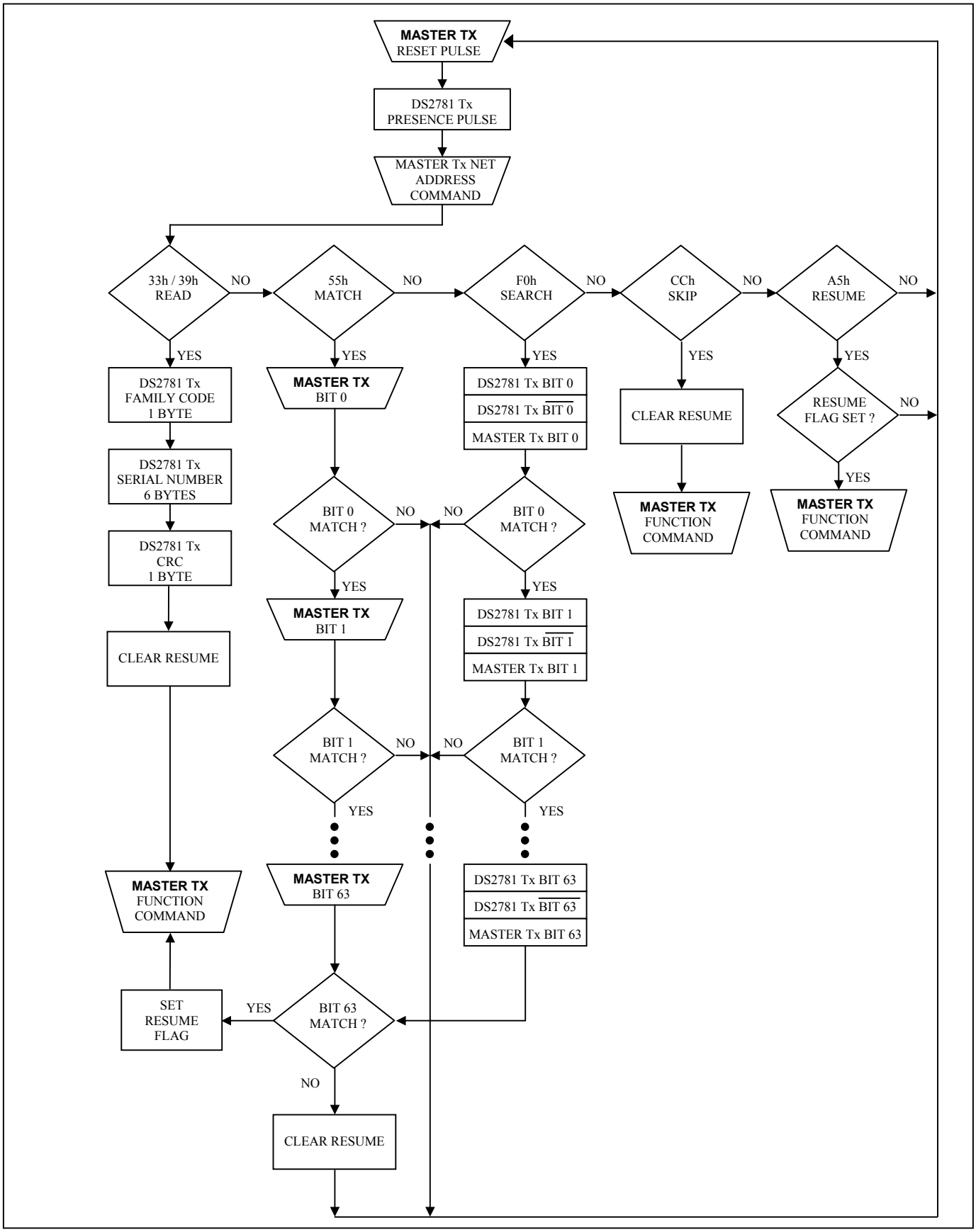
Recall Data [B8h, XX]. This command recalls the contents of the EEPROM cells to the EEPROM shadow memory for the EEPROM block containing address XX.

Lock [6Ah, XX]. This command locks (write-protects) the block of EEPROM memory containing memory address XX. The LOCK bit in the EEPROM register must be set to 1 before the lock command is executed. To help prevent unintentional locks, one must issue the lock command immediately after setting the LOCK bit (EEPROM register, address 1Fh, bit 06) to a 1. If the LOCK bit is 0 or if setting the lock bit to 1 does not immediately precede the lock command, the lock command has no effect. The lock command is permanent; a locked block can never be written again.

Table 4. Function Commands

COMMAND	DESCRIPTION	COMMAND PROTOCOL	BUS STATE AFTER COMMAND PROTOCOL	BUS DATA
Read Data	Reads data from memory starting at address XX	69h, XX	Master Rx	Up to 256 bytes of data
Write Data	Writes data to memory starting at address XX	6Ch, XX	Master Tx	Up to 256 bytes of data
Copy Data	Copies shadow RAM data to EEPROM block containing address XX	48h, XX	Master Reset	None
Recall Data	Recalls EEPROM block containing address XX to RAM	B8h, XX	Master Reset	None
Lock	Permanently locks the block of EEPROM containing address XX	6Ah, XX	Master Reset	None

Figure 25. Net Address Command Flowchart

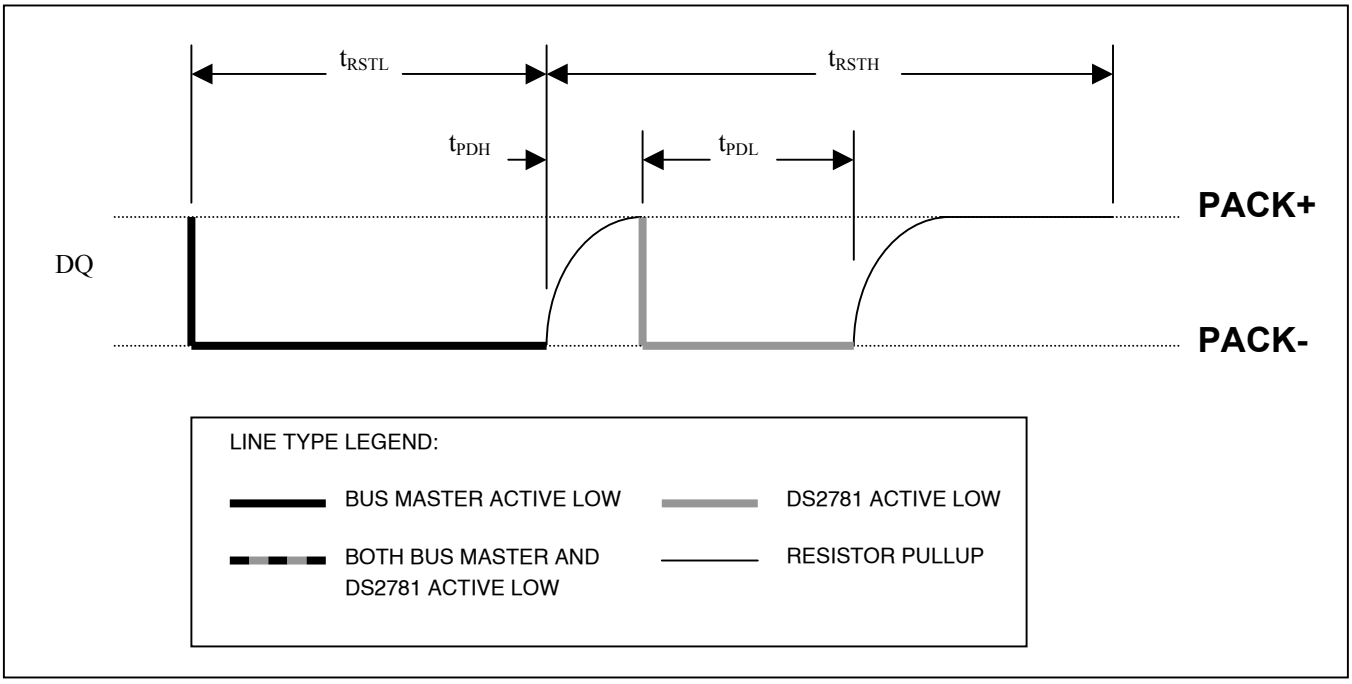


1-Wire SIGNALING

The 1-Wire bus requires strict signaling protocols to ensure data integrity. The four protocols used by the DS2781 are as follows: the initialization sequence (reset pulse followed by presence pulse), write 0, write 1, and read data. All of these types of signaling except the presence pulse are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2781 is shown in Figure 26. A presence pulse following a reset pulse indicates that the DS2781 is ready to accept a net address command. The bus master transmits (Tx) a reset pulse for t_{RSTL}. The bus master then releases the line and goes into receive mode (Rx). The 1-Wire bus line is then pulled high by the pullup resistor. After detecting the rising edge on the DQ pin, the DS2781 waits for t_{PDH} and then transmits the presence pulse for t_{PDL}.

Figure 26. 1-Wire Initialization Sequence



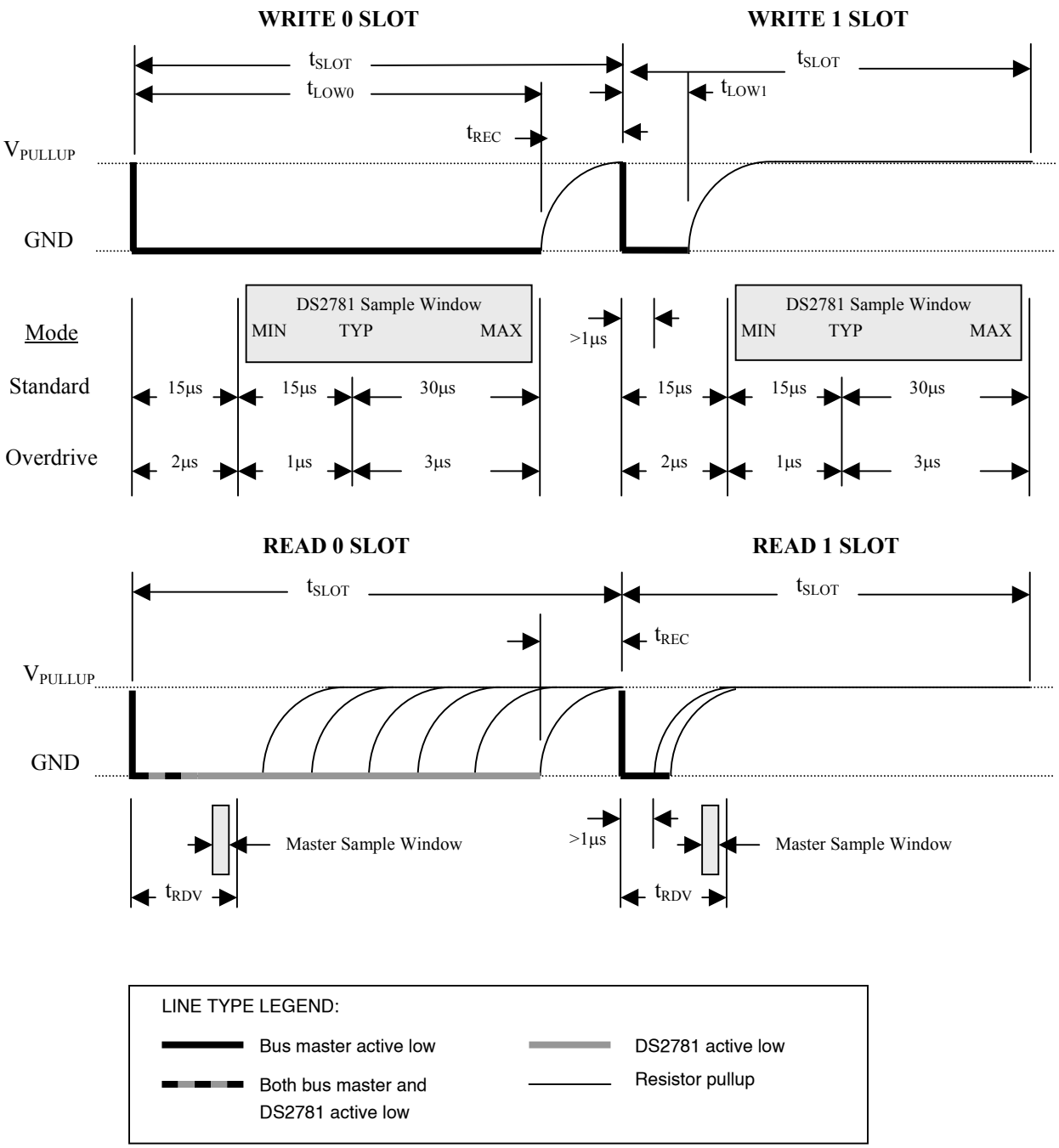
WRITE-TIME SLOTS

A write-time slot is initiated when the bus master pulls the 1-Wire bus from a logic-high (inactive) level to a logic-low level. There are two types of write-time slots: write 1 and write 0. All write-time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles. The DS2781 samples the 1-Wire bus line between 15µs and 60µs (between 2µs and 6µs for overdrive speed) after the line falls. If the line is high when sampled, a write 1 occurs. If the line is low when sampled, a write 0 occurs (see Figure 27). For the bus master to generate a write 1 time slot, the bus line must be pulled low and then released, allowing the line to be pulled high within 15µs (2µs for overdrive speed) after the start of the write-time slot. For the host to generate a write 0 time slot, the bus line must be pulled low and held low for the duration of the write-time slot.

READ-TIME SLOTS

A read-time slot is initiated when the bus master pulls the 1-Wire bus line from a logic-high level to a logic-low level. The bus master must keep the bus line low for at least 1µs and then release it to allow the DS2781 to present valid data. The bus master can then sample the data t_{RDV} from the start of the read-time slot. By the end of the read-time slot, the DS2781 releases the bus line and allows it to be pulled high by the external pullup resistor. All read-time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles. See Figure 27 for more information.

Figure 27. 1-Wire Write- and Read-Time Slots



PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 TSSOP	—	56-G2021-000
10 TDFN-EP	—	56-G0012-001

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
062708	Added Figures 14 to 17 for the RAAC, RSAC, RARC, and RSRC descriptions.	17, 18
	Added *Package Information* table.	30

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