ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to +6.0V
Operating Temperature Range (Noncondensing)……-40°C to +85°C
Storage Temperature Range……-55°C to +125°C
Lead Temperature (soldering, 10s)……+260°C
Soldering Temperature (reflow)……+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

µSOP
Junction-to-Ambient Thermal Resistance (θ_{JA})……206.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC})……42°C/W
SO
Junction-to-Ambient Thermal Resistance (θ_{JA})……73°C/W
Junction-to-Case Thermal Resistance (θ_{JC})……23°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	DS1339-2	1.8	2.0	5.5	V
		DS1339-3	2.7	3.0	5.5	
		DS1339-33	2.97	3.3	5.5	
Backup Supply Voltage	V_{BACKUP}		1.3	3.0	3.7	V
Logic 1	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Logic 0	V_{IL}		-0.3		+0.3 x V_{CC}	V
Power-Fail Voltage	V_{PF}	DS1339-2	1.58	1.70	1.80	V
		DS1339-3	2.45	2.59	2.70	
		DS1339-33	2.70	2.85	2.97	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = MIN to MAX, T_A = -40°C to +85°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}	(Note 3)			1	µA
I/O Leakage	I_{LO}	(Note 4)			1	µA
Logic 0 Out V_{OL} = 0.4V; V_{CC} > V_{CC} MIN (-3, -33); V_{CC} ≥ 2.0V (-2)	I_{OL}	(Note 4)			3	mA
Logic 0 Out V_{OL} = 0.2 (V_{CC}); 1.8V < V_{CC} < 2.0V (DS1339-2)	I_{OL}	(Note 4)			3	mA
Logic 0 Out V_{OL} = 0.2 (V_{CC}); 1.3V < V_{CC} < 1.8V (DS1339-2)	I_{OL}	(Note 4)			250	µA
V_{CC} Active Current	I_{CCA}	(Note 5)			450	µA
V_{CC} Standby Current (Note 6)	I_{CCS}	-2: V_{CC} = 2.2V		60	100	µA
		-3: V_{CC} = 3.3V		80	150	
		-33: V_{CC} = 5.5V			200	
Trickle-Charger Resistor Register 10h = A5h, V_{CC} = Typ, V_{BACKUP} = 0V	R1	(Note 7)		250		Ω
Trickle-Charger Resistor Register 10h = A6h, V_{CC} = Typ, V_{BACKUP} = 0V	R2			2000		Ω
Trickle-Charger Resistor Register 10h = A7h, V_{CC} = Typ, V_{BACKUP} = 0V	R3			4000		Ω
V_{BACKUP} Leakage Current	I_{BKLKG}			25	100	nA

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = 0V, T_A = -40°C to +85°C.**) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BACKUP} Current $\overline{EOSC}$ = 0, SQW Off	I_{BKOSC}	(Note 8)		400	700	nA
V_{BACKUP} Current $\overline{EOSC}$ = 0, SQW On	I_{BKSQW}	(Note 8)		600	1000	nA
V_{BACKUP} Current $\overline{EOSC}$ = 1	I_{BKDR}			10	100	nA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = MIN to MAX, T_A = -40°C to +85°C.) (Note 9)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode			100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 10)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time (Notes 11, 12)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 13)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 14)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 14)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line (Note 14)	C_B				400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 9)			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 15)		100		ms

POWER-UP/DOWN CHARACTERISTICS

(T_A = -40°C to +85°C) (Note 2, Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}	(Note 16)			2	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0			µs

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

Note 2: Limits at -40°C are guaranteed by design and are not production tested.

Note 3: SCL only.

Note 4: SDA and SQW/$\overline{INT}$.

Note 5: I_{CCA}—SCL at f_{SC} max, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charger disabled.

Note 6: Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charger disabled.

Note 7: V_{CC} must be less than 3.63V if the 250Ω resistor is selected.

Note 8: Using recommended crystal on X1 and X2.

Note 9: Guaranteed by design; not production tested.

Note 10: After this period, the first clock pulse is generated.

Note 11: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 12: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 13: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Note 14: C_B—total capacitance of one bus line in pF.

Note 15: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of 0.0V ≤ V_{CC} ≤ V_{CCMAX} and 1.3V ≤ V_{BACKUP} ≤ 3.7V.

Note 16: This delay applies only if the oscillator is running. If the oscillator is disabled or stopped, no power-up delay occurs.

Figure 1. Power-Up/Down Timing

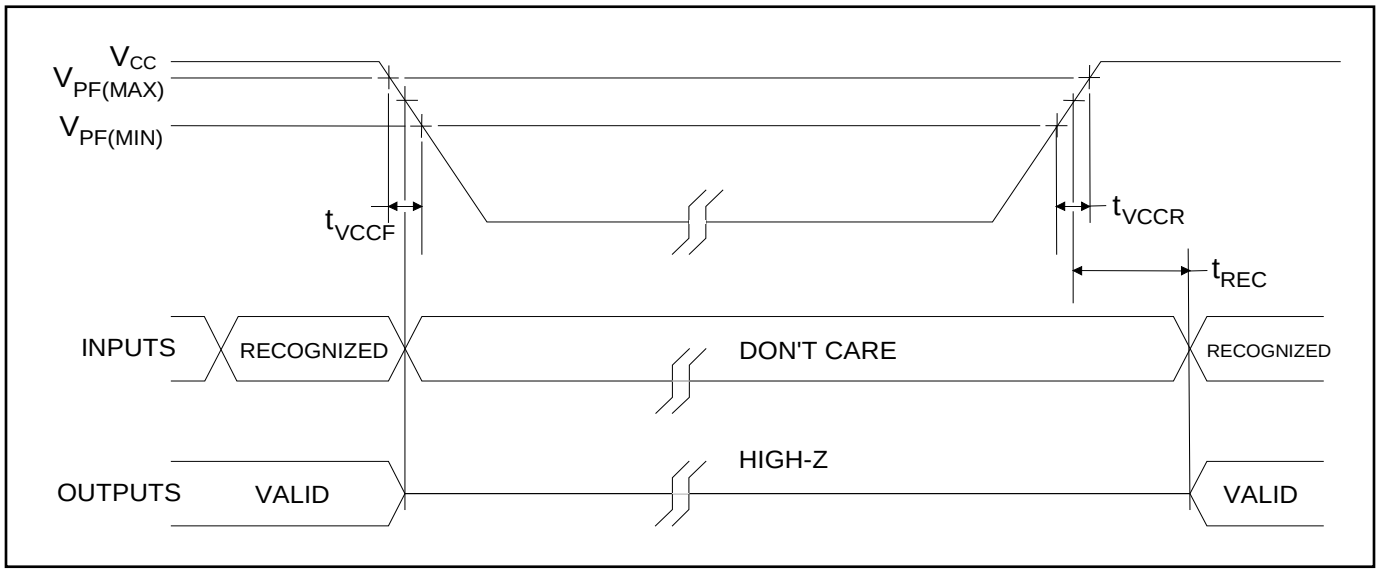


Figure 2. Timing Diagram

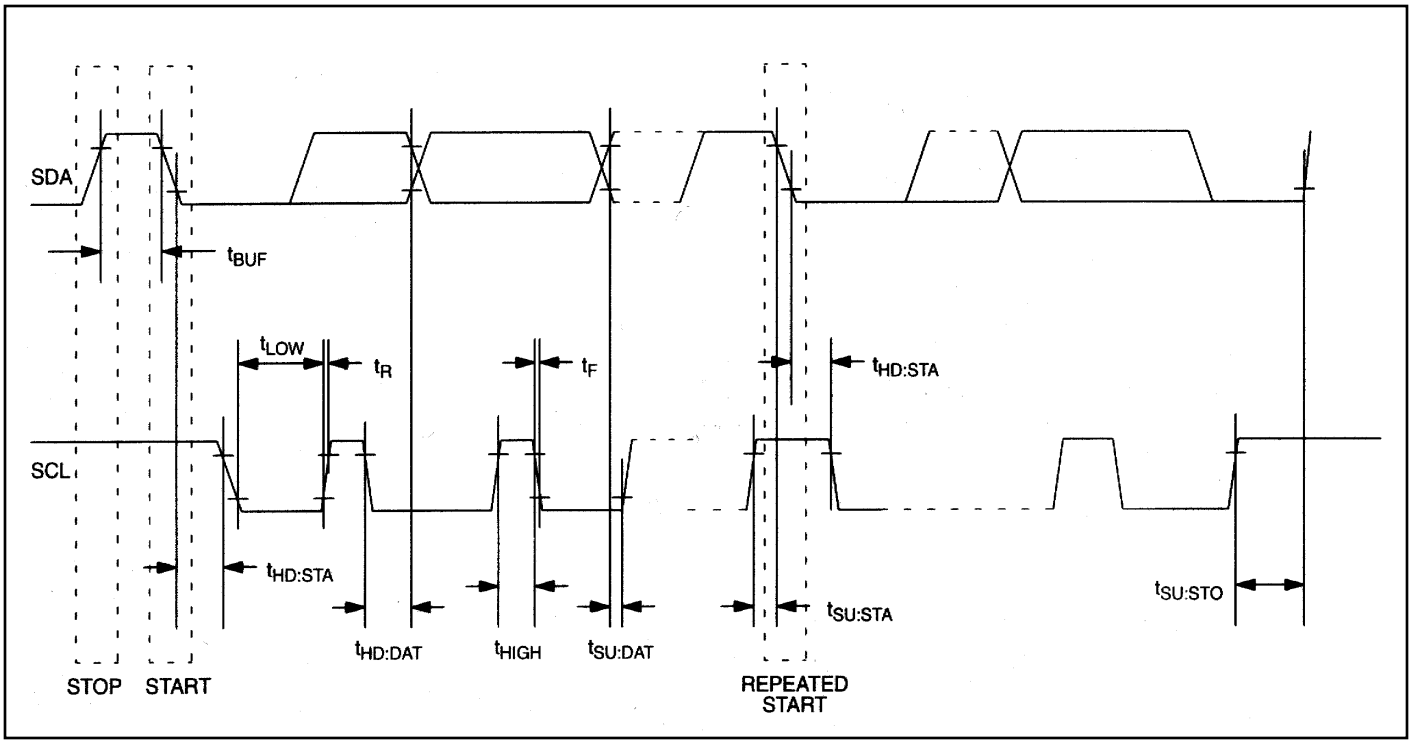
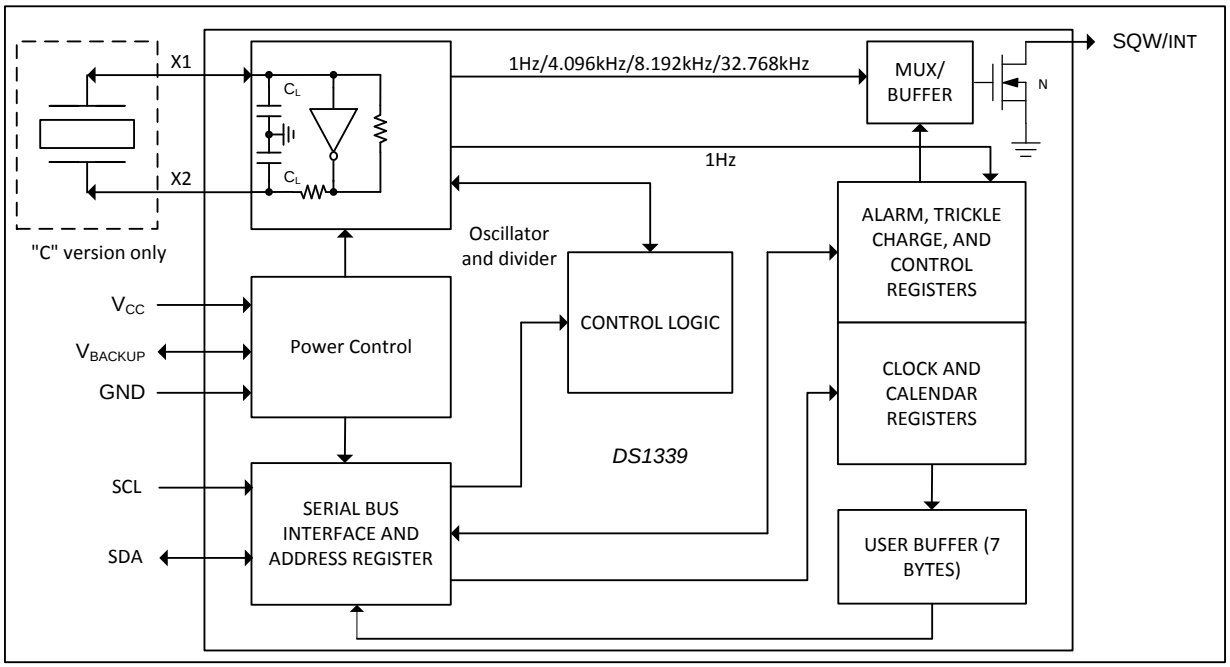
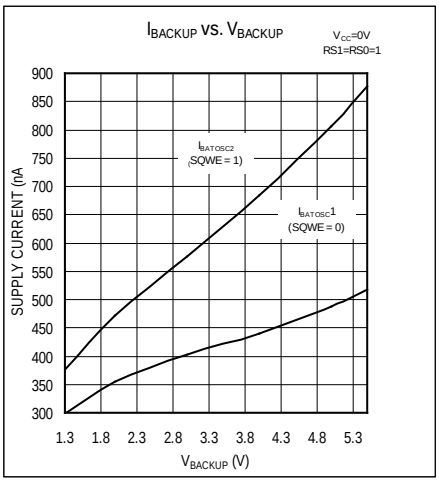


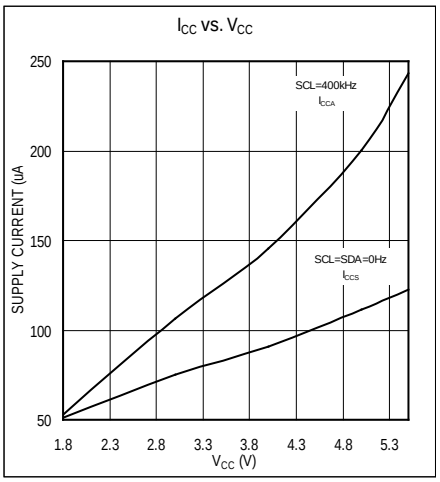
Figure 3. Block Diagram

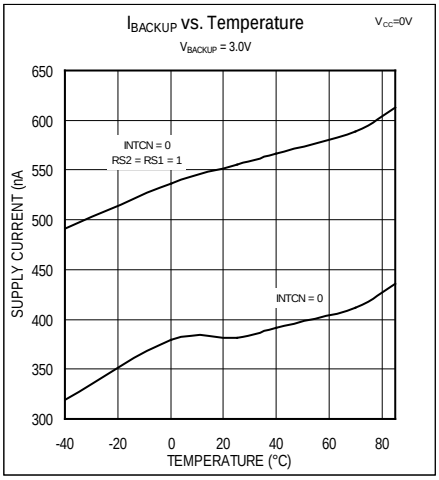


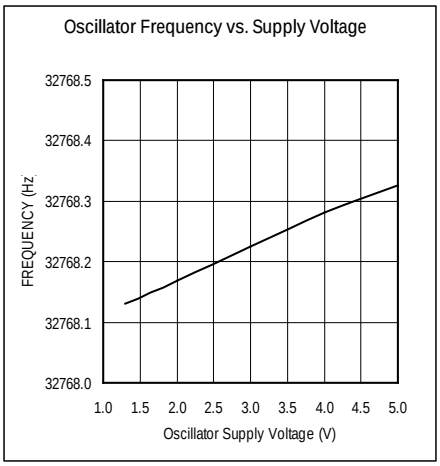
TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = 3.3v, T_A = +25°C, unless otherwise noted.)





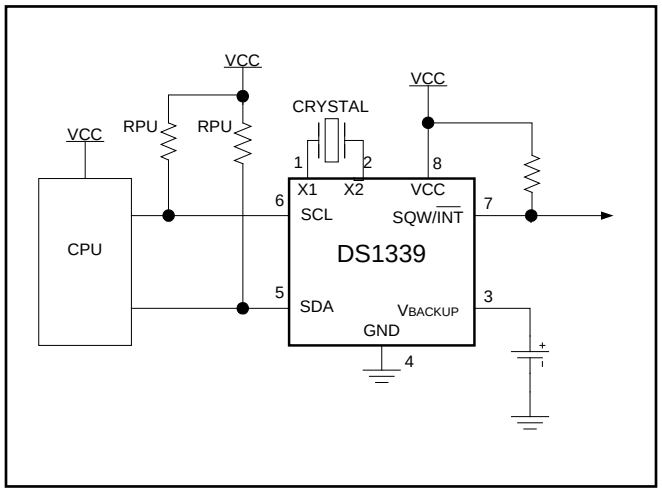




PIN DESCRIPTION

PIN		NAME	FUNCTION
µSOP	SO		
1	—	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. An external 32.768kHz oscillator can also drive the DS1339. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left unconnected. For more information about crystal selection and crystal layout considerations, refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clocks*.
2	—	X2	
3	14	V_{BACKUP}	Secondary Power Supply. Supply voltage must be held between 1.3V and 3.7V for proper operation. This pin can be connected to a primary cell, such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used in conjunction with the trickle-charge feature. Diodes should not be placed in series between the backup source and the V_{BACKUP} input, or improper operation will result. If a backup supply is not required, V_{BACKUP} must be grounded. UL recognized to ensure against reverse charging current when used with a lithium cell. For more information, visit www.maxim-ic.com/qa/info/ul.
4	15	GND	Ground. DC power is provided to the device on these pins.
5	16	SDA	Serial Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V regardless of the voltage on V_{CC}.
6	1	SCL	Serial Clock Input. SCL is used to synchronize data movement on the I²C serial interface. The pull up voltage may be up to 5.5V regardless of the voltage on V_{CC}.
7	2	SQW/$\overline{INT}$	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. The SQW/$\overline{INT}$ pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V regardless of the voltage on V_{CC}. If not used, this pin may be left unconnected.
8	3	V_{CC}	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected and V_{CC} is below V_{PF}, reads and writes are inhibited. The timekeeping and alarm functions operate when the device is powered by V_{CC} or V_{BACKUP}.
—	4–13	N.C.	No Connection. These pins are unused and must be connected to ground.

TYPICAL OPERATING CIRCUIT



DETAILED DESCRIPTION

The DS1339 serial real-time clock (RTC) is a low-power clock/date device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I²C bus. The clock/date provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1339 has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply, maintaining time, date, and alarm operation.

OPERATION

The DS1339 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels. The block diagram in Figure 3 shows the main elements of the serial real-time clock.

POWER CONTROL

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed after t_{REC} (Figure 1). On the first application of power to the device the time and date registers are reset to 01/01/00 01 00:00:00 (MM/DD/YY DOW HH:MM:SS).

Table 1. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$	No	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

OSCILLATOR CIRCUIT

The DS1339 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 2 specifies several crystal parameters for the external crystal. Figure 3 shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 2. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

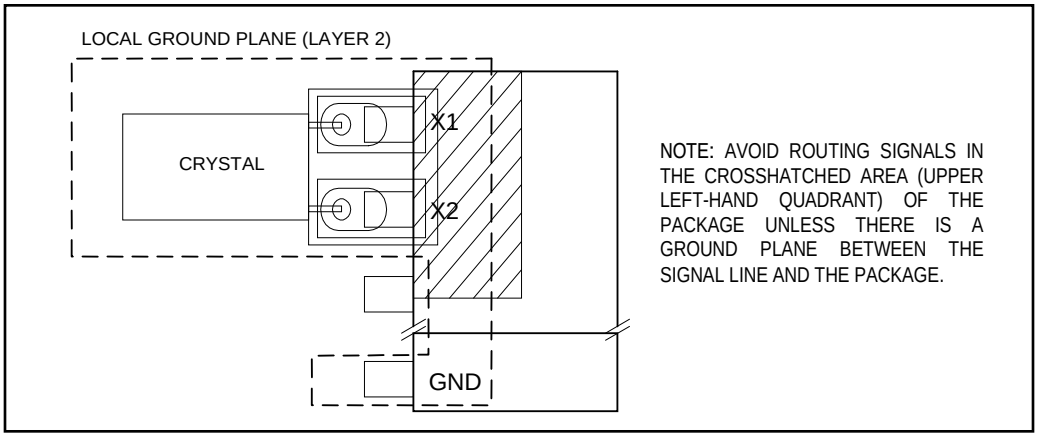
CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Figure 4 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information

DS1339C ONLY

The DS1339C integrates a standard 32,768Hz crystal in the package. Typical accuracy at nominal V_{CC} and +25°C is approximately 10ppm. Refer to *Application Note 58* for information about crystal accuracy vs. temperature.

Figure 4. Typical PC Board Layout for Crystal



ADDRESS MAP

Table 3 shows the address map for the DS1339 registers. During a multibyte access, when the address pointer reaches the end of the register space (10h), it wraps around to location 00h. On an I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 3. Timekeeper Registers

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Hours	1–12 +AM/PM 00–23
03h	0	0	0	0	0	Day			Day	1–7
04h	0	0	10 Date		Date				Date	01–31
05h	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06h	10 Year				Year				Year	00–99
07h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Alarm 1 Hours	1–12 + AM/PM 00–23
0Ah	A1M4	DY/DT	10 Date		Day, Date				Alarm 1 Day, Alarm 1 Date	1-7, 1-31
0Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Alarm 2 Hours	1–12 + AM/PM 00–23
0Dh	A2M4	DY/$\overline{DT}$	10 Date		Day, Date				Alarm 2 Day, Alarm 2 Date	1–7, 1–31
0Eh	$\overline{EOSC}$	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0Fh	OSF	0	0	0	0	0	A2F	A1F	Status	—
10h	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charger	—

Note: *Unless otherwise specified, the state of the registers are not defined when power is first applied or when V_{CC} and V_{BACKUP} falls below the $V_{BACKUP(MIN)}$.*

TIME AND DATE OPERATION

The time and date information is obtained by reading the appropriate register bytes. Table 3 shows the RTC registers. The time and date are set or initialized by writing the appropriate register bytes. The contents of the time and date registers are in the BCD format. The DS1339 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20 to 23 hours). All hours values, including the alarms, must be re-entered whenever the 12/$\overline{24}$-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START or STOP, and when the address pointer rolls over to zero. The countdown chain is reset whenever the seconds register is written. Write transfers occurs on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. If enabled, the 1Hz square-wave output transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

ALARMS

The DS1339 contains two time of day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the Alarm Enable and INTCN bits of the Control Register) to activate the SQW/$\overline{INT}$ output on an alarm match condition. Bit 7 of each of the time of day/date alarm registers are mask bits (Table 4). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h to 06h match the values stored in the time of day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 4 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to a logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{DT}$ is written to a logic 1, the alarm is the result of a match with day of the week.

The device checks for an alarm match once per second. When the RTC register values match alarm register settings, the corresponding Alarm Flag ‘A1F’ or ‘A2F’ bit is set to logic 1. If the corresponding Alarm Interrupt Enable ‘A1IE’ or ‘A2IE’ is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the SQW/$\overline{INT}$) signal. If the BBSQI bit is set to 1, the $\overline{INT}$ output activates while the part is being powered by V_{BACKUP}. The alarm output remains active until the alarm flag is cleared by the user.

Table 4. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (Bit 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (Bit 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 sec. of every min.)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

SPECIAL-PURPOSE REGISTERS

The DS1339 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

CONTROL REGISTER (0Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{EOSC}$	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator ($\overline{EOSC}$). This bit when set to logic 0 starts the oscillator. When this bit is set to a logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bit 5: Battery-Backed Square-Wave and Interrupt Enable (BBSQI). This bit when set to a logic 1 enables the square wave or interrupt output when V_{CC} is absent and the DS1339 is being powered by the V_{BACKUP} pin. When BBSQI is a logic 0, the SQW/$\overline{INT}$ pin goes high impedance when V_{CC} falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. Table 5 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

Table 5. SQW/$\overline{INT}$ Output

INTCN	RS2	RS1	SQW/$\overline{INT}$ OUTPUT	A2IE	A1IE
0	0	0	1Hz	X	X
0	0	1	4.096kHz	X	X
0	1	0	8.192kHz	X	X
0	1	1	32.768kHz	X	X
1	X	X	$\overline{A1F}$	0	1
1	X	X	$\overline{A2F}$	1	0
1	X	X	$\overline{A2F}$ + $\overline{A1F}$	1	1

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 or alarm 2 registers activate the SQW/$\overline{INT}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{INT}$ pin. This bit is set to logic 0 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to a logic 1, this bit permits the Alarm 2 Flag (A2F) bit in the status register to assert SQW/$\overline{INT}$ (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the Alarm 1 Flag (A1F) bit in the status register to assert SQW/$\overline{INT}$ (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate an interrupt signal. The A1IE bit is disabled (logic 0) when power is first applied.

STATUS REGISTER (0Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and date data. This bit is edge triggered and is set to logic 1 when the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage on both V_{CC} and V_{BACKUP} are insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to a logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the Alarm 2 Flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/$\overline{INT}$ pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the Alarm 1 Flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/$\overline{INT}$ pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

TRICKLE CHARGER REGISTER (10h)

The simplified schematic in Figure 5 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode-select (DS) bits (bits 2 and 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. The ROUT bits (bits 0 and 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Table 6 shows the bit values.

Table 6. Trickle Charger Register (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Initial power-up values

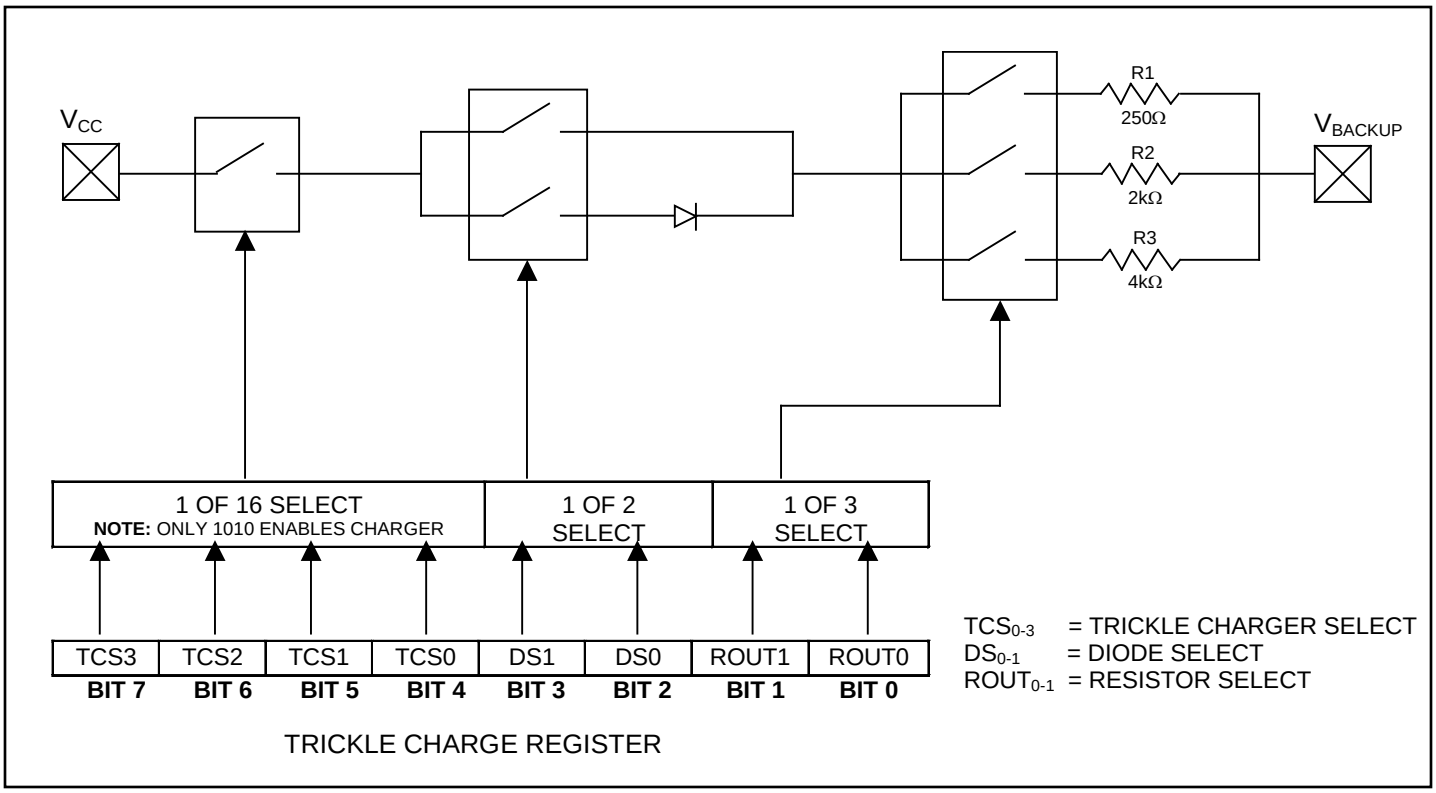
Warning: The ROUT value of 250Ω must not be selected whenever V_{CC} is greater than 3.63V.

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a 3.3V system power supply is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap or battery charges, the voltage drop between V_{CC} and V_{BACKUP} decreases and therefore the charge current decreases.

Figure 5. Programmable Trickle Charger



I²C SERIAL DATA BUS

The DS1339 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1339 operates as a slave on the I²C bus. Within the bus specifications, a standard mode (100kHz cycle rate) and a fast mode (400kHz cycle rate) are defined. The DS1339 works in both modes. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 6):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

START data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

STOP data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

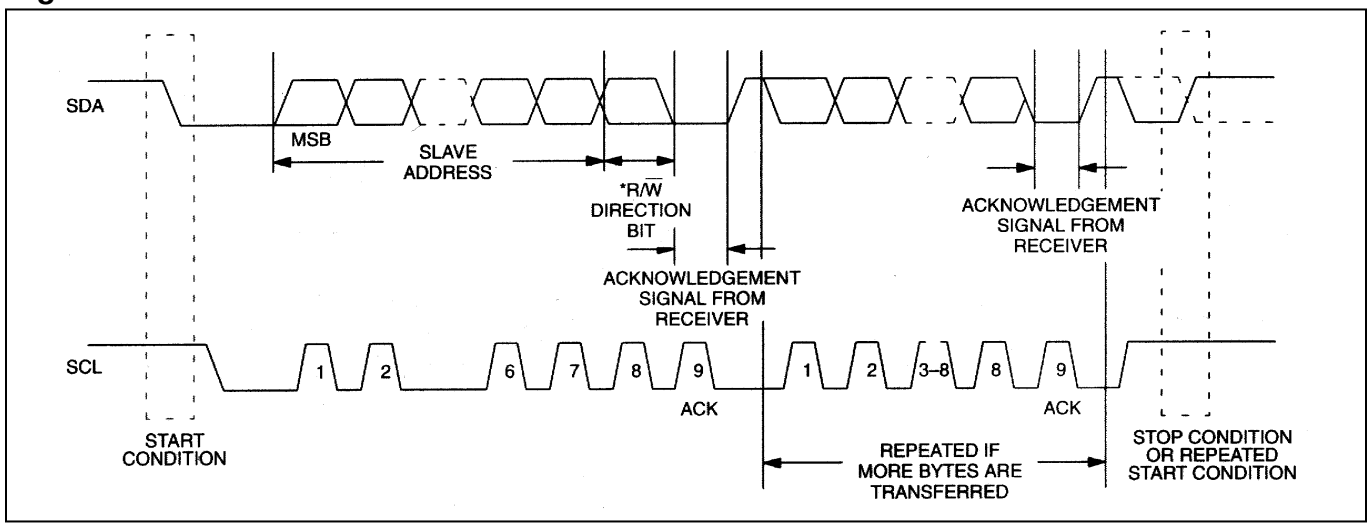
Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 6. Data Transfer on I²C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The DS1339 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 7). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1339 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 0 for a write. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. After the DS1339 acknowledges the slave address + write bit, the master transmits a register address to the DS1339. This

sets the register pointer on the DS1339, with the DS1339 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the DS1339 acknowledging each byte received. The address pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1339 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 8). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1339 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. The DS1339 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The address pointer is incremented after each byte is transferred. The DS1339 must receive a “not acknowledge” to end a read.

Figure 7. Data Write—Slave Receiver Mode

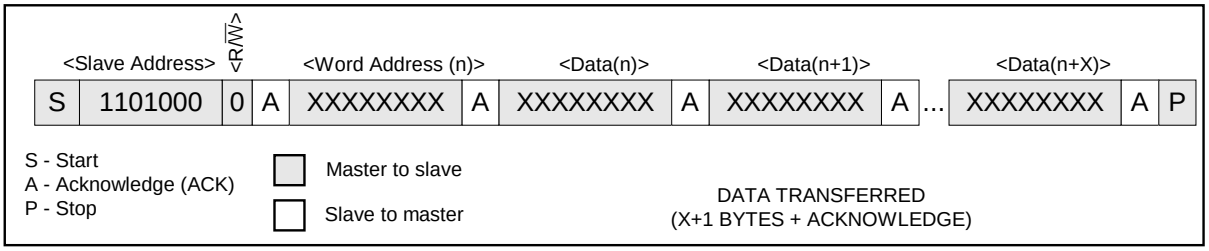


Figure 8. Data Read (from Current Pointer Location)—Slave Transmitter Mode

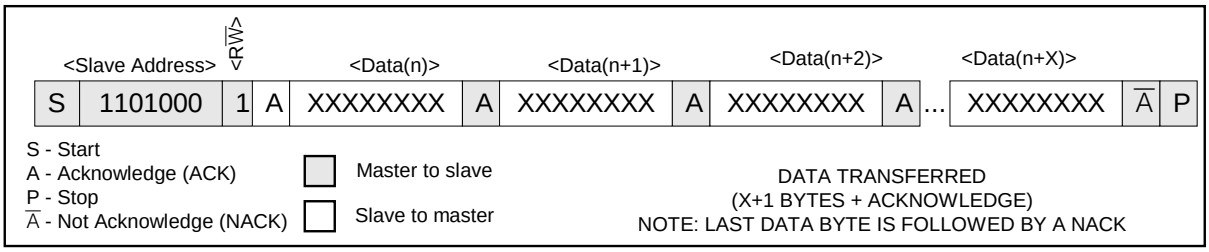
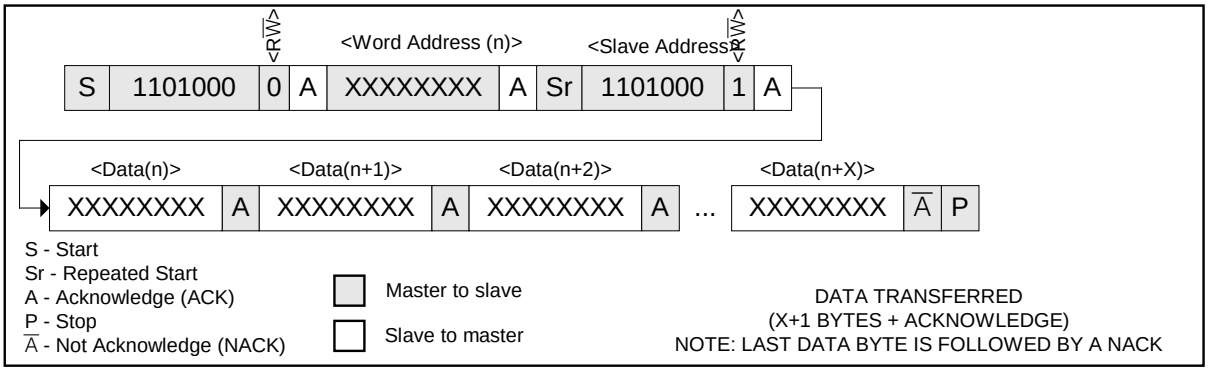


Figure 9. Data Read (Write Pointer, Then Read)—Slave Receive and Transmit



HANDLING, PCB LAYOUT, AND ASSEMBLY

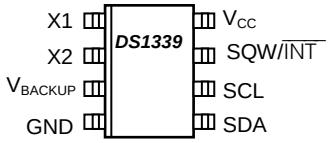
The DS1339C package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020B standard for moisture-sensitive device (MSD) classifications.

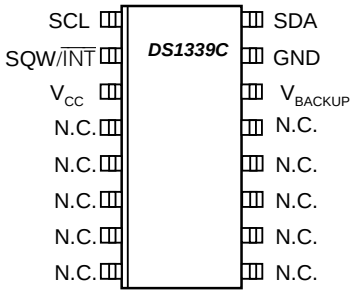
PIN CONFIGURATIONS

TOP VIEW



µSOP

TOP VIEW



SO (300 mils)

CHIP INFORMATION

PROCESS: CMOS

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 µSOP	U8+1	**21-0036**	**90-0092**
16 SO	W16#H2	**21-0042**	**90-0107**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
100108	Removed leaded part numbers from the *Ordering Information* table.	1
	Removed the pullup resistor voltage spec from the *Recommended DC Operating Conditions* table and added it to the pin descriptions.	2, 8
	Removed Note 7 from the I_{BKDR} specification in the *DC Electrical Characteristics* table.	3
	Updated the block diagram (Figure 3) to show that SQW/INT is open drain.	6
	Added the UL link to the V_{BACKUP} description in the *Pin Description* table.	8
	Removed the duplicate *Oscillator Circuit* section.	9
	Added the initial POR state for time and date registers in the *Power Control* section.	9
	Changed the series resistance (ESR) value in Table 2 from 45kΩ to 50kΩ.	10
	Added the overbar to the “A” legend for NACK in Figure 8.	18
4/11	Updated the soldering temperature and added lead temperature information to the *Absolute Maximum Ratings* section; added the *Package Thermal Characteristics* section and updated the μSOP θ_{JA} and θ_{JC} numbers; changed the V_{CC} max numbers from 2.2V to 5.5V for DS1339-2 and 3.3V to 5.5V for DS1339-3 in the *Recommended DC Operating Conditions* table.	2
	Updated the I_{CCS} parameter in the *DC Electrical Characteristics* table.	3
	Changed the 10 Hour bit to 20 Hour bit for 02h, 09h, and 0Ch in Table 1 and the *Time and Date Operation* section.	11, 12
	Updated the *Handling, PCB Layout, and Assembly* section; removed the transistor count from the *Chip Information* section; added the land pattern numbers to the *Package Information* table.	19
3/15	Updated Benefits and Features section	1

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