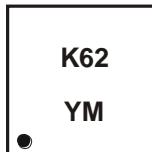


Marking Information

Site 1:



K62 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: I = 2021)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	...	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	Y	...	I	J	K	L	M	N	O	P	R	S
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2:



K62 = Product Type Marking Code
 YWX = Date Code Marking
 Y = Year (ex: 1 = 2021)
 W = Week (ex: a = Week 27; z Represents Week 52 and 53)
 X = Internal Code (ex: U = Monday)

Date Code Key

Year	2011	...	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	1	...	1	2	3	4	5	6	7	8	9	0
Week	1-26			27-52			53					
Code	A-Z			a-z			z					
Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat					
Code	T	U	V	W	X	Y	Z					

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	540 430	mA
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	630 500	mA
Continuous Drain Current (Note 6) $V_{GS} = 5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	430 340	mA
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	510 410	mA
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)			I_{DM}	1.0	A
Maximum Body Diode Forward Current (Note 6)			I_S	540	mA

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

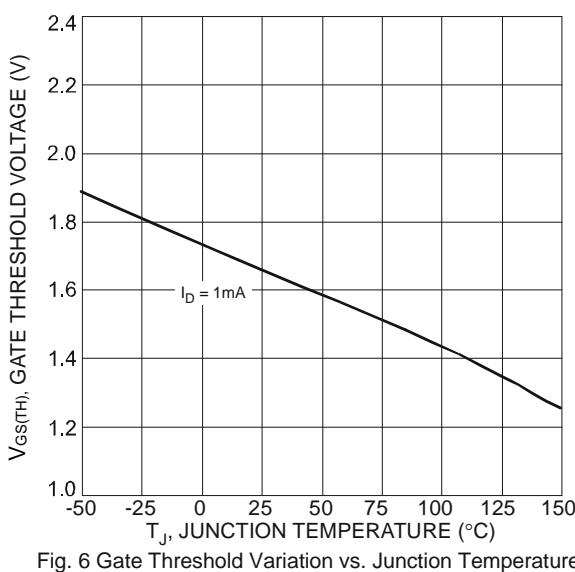
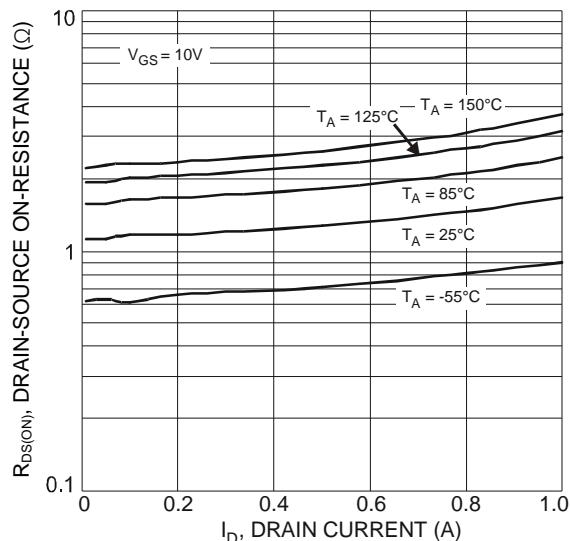
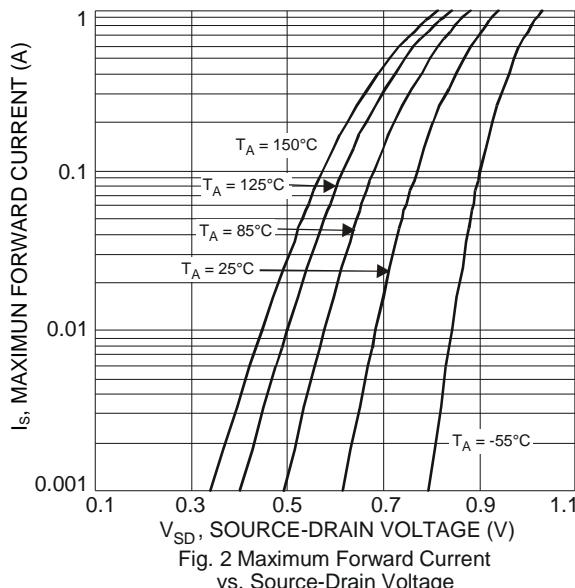
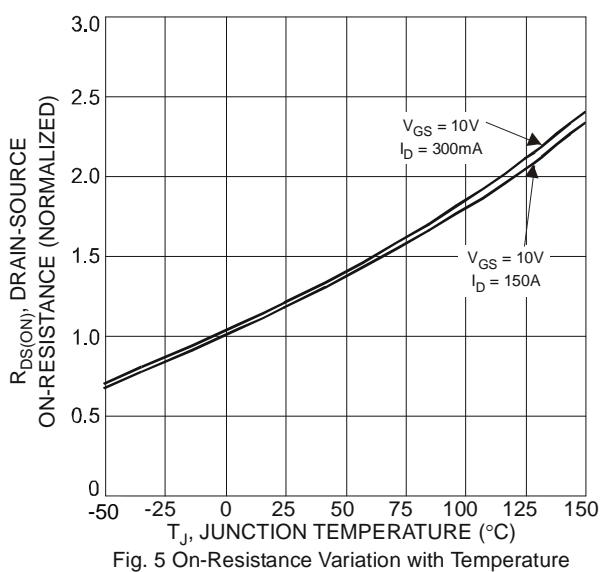
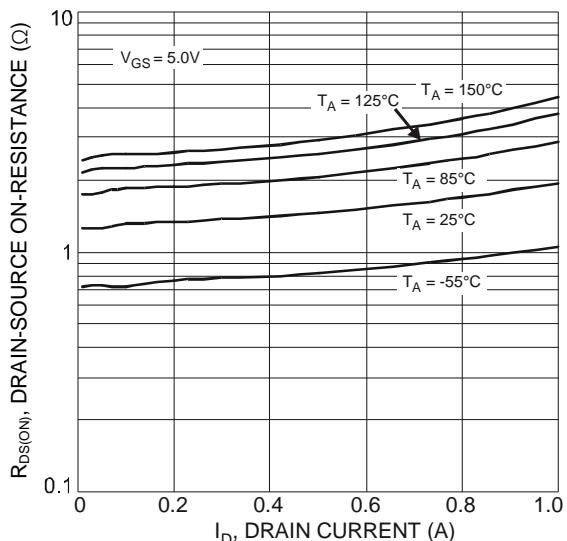
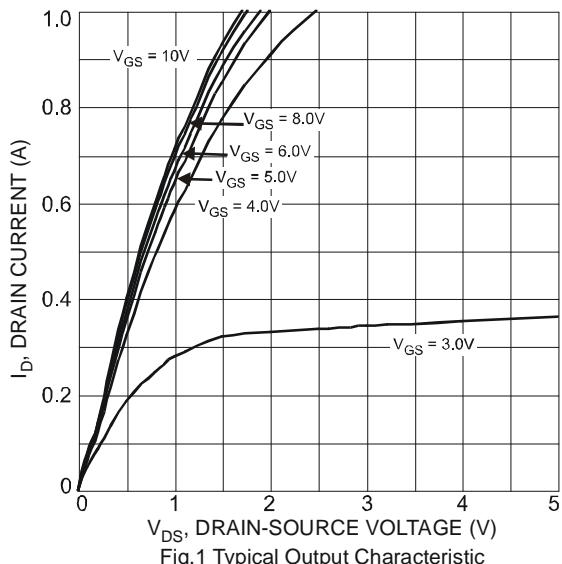
Characteristic			Symbol	Value	Unit
Total Power Dissipation (Note 5)			P_D	0.43	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State		$R_{\theta JA}$	260	$^\circ\text{C/W}$
	$t < 10\text{s}$			182	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)			P_D	0.89	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State		$R_{\theta JA}$	140	$^\circ\text{C/W}$
	$t < 10\text{s}$			98	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case (Note 6)			$R_{\theta JC}$	112	$^\circ\text{C/W}$
Operating and Storage Temperature Range			T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

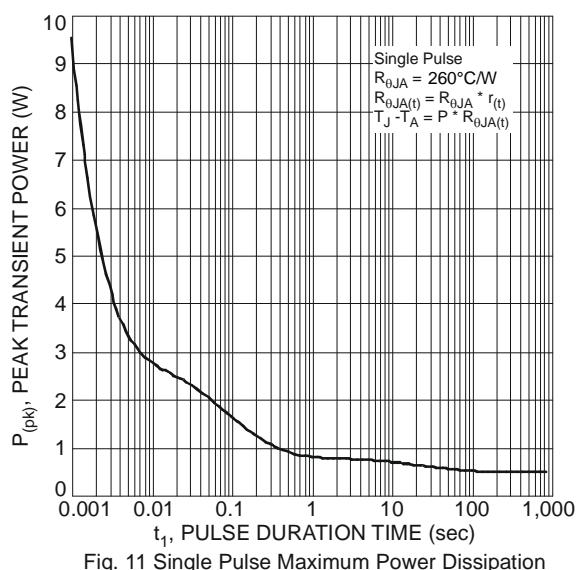
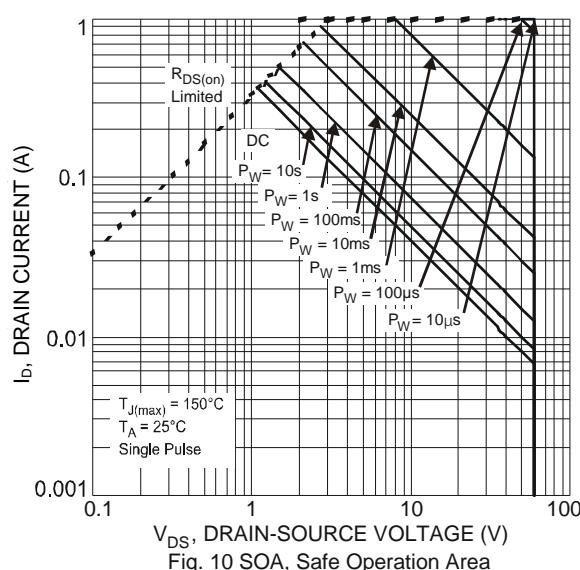
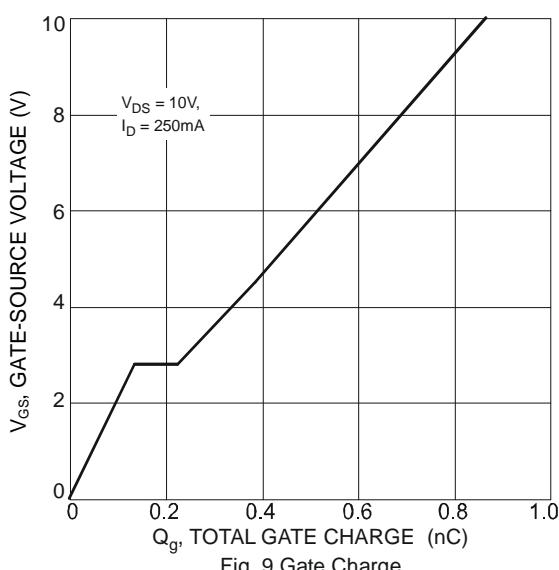
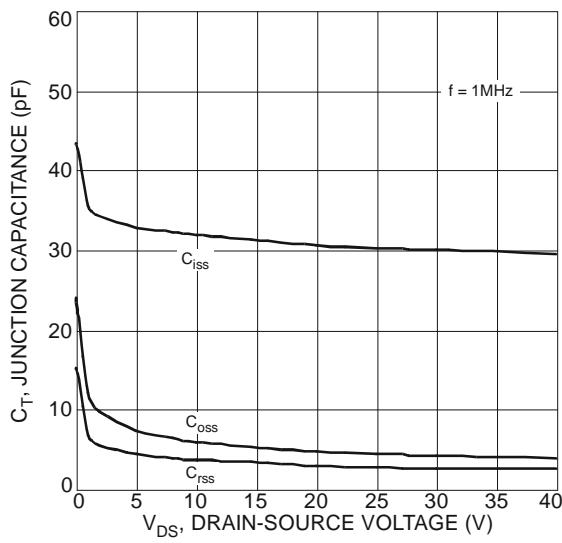
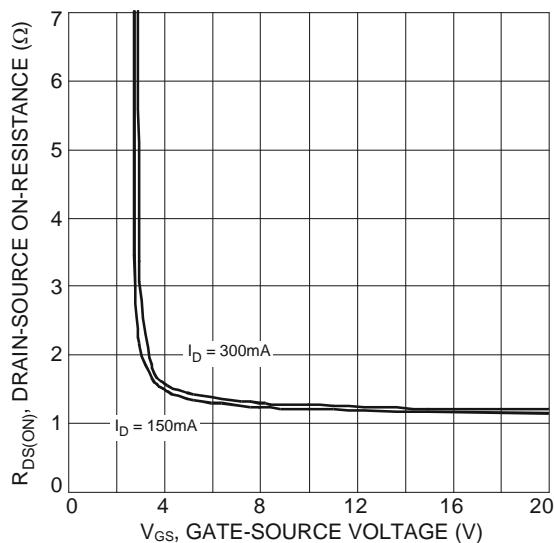
Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 10\mu\text{A}$
Zero Gate Voltage Drain Current @ $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	100	nA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	10	μA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	1.6	2.5	V	$V_{DS} = 10\text{V}, I_D = 1\text{mA}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	—	2	Ω	$V_{GS} = 10\text{V}, I_D = 500\text{mA}$
		—	—	3		$V_{GS} = 5\text{V}, I_D = 50\text{mA}$
Forward Transfer Admittance	$ Y_{fs} $	—	130	—	mS	$V_{DS} = 3\text{V}, I_D = 30\text{mA}$
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	$V_{GS} = 0\text{V}, I_S = 300\text{mA}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	30.2	—	pF	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	4.4	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	2.8	—	pF	
Gate Resistance	R_g	—	131	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	0.39	—	nC	$V_{DS} = 10\text{V}, I_D = 1\text{A}$
Total Gate Charge ($V_{GS} = 10.0\text{V}$)	Q_g	—	0.87	—	nC	
Gate-Source Charge	Q_{gs}	—	0.14	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.09	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.95	—	ns	$V_{DS} = 30\text{V}, I_D = 200\text{mA}$
Turn-On Rise Time	t_R	—	3.81	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	16.0	—	ns	
Turn-Off Fall Time	t_F	—	9.04	—	ns	

Notes:

- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
- Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
- Short duration pulse test used to minimize self-heating effect.
- Guaranteed by design. Not subject to production testing.





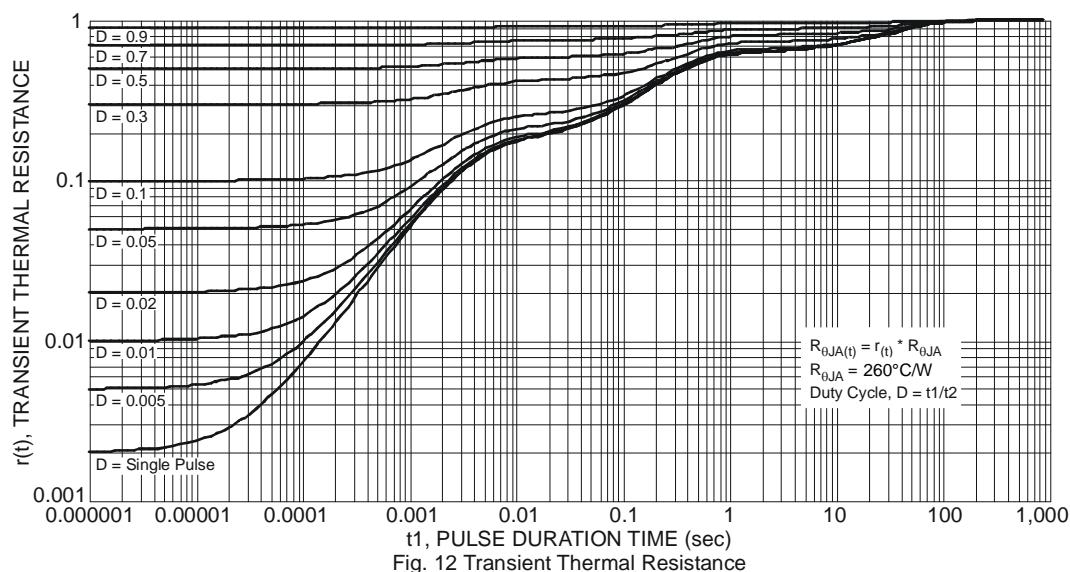
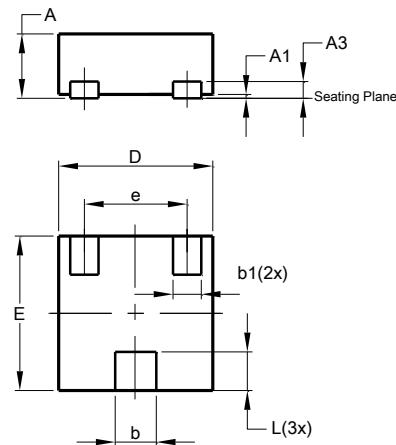


Fig. 12 Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X1-DFN1212-3



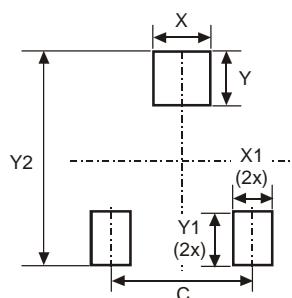
X1-DFN1212-3			
Dim	Min	Max	Typ
A	0.47	0.53	0.50
A1	0	0.05	0.02
A3	-	-	0.13
b	0.27	0.37	0.32
b1	0.17	0.27	0.22
D	1.15	1.25	1.20
E	1.15	1.25	1.20
e	-	-	0.80
L	0.25	0.35	0.30

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X1-DFN1212-3



Dimensions	Value (in mm)
C	0.80
X	0.42
X1	0.32
Y	0.50
Y1	0.50
Y2	1.50

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