

Improved, 8-Channel/Dual 4-Channel, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-		Plastic DIP (derate 10.53mW/°C above +70°C)842mW
V+	-0.3V, 44V	Narrow SO (derate 8.70mW/°C above +70°C)696mW
GND	-0.3V, 25V	CERDIP (derate 10.00mW/°C above +70°C)800mW
Digital Inputs, S, D (Note 1).....	(V- - 2V) to (V+ + 2V) or 30mA, (whichever occurs first)	Operating Temperature Ranges
Continuous Current (any terminal)	30mA	DG408/DG409C_0°C to +70°C
Peak Current, S, D (pulsed at 1ms, 10% duty cycle max)	100mA	DG408/DG409D,E_-40°C to +85°C
Continuous Power Dissipation (T _A = +70°C)		DG408/DG409AK-55°C to +125°C
TSSOP (derate 9.4mW/°C above +70°C)	755mW	Storage Temperature Range-65°C to +150°C
		Lead Temperature (soldering, 10sec)+300°C

Note 1: Signals on S_, D_, EN, A0, A1, or A2 exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS	
SWITCH								
Analog Signal Range	V _{ANALOG}	(Note 3)		-15		15	V	
Drain-Source On-Resistance	r _{DS(ON)}	I _S = -1.0mA, V _D = ±10V	T _A = +25°C	60	100		Ω	
			T _A = T _{MIN} to T _{MAX}			125		
On-Resistance Matching Between Channels	Δr _{DS(ON)}	I _S = -1.0mA, V _D = ±10V (Note 4)	T _A = +25°C	1.5	8		Ω	
			T _A = T _{MIN} to T _{MAX}			10		
On-Resistance Flatness	r _{FLAT}	I _S = -1.0mA, V _D = ±5V or 0V	T _A = +25°C	1.8	9		Ω	
			T _A = T _{MIN} to T _{MAX}			12		
Source-Off Leakage Current (Note 5)	I _{S(OFF)}	V _D = +10V, V _S = ±10V, V _{EN} = 0V	T _A = +25°C	-0.5	0.01	0.5	nA	
			T _A = T _{MIN} to T _{MAX}	C, D	-5	5		
				A	-50	50		
Drain-Off Leakage Current (Note 5)	I _{D(OFF)}	V _D = ±10V, V _S = +10V, V _{EN} = 0V	DG408	T _A = +25°C	-1	0.02	1	nA
				T _A = T _{MIN} to T _{MAX}	C, D	-10	10	
			DG409		T _A = +25°C	A	-100	
				T _A = T _{MIN} to T _{MAX}		C, D	-5	
			A		-50	50		
				Drain-On Leakage Current (Note 5)	I _{D(ON)}	V _D = ±10V, V _S = ±10V, sequence each switch on	DG408	
T _A = T _{MIN} to T _{MAX}	C, D	-20	20					
	DG409	T _A = +25°C	A				-100	100
T _A = T _{MIN} to T _{MAX}			C, D				-10	10
	A	-50	50					

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DG408/DG409

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V₊ = 15V, V₋ = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS	
INPUT								
Input Current with Input Voltage High	I _{AH}	V _A = 2.4V or 15V		-1.0		1.0	μA	
Input Current with Input Voltage Low	I _{AL}	V _{EN} = 0V or 2.4V, V _A = 0V		-1.0		1.0	μA	
SUPPLY								
Power-Supply Range				±5		±20	V	
Positive Supply Current	I ₊	V _{EN} = V _A = 0V or 4.5V	T _A = +25°C		16	30	μA	
			T _A = T _{MIN} to T _{MAX}			75		
		V _{EN} = 2.4V, V _{A(ALL)} = 0V or 2.4V	T _A = +25°C		0.075	0.5	mA	
			T _A = T _{MIN} to T _{MAX}			2		
Negative Supply Current	I ₋	V _{EN} = 2.4V, V _{A(ALL)} = 0V or 2.4V	T _A = +25°C		-1	1	μA	
			T _A = T _{MIN} to T _{MAX}			-10		10
DYNAMIC								
Transition Time	t _{TRANS}	Figure 2	T _A = +25°C		85	175	ns	
			T _A = T _{MIN} to T _{MAX}			250		
Break-Before-Make Interval	t _{OPEN}	Figure 4	T _A = +25°C		10	40	ns	
Enable Turn-On Time	t _{ON(EN)}	Figure 3	T _A = +25°C			85	150	ns
			T _A = T _{MIN} to T _{MAX}				225	
Enable Turn-Off Time	t _{OFF(EN)}	Figure 3	T _A = +25°C				150	ns
			T _A = T _{MIN} to T _{MAX}				300	
Charge Injection (Note 3)	Q	C _L = 1.0nF, V _S = 0V, R _S = 0Ω, Figure 5	T _A = +25°C			2	15	pC
Off Isolation (Note 6)	V _{ISO}	V _{EN} = 0V, R _L = 1kΩ, f = 100kHz, Figure 6	T _A = +25°C			-75		dB
Crosstalk Between Input Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{GEN} = 1V _{P-P} , R _L = 1kΩ, Figure 7	T _A = +25°C			-92		dB
Logic Input Capacitance	C _{IN}	f = 1MHz	T _A = +25°C			8		pF
Source-Off Capacitance	C _{S(OFF)}	f = 1MHz, V _{EN} = V _S = 0V, Figure 8	T _A = +25°C			3		pF
Drain-Off Capacitance	C _{D(OFF)}	f = 1MHz, V _{EN} = 0.8V, V _D = 0V, Figure 8	DG408	T _A = +25°C		26	pF	
			DG409			14		
Drain-On Capacitance	C _{D(ON)} + C _{S(ON)}	f = 1MHz, V _{EN} = 2.4V, V _D = 0V, Figure 8	DG408	T _A = +25°C		37	pF	
			DG409			25		

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ELECTRICAL CHARACTERISTICS—Single Supply

($V_+ = 12V$, $V_- = 0V$, $GND = 0V$, $V_{AH} = +2.4V$, $V_{AL} = +0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_S = -1.0mA$ $V_D = 3V$ or $10V$	$T_A = +25^\circ C$		120	175	Ω
DYNAMIC							
Transition Time (Note 3)	t_{TRANS}	$V_{S1} = 8V$, $V_{S8} = 0V$, $V_A = 0V$, Figure 2	$T_A = +25^\circ C$		115	450	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	$V_{AL} = 0V$, $V_{S1} = 5V$, Figure 3	$T_A = +25^\circ C$		100	600	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	$V_{AL} = 0V$, $V_{S1} = 5V$, Figure 3	$T_A = +25^\circ C$		75	300	ns
Charge Injection	Q	$C_L = 1.0nF$, $V_S = 0V$, $R_S = 0\Omega$	$T_A = +25^\circ C$		2		pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

Note 5: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at $+25^\circ C$.

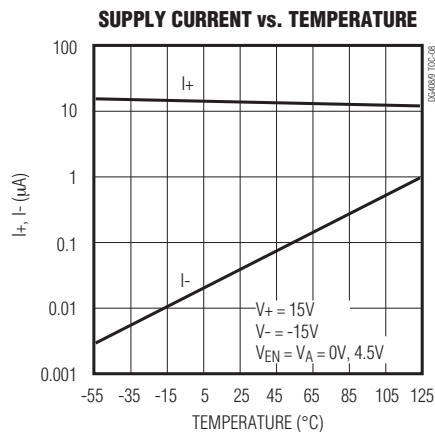
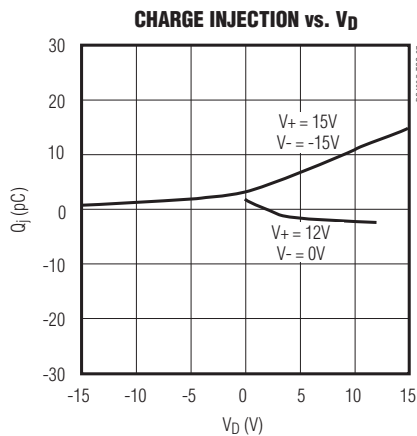
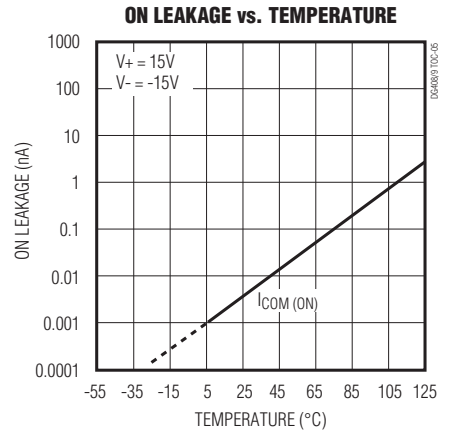
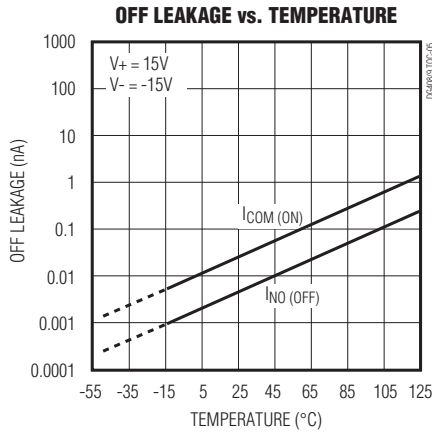
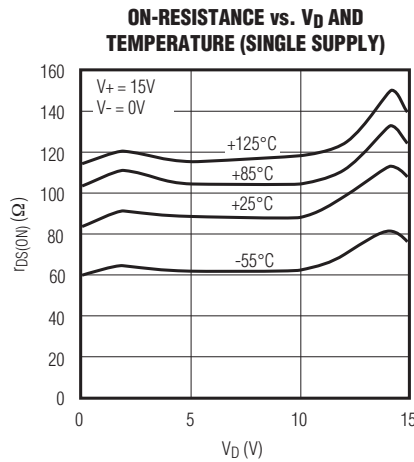
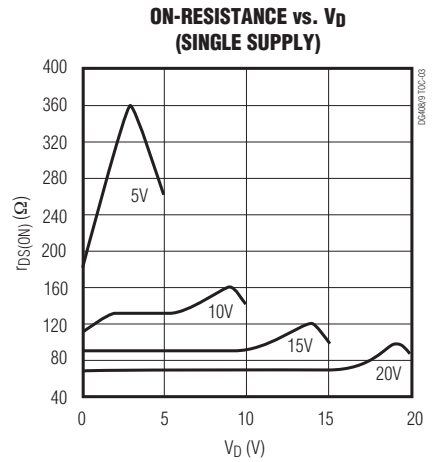
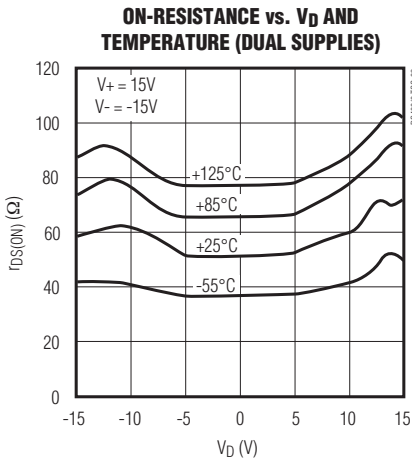
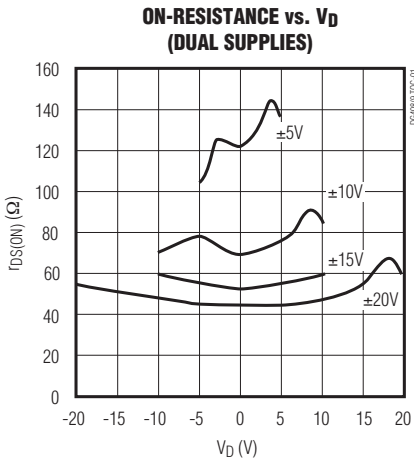
Note 6: Off isolation = $20 \log V_D/V_S$, where V_D = output and V_S = input to off switch.

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Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

DG408/DG409



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Pin Description

PIN		NAME	FUNCTION
DG408	DG409		
1, 15, 16	—	A0, A2, A1	Address Inputs
—	1, 16	A0, A1	Address Inputs
2	2	EN	Enable Input
3	3	V-	Negative Supply Voltage Input
4-7	—	S1-S4	Bidirectional Analog Inputs
—	4-7	S1A-S4A	Bidirectional Analog Inputs
8	—	D	Bidirectional Analog Output
—	8, 9	DA, DB	Bidirectional Analog Outputs
9-12	—	S8-S5	Bidirectional Analog Inputs
—	10-13	S4B-S1B	Bidirectional Analog Inputs
13	14	V+	Positive Supply Voltage Input
14	15	GND	Ground

Applications Information

Operation with Supply Voltages Other than 15V

Using supply voltages less than $\pm 15V$ reduces the analog signal range. The DG408/DG409 switches operate with $\pm 5V$ to $\pm 20V$ bipolar supplies or with a $+5V$ to $+40V$ single supply. Connect V- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies, such as $+24V$ and $-5V$. The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs, S or D. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

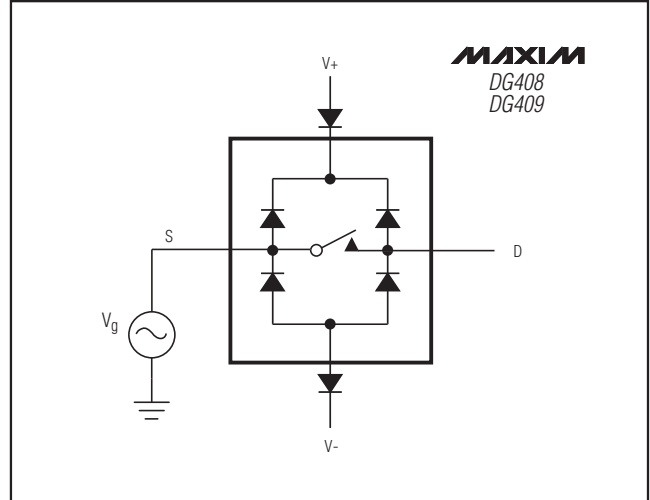


Figure 1. Overvoltage Protection Using External Blocking Diodes

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Test Circuits/Timing Diagrams

DG408/DG409

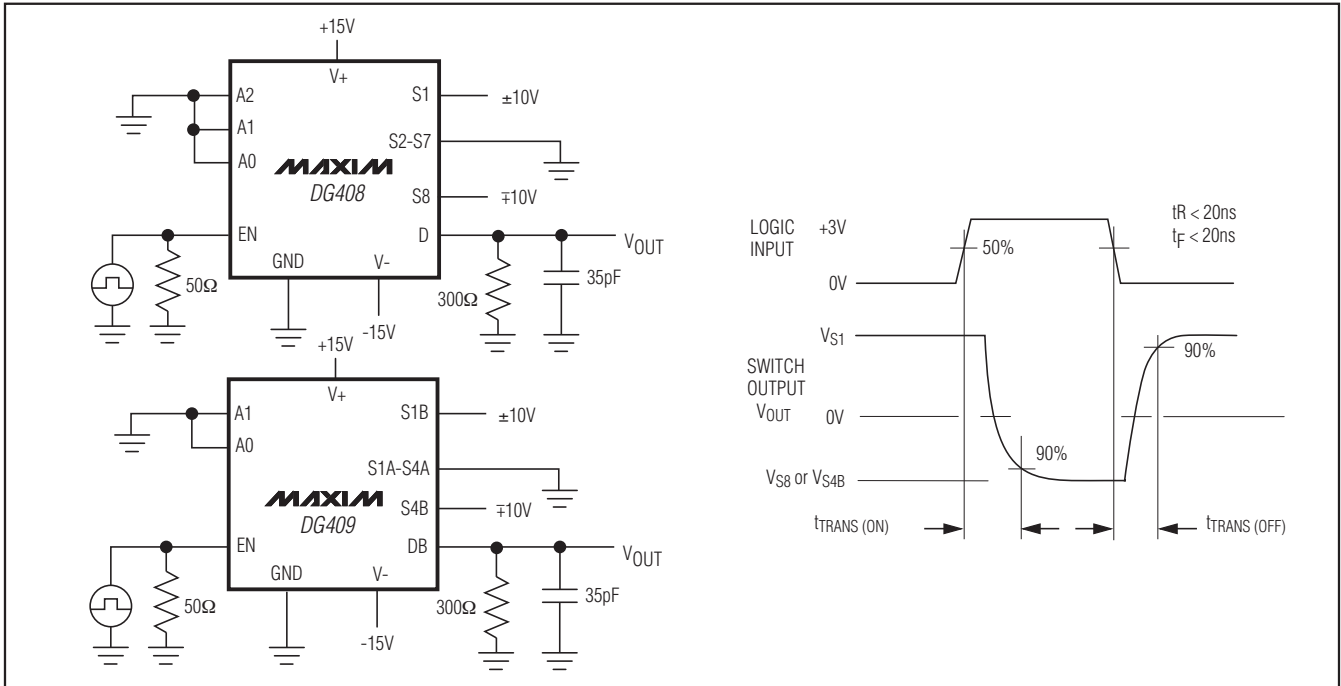


Figure 2. Transition Time

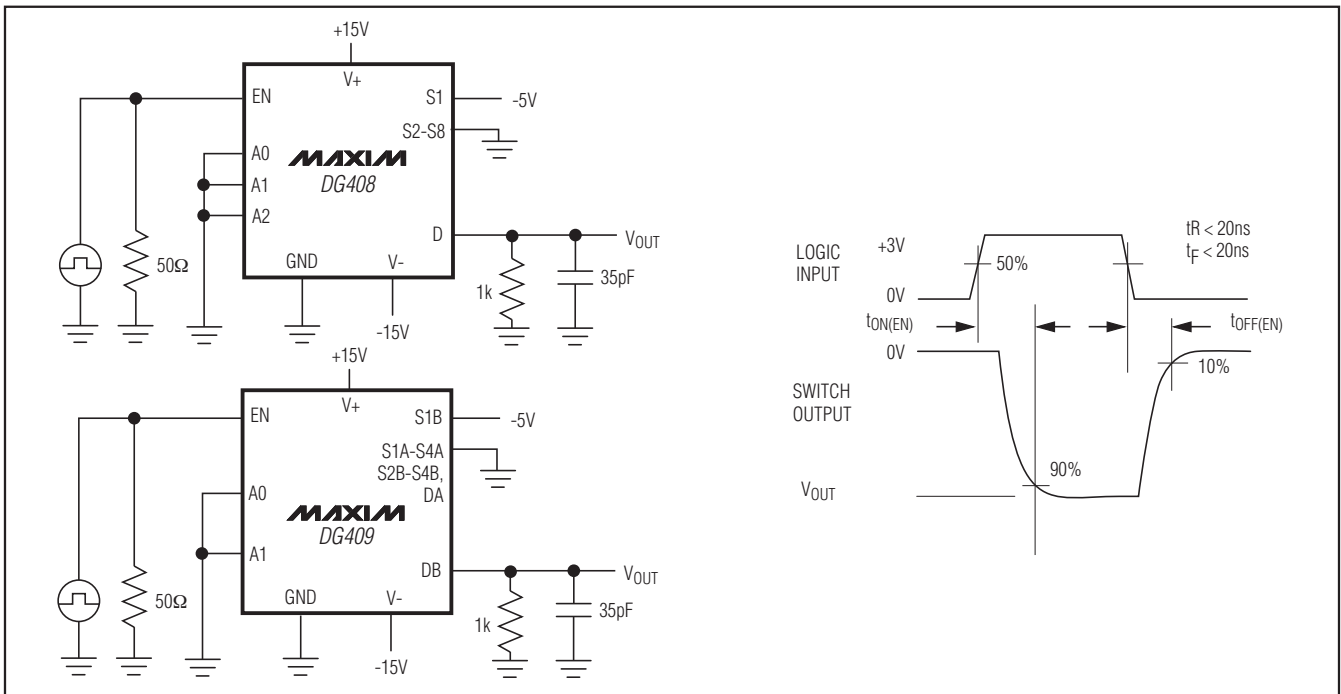


Figure 3. Enable Switching Time

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Test Circuits/Timing Diagrams (continued)

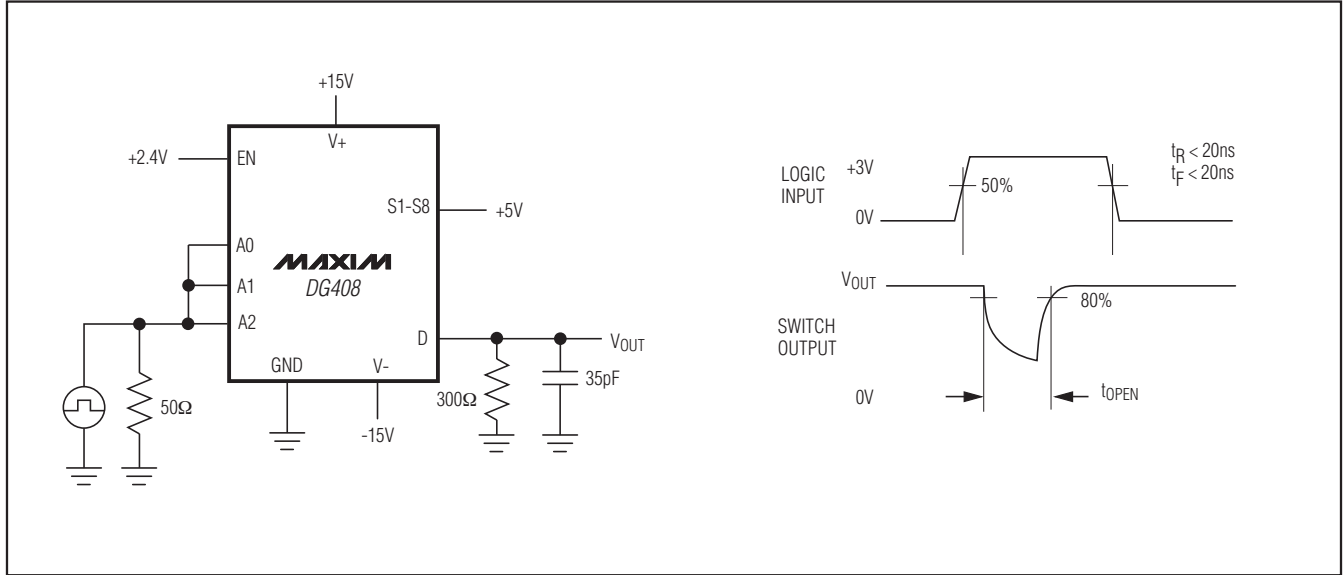


Figure 4. Break-Before-Make Interval

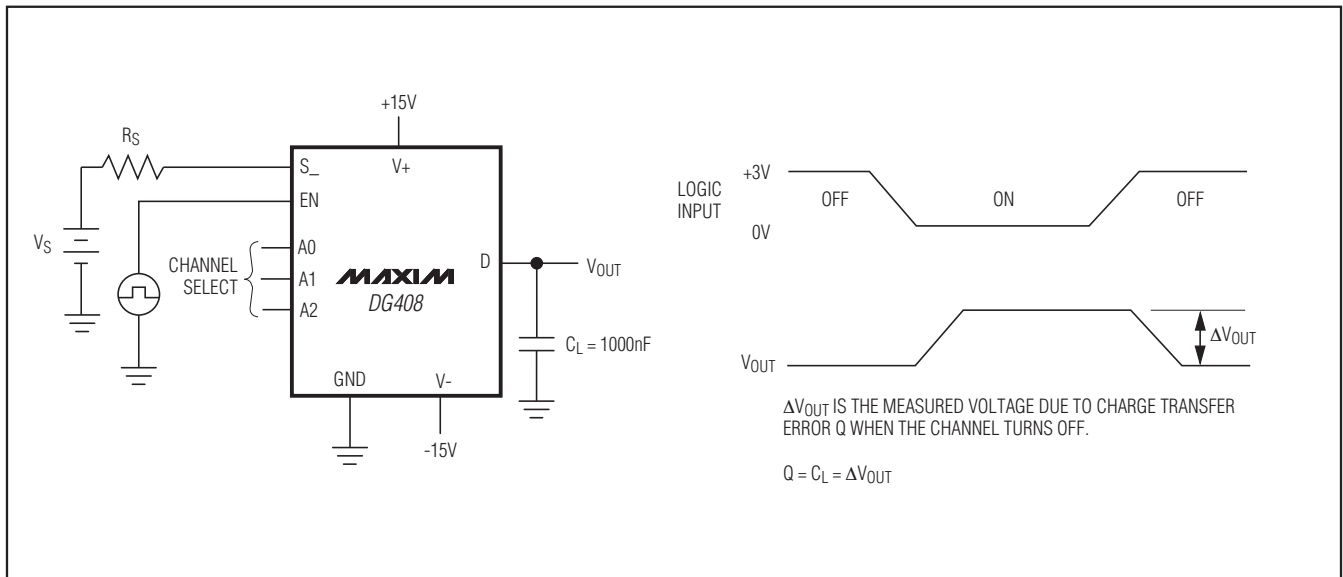


Figure 5. Charge Injection

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Test Circuits/Timing Diagrams (continued)

DG408/DG409

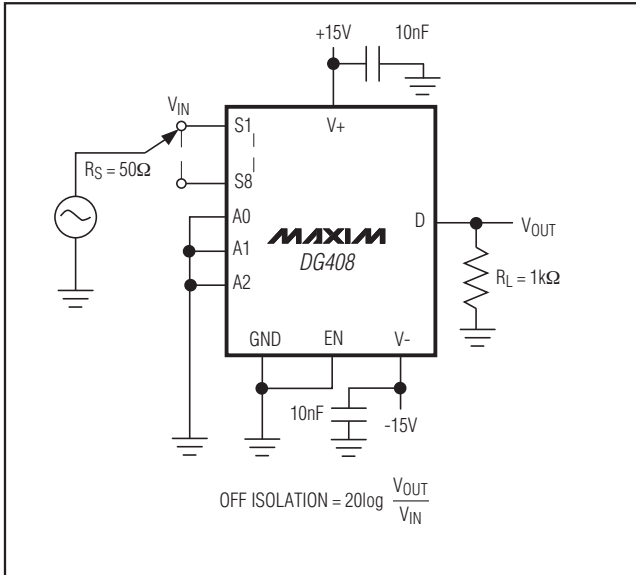


Figure 6. Off Isolation

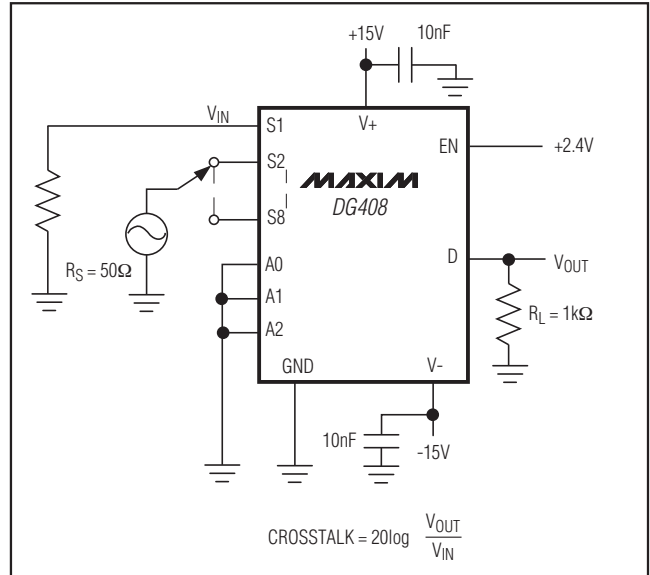


Figure 7. Crosstalk

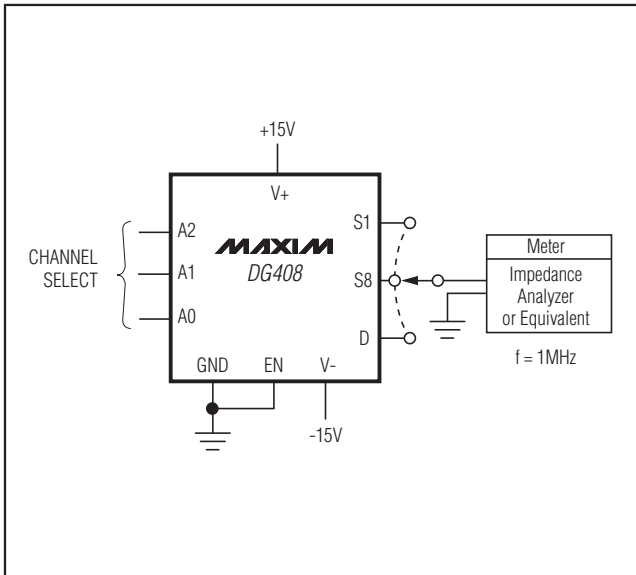
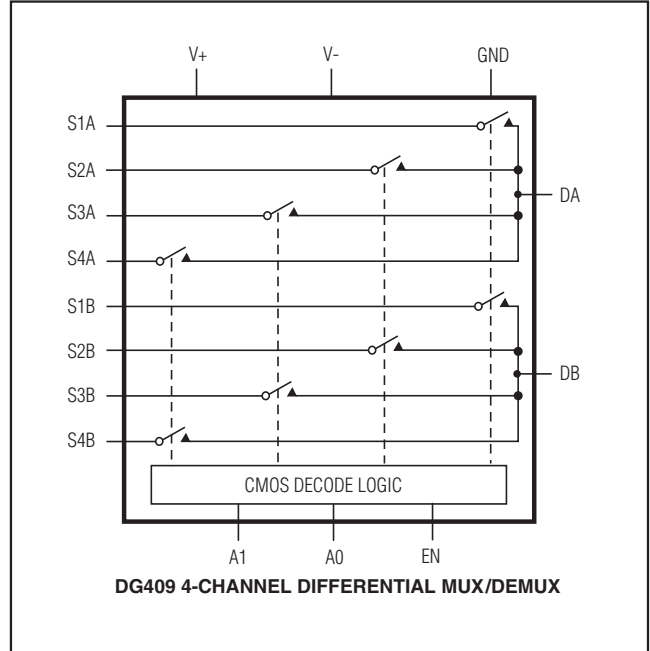
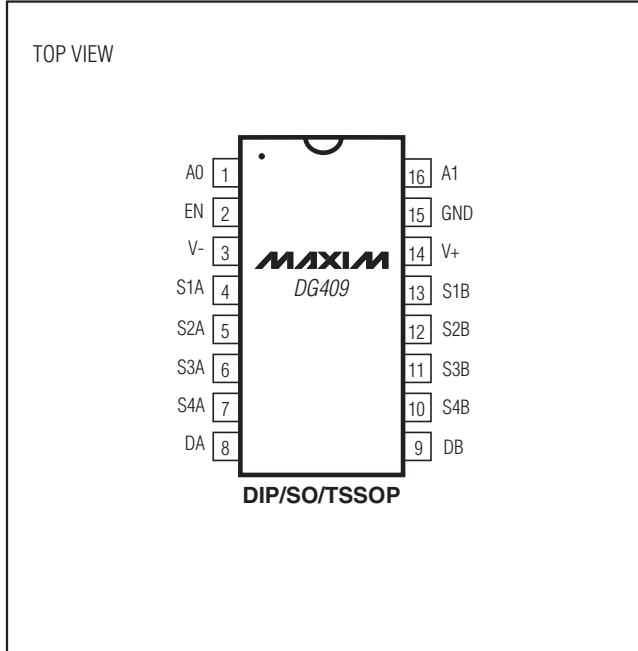


Figure 8. Source/Drain Capacitance

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Pin Configurations/Functional Diagrams/Truth Tables (continued)



A2	A1	A0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG408

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

A1	A0	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

DG409

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

Improved, 8-Channel/Dual 4-Channel, CMOS Analog Multiplexers

DG408/DG409

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DG408DK	-40°C to +85°C	16 CERDIP
DG408AK	-55°C to +125°C	16 CERDIP**
DG408MY/PR	-55°C to +125°C	16 SO***
DG408MY/PR-T	-55°C to +125°C	16 SO***
DG409CUE	0°C to +70°C	16 TSSOP
DG409CJ	0°C to +70°C	16 Plastic DIP
DG409CY	0°C to +70°C	16 Narrow SO
DG409C/D	0°C to +70°C	Dice*
DG409EUE	-40°C to +85°C	16 TSSOP
DG409DJ	-40°C to +85°C	16 Plastic DIP
DG409DK	-40°C to +85°C	16 CERDIP
DG409AK	-55°C to +125°C	12 CERDIP**
DG409MY/PR	-55°C to +125°C	16 SO***
DG409MY/PR-T	-55°C to +125°C	16 SO***

*Contact factory for dice specifications.

**Contact factory for availability and processing to MIL-STD-883.

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 TSSOP	U16-1	21-0066
16 Plastic DIP	P16-2	21-0043
16 Narrow SO	S16-5	21-0041
16 SO	S16-5	21-0041
16 CERDIP	J16-3	21-0590

Improved, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	8/02	Changed operating voltage and TSSOP packaging	—
4	9/08	Added rugged plastic information	1, 11

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