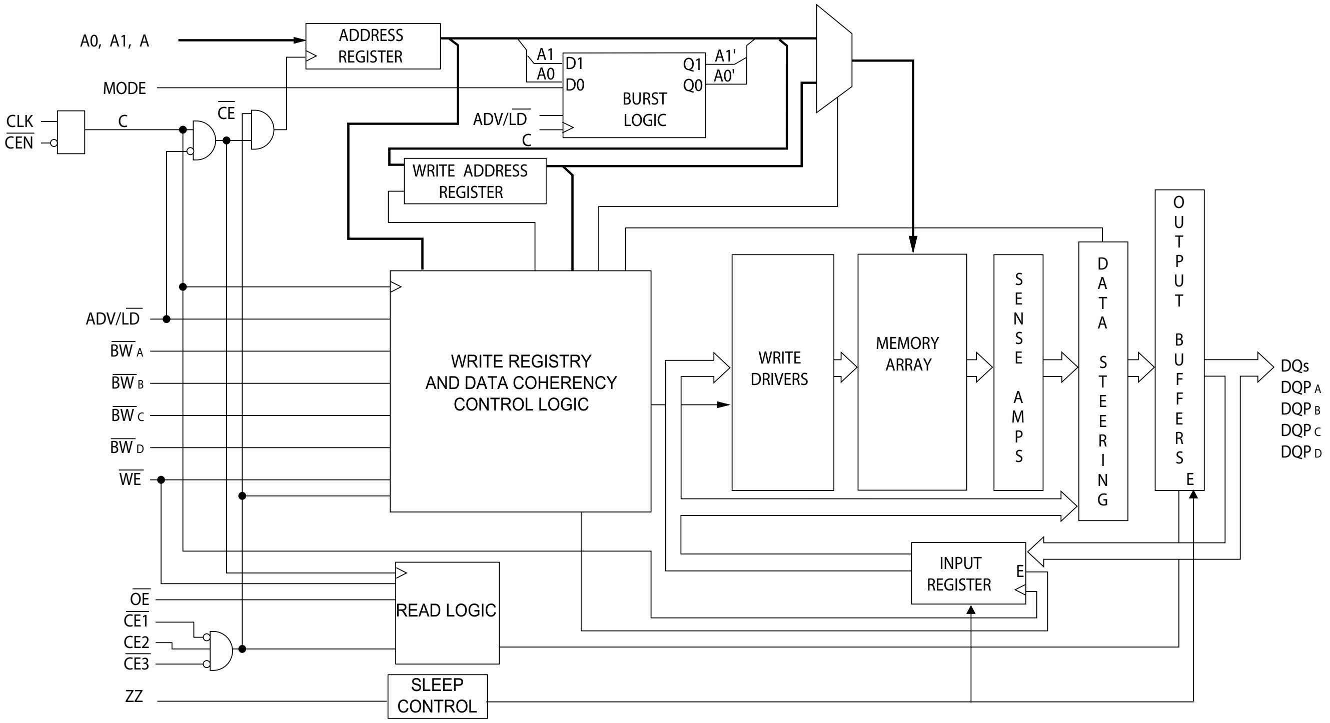
Logic Block Diagram – CY7C1461KV33



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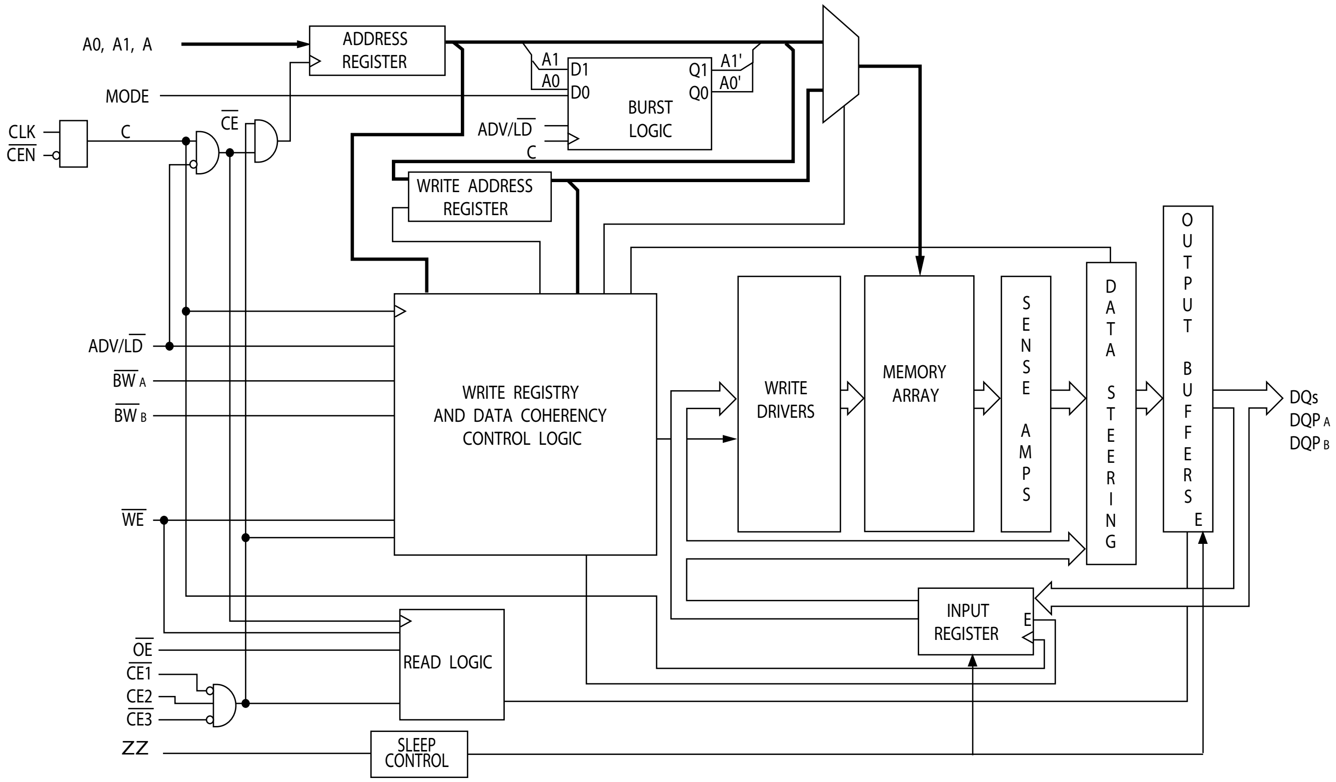

Contents

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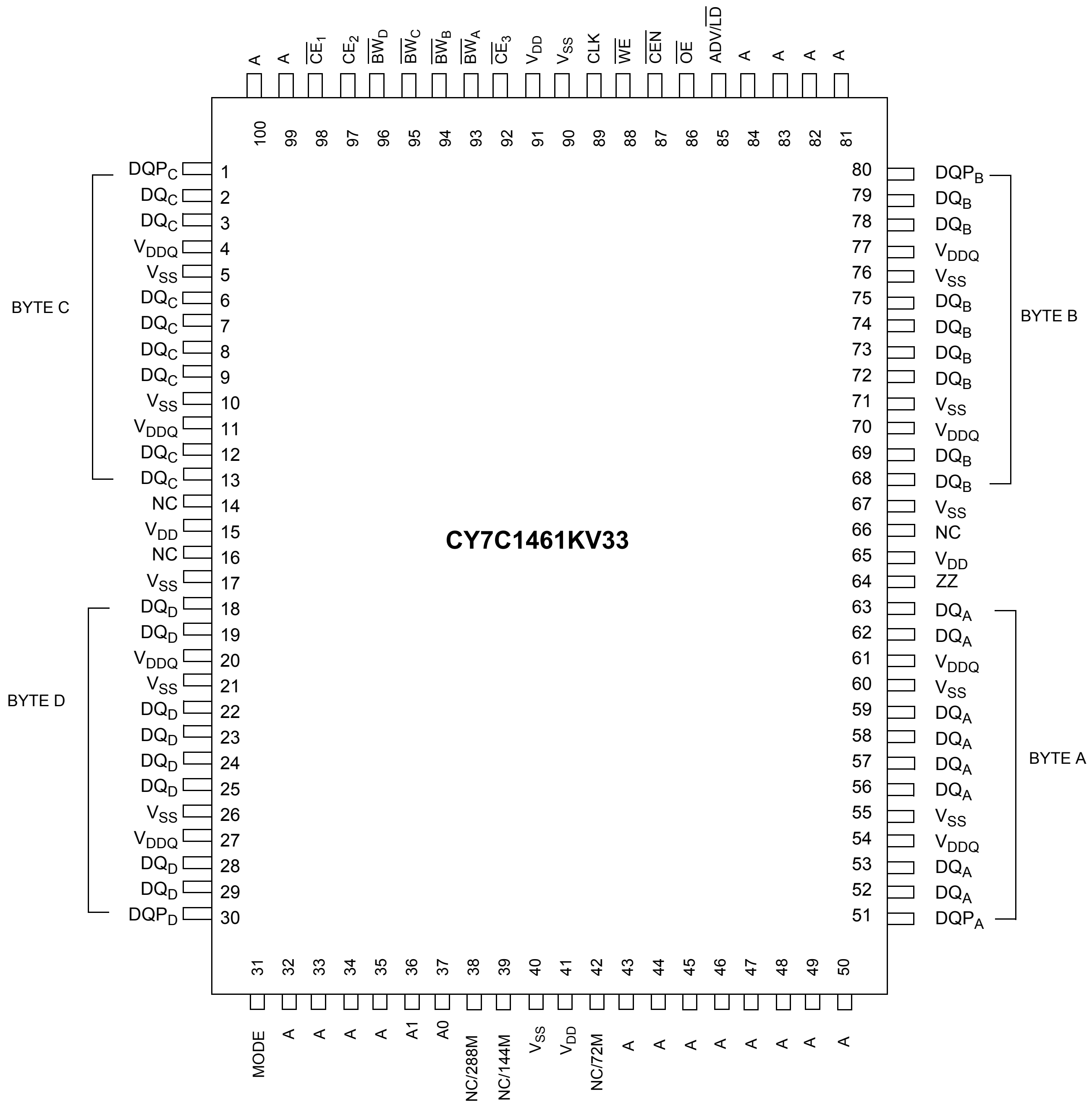
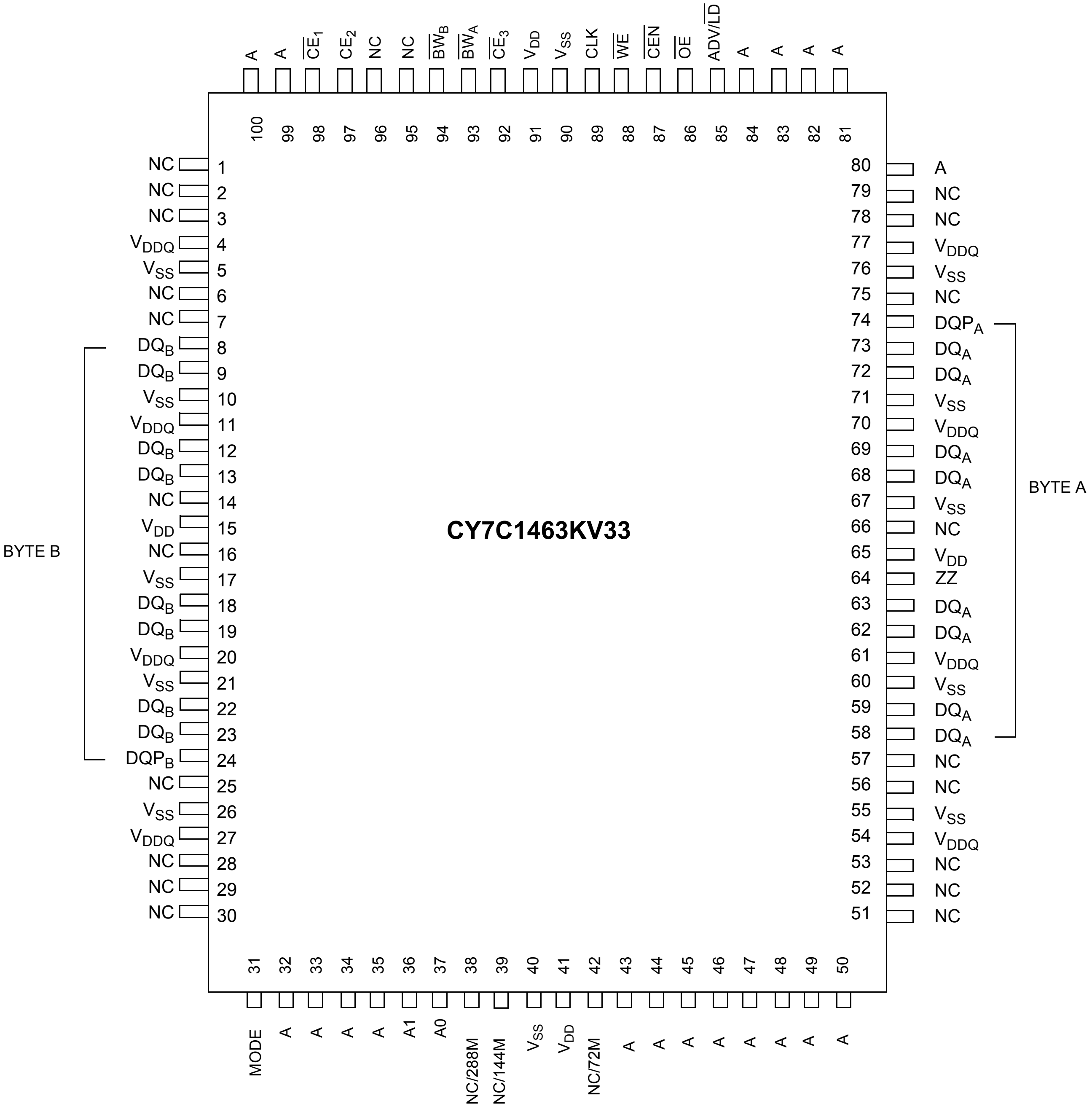
Figure 1. 100-pin TQFP pinout



Pin Configurations (continued)

Figure 2. 100-pin TQFP pinout



Pin Definitions

Pin Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs**. Used to select one of the address locations. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$	Input-Synchronous	**Byte Write Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance or Load Input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After deselecting, drive ADV/$\overline{LD}$ LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select or deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select or deselect the device.
$\overline{CE_3}$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select or deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Because deasserting $\overline{CEN}$ does not deselect the device, use $\overline{CEN}$ to extend the previous cycle when required.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non time critical sleep condition with data integrity preserved. During normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and $DQP_{[A:D]}$ are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_X is controlled by $\overline{BW_X}$ correspondingly.
MODE	Input Strap Pin	**Mode Input.** Selects the burst order of the device. When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for I/O Circuitry**.
V_{SS}	Ground	**Ground for the Device**.
NC	N/A	**No Connects**. Not internally connected to the die.
NC/72M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.

Pin Definitions (continued)

Pin Name	I/O	Description
NC/576M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/1G	N/A	**Not Connected to the Die**. Can be tied to any voltage level.

Functional Overview

The CY7C1461KV33/CY7C1463KV33 are synchronous flow through burst SRAMs designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

Accesses can be initiated by asserting all three chip enables (CE$_1$, CE$_2$, CE$_3$) active at the rising edge of the clock. If CEN is active LOW and ADV/LD is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable (WE). BW$_X$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable (WE). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables (CE$_1$, CE$_2$, CE$_3$) and an asynchronous output enable (OE) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/LD must be driven LOW after the device is deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- CEN is asserted LOW
- CE$_1$, CE$_2$, and CE$_3$ are ALL asserted active
- The write enable input signal WE is deasserted HIGH
- ADV/LD is asserted LOW

The address presented to the address inputs is latched into the address register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133 MHz device) provided OE is active LOW. After the first clock of the read access, the output buffers are controlled by OE and the internal control logic. OE must be driven LOW for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

Burst Read Accesses

The CY7C1461KV33/CY7C1463KV33 have an on-chip burst counter that provides the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW to load a new address into the SRAM, as described in Single Read Accesses. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/LD increments the internal burst counter regardless of the state of chip enable inputs or WE. WE is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) CE$_1$, CE$_2$, and CE$_3$ are ALL asserted active, and (3) the write signal WE is asserted LOW. The address presented to the address bus is loaded into the address register. The write signals are latched into the control logic block. The data lines are automatically tri-stated regardless of the state of the OE input signal. This allows the external logic to present the data on DQs and DQP$_X$.

On the next clock rise the data presented to DQs and DQP$_X$ (or a subset for byte write operations, see Truth Table on page 10 for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by BW$_X$ signals. The CY7C1461KV33/CY7C1463KV33 provide byte write capability that is described in the truth table. Asserting the (WE) with the selected byte write select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism is provided to simplify the write operations. Byte write capability is included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1461KV33/CY7C1463KV33 are common I/O devices, data must not be driven into the device when the outputs are active. The OE can be deasserted HIGH before presenting data to the DQs and DQP$_X$ inputs. This tri-states the output drivers. As a safety precaution, DQs and DQP$_X$ are automatically tri-stated during the data portion of a write cycle, regardless of the state of OE.

Burst Write Accesses

The CY7C1461KV33/CY7C1463KV33 have an on-chip burst counter that provides the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/$\overline{\text{LD}}$ must be driven LOW to load the initial address, as described in the Single Write Accesses section. When ADV/$\overline{\text{LD}}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{\text{CE}}_1$, CE$_2$, and $\overline{\text{CE}}_3$) and $\overline{\text{WE}}$ inputs are ignored and the burst counter is incremented. The correct $\overline{\text{BW}}_X$ inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. When in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. $\overline{\text{CE}}_1$, CE$_2$, and $\overline{\text{CE}}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	75	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1461KV33/CY7C1463KV33 follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE}_1$	CE_2	$\overline{CE}_3$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW}_X$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-State
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-State
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-State
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-State
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-State
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	–
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tri-State

Notes

1. X = “Don't Care.” H = logic HIGH, L = logic LOW. $\overline{BW}x$ = L signifies at least one byte write select is active, $\overline{BW}x$ = Valid signifies that the desired byte write selects are asserted, see truth table for details.
2. Write is defined by $\overline{BW}_X$, and $\overline{WE}$. See truth table for read or write.
3. When a write cycle is detected, all IOs are tri-stated, even during byte writes.
4. The DQs and DQP_X pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. $\overline{CEN}$ = H, inserts wait states.
6. Device powers up deselected and the IOs in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = Tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and DQP_X = data when $\overline{OE}$ is active.

Partial Truth Table for Read/Write

The partial truth table for read/write for CY7C1461KV33 is as follows. [8, 9]

Function (CY7C1461KV33)	$\overline{\text{WE}}$	$\overline{\text{BW}}_A$	$\overline{\text{BW}}_B$	$\overline{\text{BW}}_C$	$\overline{\text{BW}}_D$
Read	H	X	X	X	X
Write – No Bytes Written	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	L	L	H	H	H
Write Byte B – (DQ_B and DQP_B)	L	H	L	H	H
Write Byte C – (DQ_C and DQP_C)	L	H	H	L	H
Write Byte D – (DQ_D and DQP_D)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

Partial Truth Table for Read/Write

The partial truth table for read/write for CY7C1463KV33 is as follows. [8, 9]

Function (CY7C1463KV33)	$\overline{\text{WE}}$	$\overline{\text{BW}}_b$	$\overline{\text{BW}}_a$
Read	H	X	X
Write – No Bytes Written	L	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	L
Write Byte b – (DQ_b and DQP_b)	L	L	H
Write Both Bytes	L	L	L

Notes

8. X = “Don't Care.” H = logic HIGH, L = logic LOW. $\overline{\text{BW}}$x = L signifies at least one byte write select is active, $\overline{\text{BW}}$x = Valid signifies that the desired byte write selects are asserted, see truth table for details.
9. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{\text{BW}}_X$ is valid. Appropriate write is done based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to $+V_{DD}$

DC Voltage Applied to Outputs in Tri-State ....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / +10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single-Bit Upsets	25 °C	<5	5	FIT/ Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single Event Latch up	85 °C	0	0.1	FIT/ Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN54908 “Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates”.

Electrical Characteristics

Over the Operating Range

Parameter [10, 11]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage	–	3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O	3.135	V_{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage[10]	for 3.3 V I/O	2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O	1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[10]	for 3.3 V I/O	–0.3	0.8	V
		for 2.5 V I/O	–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input current of MODE	Input = V_{SS}	–30	–	µA
		Input = V_{DD}	–	5	µA
	Input current of ZZ	Input = V_{SS}	–5	–	µA
		Input = V_{DD}	–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled	–5	5	µA

Notes

[10] Overshoot: $V_{IH}(AC) < V_{DD}$ + 1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2$ V (Pulse width less than $t_{CYC}/2$).

[11] $T_{Power-up}$: Assumes a linear ramp from 0 V to V_{DD}(min.) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [10, 11]	Description	Test Conditions			Min	Max	Unit
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	7.5 ns cycle, 133 MHz	× 18	–	150	mA
				× 36	–	170	
I_{SB1}	Automatic CE power down current – TTL inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}, Inputs Switching	7.5 ns cycle, 133 MHz	× 18	–	85	mA
				× 36	–	90	
I_{SB2}	Automatic CE Power down current – CMOS inputs	V_{DD} = Max, Device Deselected, $V_{IN} \leq$ 0.3 V or $V_{IN} \geq V_{DD}$ – 0.3 V, f = 0, Inputs Static	7.5 ns cycle, 133 MHz	× 18	–	75	mA
				× 36		80	
I_{SB3}	Automatic CE power down current – CMOS inputs	V_{DD} = Max, Device Deselected, $V_{IN} \leq$ 0.3 V or $V_{IN} \geq V_{DDQ}$ – 0.3 V, f = f_{MAX}, Inputs Switching	7.5 ns cycle, 133 MHz	× 18	–	85	mA
				× 36		90	
I_{SB4}	Automatic CE power down current – TTL inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{DD}$ – 0.3 V or $V_{IN} \leq$ 0.3 V, f = 0, Inputs Static	7.5 ns cycle, 133 MHz	× 18	–	75	mA
				× 36	–	80	

Capacitance

In the following table, the capacitance parameters are listed.

Parameter [12]	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
C_{IO}	Input/output capacitance		5	pF

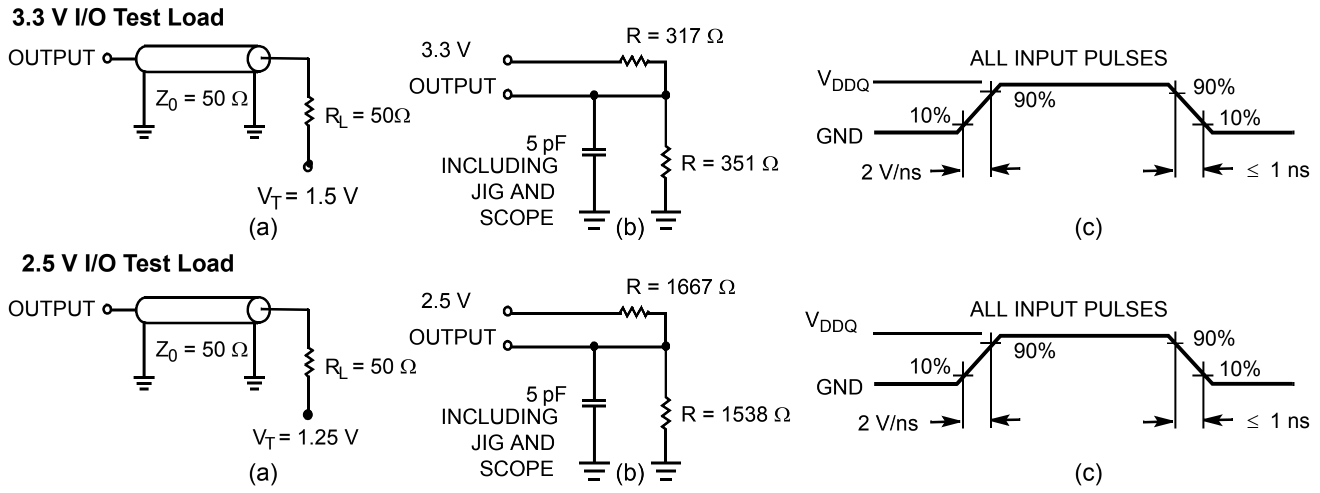
Thermal Resistance

In the following table, the thermal resistance parameters are listed.

Parameter [12]	Description	Test Conditions		100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	With Still Air (0 m/s)	35.36	°C/W
			With Air Flow (1 m/s)	31.30	°C/W
			With Air Flow (3 m/s)	28.86	°C/W
Θ_{JC}	Thermal resistance (junction to case)		–	7.52	°C/W
Θ_{JB}	Thermal resistance (junction to board)			28.89	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Note

12. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

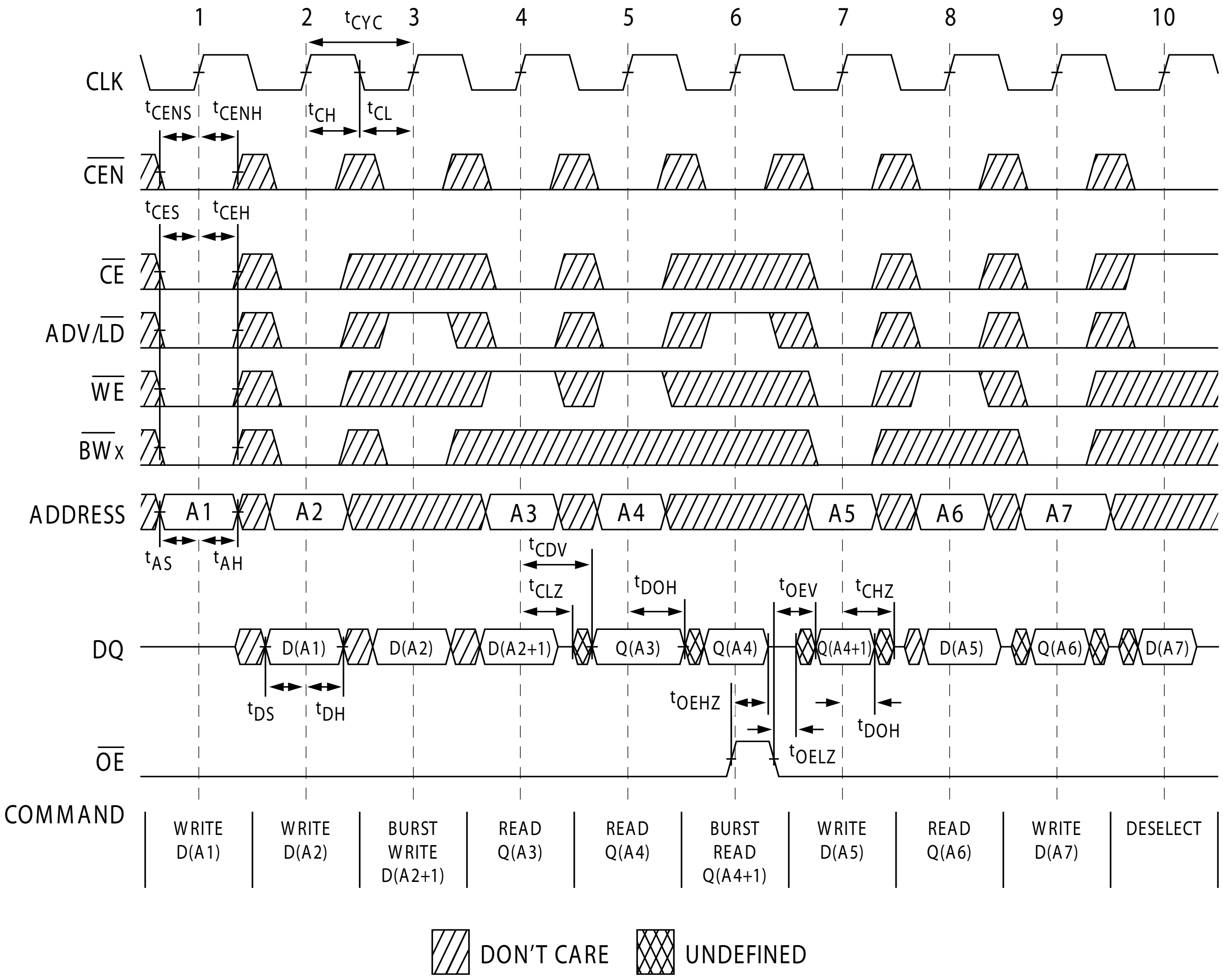
Parameter [13, 14]	Description	133 MHz		Unit
		Min	Max	
t_{POWER}[15]	–	1	–	ms
Clock				
t_{CYC}	Clock Cycle Time	7.5	–	ns
t_{CH}	Clock HIGH	2.5	–	ns
t_{CL}	Clock LOW	2.5	–	ns
Output Times				
t_{CDV}	Data Output Valid After CLK Rise	–	6.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.5	–	ns
t_{CLZ}	Clock to Low Z [16, 17, 18]	2.5	–	ns
t_{CHZ}	Clock to High Z [16, 17, 18]	–	3.8	ns
t_{OEV}	$\overline{\text{OE}}$ LOW to Output Valid	–	3.0	ns
t_{OELZ}	$\overline{\text{OE}}$ LOW to Output Low Z [16, 17, 18]	0	–	ns
t_{OEHZ}	$\overline{\text{OE}}$ HIGH to Output High Z [16, 17, 18]	–	3.0	ns
Setup Times				
t_{AS}	Address Setup Before CLK Rise	1.5	–	ns
t_{ALS}	ADV/$\overline{\text{LD}}$ Setup Before CLK Rise	1.5	–	ns
t_{WES}	$\overline{\text{WE}}$, $\overline{\text{BW}}_X$ Setup Before CLK Rise	1.5	–	ns
t_{CENS}	$\overline{\text{CEN}}$ Setup Before CLK Rise	1.5	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.5	–	ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.5	–	ns
Hold Times				
t_{AH}	Address Hold After CLK Rise	0.5	–	ns
t_{ALH}	ADV/$\overline{\text{LD}}$ Hold After CLK Rise	0.5	–	ns
t_{WEH}	$\overline{\text{WE}}$, $\overline{\text{BW}}_X$ Hold After CLK Rise	0.5	–	ns
t_{CENH}	$\overline{\text{CEN}}$ Hold After CLK Rise	0.5	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.5	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5	–	ns

Notes

13. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
14. Test conditions shown in (a) of Figure 3 on page 14 unless otherwise noted.
15. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially, before a read or write operation can be initiated.
16. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 3 on page 14. Transition is measured ± 200 mV from steady-state voltage.
17. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
18. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 4. Read/Write Waveforms [19, 20, 21]



Notes

19. For this waveform ZZ is tied LOW.
20. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
21. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

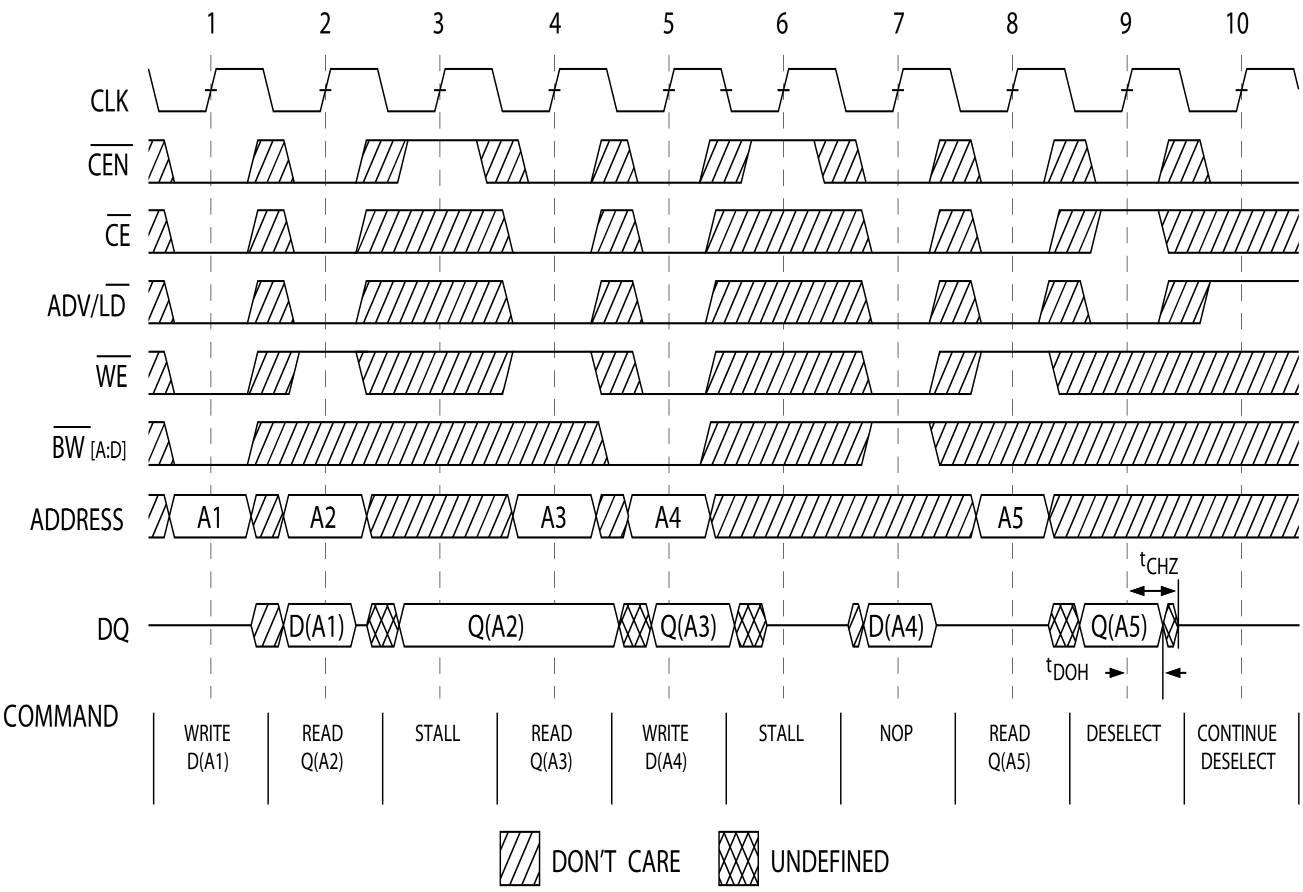


Figure 5. NOP, STALL, and DESELECT Cycles [22, 23, 24]

Notes

[22] For this waveform ZZ is tied LOW.

[23] When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

[24] The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

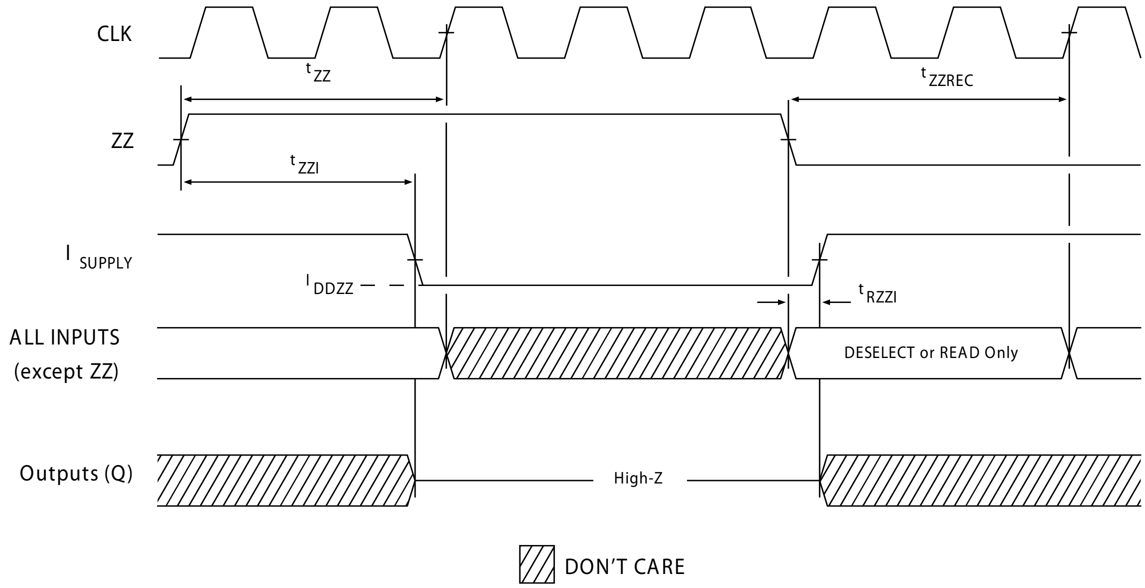


Figure 6. ZZ Mode Timing [25, 26]

Notes

[25] Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.

[26] DQs are in High Z when exiting ZZ sleep mode.

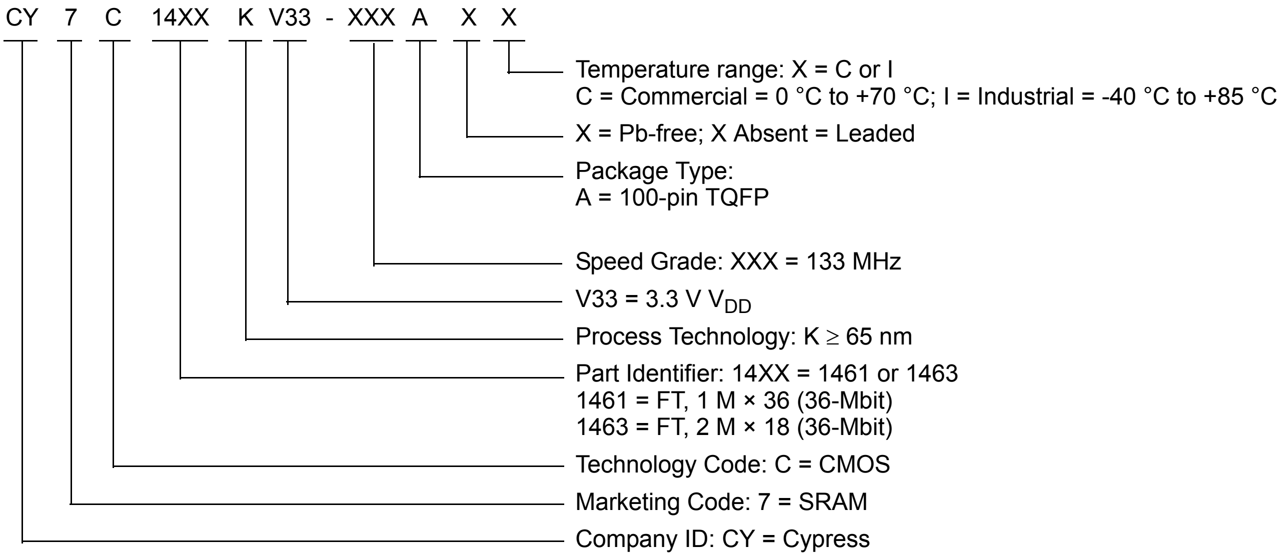
Ordering Information

Table 1 lists the ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Ordering Information

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1461KV33-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1463KV33-133AXC			
	CY7C1461KV33-133AXI			Industrial

Ordering Code Definitions



Temperature range: X = C or I
C = Commercial = 0 °C to +70 °C; I = Industrial = -40 °C to +85 °C

X = Pb-free; X Absent = Leaded

Package Type:
A = 100-pin TQFP

Speed Grade: XXX = 133 MHz

V33 = 3.3 V V_{DD}

Process Technology: K $\geq$ 65 nm

Part Identifier: 14XX = 1461 or 1463
1461 = FT, 1 M × 36 (36-Mbit)
1463 = FT, 2 M × 18 (36-Mbit)

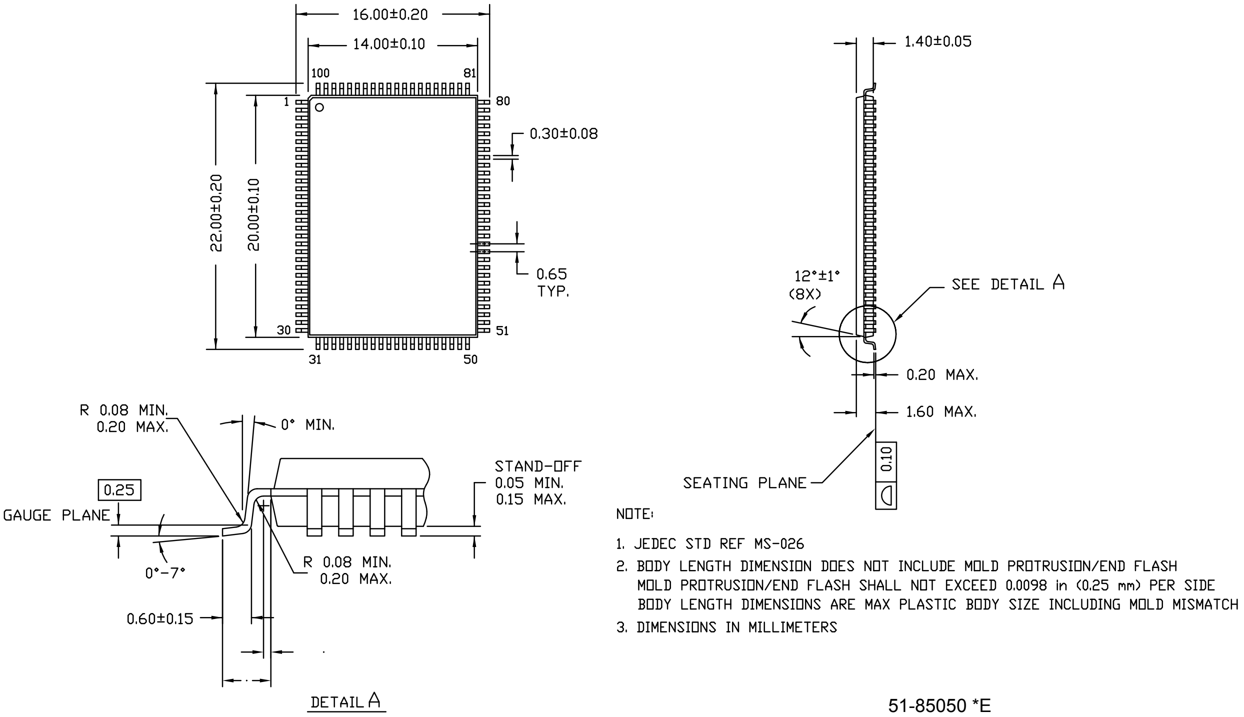
Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress

Package Diagram

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *E

Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
$\overline{CE}$	Chip Enable
$\overline{CEN}$	Clock Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1461KV33/CY7C1463KV33, 36-Mbit (1M × 36/2M × 18) Flow-Through SRAM with NoBL™ Architecture
Document Number: 001-66681

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*E	4680529	04/09/2015	PRIT	Changed status from Preliminary to Final.
*F	4757974	05/07/2015	DEVM	Updated Functional Overview: Updated ZZ Mode Electrical Characteristics: Changed maximum value of I_{DDZZ} parameter from 89 mA to 75 mA.
*G	5298825	06/07/2016	PRIT	Added Industrial Temperature Range related information in all instances across the document. Updated Neutron Soft Error Immunity: Updated details in “Typ” and “Max” columns corresponding to LSBU parameter. Updated Ordering Information: Updated part numbers. Updated to new template.

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