## Logic Block Diagram – CY7C1303BV25

D$_{[17:0]}$  18

A$_{(18:0)}$  19

Address Register

$\overline{K}$

K

CLK Gen.

V$_{REF}$
$\overline{WPS}$
$\overline{BWS_0}$
$\overline{BWS_1}$

Control Logic

Write Data Reg

Write Data Reg

Write Add. Decode

512 K × 18 Memory Array

512 K × 18 Memory Array

Read Add. Decode

Read Data Reg.

Address Register

A$_{(18:0)}$  19

Control Logic

$\overline{RPS}$

C

$\overline{C}$

36  18

18

18

Reg.

Reg.

Reg.

18

18

18

Q$_{[17:0]}$

# Contents

## Pin Configuration

**Figure 1.  165-ball FBGA (13 × 15 × 1.4 mm) pinout**

**CY7C1303BV25 (1M × 18)**

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|----|----|
| **A** | NC | Gnd/144 M | NC/36 M | $\overline{\text{WPS}}$ | $\overline{\text{BWS}}_1$ | $\overline{\text{K}}$ | NC | $\overline{\text{RPS}}$ | A | Gnd/72 M | NC |
| **B** | NC | Q9 | D9 | A | NC | K | $\overline{\text{BWS}}_0$ | A | NC | NC | Q8 |
| **C** | NC | NC | D10 | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | Q7 | D8 |
| **D** | NC | D11 | Q10 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | D7 |
| **E** | NC | NC | Q11 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | D6 | Q6 |
| **F** | NC | Q12 | D12 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | Q5 |
| **G** | NC | D13 | Q13 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | D5 |
| **H** | NC | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | NC | NC | D14 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | Q4 | D4 |
| **K** | NC | NC | Q14 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | D3 | Q3 |
| **L** | NC | Q15 | D15 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | Q2 |
| **M** | NC | NC | D16 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | Q1 | D2 |
| **N** | NC | D17 | Q16 | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | D1 |
| **P** | NC | NC | Q17 | A | A | C | A | A | NC | D0 | Q0 |
| **R** | TDO | TCK | A | A | A | $\overline{\text{C}}$ | A | A | A | TMS | TDI |

## Pin Definitions

| Name | I/O | Description |
|---|---|---|
| $D_{[x:0]}$ | Input-Synchronous | **Data input signals, sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations.** CY7C1303BV25 – $D_{[17:0]}$ |
| $\overline{WPS}$ | Input-Synchronous | **Write Port Select, active LOW.** Sampled on the rising edge of the K clock. When asserted active, a Write operation is initiated. Deasserting deselects the Write port. Deselecting the Write port causes $D_{[x:0]}$ to be ignored. |
| $\overline{BWS}_0$, $\overline{BWS}_1$ | Input-Synchronous | **Byte Write Select 0 and 1- active LOW.** Sampled on the rising edge of the K and $\overline{K}$ clocks during Write operations. Used to select which byte is written into the device during the current portion of the Write operations. CY7C1303BV25 - $\overline{BWS}_0$ controls $D_{[8:0]}$ and $\overline{BWS}_1$ controls $D_{[17:9].]}$ Bytes not written remain unaltered. Deselecting a Byte Write Select causes the corresponding byte of data to be ignored and not written into the device. |
| A | Input-Synchronous | **Address Inputs.** Sampled on the rising edge of the K clock during active Read operations and on the rising edge of $\overline{K}$ for Write operations. These address inputs are multiplexed for both Read and Write operations. Internally, the device is organized as 1M × 18 (2 arrays each of 512K × 18) for CY7C1303BV25. Therefore, only 19 address inputs are needed to access the entire memory array of CY7C1303BV25. These inputs are ignored when the appropriate port is deselected. |
| $Q_{[x:0]}$ | Outputs-Synchronous | **Data Output signals.** These pins drive out the requested data during a Read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during Read operations or K and $\overline{K}$ when in single clock mode. When the Read port is deselected, $Q_{[x:0]}$ are automatically three-stated. CY7C1303BV25 - $Q_{[17:0]}$ |
| $\overline{RPS}$ | Input-Synchronous | **Read Port Select, active LOW.** Sampled on the rising edge of positive input clock (K). When active, a Read operation is initiated. Deasserting causes the Read port to be deselected. When deselected, the pending access is allowed to complete and the output drivers are automatically three-stated following the next rising edge of the K clock. Each read access consists of a burst of two sequential 18-bit transfers. |
| C | Input-Clock | **Positive Input Clock for Output Data**. C is used in conjunction with $\overline{C}$ to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details. |
| $\overline{C}$ | Input-Clock | **Negative Input Clock for Output Data**. $\overline{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details. |
| K | Input-Clock | **Positive Input Clock Input.** The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K. |
| $\overline{K}$ | Input-Clock | **Negative Input Clock Input.** $\overline{K}$ is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. |
| ZQ | Input | **Output Impedance Matching Input.** This input is used to tune the device outputs to the system data bus impedance. $Q_{[x:0]}$ output impedance are set to 0.2 × RQ, where RQ is a resistor connected between ZQ and ground. Alternately, this pin can be connected directly to $V_{DDQ}$, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected. |
| TDO | Output | **TDO pin for JTAG**. |
| TCK | Input | **TCK pin for JTAG**. |
| TDI | Input | **TDI pin for JTAG**. |
| TMS | Input | **TMS pin for JTAG**. |
| NC/36M | N/A | **Address expansion for 36M.** This pin is not connected to the die and so can be tied to any voltage level on CY7C1303BV25 |
| GND/72M | Input | **Address expansion for 72M.** This pin has to be tied to GND on CY7C1303BV25. |
| GND/144M | Input | **Address expansion for 144M.** This pin has to be tied to GND on CY7C1303BV25. |
| NC | N/A | **Not connected to the die.** Can be tied to any voltage level. |

## Pin Definitions (continued)

| Name | I/O | Description |
|---|---|---|
| $V_{REF}$ | Input-Reference | **Reference Voltage Input.** Static input used to set the reference level for HSTL inputs and Outputs as well as AC measurement points. |
| $V_{DD}$ | Power Supply | **Power supply inputs to the core of the device**. |
| $V_{SS}$ | Ground | **Ground for the device**. |
| $V_{DDQ}$ | Power Supply | **Power supply inputs for the outputs of the device**. |

## Functional Overview

The CY7C1303BV25 are synchronous pipelined Burst SRAM equipped with both a Read port and a Write port. The Read port is dedicated to Read operations and the Write port is dedicated to Write operations. Data flows into the SRAM through the Write port and out through the Read port. These devices multiplex the address inputs in order to minimize the number of address pins required. By having separate Read and Write ports, this architecture completely eliminates the need to "turn-around" the data bus and avoids any possible data contention, thereby simplifying system design. Each access consists of two 18-bit data transfers in the case of CY7C1303BV25, in one clock cycle.

Accesses for both ports are initiated on the rising edge of the Positive Input Clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and $\overline{K}$) and all output timings are referenced to rising edge of output clocks (C and $\overline{C}$ or K and $\overline{K}$ when in single clock mode).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the output clocks (C and $\overline{C}$, or K and $\overline{K}$ when in single clock mode).

All synchronous control ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS}_{[x:0]}$) inputs pass through input registers controlled by the rising edge of input clocks (K and $\overline{K}$).

The following descriptions take CY7C1303BV25 as an example.

### Read Operations

The CY7C1303BV25 is organized internally as 2 arrays of 512K × 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting $\overline{RPS}$ active at the rising edge of the positive input clock (K). The address is latched on the rising edge of the K clock. Following the next K clock rise the corresponding lower order 18-bit word of data is driven onto the $Q_{[17:0]}$ using C as the output timing reference. On the subsequent rising edge of $\overline{C}$ the higher order data word is driven onto the $Q_{[17:0]}$. The requested data is valid 2.5 ns from the rising edge of the output clock (C and $\overline{C}$, or K and $\overline{K}$ when in single clock mode, 167 MHz device).

Synchronous internal circuitry automatically three-states the outputs following the next rising edge of the positive output clock (C). This allows for a seamless transition between devices without the insertion of wait states in a depth expanded memory.

### Write Operations

Write operations are initiated by asserting $\overline{WPS}$ active at the rising edge of the positive input clock (K). On the same K clock rise the data presented to $D_{[17:0]}$ is latched and stored into the

lower 18-bit Write Data register provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$), the address is latched and the information presented to $D_{[17:0]}$ is stored into the Write Data register provided $\overline{BWS}_{[1:0]}$ are both asserted active. The 36-bits of data are then written into the memory array at the specified location.

When deselected, the Write port ignores all inputs after the pending Write operations have been completed.

### Byte Write Operations

Byte Write operations are supported by the CY7C1303BV25. A Write operation is initiated as described in the Write Operation section above. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$ which are sampled with each set of 18-bit data word. Asserting the appropriate Byte Write Select input during the data portion of a write allows the data being presented to be latched and written into the device. Deasserting the Byte Write Select input during the data portion of a write allows the data stored in the device for that byte to remain unaltered. This feature can be used to simplify Read/Modify/Write operations to a Byte Write operation.

### Single Clock Mode

The CY7C1303BV25 can be used with a single clock mode. In this mode the device recognizes only the pair of input clocks (K and $\overline{K}$) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/$\overline{K}$ and C/$\overline{C}$ clocks. All timing parameters remain the same in this mode. To use this mode of operation, the user must tie C and $\overline{C}$ HIGH at power-up. This function is a strap option and not alterable during device operation.

### Concurrent Transactions

The Read and Write ports on the CY7C1303BV25 operate completely independently of one another. Since each port latches the address inputs on different clock edges, the user can Read or Write to any location, regardless of the transaction on the other port. Also, reads and writes can be started in the same clock cycle. If the ports access the same location at the same time, the SRAM delivers the most recent information associated with the specified address location. This includes forwarding data from a Write cycle that was initiated on the previous K clock rise.

### Depth Expansion

The CY7C1303BV25 has a Port Select input for each port. This allows for easy depth expansion. Both Port Selects are sampled on the rising edge of the Positive Input Clock only (K). Each port select input can deselect the specified port. Deselecting a port

does not affect the other port. All pending transactions (Read and Write) are completed prior to the device being deselected.

## Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and $V_{SS}$ to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5 × the value of the intended line impedance driven by the SRAM, The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 $\Omega$ and 350 $\Omega$, with $V_{DDQ}$ = 1.5 V. The output impedance is adjusted every 1024 cycles to account for drifts in supply voltage and temperature.

## Application Example

Figure 2 shows four QDR I used in an application.

**Figure 2. Application Example**
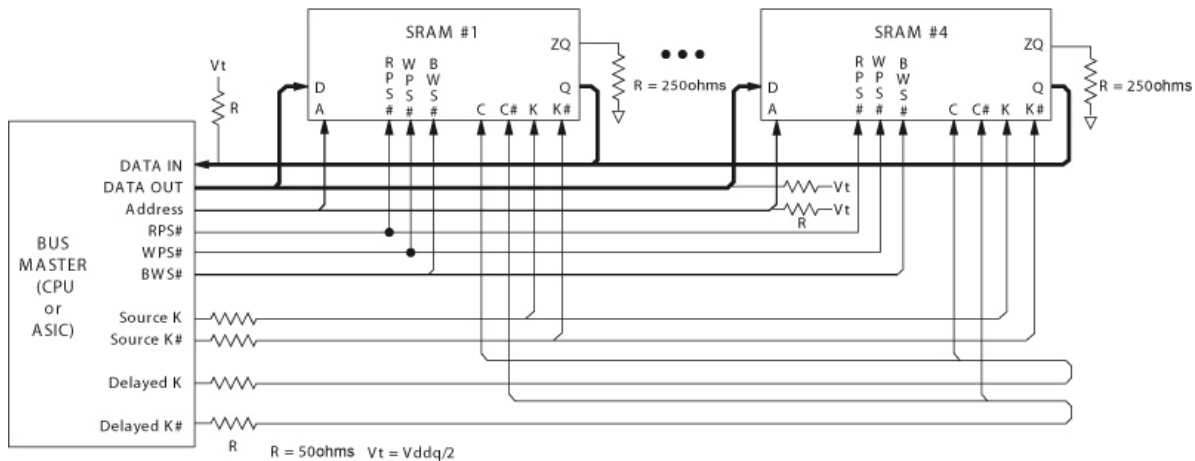
## Truth Table

The truth table for CY7C1303BV25 follow. [1, 2, 3, 4, 5, 6]

| Operation | K | RPS | WPS | DQ | DQ |
|---|---|---|---|---|---|
| Write cycle: <br> Load address on the rising edge of $\overline{K}$ clock; input write data on K and $\overline{K}$ rising edges. | L–H | X | L | D(A+0) at K(t) ↑ | $\underline{D}$(A+1) at $\overline{K}$(t) ↑ |
| Read cycle: <br> Load address on the rising edge of K clock; wait one cycle; read data on 2 consecutive C and $\overline{C}$ rising edges. | L–H | L | X | Q(A+0) at C(t+1)↑ | Q(A+1) at $\overline{C}$(t+1) ↑ |
| NOP: No operation | L–H | H | H | D = X <br> Q = High Z | D = X <br> Q = High Z |
| Standby: Clock stopped | Stopped | X | X | Previous state | Previous state |

## Write Cycle Descriptions

The write cycle description table for CY7C1303BV25 follow. [7, 8]

| $\overline{BWS}_0$ | $\overline{BWS}_1$ | K | $\overline{K}$ | Comments |
|---|---|---|---|---|
| L | L | L–H | – | During the data portion of a Write sequence, both bytes ($D_{[17:0]}$) are written into the device. |
| L | L | – | L–H | During the data portion of a Write sequence, both bytes ($D_{[17:0]}$) are written into the device. |
| L | H | L–H | – | During the data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ remains unaltered. |
| L | H | – | L–H | During the data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ remains unaltered. |
| H | L | L–H | – | During the data portion of a Write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ remains unaltered. |
| H | L | – | L–H | During the data portion of a Write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ remains unaltered. |
| H | H | L–H | – | No data is written into the device during this portion of a write operation. |
| H | H | – | L–H | No data is written into the device during this portion of a write operation. |

**Notes**
1. X = Do not Care, H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
2. Device power-ups deselected and the outputs in a three-state condition.
3. "A" represents address location latched by the devices when transaction was initiated. A + 0, A + 1 represent the addresses sequence in the burst.
4. "t" represents the cycle at which a Read/Write operation is started. t+1 is the first clock cycle succeeding the "t" clock cycle.
5. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on C and $\overline{C}$ rising edges, except when in single clock mode.
6. It is recommended that K = $\overline{K}$ and C = $\overline{C}$ when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. X = Do not Care, H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
8. Assumes a Write cycle was initiated per the Write Port Cycle Description Truth Table. $\overline{BWS}_0$, $\overline{BWS}_1$, in the case of CY7C1303BV25 can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

# IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1 to 1900. The TAP operates using JEDEC standard 2.5 V I/O logic levels.

## Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ($V_{SS}$) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to $V_{DD}$ through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device comes up in a reset state which does not interfere with the operation of the device.

## Test Access Port

### Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

### Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

### Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram on page 11. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

### Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction Codes on page 15). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

## Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

## TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

### Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in TAP Controller Block Diagram on page 12. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

### Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

### Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order on page 16 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

### Identification (ID) Register

The ID register is loaded with a vendor specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions on page 15.

## TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes on page 15. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

### IDCODE

The IDCODE instruction causes a vendor specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

### SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is given during the "Update IR" state.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that are captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times ($t_{CS}$ and $t_{CH}$). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while data captured is shifted out, the preloaded data can be shifted in.

### BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

### EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

### EXTEST Output Bus Tri-state

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at bit #47. When this scan cell, called the "extest output bus tri-state", is latched into the preload register during the "Update-DR" state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the "Shift-DR" state. During "Update-DR", the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the "Test-Logic-Reset" state.

### Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.
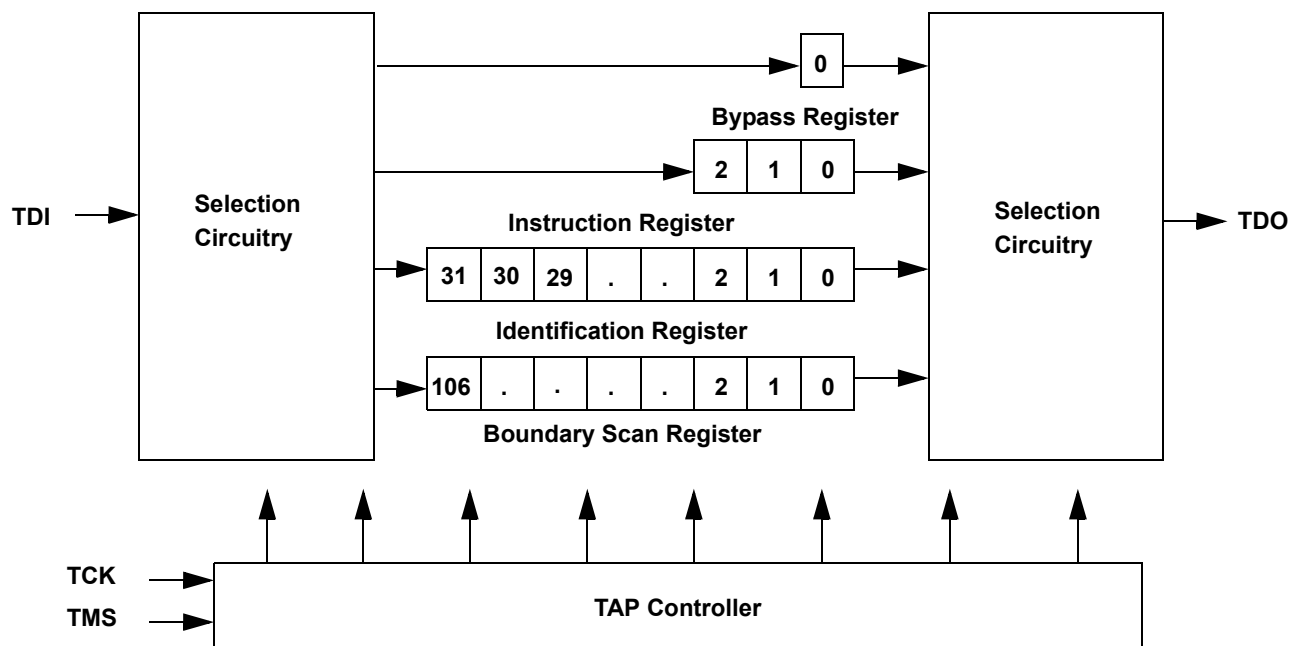
## TAP Controller State Diagram

The state diagram for the TAP controller follows. [9]
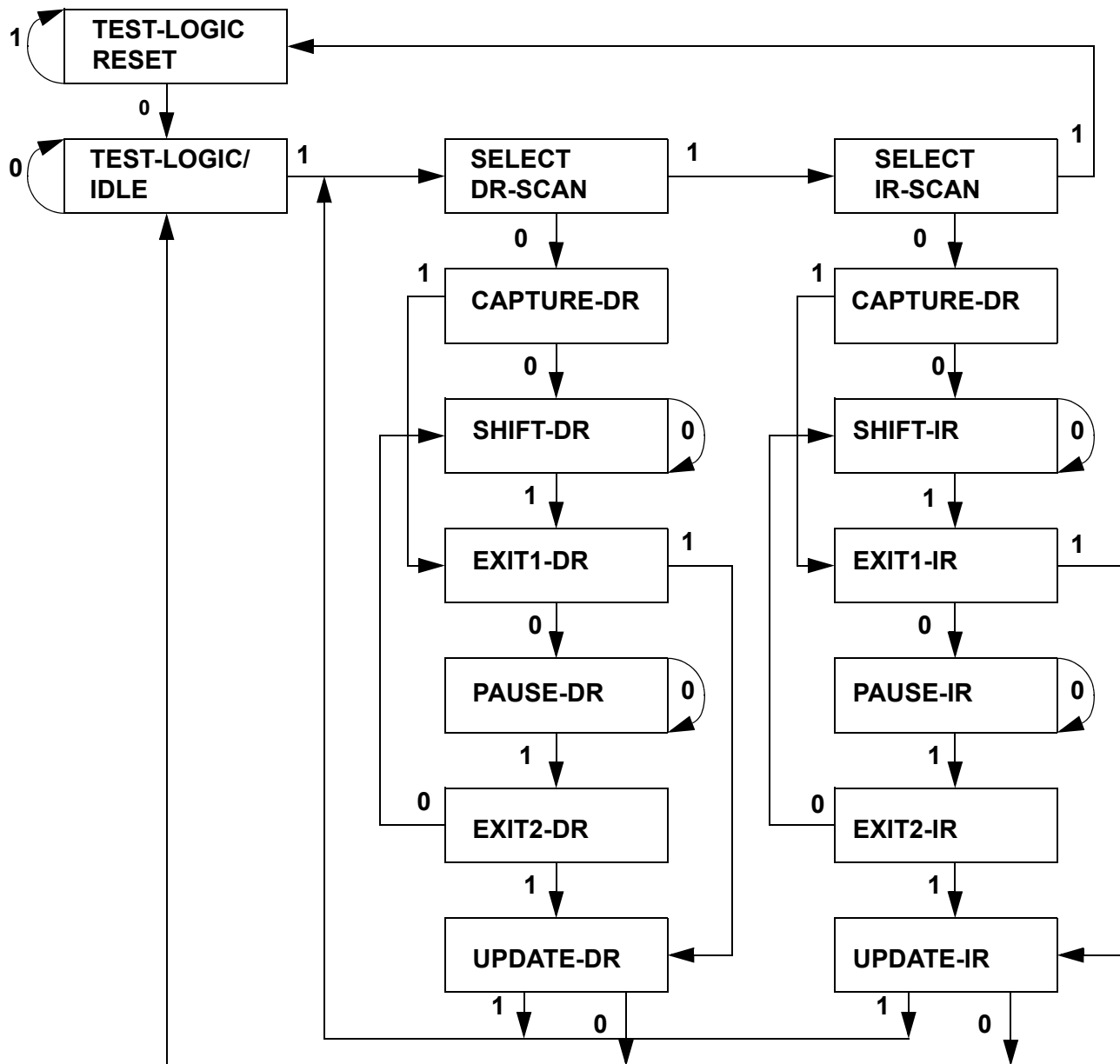
## TAP Controller Block Diagram



## TAP Electrical Characteristics

Over the Operating Range

| Parameter [10, 11, 12] | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH voltage | $I_{OH} = -2.0$ mA | 1.7 | – | V |
| $V_{OH2}$ | Output HIGH voltage | $I_{OH} = -100$ μA | 2.1 | – | V |
| $V_{OL1}$ | Output LOW voltage | $I_{OL} = 2.0$ mA | – | 0.7 | V |
| $V_{OL2}$ | Output LOW voltage | $I_{OL} = 100$ μA | – | 0.2 | V |
| $V_{IH}$ | Input HIGH voltage | | 1.7 | $V_{DD} + 0.3$ | V |
| $V_{IL}$ | Input LOW voltage | | –0.3 | 0.7 | V |
| $I_X$ | Input and output load current | $GND \leq V_I \leq V_{DDQ}$ | –5 | 5 | μA |

**Notes**
10. These characteristic pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics on page 17.
11. Overshoot: $V_{IH(AC)} < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL(AC)} > -1.5$ V (Pulse width less than $t_{CYC}/2$).
12. All Voltage referenced to Ground.

## TAP AC Switching Characteristics

Over the Operating Range

| Parameter [13, 14] | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{TCYC}$ | TCK clock cycle time | 50 | – | ns |
| $t_{TF}$ | TCK clock frequency | – | 20 | MHz |
| $t_{TH}$ | TCK clock HIGH | 20 | – | ns |
| $t_{TL}$ | TCK clock LOW | 20 | – | ns |
| **Setup Times** | | | | |
| $t_{TMSS}$ | TMS setup to TCK clock rise | 10 | – | ns |
| $t_{TDIS}$ | TDI setup to TCK clock rise | 10 | – | ns |
| $t_{CS}$ | Capture setup to TCK rise | 10 | – | ns |
| **Hold Times** | | | | |
| $t_{TMSH}$ | TMS hold after TCK clock rise | 10 | – | ns |
| $t_{TDIH}$ | TDI hold after clock rise | 10 | – | ns |
| $t_{CH}$ | Capture hold after clock rise | 10 | – | ns |
| **Output Times** | | | | |
| $t_{TDOV}$ | TCK clock LOW to TDO valid | – | 20 | ns |
| $t_{TDOX}$ | TCK clock LOW to TDO invalid | 0 | – | ns |

**Notes**
13. $t_{CS}$ and $t_{CH}$ refer to the setup and hold time requirements of latching data from the boundary scan register.
14. Test conditions are specified using the load in TAP AC test conditions. $t_R/t_F$ = 1 ns.

## TAP Timing and Test Conditions

Figure 3 shows the TAP timing and test conditions. [15]

**Figure 3. TAP Timing and Test Conditions**

## Identification Register Definitions

| Instruction Field | Value | Description |
|---|---|---|
| | CY7C1303BV25 | |
| Revision Number (31:29) | 000 | Version number. |
| Cypress Device ID (28:12) | 01011010010010101 | Defines the type of SRAM. |
| Cypress JEDEC ID (11:1) | 00000110100 | Allows unique identification of SRAM vendor. |
| ID Register Presence (0) | 1 | Indicate the presence of an ID register. |

## Scan Register Sizes

| Register Name | Bit Size |
|---|---|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 107 |

## Instruction Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures the I/O ring contents. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation. |
| SAMPLE Z | 010 | Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operation. |

## Boundary Scan Order

| Bit # | Bump ID | Bit # | Bump ID | Bit # | Bump ID | Bit # | Bump ID |
|-------|---------|-------|---------|-------|---------|-------|---------|
| 0 | 6R | 27 | 11H | 54 | 7B | 81 | 3G |
| 1 | 6P | 28 | 10G | 55 | 6B | 82 | 2G |
| 2 | 6N | 29 | 9G | 56 | 6A | 83 | 1J |
| 3 | 7P | 30 | 11F | 57 | 5B | 84 | 2J |
| 4 | 7N | 31 | 11G | 58 | 5A | 85 | 3K |
| 5 | 7R | 32 | 9F | 59 | 4A | 86 | 3J |
| 6 | 8R | 33 | 10F | 60 | 5C | 87 | 2K |
| 7 | 8P | 34 | 11E | 61 | 4B | 88 | 1K |
| 8 | 9R | 35 | 10E | 62 | 3A | 89 | 2L |
| 9 | 11P | 36 | 10D | 63 | 1H | 90 | 3L |
| 10 | 10P | 37 | 9E | 64 | 1A | 91 | 1M |
| 11 | 10N | 38 | 10C | 65 | 2B | 92 | 1L |
| 12 | 9P | 39 | 11D | 66 | 3B | 93 | 3N |
| 13 | 10M | 40 | 9C | 67 | 1C | 94 | 3M |
| 14 | 11N | 41 | 9D | 68 | 1B | 95 | 1N |
| 15 | 9M | 42 | 11B | 69 | 3D | 96 | 2M |
| 16 | 9N | 43 | 11C | 70 | 3C | 97 | 3P |
| 17 | 11L | 44 | 9B | 71 | 1D | 98 | 2N |
| 18 | 11M | 45 | 10B | 72 | 2C | 99 | 2P |
| 19 | 9L | 46 | 11A | 73 | 3E | 100 | 1P |
| 20 | 10L | 47 | Internal | 74 | 2D | 101 | 3R |
| 21 | 11K | 48 | 9A | 75 | 2E | 102 | 4R |
| 22 | 10K | 49 | 8B | 76 | 1E | 103 | 4P |
| 23 | 9J | 50 | 7C | 77 | 2F | 104 | 5P |
| 24 | 9K | 51 | 6C | 78 | 3F | 105 | 5N |
| 25 | 10J | 52 | 8A | 79 | 1G | 106 | 5R |
| 26 | 11J | 53 | 7A | 80 | 1F | | |

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ............................... –65 °C to + 150 °C

Ambient temperature
with power applied .................................. –55 °C to + 125 °C

Supply voltage on $V_{DD}$ relative to GND ...... –0.5 V to + 3.6 V

Supply voltage on $V_{DDQ}$ relative to GND ..... –0.5 V to + $V_{DD}$

DC applied to outputs
in High Z state .................................. –0.5 V to $V_{DDQ}$ + 0.5 V

DC input voltage[16] ........................... –0.5 V to $V_{DD}$ + 0.5 V

Current into outputs (LOW) ........................................ 20 mA

Static discharge voltage
(per MIL-STD-883, Method 3015) ......................... > 2001 V

Latch-up Current .................................................. > 200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$) | $V_{DD}$[17] | $V_{DDQ}$[17] |
|---|---|---|---|
| Commercial | 0 °C to + 70 °C | 2.5 ± 0.1 V | 1.4 V to 1.9 V |

## Neutron Soft Error Immunity

| Parameter | Description | Test Conditions | Typ | Max* | Unit |
|---|---|---|---|---|---|
| LSBU | Logical single-bit upsets | 25 °C | 320 | 368 | FIT/Mb |
| LMBU | Logical multi-bit upsets | 25 °C | 0 | 0.01 | FIT/Mb |
| SEL | Single event latch-up | 85 °C | 0 | 0.1 | FIT/Dev |

\* *No LMBU or SEL events occurred during testing*; this column represents a statistical $\chi^2$, 95% confidence limit calculation. For more details refer to Application Note, Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates – AN54908.

## Electrical Characteristics

Over the Operating Range

### DC Electrical Characteristics

Over the Operating Range

| Parameter [18] | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | 2.4 | 2.5 | 2.6 | V |
| $V_{DDQ}$ | I/O supply voltage | | 1.4 | 1.5 | 1.9 | V |
| $V_{OH}$ | Output HIGH voltage | Note 19 | $V_{DDQ}/2 - 0.12$ | – | $V_{DDQ}/2 + 0.12$ | V |
| $V_{OL}$ | Output LOW voltage | Note 20 | $V_{DDQ}/2 - 0.12$ | – | $V_{DDQ}/2 + 0.12$ | V |
| $V_{OH(LOW)}$ | Output HIGH voltage | $I_{OH}$ = –0.1 mA, nominal impedance | $V_{DDQ} - 0.2$ | – | $V_{DDQ}$ | V |
| $V_{OL(LOW)}$ | Output LOW voltage | $I_{OL}$ = 0.1 mA, nominal impedance | $V_{SS}$ | – | 0.2 | V |
| $V_{IH}$ | Input HIGH voltage [16] | | $V_{REF} + 0.1$ | – | $V_{DDQ} + 0.3$ | V |
| $V_{IL}$ | Input LOW voltage [16, 21] | | –0.3 | – | $V_{REF} - 0.1$ | V |
| $V_{REF}$ | Input Reference voltage [22] | Typical value = 0.75 V | 0.68 | 0.75 | 0.95 | V |
| $I_X$ | Input Leakage current | GND ≤ $V_I$ ≤ $V_{DDQ}$ | –5 | – | 5 | μA |
| $I_{OZ}$ | Output Leakage current | GND ≤ $V_I$ ≤ $V_{DDQ}$, output disabled | –5 | – | 5 | μA |

### Notes
16. Overshoot: $V_{IH(AC)}$ < $V_{DDQ}$ + 0.85 V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL(AC)}$ > –1.5 V (Pulse width less than $t_{CYC}/2$).
17. Power-up: Assumes a linear ramp from 0 V to $V_{DD(min.)}$ within 200 ms. During this time $V_{IH}$ < $V_{DD}$ and $V_{DDQ}$ ≤ $V_{DD}$.
18. All Voltage referenced to Ground.
19. Output are impedance controlled. $I_{OH}$ = –$V_{DDQ}/2$)/(RQ/5) for values of 175 Ω ≤ RQ ≤ 350 Ω.
20. Output are impedance controlled. $I_{OL}$ = ($V_{DDQ}/2$)/(RQ/5) for values of 175 Ω ≤ RQ ≤ 350 Ω.
21. This spec is for all inputs except C and C̄ Clock. For C and C̄ Clock, $V_{IL(Max.)}$ = $V_{REF}$ – 0.2 V.
22. $V_{REF(Min.)}$ = 0.68 V or 0.46 $V_{DDQ}$, whichever is larger, $V_{REF(Max.)}$ = 0.95 V or 0.54 $V_{DDQ}$, whichever is smaller.

## Electrical Characteristics (continued)

Over the Operating Range

### DC Electrical Characteristics (continued)

Over the Operating Range

| Parameter [18] | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ operating supply | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = 1/$t_{CYC}$ | – | – | 500 | mA |
| $I_{SB1}$ | Automatic power-down current | Max. $V_{DD}$, both ports deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = $f_{MAX}$ = 1/$t_{CYC}$, inputs static | – | – | 240 | mA |

### AC Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH voltage | | $V_{REF}$ + 0.2 | – | – | V |
| $V_{IL}$ | Input LOW voltage | | – | – | $V_{REF}$ − 0.2 | V |

## Thermal Resistance

| Parameter [23] | Description | Test Conditions | 165-ball FBGA Package | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 16.7 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 6.5 | °C/W |

## Capacitance

| Parameter [23] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{DD}$ = 2.5 V, $V_{DDQ}$ = 1.5 V | 5 | pF |
| $C_{CLK}$ | Clock input capacitance | | 6 | pF |
| $C_O$ | Output capacitance | | 7 | pF |

## AC Test Loads and Waveforms

### Figure 4. AC Test Loads and Waveforms
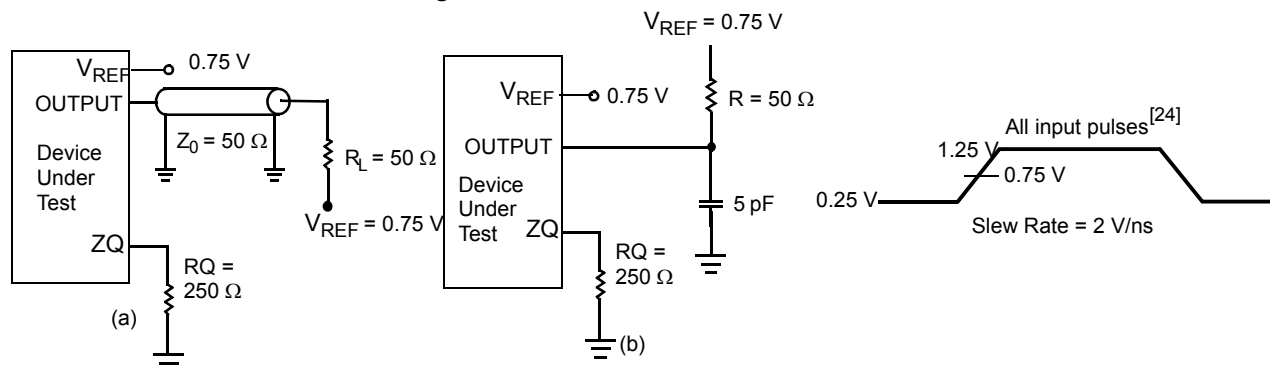


## Notes

23. Tested initially and after any design or process change that may affect these parameters.
24. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, $V_{REF}$ = 0.75 V, RQ = 250 Ω, $V_{DDQ}$ = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified $I_{OL}/I_{OH}$ and load capacitance shown in (a) of Figure 4.

## Switching Characteristics

Over the Operating Range

| Parameter [25] | | Description | 167 MHz | | Unit |
|---|---|---|---|---|---|
| Cypress Parameter | Consortium Parameter | | Min | Max | |
| $t_{Power}$[26] | | $V_{CC}$(typical) to the first access read or write | 10 | – | μs |
| **Cycle Time** | | | | | |
| $t_{CYC}$ | $t_{KHKH}$ | K clock and C clock cycle time | 6.0 | – | ns |
| $t_{KH}$ | $t_{KHKL}$ | Input clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH | 2.4 | – | ns |
| $t_{KL}$ | $t_{KLKH}$ | Input clock (K/$\overline{K}$ and C/$\overline{C}$) LOW | 2.4 | – | ns |
| $t_{KH\overline{K}H}$ | $t_{KH\overline{K}H}$ | K/$\overline{K}$ clock rise to $\overline{K}$/K clock rise and C/$\overline{C}$ to C/$\overline{C}$ rise (rising edge to rising edge) | 2.7 | 3.3 | ns |
| $t_{KHCH}$ | $t_{KHCH}$ | K/$\overline{K}$ clock rise to C/$\overline{C}$ Clock rise (rising edge to rising edge) | 0.0 | 2.0 | ns |
| **Setup Times** | | | | | |
| $t_{SA}$ | $t_{SA}$ | Address setup to clock (K and $\overline{K}$) Rise | 0.7 | – | ns |
| $t_{SC}$ | $t_{SC}$ | Control setup to clock (K and $\overline{K}$) Rise ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS_0}$, $\overline{BWS_1}$) | 0.7 | – | ns |
| $t_{SD}$ | $t_{SD}$ | $D_{[x:0]}$ setup to clock (K and $\overline{K}$) Rise | 0.7 | – | ns |
| **Hold Times** | | | | | |
| $t_{HA}$ | $t_{HA}$ | Address hold after clock (K and $\overline{K}$) Rise | 0.7 | – | ns |
| $t_{HC}$ | $t_{HC}$ | Control signals hold after clock (K and $\overline{K}$) Rise ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS_0}$, $\overline{BWS_1}$) | 0.7 | – | ns |
| $t_{HD}$ | $t_{HD}$ | $D_{[x:0]}$ hold after clock (K and $\overline{K}$) Rise | 0.7 | – | ns |
| **Output Times** | | | | | |
| $t_{CO}$ | $t_{CHQV}$ | C/$\overline{C}$ clock rise (or K/$\overline{K}$ in single clock mode) to data valid | – | 2.5 | ns |
| $t_{DOH}$ | $t_{CHQX}$ | Data output hold after output C/$\overline{C}$ clock rise (active to active) | 1.2 | – | ns |
| $t_{CHZ}$ | $t_{CHZ}$ | Clock (C and $\overline{C}$) rise to high Z (active to high Z) [27, 28] | – | 2.5 | ns |
| $t_{CLZ}$ | $t_{CLZ}$ | Clock (C and $\overline{C}$) rise to low Z [27, 28] | 1.2 | – | ns |

**Notes**
25. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, $V_{REF}$ = 0.75 V, RQ = 250 Ω, $V_{DDQ}$ = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified $I_{OL}/I_{OH}$ and load capacitance shown in (a) of Figure 4 on page 18.
26. This part has a voltage regulator that steps down the voltage internally; $t_{Power}$ is the time power needs to be supplied above $V_{DD}$ minimum initially before a read or write operation can be initiated.
27. At any given voltage and temperature $t_{CHZ}$ is less than $t_{CLZ}$ and, $t_{CHZ}$ less than $t_{CO}$.
28. $t_{CHZ}$, $t_{CLZ}$, are specified with a load capacitance of 5 pF as in part (b) of Figure 4 on page 18. Transition is measured ±100 mV from steady-state voltage.

## Switching Waveforms

**Figure 5. Switching Waveforms** [29, 30, 31]



DON'T CARE    UNDEFINED
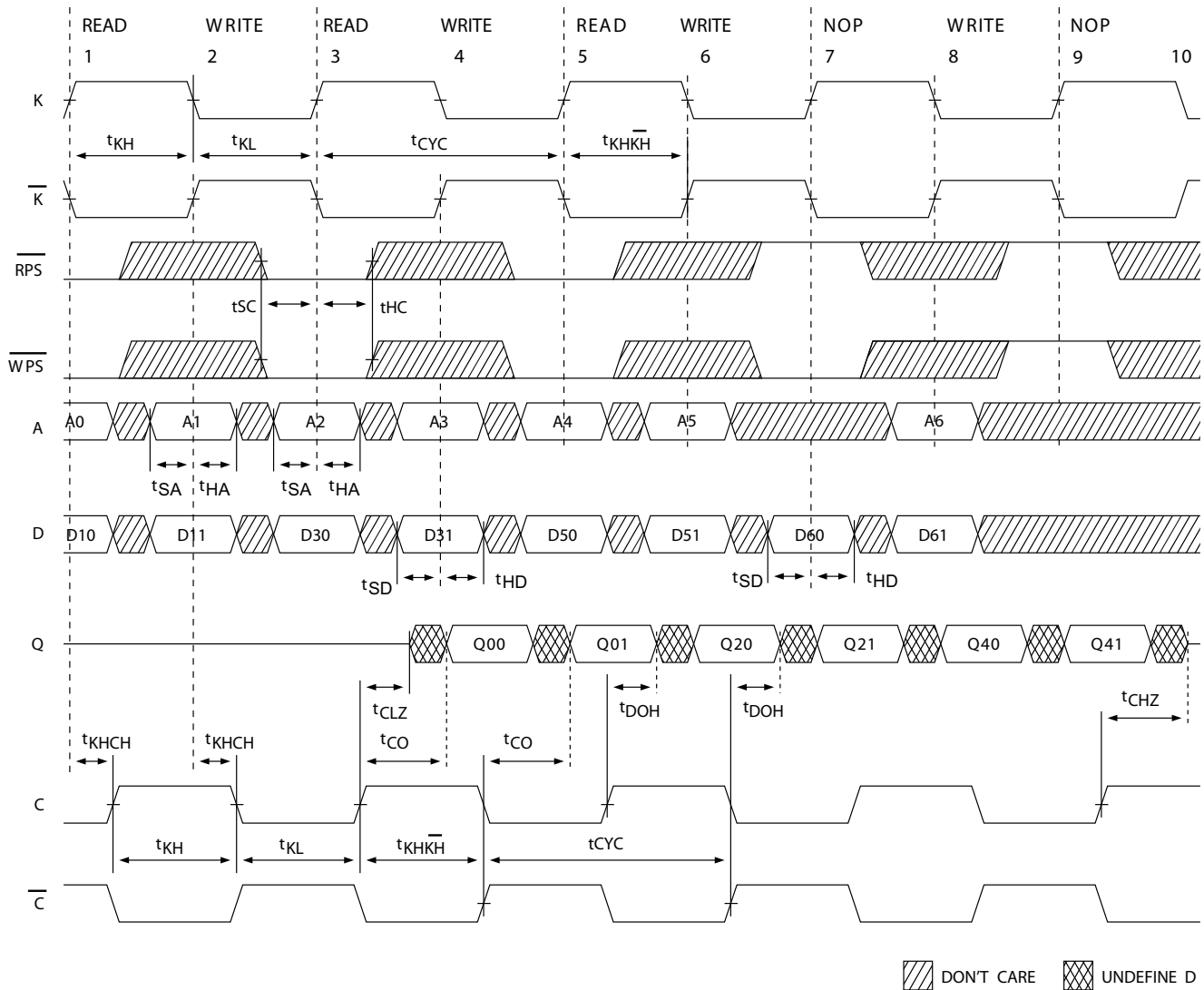
**Notes**
29. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, i.e., A0 + 1.
30. Outputs are disabled (High Z) one clock cycle after a NOP.
31. In this example, if address A2 = A1 then data Q20 = D10 and Q21 = D11. Write data is forwarded immediately as read results. This note applies to the whole diagram.
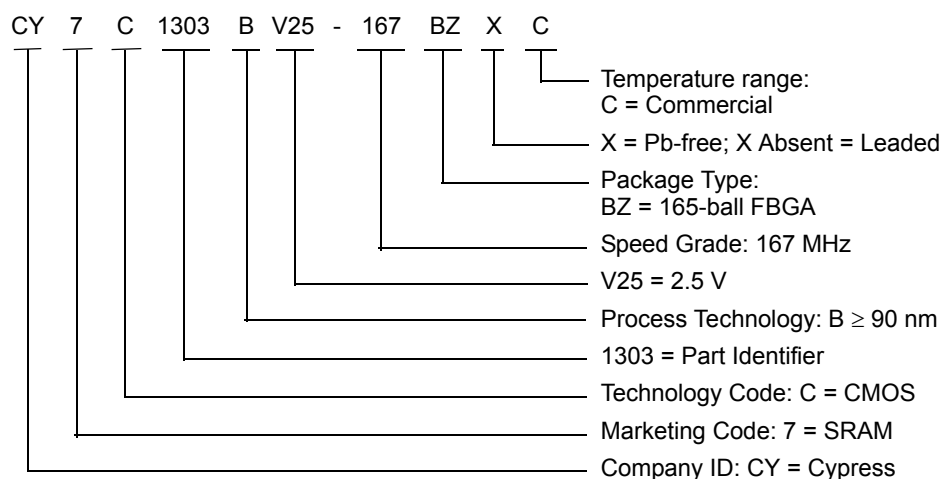
## Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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| Speed (MHz) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 167 | CY7C1303BV25-167BZC | 51-85180 | 165-ball FBGA (13 × 15 × 1.4 mm) | Commercial |

### Ordering Code Definitions

CY 7 C 1303 B V25 - 167 BZ X C

Temperature range:
C = Commercial

X = Pb-free; X Absent = Leaded

Package Type:
BZ = 165-ball FBGA

Speed Grade: 167 MHz

V25 = 2.5 V

Process Technology: B ≥ 90 nm

1303 = Part Identifier

Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress

## Package Diagram

**Figure 6. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter) Package Outline, 51-85180**



NOTES :
SOLDER PAD TYPE : NON-SOLDER MASK DEFINED (NSMD)
JEDEC REFERENCE : MO-216 / ISSUE E
PACKAGE CODE : BB0AC/BW0AC
PACKAGE WEIGHT : SEE CYPRESS PACKAGE MATERIAL DECLARATION
    DATASHEET (PMDD) POSTED ON THE CYPRESS WEB.
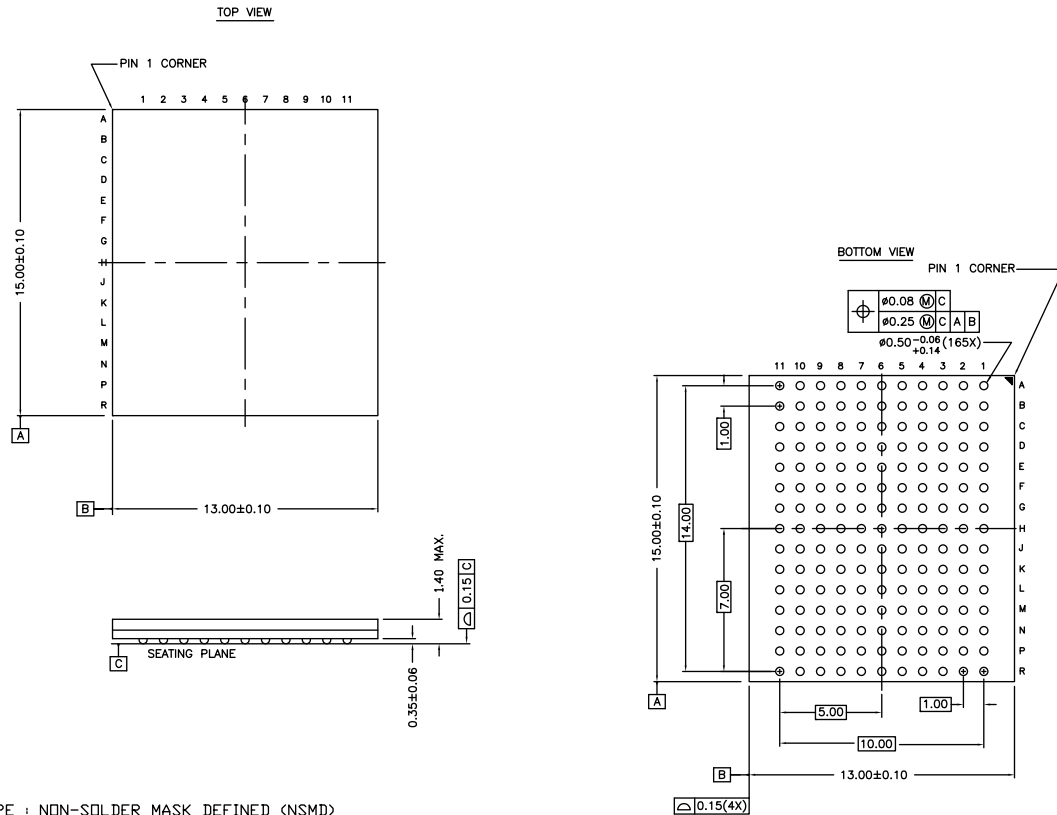
51-85180 *G

## Acronyms

| Acronym | Description |
|---------|-------------|
| DDR | Double Data Rate |
| FBGA | Fine-Pitch Ball Grid Array |
| HSTL | High-Speed Transceiver Logic |
| I/O | Input/Output |
| JEDEC | Joint Electron Device Engineering Council |
| JTAG | Joint Test Action Group |
| LMBU | Logical Multi-Bit Upsets |
| LSB | Least Significant Bit |
| LSBU | Logical Single-Bit Upsets |
| MSB | Most Significant Bit |
| PLL | Phase-Locked Loop |
| QDR | Quad Data Rate |
| SEL | Single Event Latch-up |
| SRAM | Static Random Access Memory |
| TAP | Test Access Port |
| TCK | Test Clock |
| TDI | Test Data In |
| TDO | Test Data Out |
| TMS | Test Mode Select |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| kΩ | kilohm |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mV | millivolt |
| mm | millimeter |
| ms | millisecond |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| ps | picosecond |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7C1303BV25, 18-Mbit Burst of Two-Pipelined SRAM with QDR® Architecture<br>Document Number: 38-05627 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 253010 | SYT | 08/13/04 | New data sheet. |
| *A | 436864 | NXR | See ECN | Changed status from Preliminary to Final.<br>Updated Features (Changed C/C description).<br>Updated Selection Guide (Removed 133 MHz and 100 MHz from product offering).<br>Updated Pin Definitions (Updated C/C̅ description, updated ZQ description (Alternately, this pin can be connected directly to $V_{DDQ}$, which enables the minimum impedance mode.)).<br>Updated TAP AC Switching Characteristics (Changed minimum value of $t_{TCYC}$ parameter from 100 ns to 50 ns, changed maximum value of $t_{TF}$ parameter from 10 MHz to 20 MHz, changed minimum value of $t_{TH}$ and $t_{TL}$ parameters from 40 ns to 20 ns).<br>Updated Maximum Ratings (Included Maximum Ratings for Supply Voltage on $V_{DDQ}$ Relative to GND, changed the Maximum Ratings for DC Input Voltage from $V_{DDQ}$ to $V_{DD}$).<br>Updated Operating Range (Updated Note 17 (Modified test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$), included the Industrial Operating Range).<br>Updated Electrical Characteristics (Changed description of $I_X$ parameter from Input Load current to Input Leakage Current, removed 133 MHz and 100 MHz from product offering).<br>Updated Ordering Information (Updated table and replaced Package Name Column with Package Diagram). |
| *B | 2755901 | VKN | 08/25/09 | Added Neutron Soft Error Immunity.<br>Updated Ordering Information (Updated table by including parts that are available, and modified the disclaimer for the Ordering information).<br>Updated Package Diagram. |
| *C | 2998771 | NJY | 08/02/10 | Updated Package Diagram.<br>Updated to new template. |
| *D | 3310077 | OSN | 07/12/2011 | Added Units of Measure.<br>Updated to new template. |
| *E | 3534369 | PRIT | 02/24/2012 | Updated Configurations (Removed CY7C1306BV25 related information).<br>Updated Functional Description (Removed CY7C1306BV25 related information).<br>Updated Selection Guide (Removed CY7C1306BV25 related information).<br>Removed Logic Block Diagram – CY7C1306BV25.<br>Updated Pin Configuration (Removed CY7C1306BV25 related information).<br>Updated Pin Definitions (Removed CY7C1306BV25 related information).<br>Updated Functional Overview (Removed CY7C1306BV25 related information).<br>Updated Truth Table (Removed CY7C1306BV25 related information).<br>Updated Write Cycle Descriptions (Removed CY7C1306BV25 related information).<br>Updated Identification Register Definitions (Removed CY7C1306BV25 related information).<br>Updated Operating Range (Removed Industrial Operating Range).<br>Updated Package Diagram. |
| *F | 3690005 | PRIT | 07/24/2012 | No technical updates.<br>Completing Sunset Review. |

## Document History Page (continued)

| | | | | |
|---|---|---|---|---|
| Document Title: CY7C1303BV25, 18-Mbit Burst of Two-Pipelined SRAM with QDR® Architecture<br>Document Number: 38-05627 | | | | |
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *G | 4064320 | PRIT | 07/16/2013 | Updated Package Diagram:<br>spec 51-85180 – Changed revision from *E to *F.<br>Updated to new template.<br>Completing Sunset Review. |
| *H | 4567085 | PRIT | 11/11/2014 | Updated Functional Description:<br>Added "For a complete list of related documentation, click here." at the end. |
| *I | 5374246 | PRIT | 07/26/2016 | Updated Package Diagram:<br>spec 51-85180 – Changed revision from *F to *G.<br>Updated to new template.<br>Completing Sunset Review. |
| *J | 6012218 | AESATMP9 | 01/03/2018 | Updated logo and copyright. |

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