Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied.. –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1] .... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1] .... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) .... 20 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-12		-15		
				Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_{OUT} \leq V_{CC}$, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Comm'l		190		170	mA
			Ind'l		-		190	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}			40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V, or $V_{IN} \leq$ 0.3V, f = 0	Com'l/Ind'l		8		8	mA
			Com'l L		0.5		0.5	mA

Notes:
1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.

Electrical Characteristics Over the Operating Range (continued)

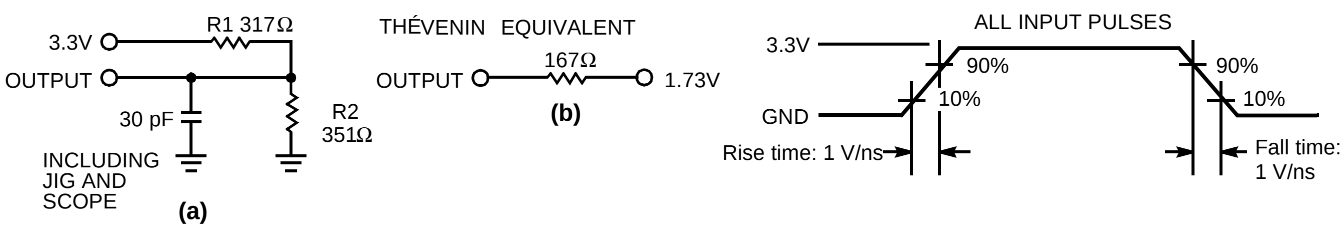
Parameter	Description	Test Conditions		-17 Min.	-17 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_{OUT} \leq V_{CC}$, Output Disabled		–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., $f = f_{MAX} = 1/t_{RC}$	Comm’l		160		150		130	mA
			Ind’l		180		170		150	
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$			40		40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} – 0.3V$, $V_{IN} \geq V_{CC} – 0.3V$, or $V_{IN} \leq 0.3V$, f=0	Com’l/Ind’l		8		8		8	mA
			Com’l L		0.5		0.5		0.5	mA

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Note:
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



[+] Feedback

Switching Characteristics[4] Over the Operating Range

Parameter	Description	-12		-15		-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		17		ns
t_{AA}	Address to Data Valid		12		15		17	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		17	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		6		7		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		6		7		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		17	ns
t_{DBE}	Byte Enable to Data Valid		6		7		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		0		ns
t_{HZBE}	Byte Disable to High Z		6		7		8	ns
WRITE CYCLE[7, 8]								
t_{WC}	Write Cycle Time	12		15		17		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		12		ns
t_{AW}	Address Set-Up to Write End	10		12		12		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		12		ns
t_{SD}	Data Set-Up to Write End	7		8		9		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		6		7		8	ns
t_{BW}	Byte Enable to End of Write	10		12		12		ns

Notes:

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics[4] Over the Operating Range (continued)

Parameter	Description	-20		-25		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	20		25		ns
t_{AA}	Address to Data Valid		20		25	ns
t_{OHA}	Data Hold from Address Change	3		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		25	ns
t_{DBE}	Byte Enable to Data Valid		8		10	ns
t_{LZBE}	Byte Enable to Low Z	0		0		ns
t_{HZBE}	Byte Disable to High Z		8		10	ns
WRITE CYCLE[7, 8]						
t_{WC}	Write Cycle Time	20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	13		15		ns
t_{AW}	Address Set-Up to Write End	13		15		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	13		15		ns
t_{SD}	Data Set-Up to Write End	9		10		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		8		10	ns
t_{BW}	Byte Enable to End of Write	13		15		ns

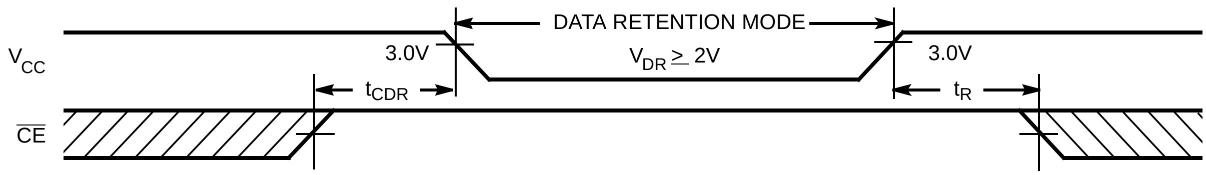
Data Retention Characteristics Over the Operating Range (For L version only)

Parameter	Description	Conditions[10]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		330	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0		ns
t_R[9]	Operation Recovery Time		t_{RC}		ns

Notes:

9. $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 and slower speeds.
10. No input may exceed V_{CC} + 0.5V.

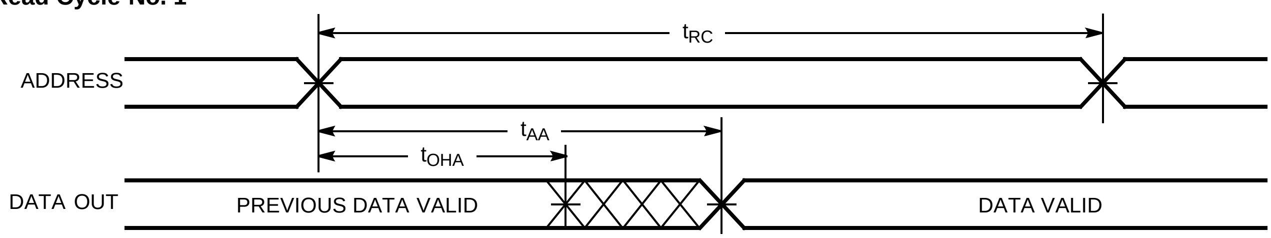
Data Retention Waveform



1041BV33–

Switching Waveforms

Read Cycle No. 1[11, 12]



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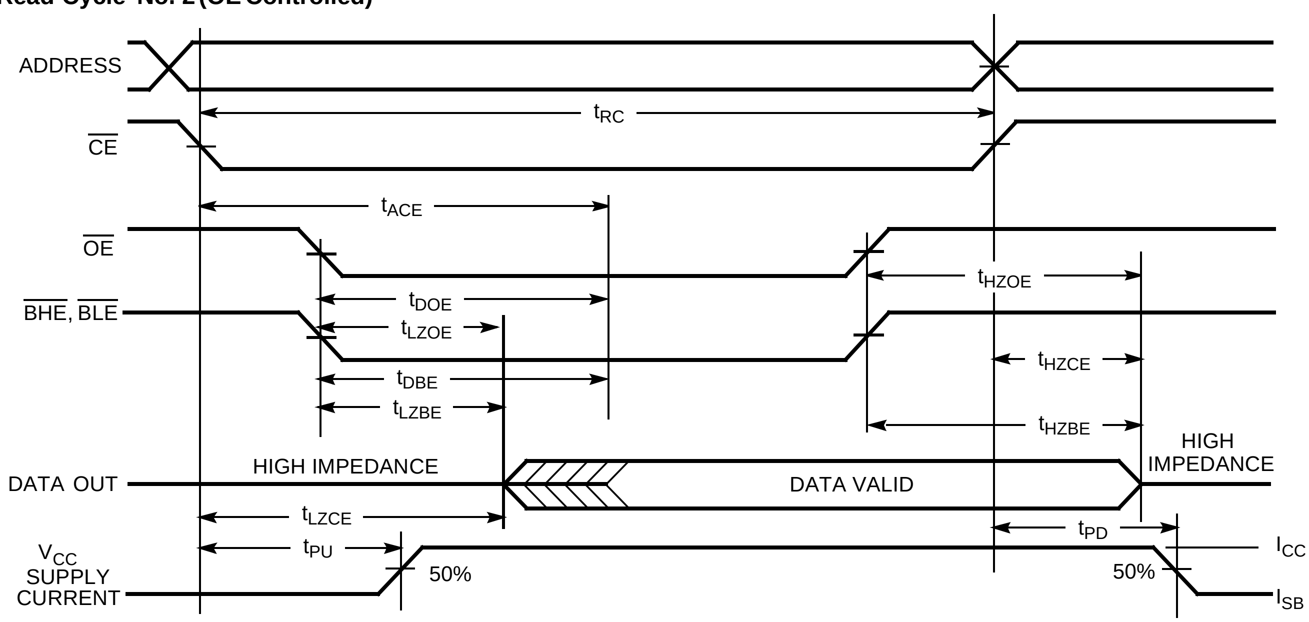
Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]



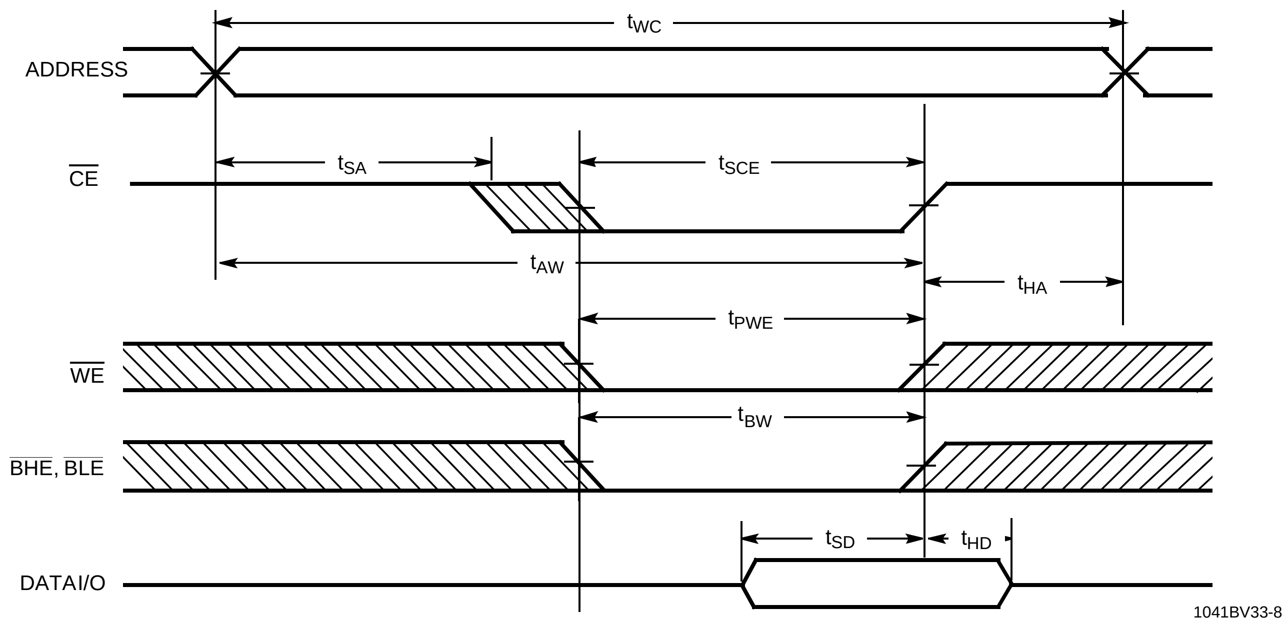
1041BV33-7

Notes:

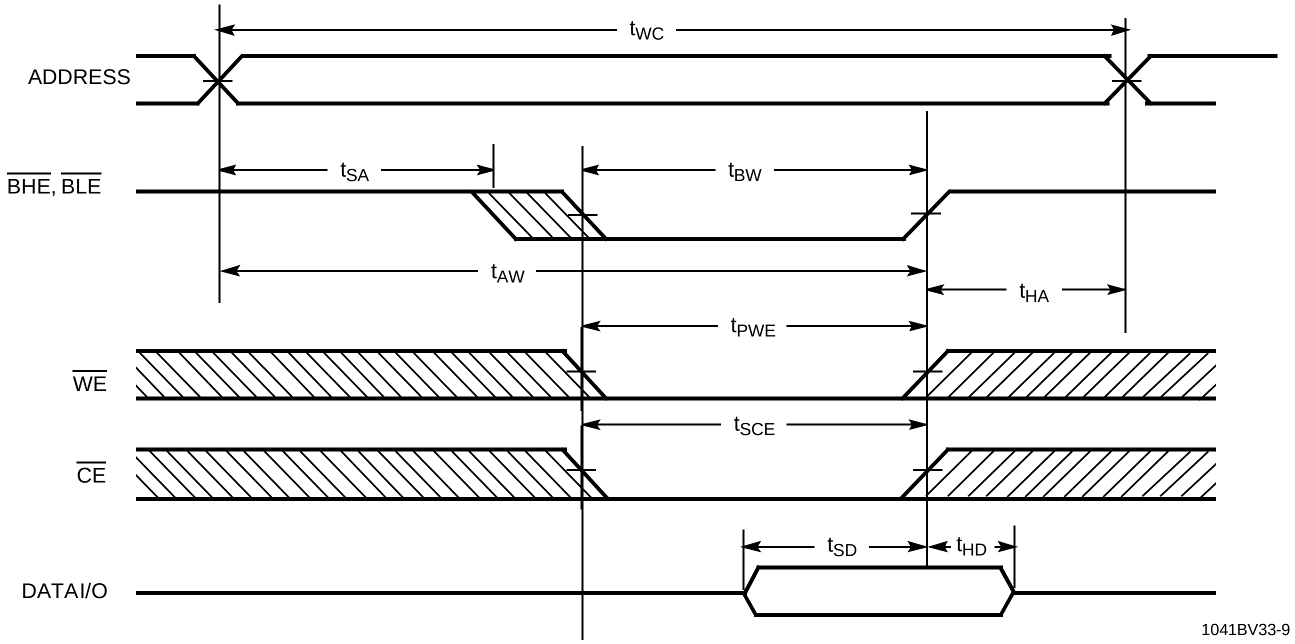
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[14, 15]



Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)

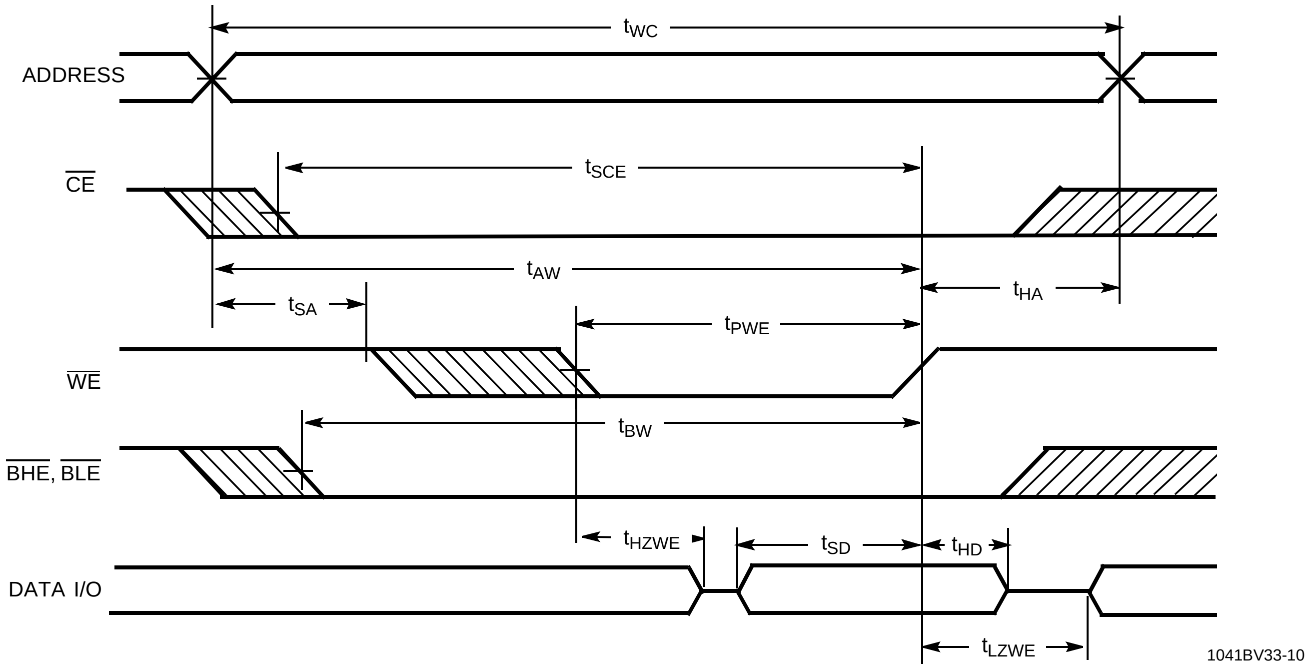


Notes:

14. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high–impedance state.

Switching Waveforms (continued)

Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

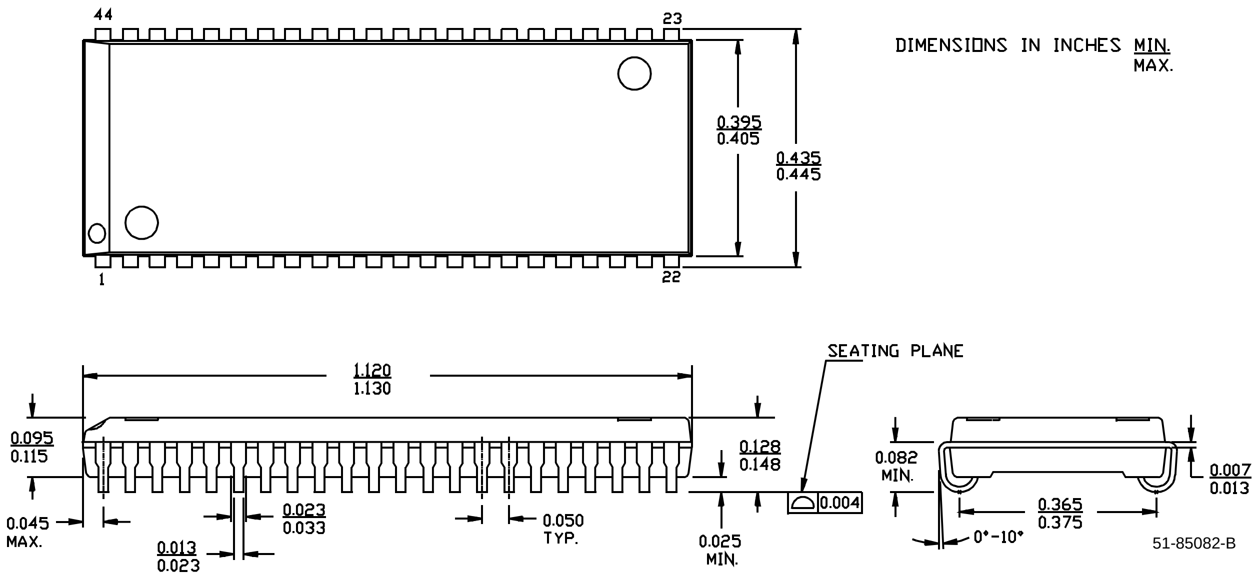
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

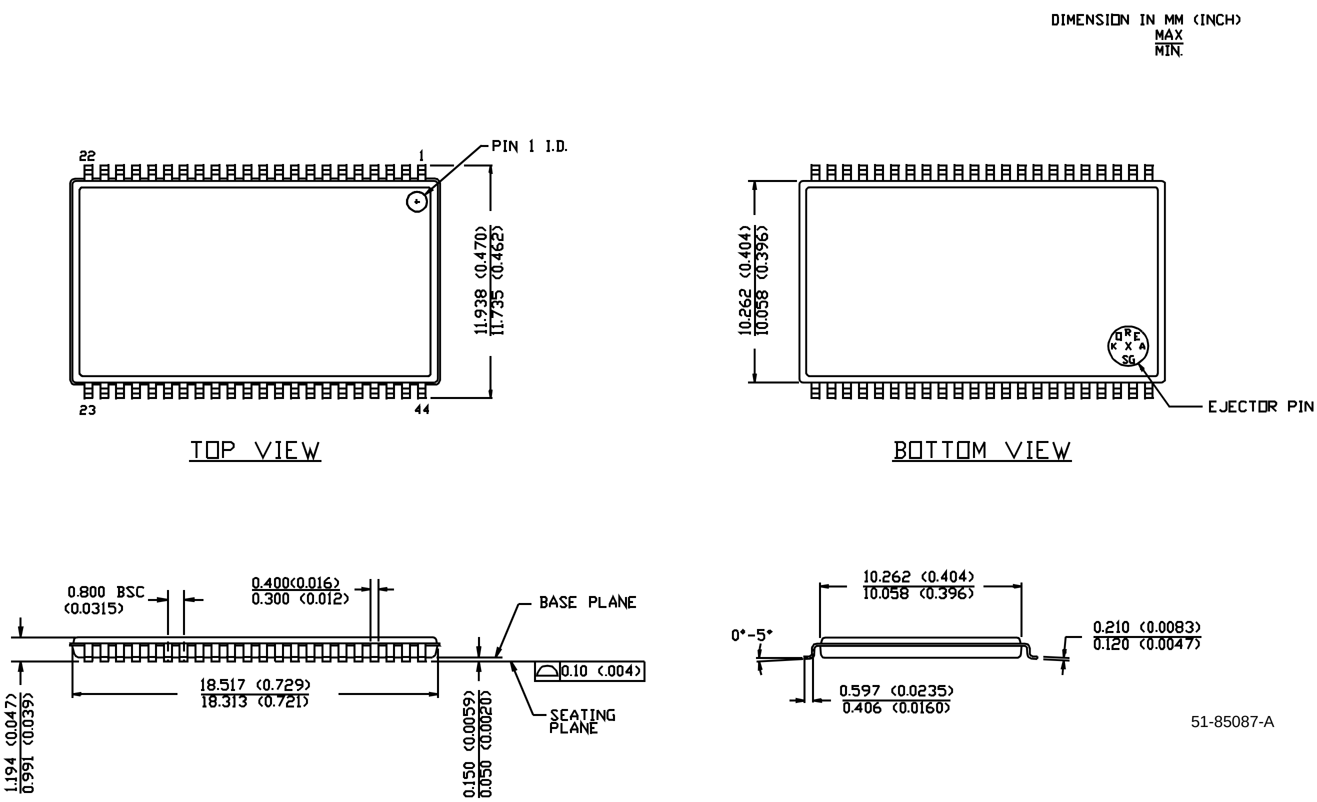
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1041BV33-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1041BV33L-12VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BV33-12ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33L-12ZC	Z44	44-Pin TSOP II Z44	
15	CY7C1041BV33-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1041BV33L-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BV33-15ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33L-15ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33-15VI	V34	44-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1041BV33-15ZI	Z44	44-Pin TSOP II Z44	
17	CY7C1041BV33-17VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1041BV33L-17VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BV33-17ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33L-17ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33-17VI	V34	44-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1041BV33-17ZI	Z44	44-Pin TSOP II Z44	
20	CY7C1041BV33-20VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1041BV33L-20VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BV33-20ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33L-20ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33-20VI	V34	44-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1041BV33-20ZI	Z44	44-Pin TSOP II Z44	
25	CY7C1041BV33-25VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1041BV33L-25VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BV33-25ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33L-25ZC	Z44	44-Pin TSOP II Z44	
	CY7C1041BV33-25VI	V34	44-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1041BV33-25ZI	Z44	44-Pin TSOP II Z44	

Package Diagrams

44-Lead (400-Mil) Molded SOJ V34



44-Pin TSOP II Z44



Document Title: CY7C1041BV33 256K x 16 SRAM Document Number: 38-05168				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111840	11/17/01	DSG	Change from Spec number: 38-00932 to 38-05168