

## Contents

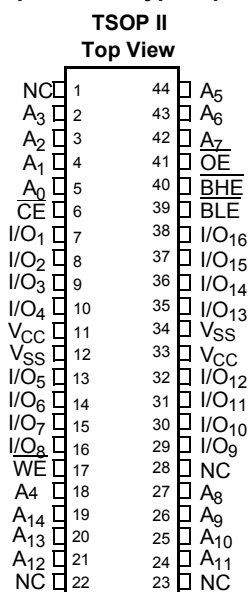
<b>Selection Guide</b> .....	<b>3</b>	<b>Package Diagrams</b> .....	<b>13</b>
<b>Pin Configuration</b> .....	<b>3</b>	<b>Acronyms</b> .....	<b>14</b>
<b>Pin Definitions</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>14</b>
<b>Maximum Ratings</b> .....	<b>5</b>	Units of Measure .....	14
<b>Operating Range</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>15</b>
<b>Electrical Characteristics</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>17</b>
<b>Capacitance</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	17
<b>Thermal Resistance</b> .....	<b>6</b>	Products .....	17
<b>AC Test Loads and Waveforms</b> .....	<b>6</b>	PSoC® Solutions .....	17
<b>Switching Characteristics</b> .....	<b>7</b>	Cypress Developer Community .....	17
<b>Switching Waveforms</b> .....	<b>8</b>	Technical Support .....	17
<b>Truth Table</b> .....	<b>11</b>		
<b>Ordering Information</b> .....	<b>12</b>		
Ordering Code Definitions .....	12		

## Selection Guide

Description		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial/Industrial	90	85	80	mA
	Automotive	—	—	85	mA
Maximum CMOS Standby Current	Commercial/Industrial	5	5	5	mA
	Automotive	—	—	10	mA

## Pin Configuration

Figure 1. 44-pin TSOP Type II pinout (Top View) <sup>[1]</sup>



### Note

1. NC pins are not connected on the die.

## Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A <sub>0</sub> –A <sub>14</sub>	5, 4, 3, 2, 18, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19	Input	<b>Address Inputs used to select one of the address locations.</b>
I/O <sub>1</sub> –I/O <sub>16</sub>	7–10, 13–16, 29–32, 35–38	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.
NC	1, 22, 23, 28	No Connect	<b>No Connects.</b> Not connected to the die.
$\overline{\text{WE}}$	17	Input/Control	<b>Write Enable Input, active LOW.</b> When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{\text{CE}}$	6	Input/Control	<b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}, \overline{\text{BLE}}$	40, 39	Input/Control	<b>Byte Write Select Inputs, active LOW.</b> $\overline{\text{BHE}}$ controls I/O <sub>16</sub> –I/O <sub>9</sub> , $\overline{\text{BLE}}$ controls I/O <sub>8</sub> –I/O <sub>1</sub> .
$\overline{\text{OE}}$	41	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V <sub>SS</sub>	12, 34	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	11, 33	Power Supply	<b>Power Supply inputs to the device.</b>

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to relative GND [2] ..... -0.5 V to +4.6 V

DC voltage applied to outputs in high Z State [2] ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage [2] ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	0 °C to +70 °C	3.3 V $\pm$ 10%
Industrial	-40 °C to +85 °C	3.3 V $\pm$ 10%
Automotive	-40 °C to +125 °C	3.3 V $\pm$ 10%

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		-15		Unit
				Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = −4.0 mA		2.4	−	2.4	−	2.4	−	V
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA		−	0.4	−	0.4	−	0.4	V
V <sub>IH</sub>	Input HIGH voltage			2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage <sup>[2]</sup>			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Commercial / Industrial	−1	+1	−1	+1	−1	+1	μA
			Automotive	−	−	−	−	−20	+20	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	Commercial / Industrial	−1	+1	−1	+1	−1	+1	μA
			Automotive	−	−	−	−	−20	+20	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Commercial / Industrial	−	90	−	85	−	80	mA
			Automotive	−	−	−	−	−	85	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL Inputs	Max V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Commercial / Industrial	−	15	−	15	−	15	mA
			Automotive	−	−	−	−	−	20	mA
I <sub>SB2</sub>	Automatic CE power-down current – CMOS inputs	Max V <sub>CC</sub> , CE ≥ V <sub>CC</sub> − 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0	Commercial / Industrial	−	5	−	5	−	5	mA
			Automotive	−	−	−	−	−	10	mA

### Note

2.  $V_{IL}(\text{min}) = -2.0 \text{ V}$  and  $V_{IH}(\text{max}) = V_{CC} + 0.5 \text{ V}$  for pulse durations of less than 20 ns.

## Capacitance

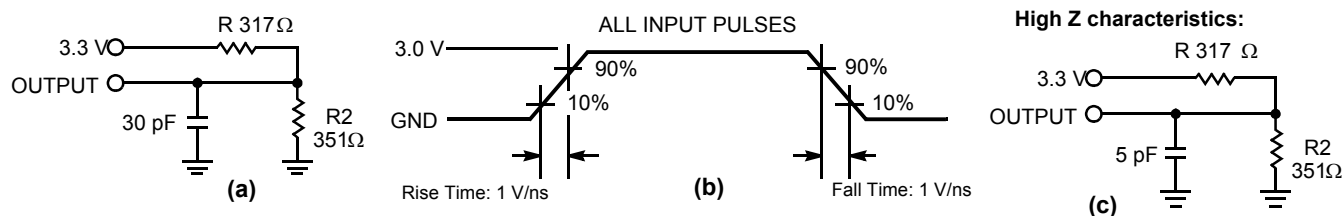
Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$	8	pF
$C_{OUT}$	Output capacitance		8	pF

## Thermal Resistance

Parameter <sup>[3]</sup>	Description	Test Conditions	44-pin TSOP-II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	76.92	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		15.86	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[4]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

## Switching Characteristics

Over the Operating Range

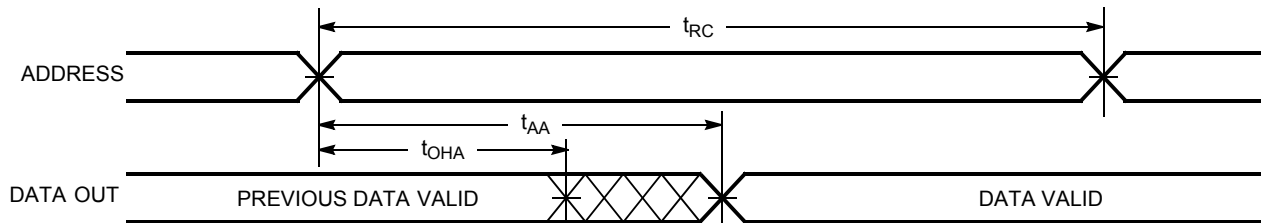
Parameter <sup>[5]</sup>	Description	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t <sub>RC</sub>	Read cycle time	10	–	12	–	15	–	ns
t <sub>AA</sub>	Address to data valid	–	10	–	12	–	15	ns
t <sub>OHA</sub>	Data hold from address change	3	–	3	–	3	–	ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to data valid	–	10	–	12	–	15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	5	–	6	–	7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to low Z <sup>[6]</sup>	0	–	0	–	0	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to high Z <sup>[6, 7]</sup>	–	5	–	6	–	7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to low Z <sup>[6]</sup>	3	–	3	–	3	–	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to high Z <sup>[6, 7]</sup>	–	5	–	6	–	7	ns
t <sub>PU</sub> <sup>[8]</sup>	$\overline{CE}$ LOW to power-up	0	–	0	–	0	–	ns
t <sub>PD</sub> <sup>[8]</sup>	$\overline{CE}$ HIGH to power-down	–	10	–	12	–	15	ns
t <sub>DBE</sub>	Byte enable to data valid	–	5	–	6	–	7	ns
t <sub>LZBE</sub>	Byte enable to low Z	0	–	0	–	0	–	ns
t <sub>HZBE</sub>	Byte disable to high Z	–	5	–	6	–	7	ns
Write Cycle <sup>[9, 10]</sup>								
t <sub>WC</sub>	Write cycle time	10	–	12	–	15	–	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end	8	–	9	–	10	–	ns
t <sub>AW</sub>	Address set-up to write end	7	–	8	–	10	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	0	–	0	–	ns
t <sub>SA</sub>	Address set-up to write start	0	–	0	–	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	7	–	8	–	10	–	ns
t <sub>SD</sub>	Data set-up to write end	5	–	6	–	8	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	0	–	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low Z <sup>[6]</sup>	3	–	3	–	3	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to high Z <sup>[6, 7]</sup>	–	5	–	6	–	7	ns
t <sub>BW</sub>	Byte enable to end of write	7	–	8	–	9	–	ns

### Notes

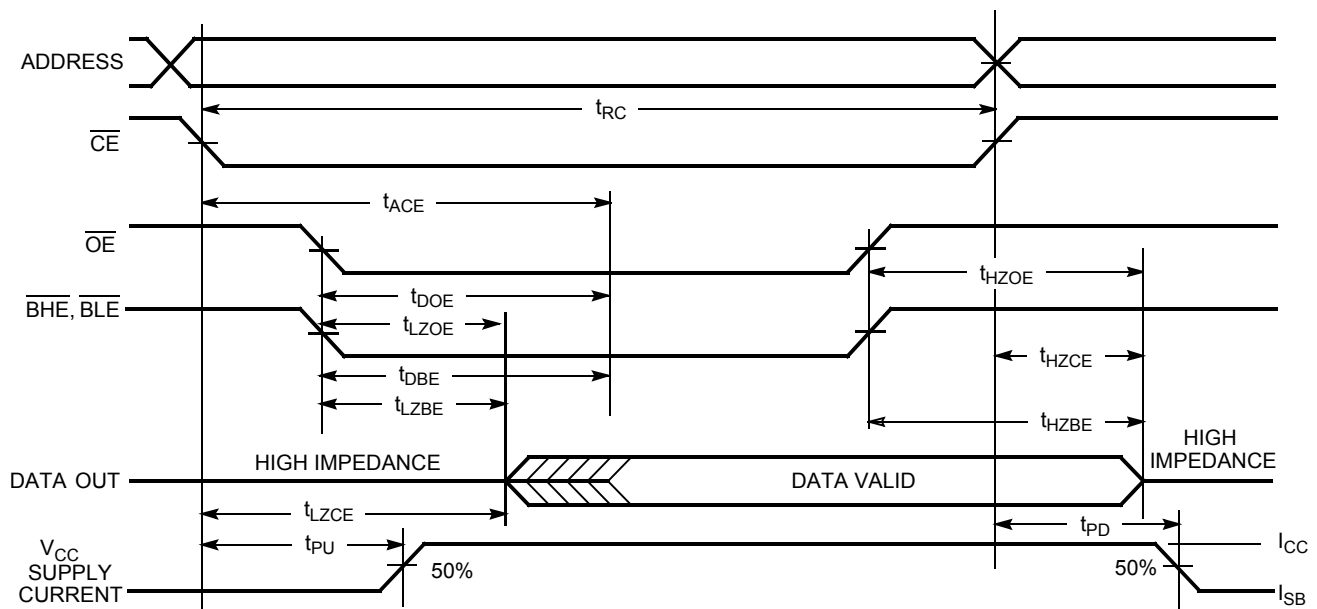
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

**Figure 3. Read Cycle No. 1** [11, 12]



**Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [12, 13]

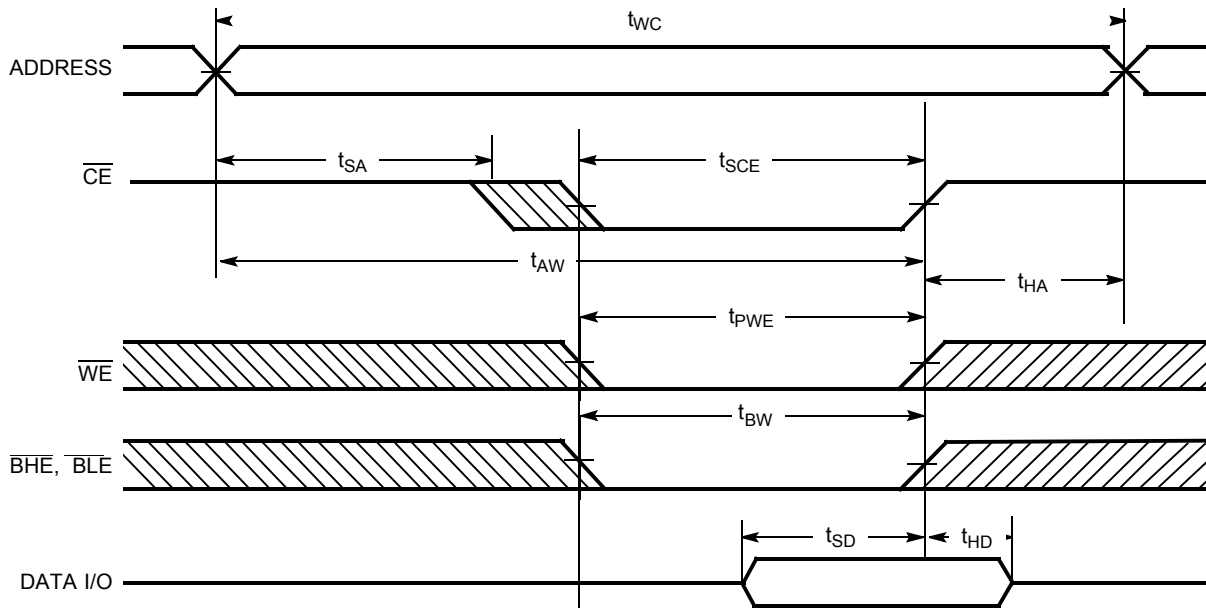


### Notes

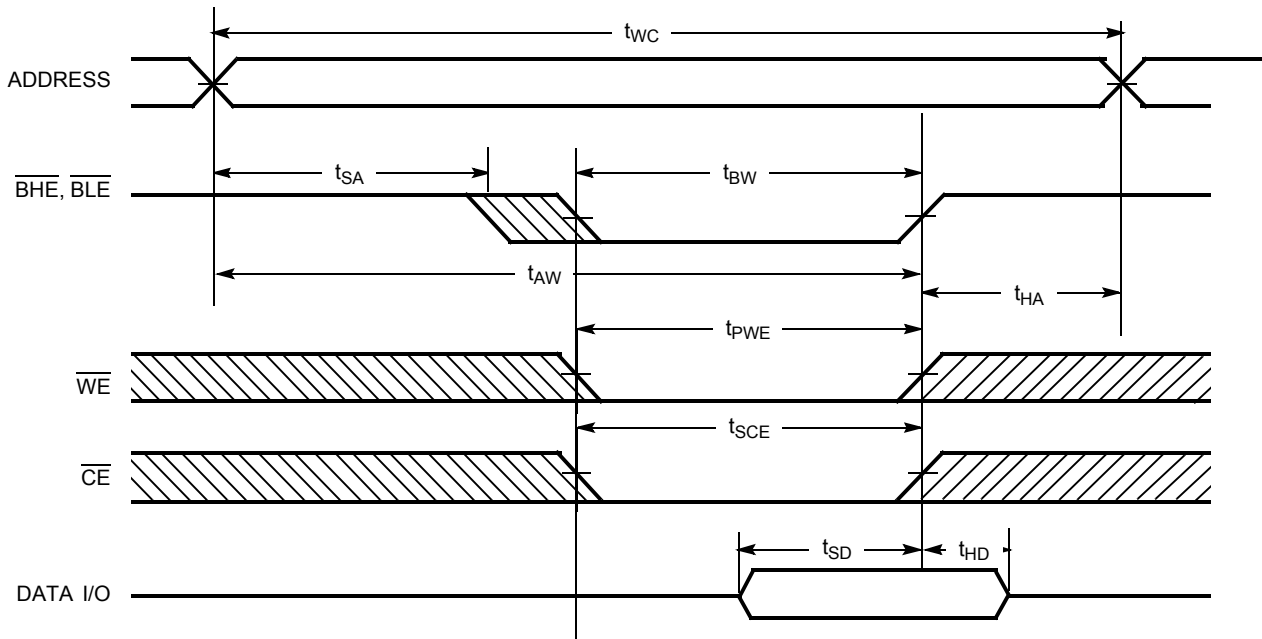
11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BHE} = V_{IL}$ .
12.  $\overline{WE}$  is HIGH for Read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms (continued)

**Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [14, 15]



**Figure 6. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**



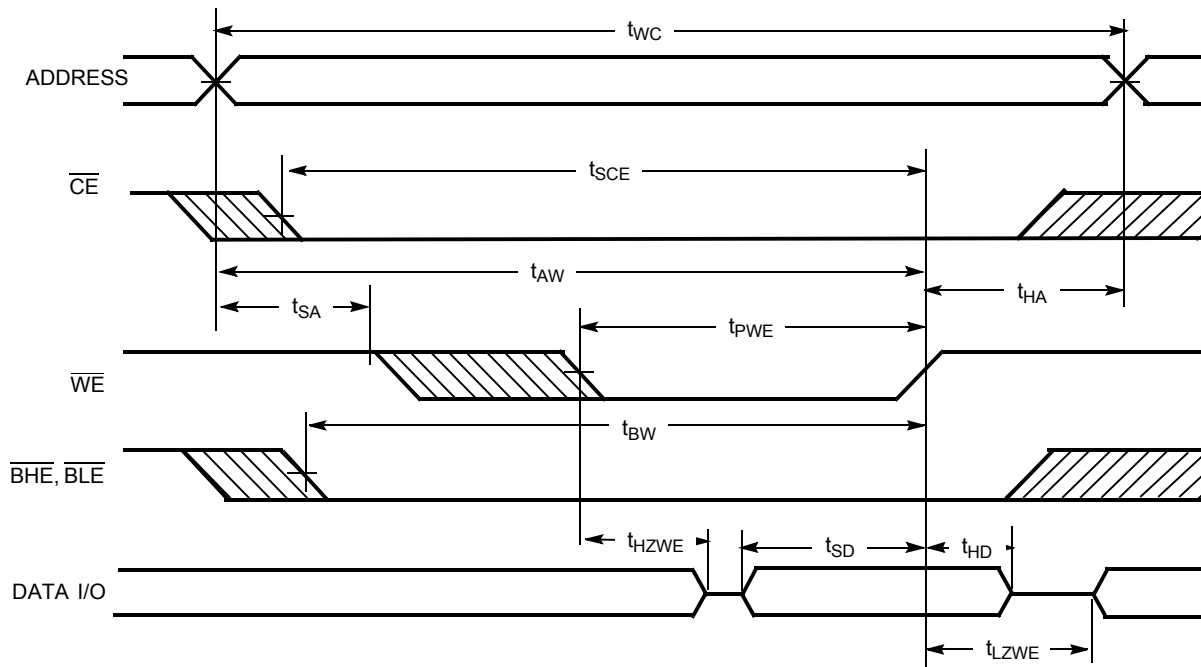
### Notes

14. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.



**Switching Waveforms** (continued)

**Figure 7. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) <sup>[16]</sup>**



**Note**

16. The minimum write pulse width for Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{\text{SD}}$  and  $t_{\text{HZWE}}$ .

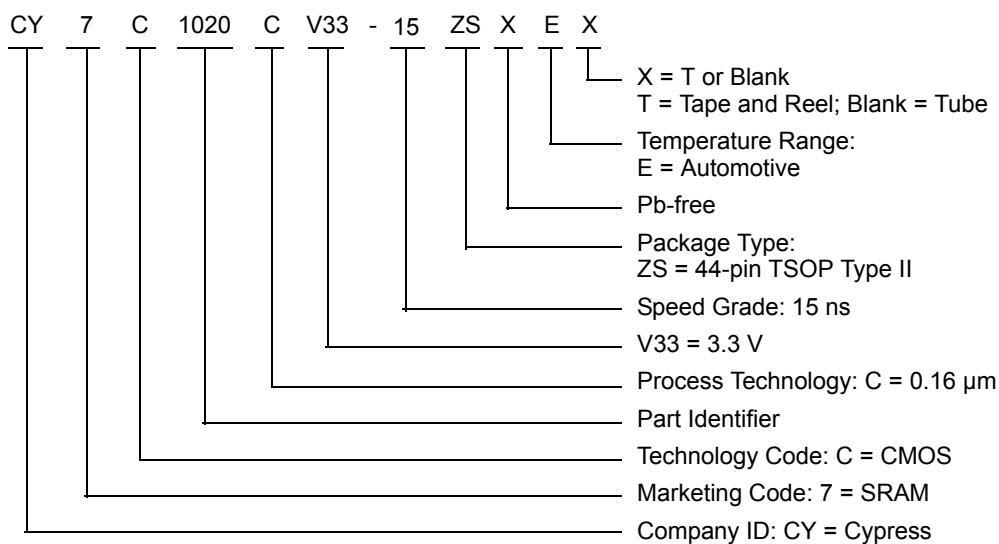
**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>1</sub> –I/O <sub>8</sub>	I/O <sub>9</sub> –I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data out	Data out	Read – All bits	Active (I <sub>CC</sub> )
			L	H	Data out	High Z	Read – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High Z	Data out	Read – Upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data in	Data in	Write – All bits	Active (I <sub>CC</sub> )
			L	H	Data in	High Z	Write – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High Z	Data in	Write – Upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

## Ordering Information

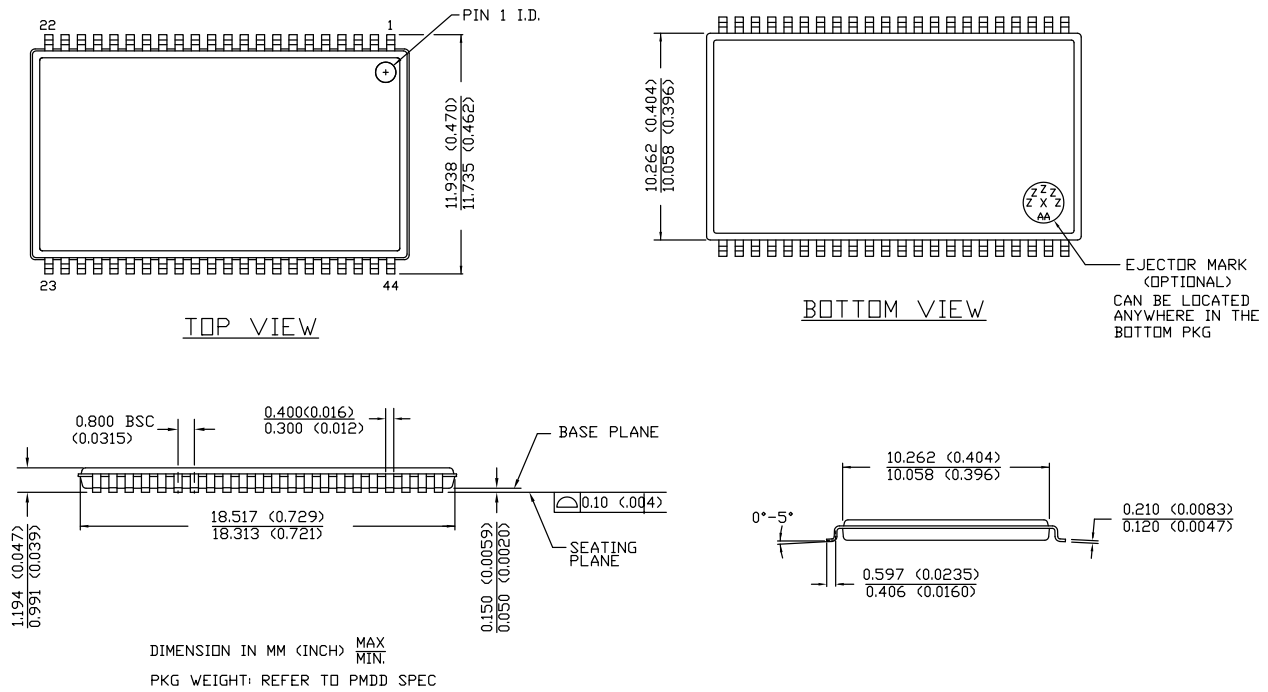
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1020CV33-15ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1020CV33-15ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	Automotive

## Ordering Code Definitions



## Package Diagrams

Figure 8. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 \*E

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1020CV33, 512 K (32 K × 16) Static RAM Document Number: 38-05133				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	109428	12/16/01	HGK	New data sheet.
*A	115045	05/30/02	HGK	Added 8 ns speed bin related information in all instances across the document. Updated <a href="#">Selection Guide</a> : Changed value of “Maximum Operating Current” corresponding to 10 ns speed bin from 100 mA to 90 mA. Changed value of “Maximum Operating Current” corresponding to 12 ns speed bin from 100 mA to 85 mA. Changed value of “Maximum Operating Current” corresponding to 15 ns speed bin from 100 mA to 80 mA. Updated <a href="#">Electrical Characteristics</a> : Changed maximum value of I <sub>CC</sub> parameter corresponding to 10 ns speed bin from 100 mA to 90 mA. Changed maximum value of I <sub>CC</sub> parameter corresponding to 12 ns speed bin from 100 mA to 85 mA. Changed maximum value of I <sub>CC</sub> parameter corresponding to 15 ns speed bin from 100 mA to 80 mA. Changed maximum value of I <sub>SB1</sub> parameter corresponding to 10 ns, 12 ns and 15 ns speed bins from 40 mA to 15 mA. Updated <a href="#">Ordering Information</a> : Updated part numbers.
*B	117615	08/14/02	DFP	Removed SOJ package related information in all instances across the document. Removed 8 ns speed bin related information in all instances across the document. Updated <a href="#">Pin Configuration</a> : Updated <a href="#">Figure 1</a> (Replaced “A <sub>4</sub> ” with “NC” for pin 1 and replaced “NC” with “A <sub>4</sub> ” for pin 18). Updated <a href="#">Ordering Information</a> : Updated part numbers.
*C	262949	See ECN	RKF	Added Automotive Temperature Range related information in all instances across the document. Updated <a href="#">Ordering Information</a> : Updated part numbers.
*D	334398	See ECN	SYT	Updated <a href="#">Ordering Information</a> : Updated part numbers (Added Lead-Free Product Information).
*E	493543	See ECN	NXR	Updated <a href="#">Pin Configuration</a> : Added Note 1 and referred the same note in <a href="#">Figure 1</a> . Updated <a href="#">Electrical Characteristics</a> : Changed the description of I <sub>IX</sub> parameter from “Input Load Current” to “Input Leakage Current”. Removed I <sub>OS</sub> parameter and its details. Updated <a href="#">Ordering Information</a> : Updated part numbers.
*F	2897691	03/23/2010	RAME	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagrams</a> .
*G	3057593	10/13/2010	PRAS	Updated <a href="#">Ordering Information</a> : Updated part numbers. Added <a href="#">Ordering Code Definitions</a> .

**Document History Page** *(continued)*

Document Title: CY7C1020CV33, 512 K (32 K × 16) Static RAM Document Number: 38-05133				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*H	3100106	12/02/2010	PRAS	Minor edits across the document. Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*I	4146968	10/04/2013	VINI	Updated <a href="#">Package Diagrams</a> : spec 51-85087 – Changed revision from *C to *E. Updated to new template. Completing Sunset Review.
*J	4567799	11/12/2014	VINI	Updated <a href="#">Functional Description</a> : Added “For a complete list of related resources, <a href="#">click here</a> .” at the end. Updated <a href="#">Switching Characteristics</a> : Added Note 10 and referred the same note in “Write Cycle”. Updated <a href="#">Switching Waveforms</a> : Added Note 16 and referred the same note in <a href="#">Figure 7</a> . Completing Sunset Review.
*K	4573200	11/18/2014	VINI	No technical updates.
*L	5004033	11/05/2015	VINI	Updated to new template. Completing Sunset Review.

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