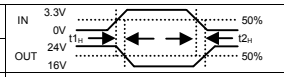
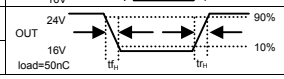
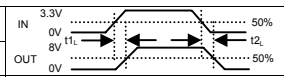
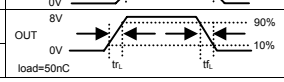
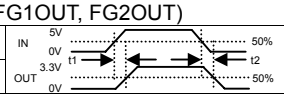
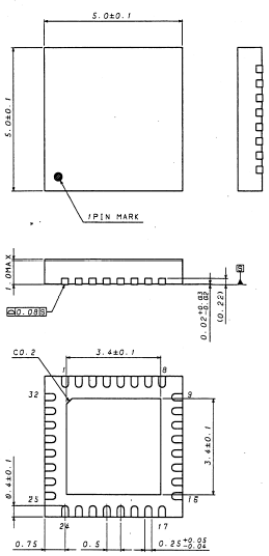
○DC Electrical characteristics (Unless otherwise specified, Ta=25℃, V_{MM}=24V, Vcc=3.3V)

Item	Symbol	Target value			Unit	Conditions
		Min.	Typ.	Max.		
Whole						
Circuit current1	$I_{MM}1$	-	**TBD**	3	mA	ENABLE=L
Circuit current2	$I_{MM}2$	-	**TBD**	200	uA	ENABLE=H
Circuit current3	I_{CC}	-	**TBD**	0.5	mA	
Driver block						
〈Input〉 (UHIN,ULIN,VHIN,VLIN,WHIN,WLIN)						
High level input current	I_{INHD}	40	55	80	uA	xHIN=xLIN=5.5V
High level input voltage	V_{INHD}	2.0	-	Vcc	V	
Low level input voltage	V_{INLD}	0	-	0.8	V	
〈High side FET driver〉 (**VREGH**, UHOUT, VHOUT, WHOUT)						
VREGH voltage	**V_{REGH}**	**V_{MM}-8.8**	**V_{MM}-8.0**	**V_{MM}-7.2**	**V**	
High level output voltage	$V_{OH}H_{OUT}$	V_{MM}-0.50	V_{MM}-0.25	V_{MM}-0.10	V	I_O=-10mA
Low level output voltage	$V_{OL}H_{OUT}$	V_{MM}-8.70	V_{MM}-7.75	V_{MM}-6.70	V	I_O=10mA
〈Low side FET driver〉 (**VREGL**, ULOUT, VLOUT, WLOUT)						
VREGL voltage	**V_{REGL}**	**7.2**	**8.0**	**8.8**	**V**	
High level output voltage	$V_{OH}L_{OUT}$	6.70	7.75	8.70	V	I_O=-10mA
Low level output voltage	$V_{OL}L_{OUT}$	0.10	0.25	0.50	V	I_O=10mA
Current limit block						
RS input current	I_{RS}	-2.0	-0.1	-	uA	RS=0V, VREF=1.0V
VREF input current	I_{VREF}	-2.0	-0.1	-	uA	RS=1.0V, VREF=0V
VREF input voltage range	V_{REF}	0	-	1.0	V	
Comparator input offset voltage	V_{OFS}	-8	-	8	mV	**Ta=-25～+85℃**
Hall, FG signal block (HallAIN, HallBIN, HallCIN, FG1IN, FG2IN, HallAOUT, HallBOUT, HallCOUT, FG1OUT, FG2OUT)						
High level input current	I_{INH}	40	55	80	uA	HallxIN=FGxIN=5.5V
High level input voltage	V_{INH}	2.0	-	Vcc	V	
Low level input voltage	V_{INL}	0	-	0.8	V	
High level output voltage	V_{OH}	Vcc-0.08	Vcc-0.04	-	V	I_O=-1mA
Low level output voltage	V_{OL}	-	0.04	0.08	V	I_O=1mA
ENABLE signal block						
High level input current	I_{ENH}	40	55	80	uA	ENABLE=5.5V
High level input voltage	V_{ENH}	2.0	-	Vcc	V	
Low level input voltage	V_{ENL}	0	-	0.8	V	

○AC Electrical characteristics (Ta=25℃, V_{MM}=24V, Vcc=3.3V)

Item	Symbol	Target value			Unit	Conditions
		Min.	Typ.	Max.		
Driver block						
〈High side FET driver〉 (UHOUT, VHOUT, WHOUT)						
Propagation delay time1	$t1_H$	-	70	-	ns	
Propagation delay time2	$t2_H$	-	70	-	ns	
Output transition time1	tr_H	-	150	-	ns	
Output transition time2	tf_H	-	150	-	ns	
〈Low side FET driver〉 (ULOUT, VLOUT, WLOUT)						
Propagation delay time1	$t1_L$	-	70	-	ns	
Propagation delay time2	$t2_L$	-	70	-	ns	
Output transition time1	tr_L	-	150	-	ns	
Output transition time2	tf_L	-	150	-	ns	
Hall signal, FG signal block (HallAIN, HallBIN, HallCIN, FG1IN, FG2IN, HallAOUT, HallBOUT, HallCOUT, FG1OUT, FG2OUT)						
Propagation delay time1	t1	-	15	-	ns	
Propagation delay time2	t2	-	50	-	ns	

○Package outline

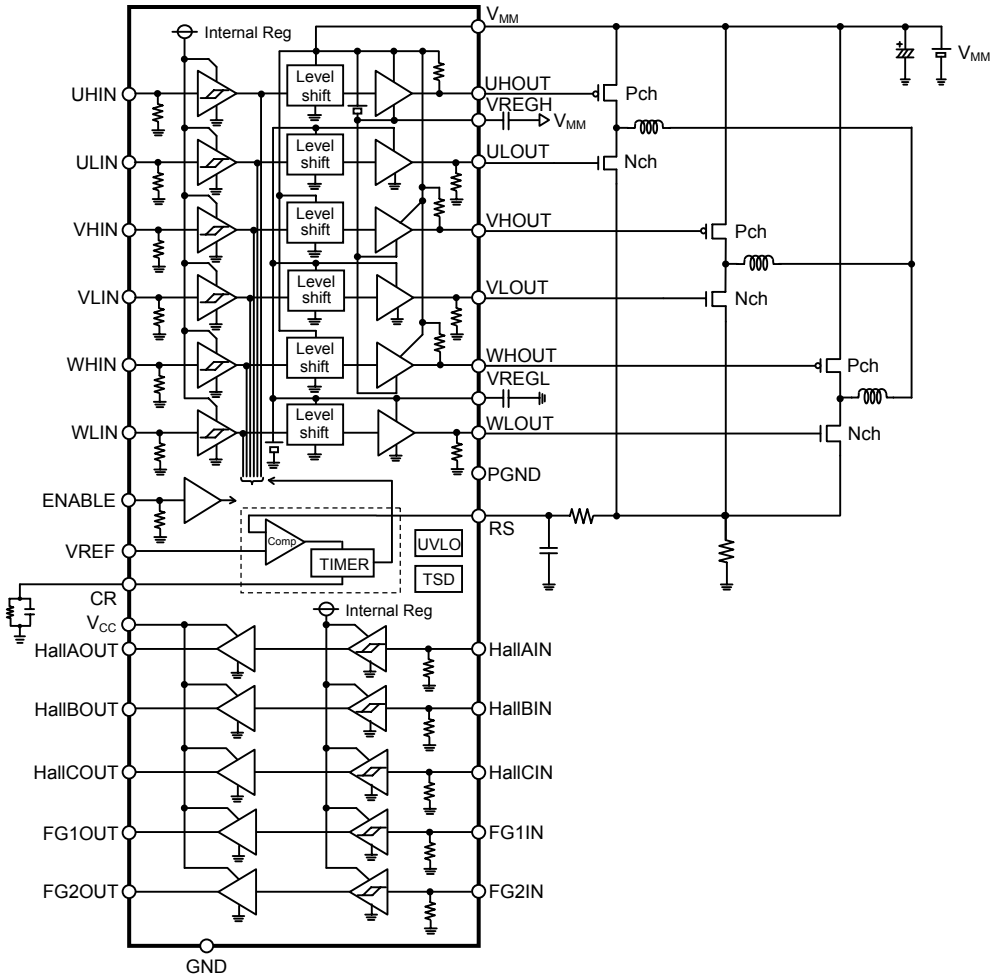


VQFN032V5050 (Unit:mm)

○Terminal No., Terminal name

Pin No.	Pin name	Pin No.	Pin name
1	**GND**	17	**PGND**
2	**HallAOUT**	18	**UHOUT**
3	**HallBOUT**	19	**ULOUT**
4	**HallCOUT**	20	**VHOUT**
5	**FG1OUT**	21	**VLOUT**
6	**FG2OUT**	22	**WHOUT**
7	**ENABLE**	23	**WLOUT**
8	**V_{CC}**	24	**V_{MM}**
9	**WLIN**	25	**VREGH**
10	**WHIN**	26	**VREGL**
11	**VLIN**	27	**FG2IN**
12	**VHIN**	28	**FG1IN**
13	**ULIN**	29	**HallCIN**
14	**UHIN**	30	**HallBIN**
15	**VREF**	31	**HallAIN**
16	**RS**	32	**CR**

○Block diagram



Because this document is the target specification, it is possible to change the contents.

○Operation Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Power supply lines

As return of current regenerated by back EMF of motor happens, take steps such as putting capacitor between power supply and GND as an electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) GND potential

The potential of GND pin must be minimum potential in all operating conditions.

(4) Metal on the backside (Define the side where product markings are printed as front)

The metal on the backside is shorted with the backside of IC chip therefore it should be connected to GND. Be aware that there is a possibility of malfunction or destruction if it is shorted with any potential other than GND.

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

(6) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(7) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(8) Thermal shutdown circuit

The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes Tjmax=150℃, and higher, the output to the FET will be open. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.

(9) Ground wiring pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

(10) Mounting errors and inter-pin short

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

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