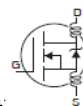


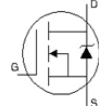
**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.054	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	8.86	11	m $\Omega$	$V_{GS} = 10V, I_D = 37A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
$g_{fs}$	Forward Trans conductance	120	—	—	S	$V_{DS} = 25V, I_D = 37A$ ③
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 55V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

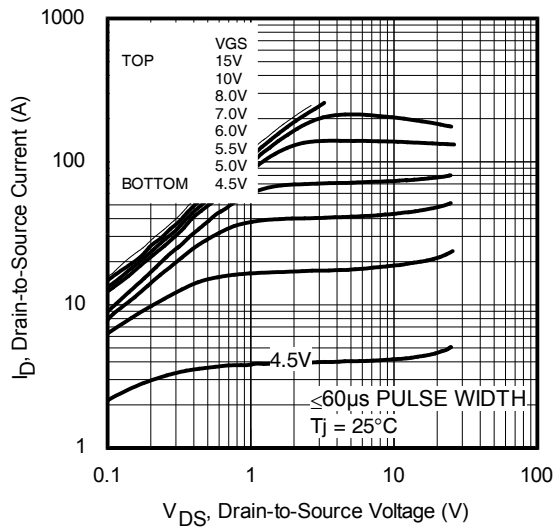
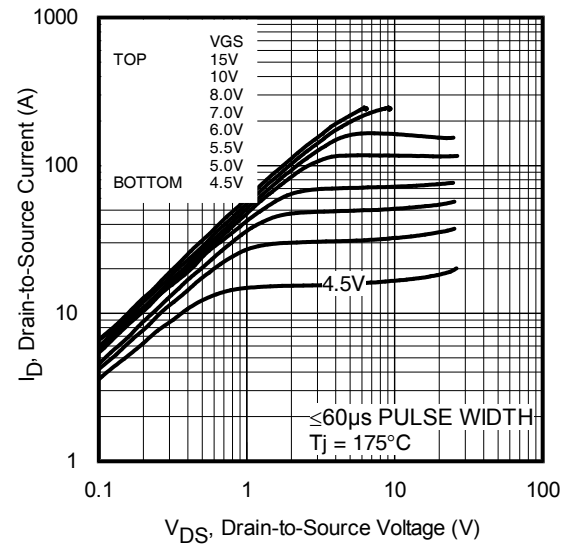
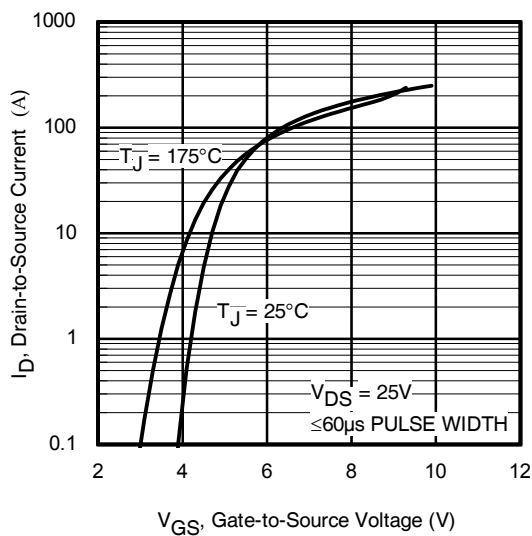
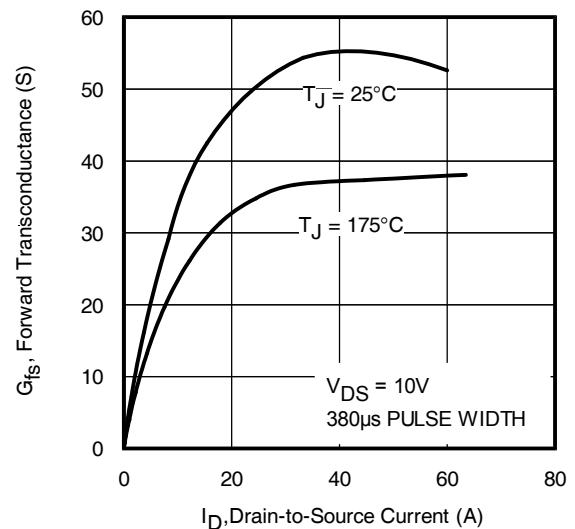
$Q_g$	Total Gate Charge	—	40	60	nC	$I_D = 37A$
$Q_{gs}$	Gate-to-Source Charge	—	11	—		$V_{DS} = 44V$
$Q_{gd}$	Gate-to-Drain Charge	—	15	—		$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 28V$
$t_r$	Rise Time	—	61	—		$I_D = 37A$
$t_{d(off)}$	Turn-Off Delay Time	—	40	—		$R_G = 12\Omega$
$t_f$	Fall Time	—	35	—		$V_{GS} = 10V$ ③
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	1720	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	290	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	160	—		$f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	1000	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	230	—		$V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance	—	360	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 44V$ ④

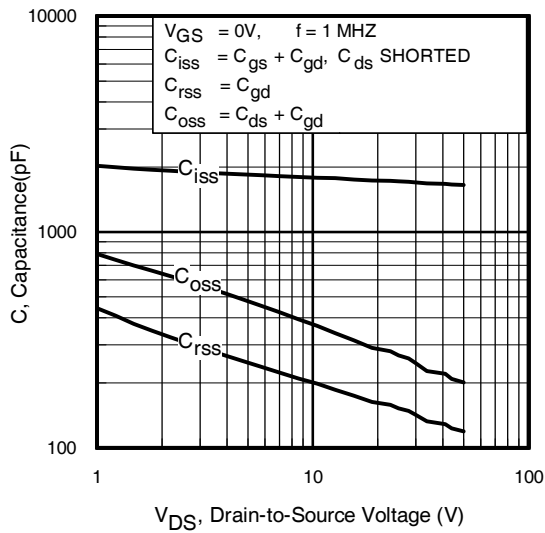
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	37	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	250		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 37A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	20	40	ns	$T_J = 25^\circ\text{C}, I_F = 37A, V_{DD} = 28V$
$Q_{rr}$	Reverse Recovery Charge	—	14	28	nC	$di/dt = 100A/\mu s$ ③
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

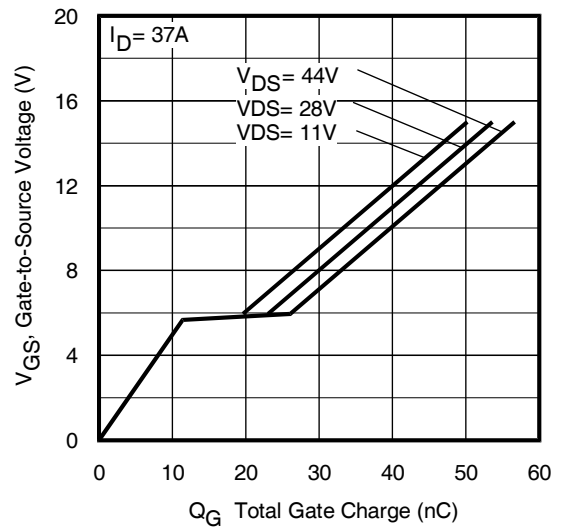
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.11mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 37A$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0ms$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑤ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.11mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 37A$ ,  $V_{GS} = 10V$ .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

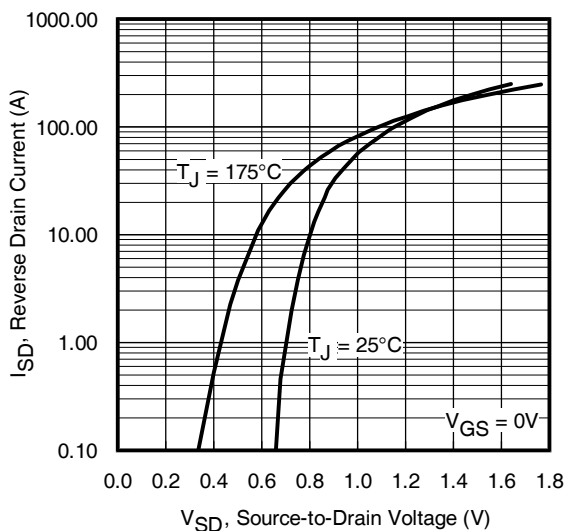

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Typical Forward Trans conductance Vs. Drain Current



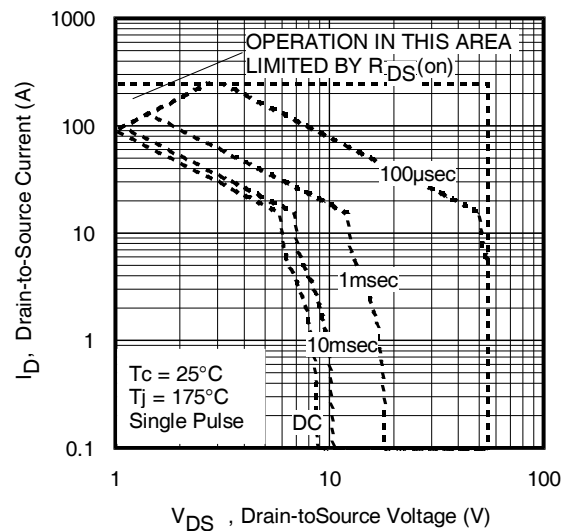
**Fig 5.** Typical Capacitance vs.  
Drain-to-Source Voltage



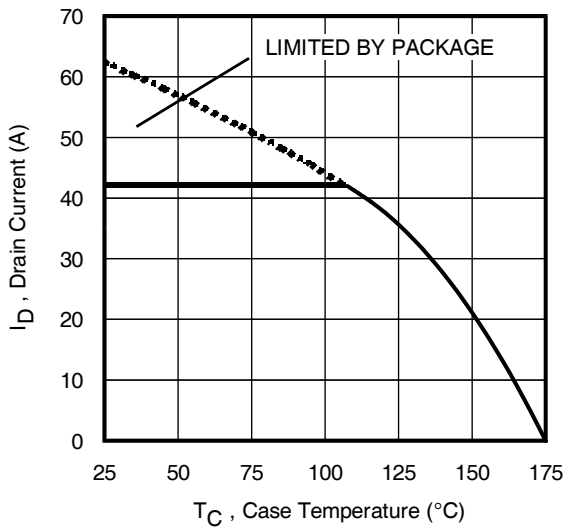
**Fig 6.** Typical Gate Charge vs.  
Gate-to-Source Voltage



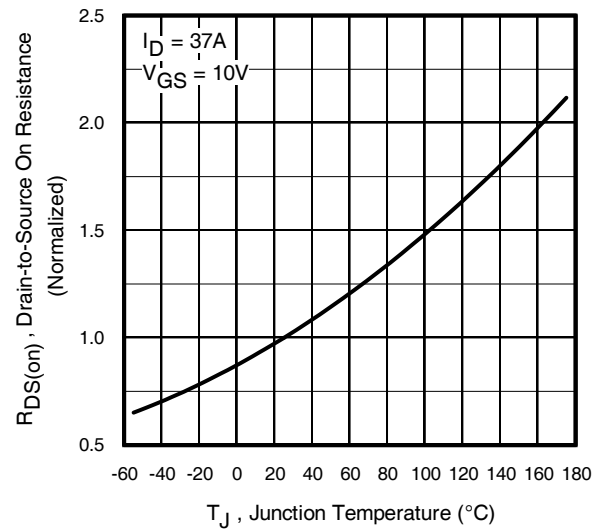
**Fig. 7** Typical Source-to-Drain Diode  
Forward Voltage



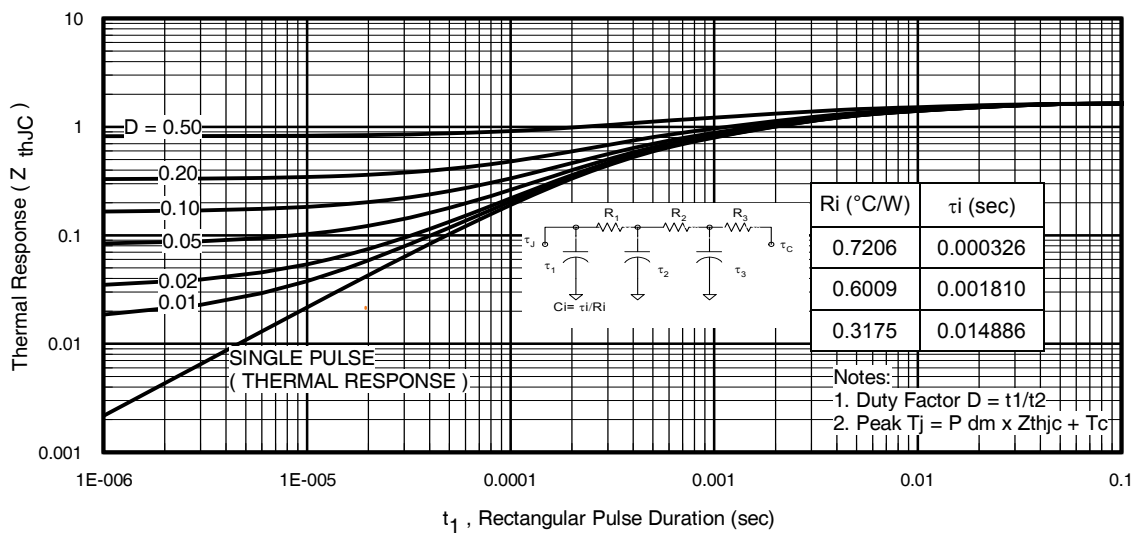
**Fig 8.** Maximum Safe Operating Area



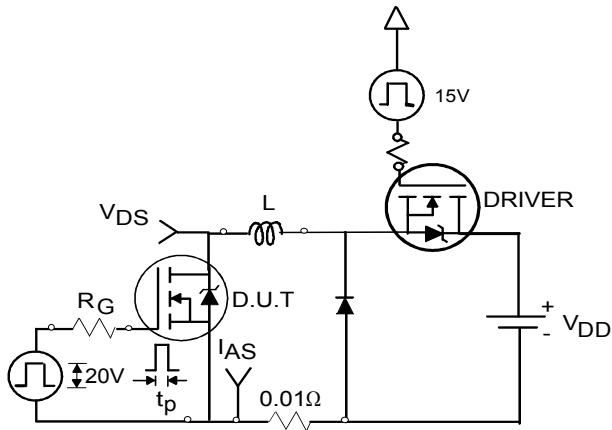
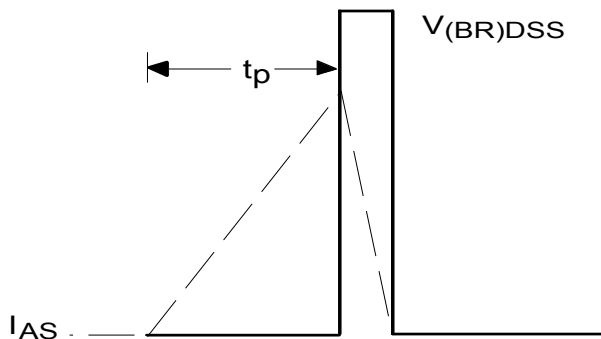
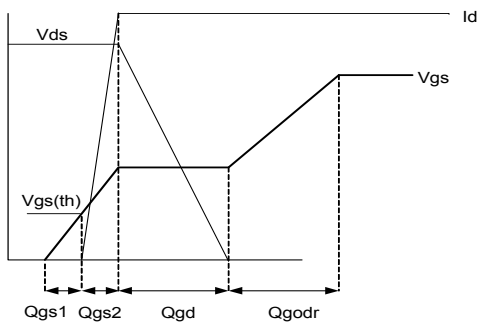
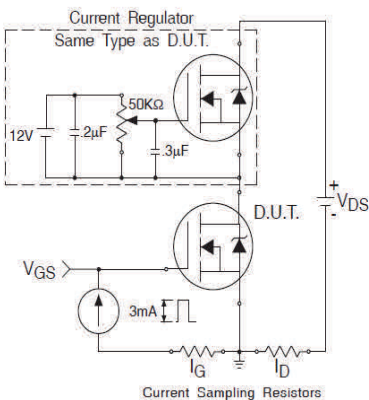
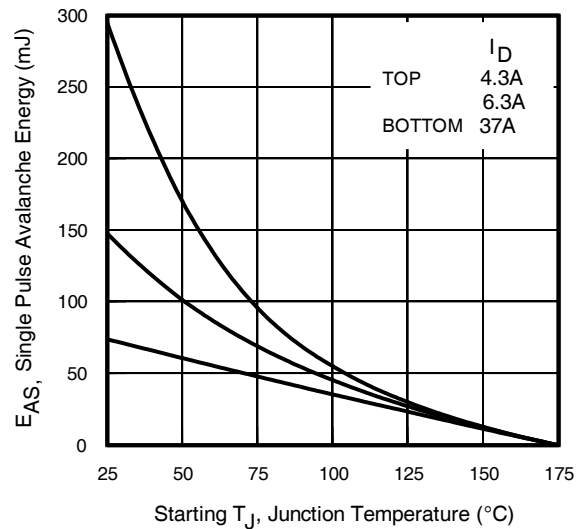
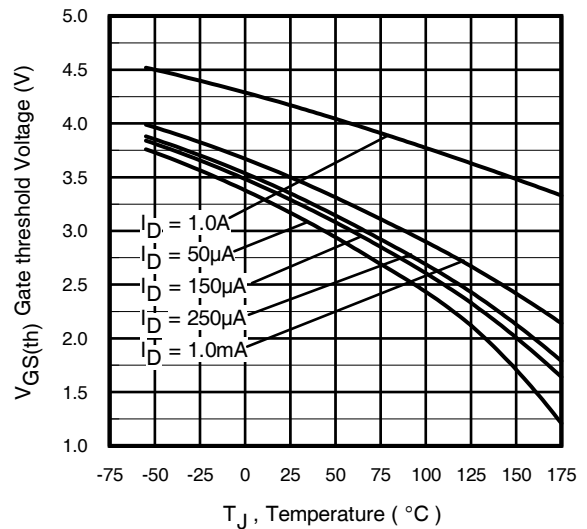
**Fig 9.** Maximum Drain Current Vs. Case Temperature

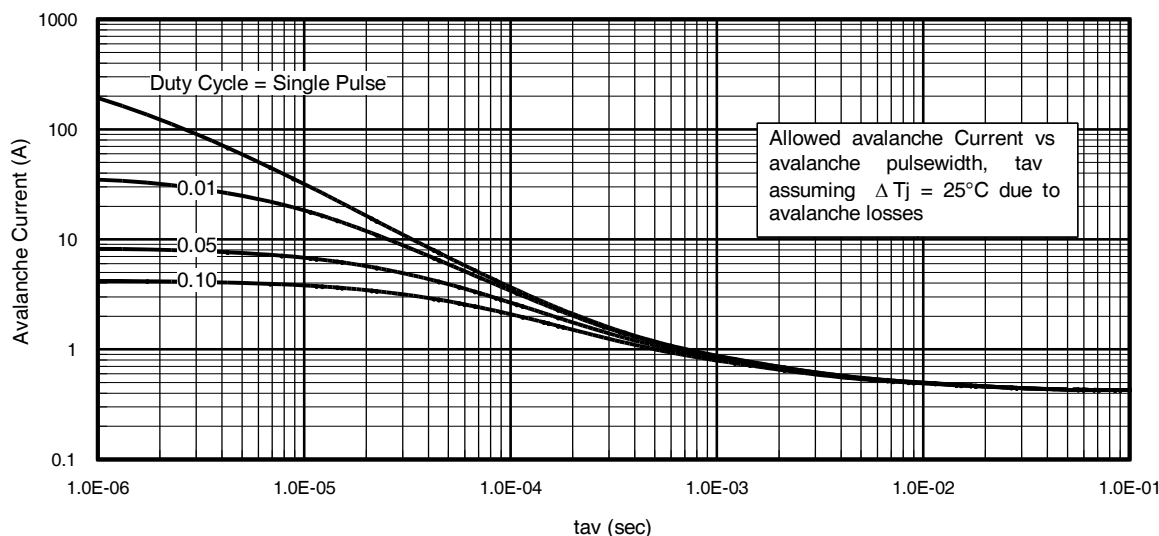


**Fig 10.** Normalized On-Resistance Vs. Temperature

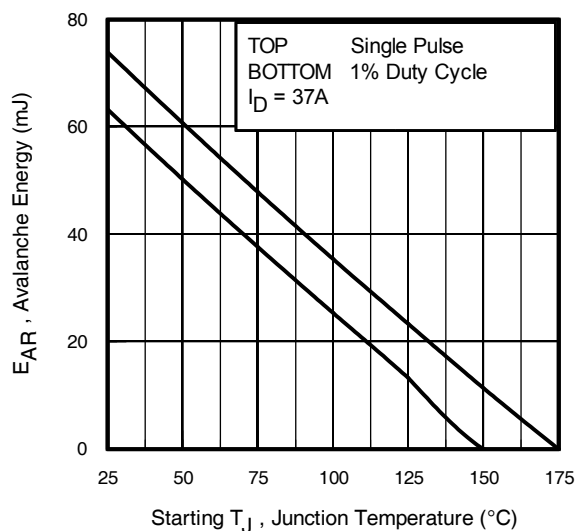


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a.** Unclamped Inductive Test Circuit

**Fig 12b.** Unclamped Inductive Waveforms

**Fig 13a.** Gate Charge Waveform

**Fig 13b.** Gate Charge Test Circuit

**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

**Fig 14.** Threshold Voltage Vs. Temperature



**Fig 15.** Typical Avalanche Current Vs. Pulse width



**Fig 16.** Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**

(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

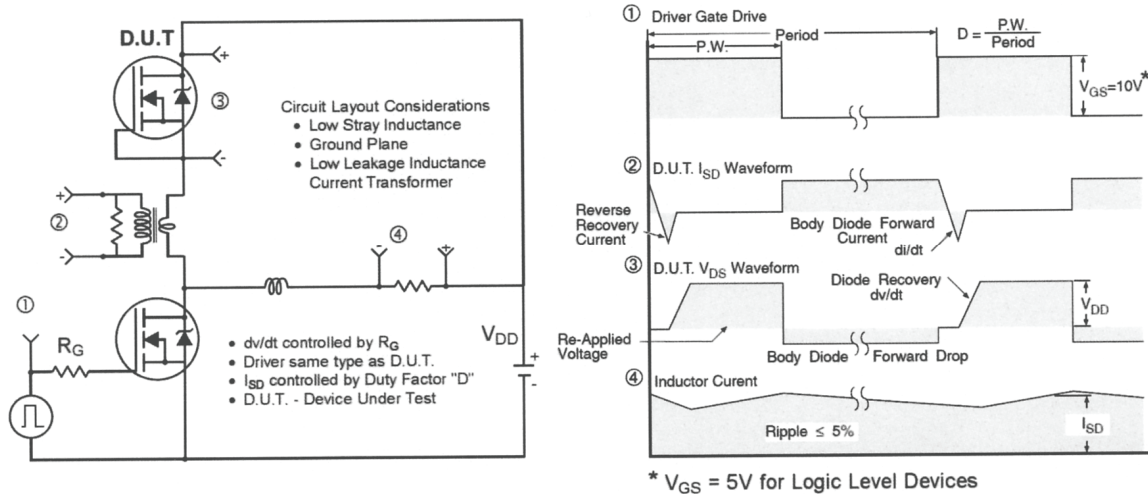


Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs

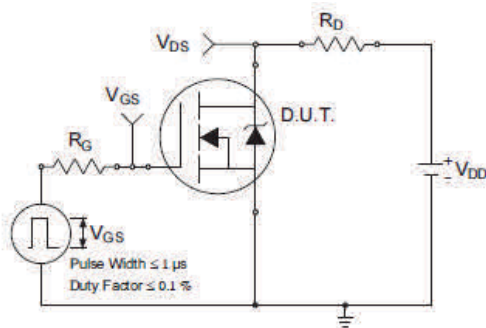


Fig 18a. Switching Time Test Circuit

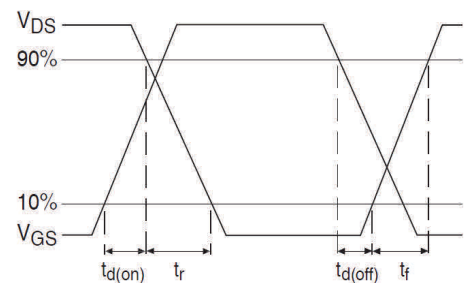
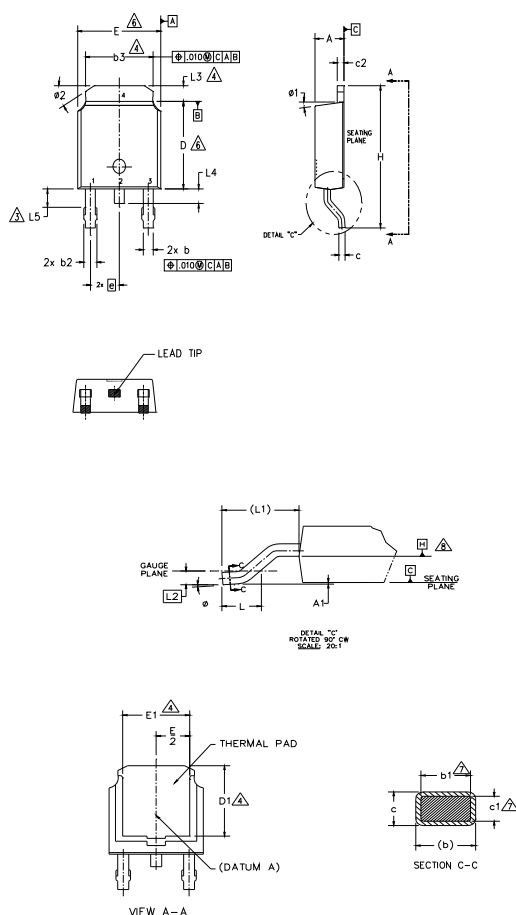


Fig 18b. Switching Time Waveforms

## D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))



### NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	7
A1	—	0.13	—	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	
b2	0.76	1.14	.030	.045	4
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	
c2	0.46	0.89	.018	.035	6
D	5.97	6.22	.235	.245	
D1	5.21	—	.205	—	
E	6.35	6.73	.250	.265	
E1	4.32	—	.170	—	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		4
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4	—	1.02	—	.040	
L5	1.14	1.52	.045	.060	3
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

### LEAD ASSIGNMENTS

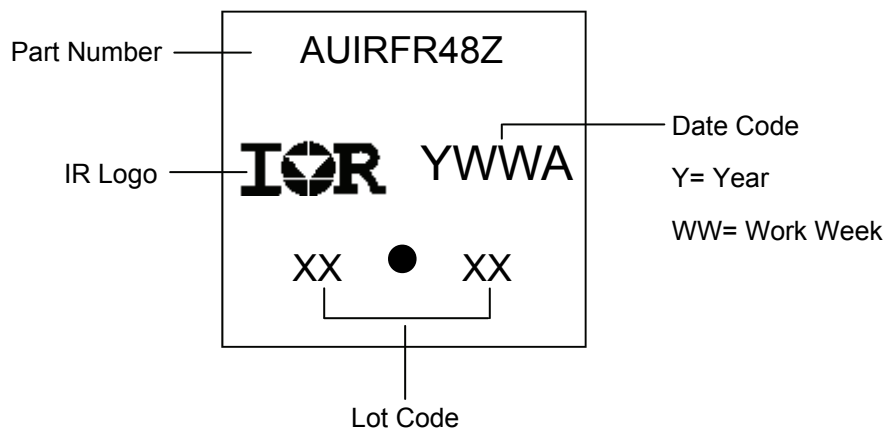
### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

### IGBT & CoPAK

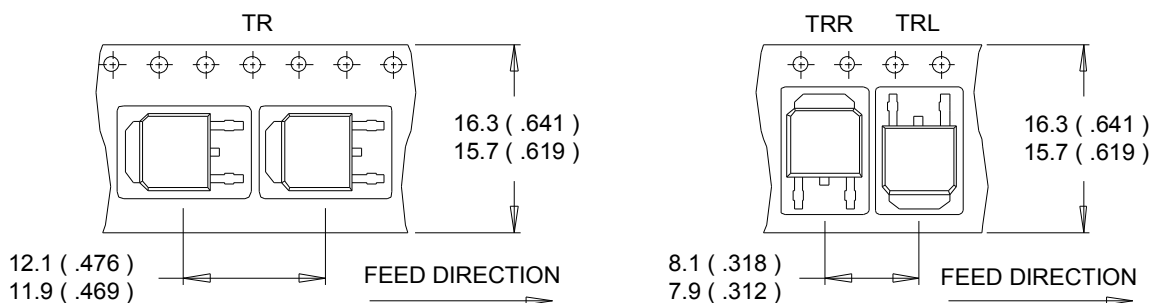
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

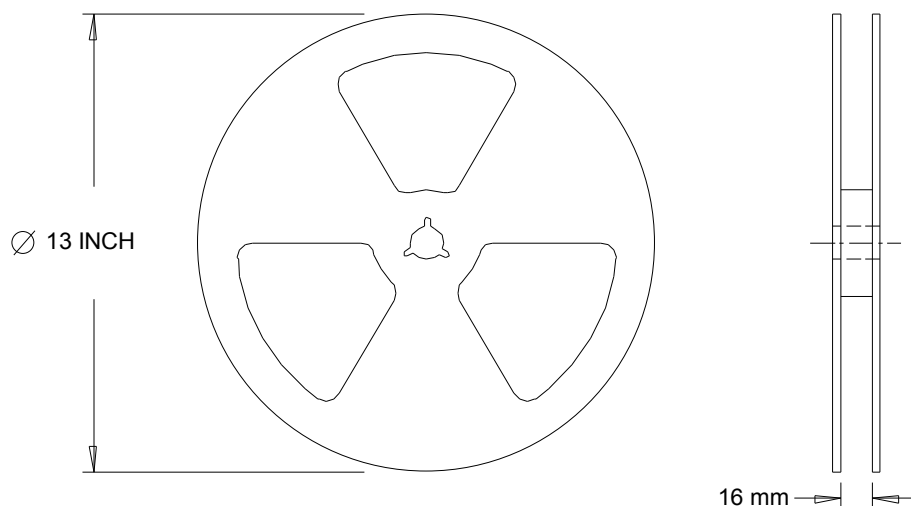


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**D-Pak (TO-252AA) Tape & Reel Information** (Dimensions are shown in millimeters (inches))

**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		D-Pak	MSL1
<b>ESD</b>	Machine Model	Class M4 (+/-425V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H1B (+/-1000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/-1125V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
12/1/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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