Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Min.	Max.	Units	Conditions
Supply Voltage	V_{CC}	0	4.5	V	
Input Logic Voltage	V_i	0	4.5	V	
Reflow Soldering Temperature			260	°C	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Conditions
Operating Temperature	T_A	-40	105	°C	
Storage Temperature	Ts	-40	125	°C	
Supply Voltage	V_{CC}	2.4	3.6	V	

Electrical & Optical Specifications (Ta=25°C)

Parameters	Symbol	Minimum	Typical	Maximum	Units	Conditions
Input						
Logic High Voltage, LEDON	V_{IH}	1.6		Vcc	V	
Logic High Voltage, ENB	V_{IH}	1.4		Vcc	V	For Vcc = 2.4V
		1.5		Vcc	V	For 2.4V < Vcc ≤ 3V
		1.7		Vcc	V	For 3V < Vcc ≤ 3.6V
Logic Low Voltage, LEDON	V_{IL}	0		0.3	V	
Logic Low Voltage, ENB	V_{IL}	0		0.3	V	
Logic High Input Current, LEDON	I_{IH}		0.1	1	uA	$V_I \geq V_{IH}$
Logic High Input Current, ENB	I_{IH}		0.1	1	µA	$V_I \geq V_{IH}$
Logic Low Input Current, LEDON	I_{IL}		0.1	1	µA	$V_I \leq V_{IL}$
Logic Low Input Current, ENB	I_{IL}		0.1	1	µA	$V_I \leq V_{IL}$
Shutdown Current	I_{SD}		0.3	1	µA	Vcc=3V, ENB=3V
Idle Current	Icc		500	650	µA	Vcc=3V, ENB=0V
Output						
Digital Output	V_{OL}	0		0.3	V	$I_{DOUT(Low)}$ = 2mA, Vcc = 3V
Rise Time(DOUT)	T_R		1		us	Vcc = 3V, R2 = 10kΩ, Frequency = 10kHz
Fall Time(DOUT)	T_F		1		us	Vcc = 3V, R2 = 10kΩ, Frequency = 10kHz
Transmitter						
Rise Time (LEDA)	T_R		40		ns	Vcc = 3V , I_{LED} = 120mA, Freq = 10kHz
Fall Time (LEDA)	T_F		40		ns	Vcc = 3V , I_{LED} = 120mA, Freq = 10kHz
Max I_{LED} Pulse Width	Max-PW		120		µs	Vcc=3V, ENB=0V
I_{LED} Pulse Current	I_{LED}		120	300	mA	Vcc=3V, R1 = 10Ω

Electrical & Optical Specification (continued)

Parameters	Symbol	Minimum	Typical	Maximum	Units	Conditions
Receiver						
Photodiode input current (PD)	I_{PD}	0		3	µA	
Current Gain	I_{PFILT}/I_{PD}		20		times	Vcc = 3V
Hysterisis Comparator						
Hysterisis	V_{HYS}		40		mV	Vcc= 3.0V
Threshold voltage	V_{TH}		655		mV	Vcc= 3.0V
Sunlight Cancellation						
DC Current, PD	I_{DC}		100		µA	Vcc= 3.0V

APDS-9700 pin-out and I/O Configurations

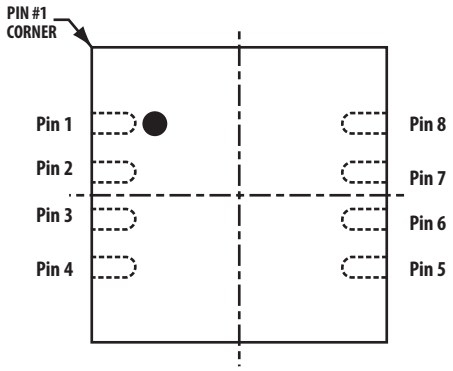


Figure 1. APDS-9700 pin-out and I/O Configurations

I/O Pins Configuration Table

Pin	Symbol	Type	Description
1	LEDON	Digital I/P	LED Driver Input LEDA will turn off when LEDON is stuck in high state for > Max-PW
2	ENB	Digital I/P	Power Down Enable ENB = 0 Normal mode operation ENB = 1 Shut down mode
3	DOUT	Digital O/P	Digital Output An open drain output that requires a pull-up resistor of recommended value 10k Ω DOUT = Low when $V_{PFILT} > V_{TH}$ DOUT = High when $V_{PFILT} < V_{TH}$
4	GND	Ground	Ground
5	PD	Analog I/P	Photo-Detector Input Connect to Cathode of photo-detector (proximity sensor)
6	PFILT	Analog O/P	Analog Output Connect to integration circuit (R3 & CX3)
7	LEDA	Analog O/P	LED Driver Output Connect to Anode of LED (proximity sensor) LEDA will turn off when LEDON is stuck in high state for > Max-PW
8	VCC	Supply	Voltage Supply

Application Circuit for APDS-9700

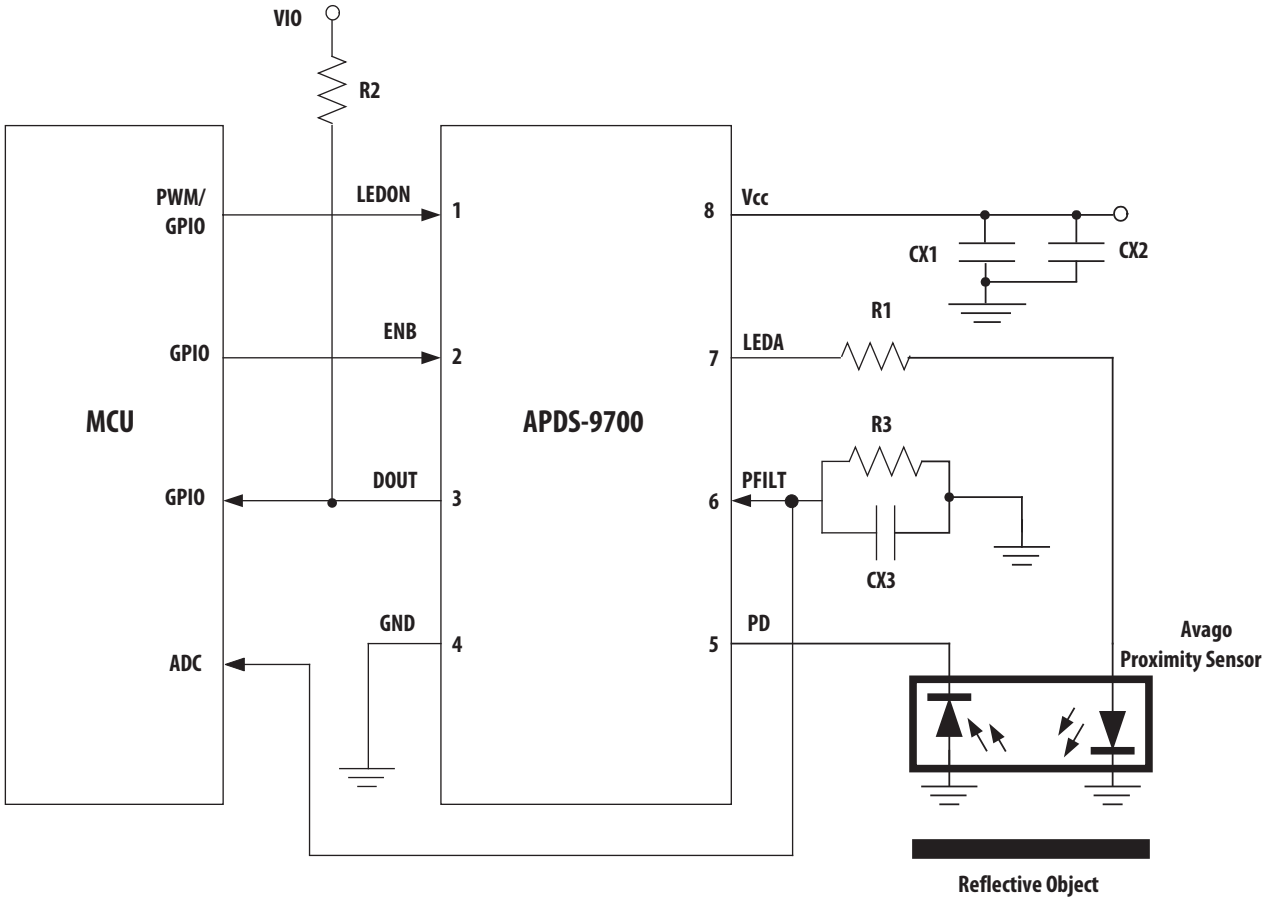


Figure 2. Typical Application Circuit for APDS-9700

Recommended Avago Proximity Sensor	Description
HSDL-9100	Integrated Reflective Proximity Sensor

Component	Recommended Values (with HSDL-9100)
R1	10 Ω
R2	10k Ω
R3	100k Ω to 500k Ω
CX1	100 nF ± 20% X 7R, Ceramic,
CX2	6.8 µF ± 20%, Tantalum
CX3	3.3 nF ± 20% X 7R, Ceramic

APDS-9700 Block Diagram

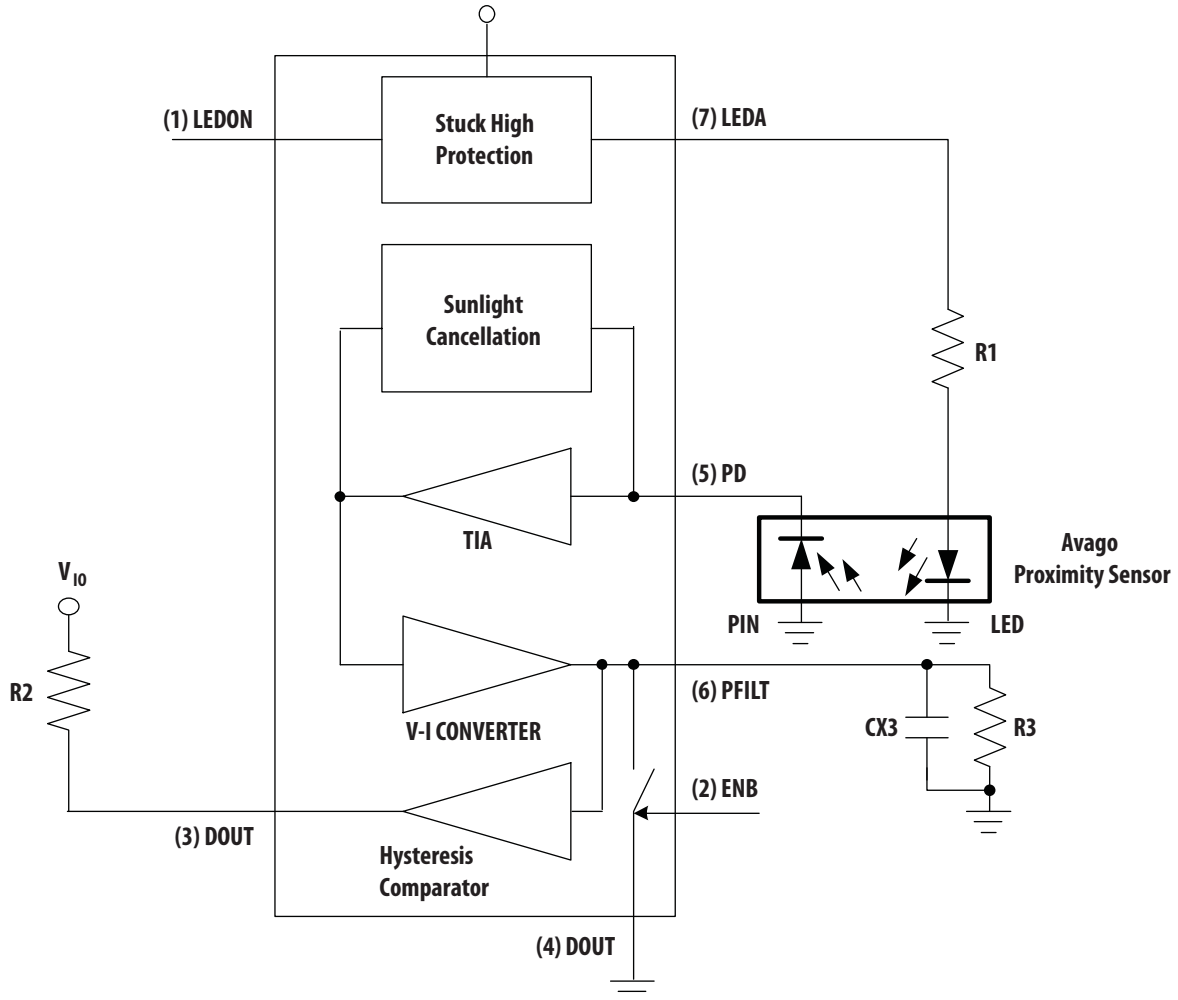
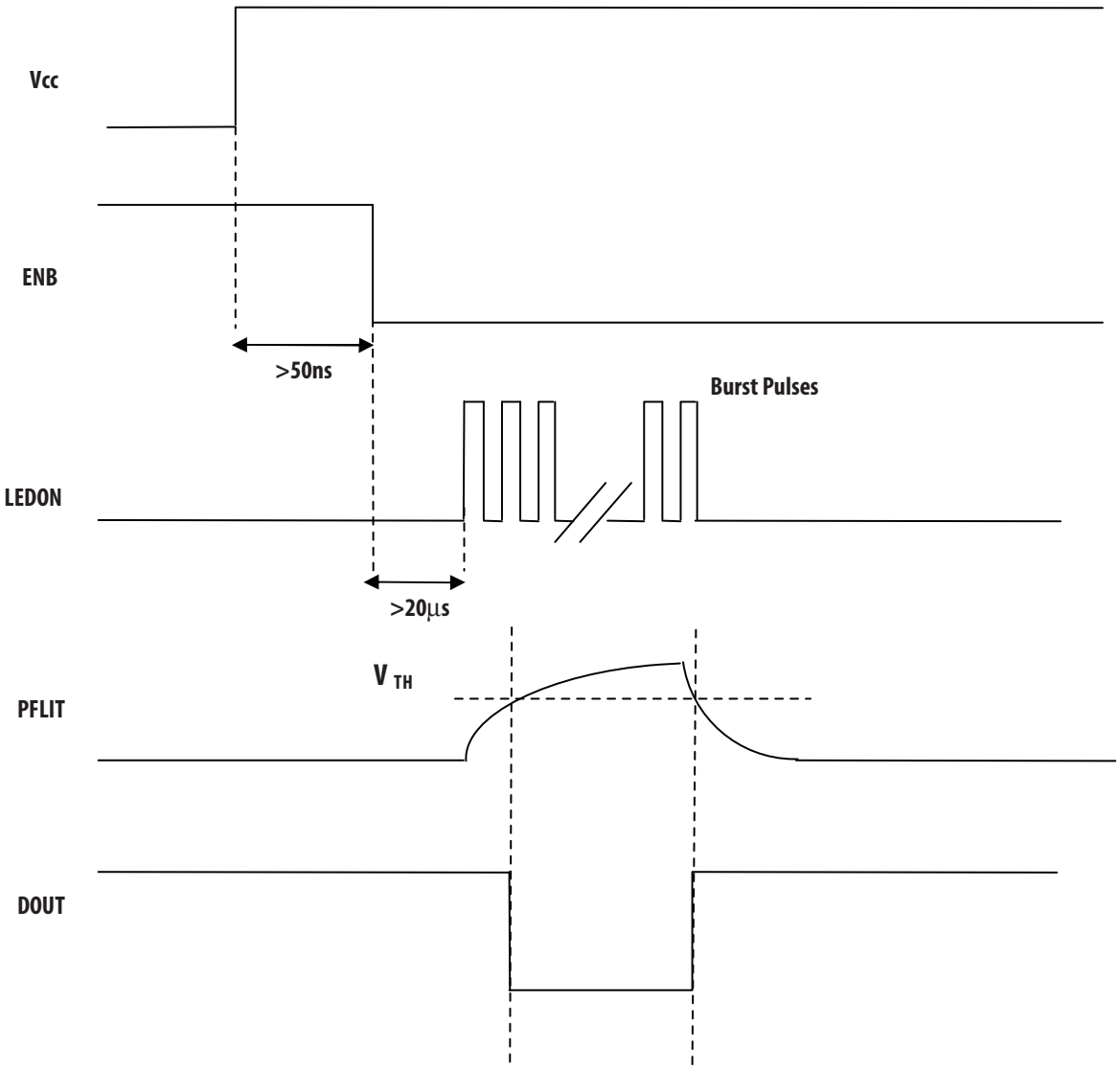


Figure 3. APDS-9700 Block Diagram

APDS-9700 Typical Timing Waveforms



Note:
Pulses at LEDON can only be activated at least 20us after ENB turn from high to low.

Figure 4. APDS-9700 Typical Timing Waveforms

APDS-9700 Performance Charts (Typical Conditions)

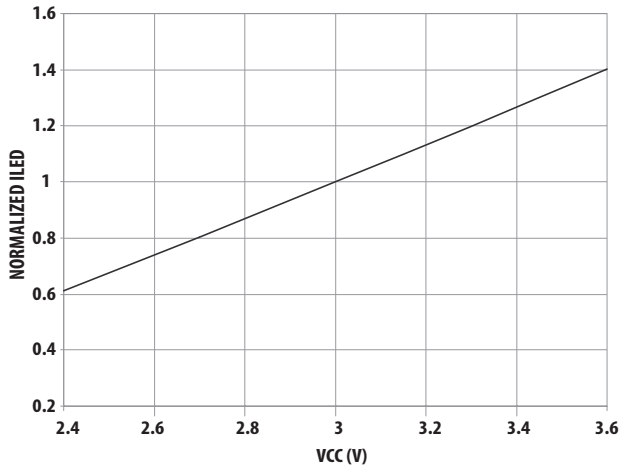


Figure 5. Normalized ILED Vs Vcc (T=25 °C, R1=10Ω)

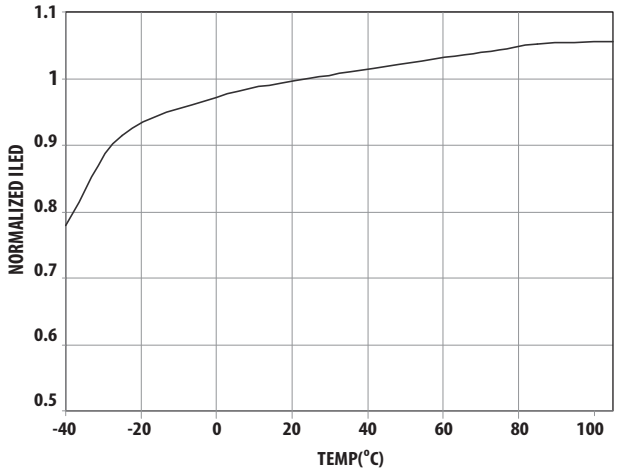


Figure 6. Normalized ILED VS Temp (VCC=3V,R1=10Ω)

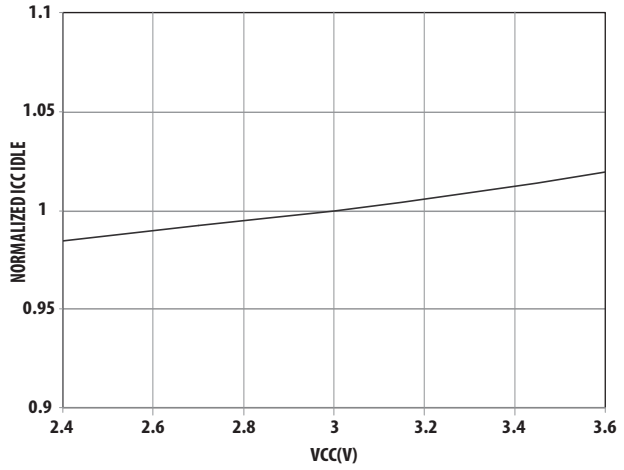


Figure 7. Normalized ICC Idle Vs Vcc (T=25°C)

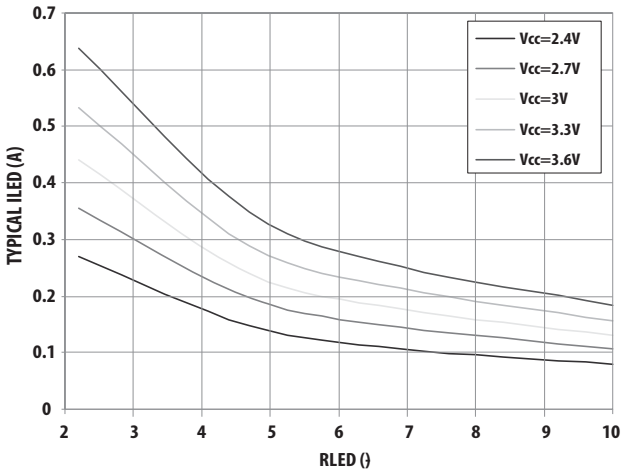


Figure 8. ILED VS RLED (T=25°C)

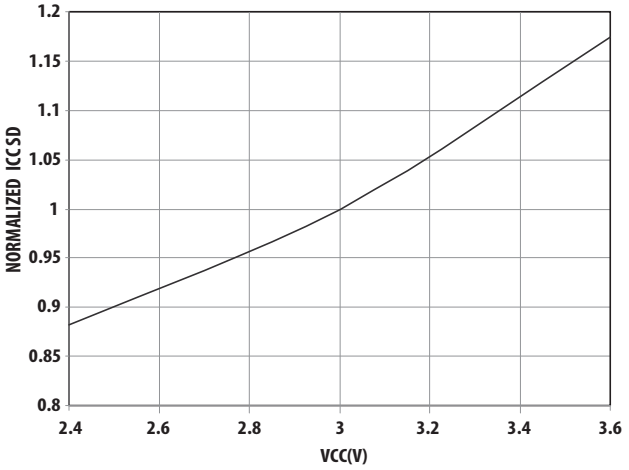


Figure 9. Normalized ICC SD VS VCC (T=25°C)

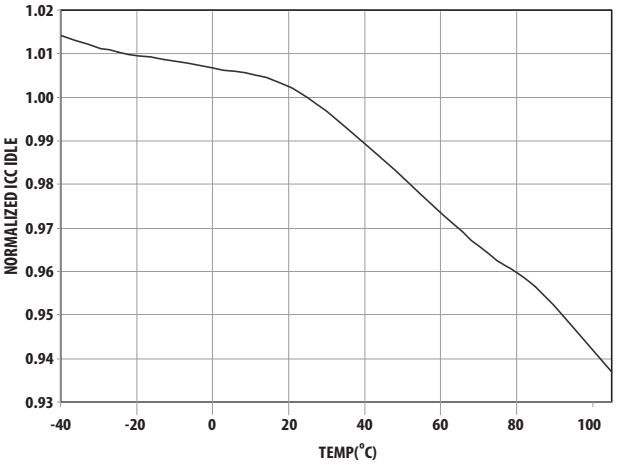
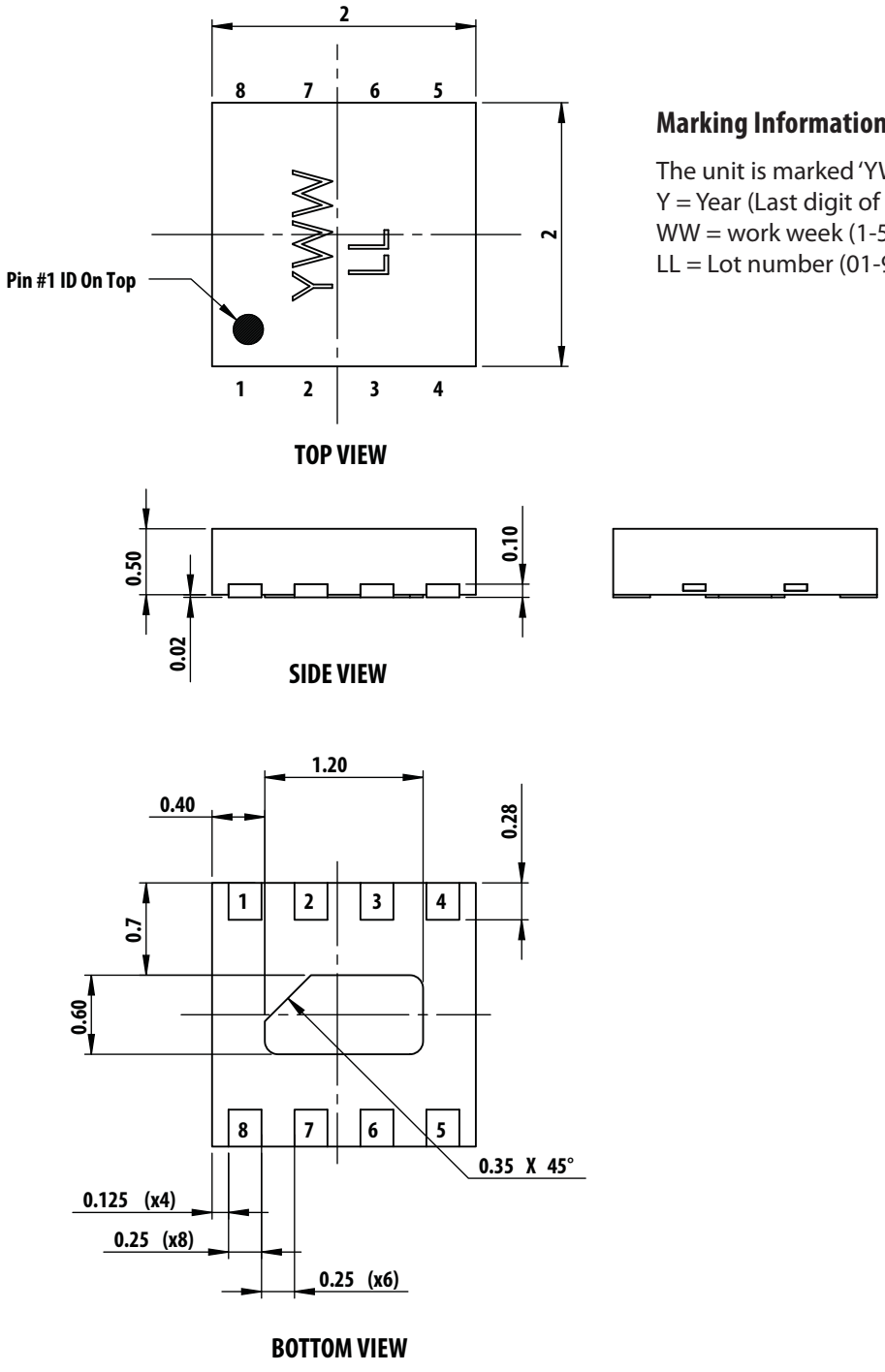


Figure 10. Normalized ICC IDLE VS TEMP (VCC=3V)

APDS-9700 Package Dimensions



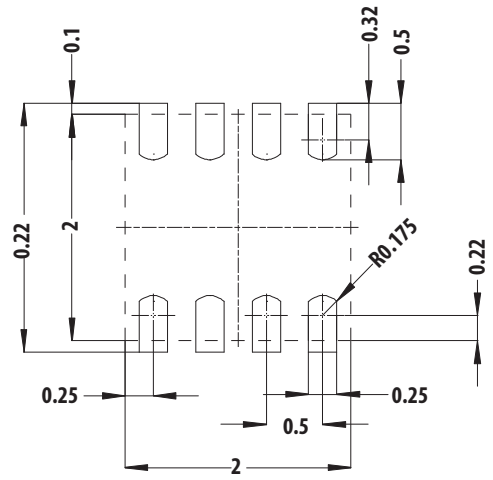
Marking Information

The unit is marked 'YWW LL' on the chip.
Y = Year (Last digit of the year)
WW = work week (1-54)
LL = Lot number (01-99)

Dimensions in mm. Tolerance ±0.1mm

Figure 11. Package Outline Dimensions and land patterm

Recommended Minimum Land pattern and Keep-out Area



SOLDER LAND PATTERN

Dimension in mm. Tolerances +0.1mm

Figure 12. Recommended Minimum Land pattern and Keep-out Area

Keep-out Area Recommendations:

1. Area of Solder Land pattern = 2.3mm x 2.1mm
2. Module placement tolerance & keep out on each side with no lead = 0.55mm & keep out on each side solder lead = 0.8mm
3. Keep-out area = 3.9mm x 3.2mm

APDS-9700 Tape Dimensions

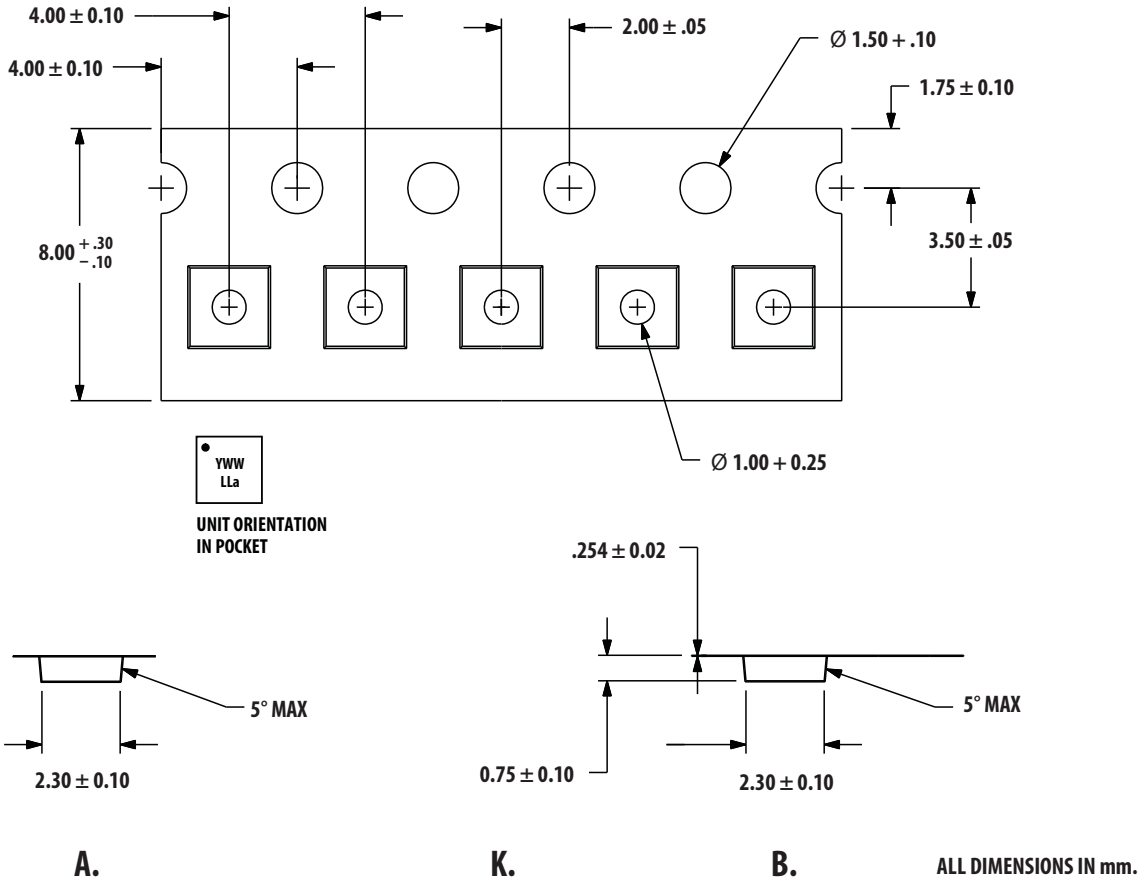


Figure 13. APDS-9700 Tape Dimensions

Reel Drawings

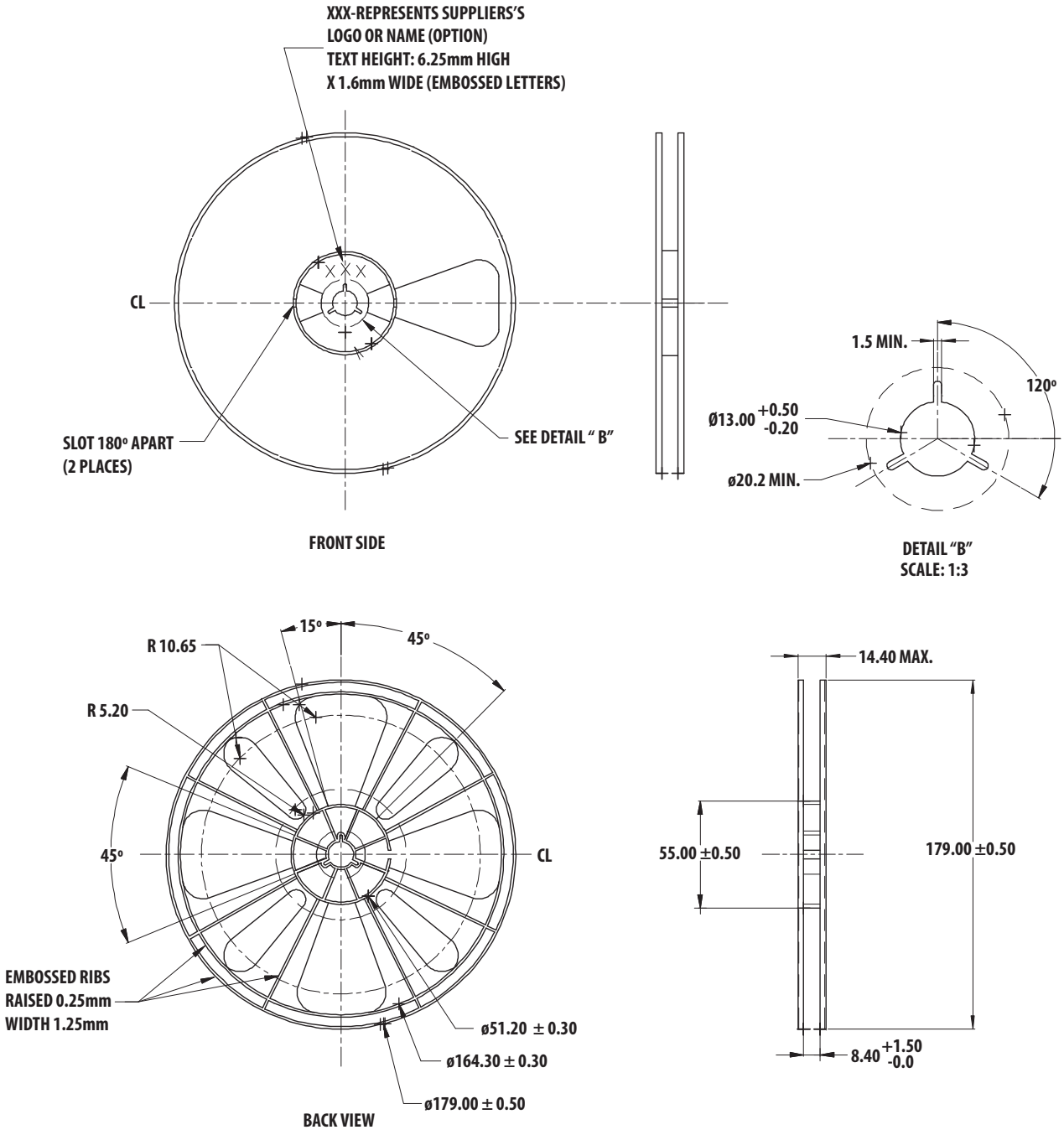


Figure 14. Reel Dimension Drawing

APDS-9700 Packaging

All APDS-9700 options are shipped in ESD proof package.

This part is compliant to JEDEC MSL1.

Recommended Storage Conditions

Storage Temperature	The units in tape and reel are recommended to be kept in a controlled climate environment, with temp at 25 +5/-10°C and relative humidity at 55 +/-15%.
Time from unsealing to soldering	This part is compliant to JEDEC MSL-1 (unlimited floor life at < 30'C / 85%RH)

Recommended Reflow Profile

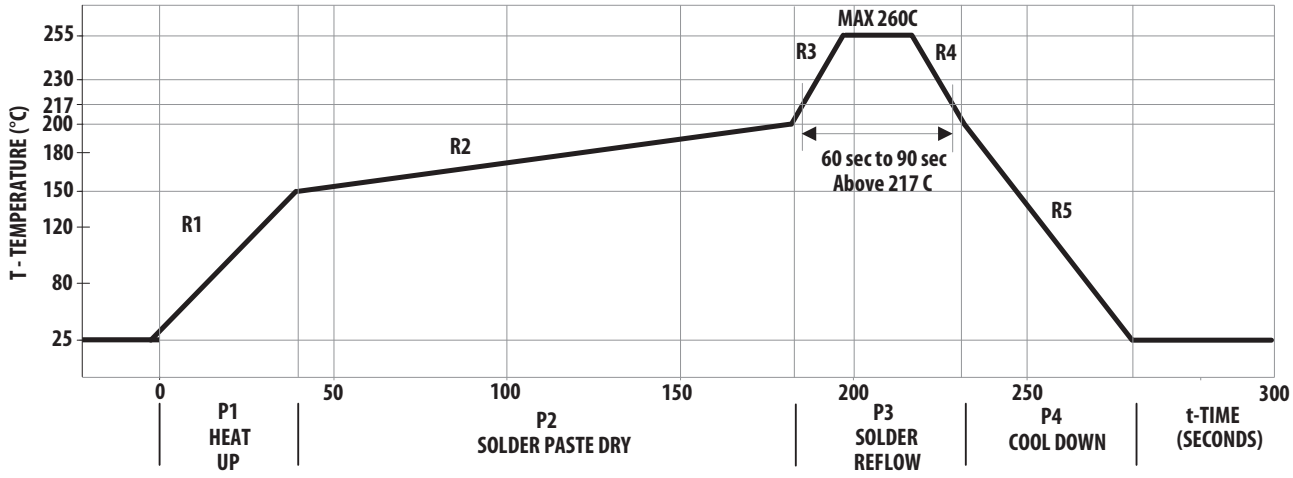


Figure 15. Recommended Reflow Profile

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and APDS-9700 pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and APDS-9700 pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 40 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 40 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and APDS-9700 pins to change dimensions evenly, putting minimal stresses on the APDS-9700.

It is recommended to perform reflow soldering no more than twice.

AV02-0893EN - March 4, 2010