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REVISION HISTORY

6/09—Rev. 0 to Rev. A

Updated Outline Dimensions 15
Changes to Ordering Guide 15

1/07—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.5 V) or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 2.2 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.5		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		60		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			70	µA
		I_{OUT} = 100 µA		75		µA
		I_{OUT} = 100 µA, T_J = −40°C to +125°C			85	µA
		I_{OUT} = 100 mA		210		µA
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			250	µA
		I_{OUT} = 300 mA		365		µA
		I_{OUT} = 300 mA, T_J = −40°C to +125°C			420	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.1		µA
		EN = GND, T_J = −40°C to +125°C			1.0	µA
FIXED OUTPUT VOLTAGE ACCURACY (ADP1712 FIXED, ADP1713, AND ADP1714)	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		100 µA < I_{OUT} < 300 mA, T_J = −40°C to +125°C	−2		+2	%
ADJUSTABLE OUTPUT VOLTAGE ACCURACY (ADP1712 ADJUSTABLE)[1]	V_{OUT}	I_{OUT} = 10 mA	0.792	0.8	0.808	V
		100 µA < I_{OUT} < 300 mA, T_J = −40°C to +125°C	0.784	0.8	0.816	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−0.25		+0.25	%/V
LOAD REGULATION[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 300 mA		0.001		%/mA
		I_{OUT} = 10 mA to 300 mA, T_J = −40°C to +125°C			0.004	%/mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 100 mA, V_{OUT} ≥ 3.0 V		60	70	mV
		I_{OUT} = 100 mA, V_{OUT} ≥ 3.0 V, T_J = −40°C to +125°C			80	mV
		I_{OUT} = 300 mA, V_{OUT} ≥ 3.0 V		170	205	mV
		I_{OUT} = 300 mA, V_{OUT} ≥ 3.0 V, T_J = −40°C to +125°C			230	mV
		I_{OUT} = 100 mA, 2.5 V ≤ V_{OUT} < 3.0 V		70	85	mV
		I_{OUT} = 100 mA, 2.5 V ≤ V_{OUT} < 3.0 V, T_J = −40°C to +125°C			95	mV
		I_{OUT} = 300 mA, 2.5 V ≤ V_{OUT} < 3.0 V		200	235	mV
		I_{OUT} = 300 mA, 2.5 V ≤ V_{OUT} < 3.0 V, T_J = −40°C to +125°C			270	mV
START-UP TIME[4]	$T_{START-UP}$					
ADP1712 Adjustable and ADP1714				70		µs
ADP1712 External Soft Start		C_{SS} = 10 nF		7.3		ms
ADP1713		With 10 nF bypass capacitor		90		µs
CURRENT LIMIT THRESHOLD[5]	I_{LIMIT}		380	500	700	mA
THERMAL SHUTDOWN THRESHOLD	TS_{SD}	T_J rising		150		°C
THERMAL SHUTDOWN HYSTERESIS	TS_{SD-HYS}			15		°C
SOFT-START SOURCE CURRENT (ADP1712 WITH EXTERNAL SOFT START)	$SS_{I-SOURCE}$	SS = GND	0.8	1.2	1.5	µA
UVLO ACTIVE THRESHOLD	$UVLO_{ACTIVE}$	V_{IN} falling	2			V
UVLO INACTIVE THRESHOLD	$UVLO_{INACTIVE}$	V_{IN} rising			2.45	V
UVLO HYSTERESIS	$UVLO_{HYS}$			250		mV
V_{OUT} to V_{TRK} ACCURACY (ADP1714)	$V_{TRK-ERROR}$	0 V ≤ V_{TRK} ≤ (0.5 × $V_{OUT(NOM)}$), $V_{OUT(NOM)}$ ≤ 1.8 V, T_J = −40°C to +125°C	−40		+40	mV
		0 V ≤ V_{TRK} ≤ (0.5 × $V_{OUT(NOM)}$), $V_{OUT(NOM)}$ > 1.8 V, T_J = −40°C to +125°C	−80		+80	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
EN INPUT LOGIC HIGH	V_{IH}	2.5 V ≤ V_{IN} ≤ 5.5 V	1.8			V
EN INPUT LOGIC LOW	V_{IL}	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN INPUT LEAKAGE CURRENT	$V_{I-LEAKAGE}$	EN = IN or GND		0.1	1	µA
ADJ INPUT BIAS CURRENT (ADP1712 ADJUSTABLE)	ADJ_{I-BIAS}			30	100	nA
OUTPUT NOISE	OUT_{NOISE}					
ADP1713		10 Hz to 100 kHz, V_{IN} = 5.0 V, V_{OUT} = 0.75 V, with 10 nF bypass capacitor		40		µV rms
ADP1712 and ADP1714		10 Hz to 100 kHz, V_{IN} = 5.0 V, V_{OUT} = 3.3 V		380		µV rms
POWER SUPPLY REJECTION RATIO	PSRR					
ADP1713		1 kHz, V_{IN} = 5.0 V, V_{OUT} = 0.75 V, with 10 nF bypass capacitor		72		dB
ADP1712 and ADP1714		1 kHz, V_{IN} = 5.0 V, V_{OUT} = 3.3 V		65		dB

[1] Accuracy when OUT is connected directly to ADJ. When OUT voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of resistors used.
[2] Based on an end-point calculation using 10 mA and 300 mA loads. See Figure 10 for typical load regulation performance for loads less than 10 mA.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.5 V.
[4] Start-up time is defined as the time between the rising edge of EN to OUT being at 95% of its nominal value.
[5] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN to GND	−0.3 V to +6 V
OUT to GND	−0.3 V to IN
EN to GND	−0.3 V to +6 V
SS/ADJ/BYP/TRK to GND	−0.3 V to +6 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Lead Temperature, Soldering (10 sec)	300°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
5-Lead TSOT	170	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

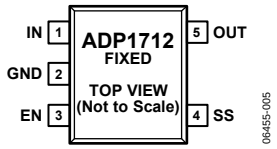

Figure 5. 5-Lead TSOT (UJ-Suffix)

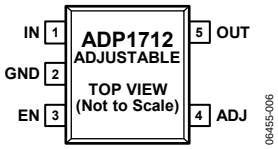

Figure 6. 5-Lead TSOT (UJ-Suffix)

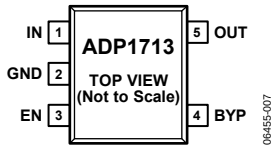

Figure 7. 5-Lead TSOT (UJ-Suffix)

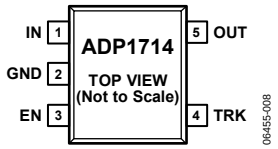

Figure 8. 5-Lead TSOT (UJ-Suffix)

Table 4. Pin Function Descriptions

ADP1712 Fixed Pin No.	ADP1712 Adjustable Pin No.	ADP1713 Pin No.	ADP1714 Pin No.	Mnemonic	Description
1	1	1	1	IN	Regulator Input Supply. Bypass IN to GND with a 2.2 µF or greater capacitor.
2	2	2	2	GND	Ground.
3	3	3	3	EN	Enable Input. Drive EN high to turn on the regulator; drive it low to turn off the regulator. For automatic startup, connect EN to IN.
4				SS	Soft Start. Connect a capacitor between SS and GND to set the output start-up time.
	4			ADJ	Adjust. A resistor divider from OUT to ADJ sets the output voltage.
		4		BYP	Bypass. Connect a 1 nF or greater capacitor (10 nF recommended) between BYP and GND to reduce the internal reference noise for low noise applications.
			4	TRK	Track. The output follows the voltage placed on the TRK pin. (See the Theory of Operation section for a more detailed description.)
5	5	5	5	OUT	Regulated Output Voltage. Bypass OUT to GND with a 2.2 µF or greater capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 2.2 µF, T_A = 25°C, unless otherwise noted.

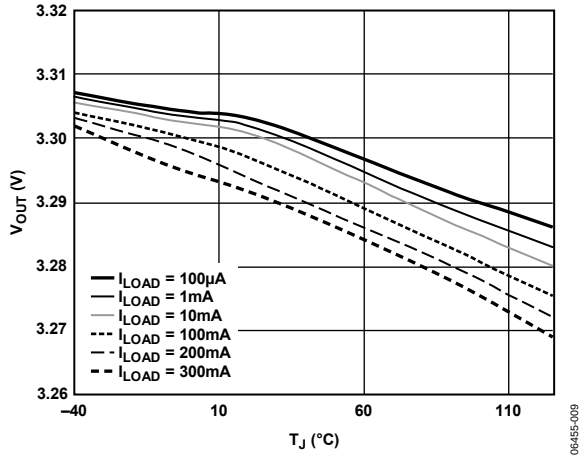

Figure 9. Output Voltage vs. Junction Temperature

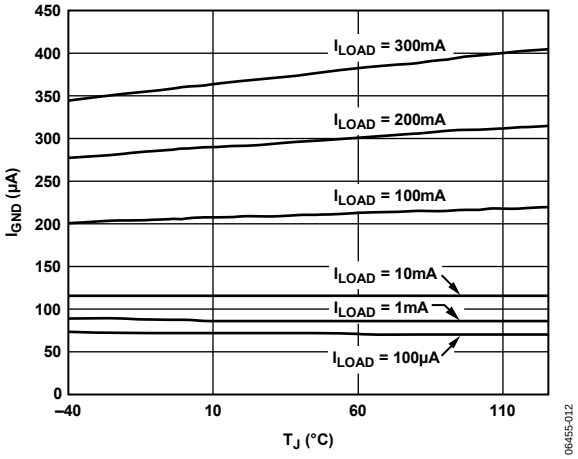

Figure 12. Ground Current vs. Junction Temperature

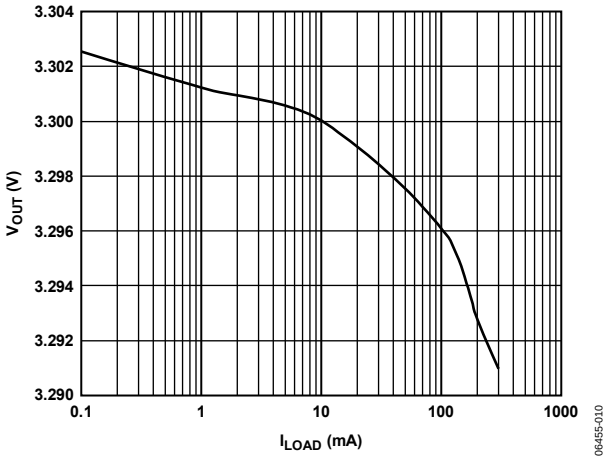

Figure 10. Output Voltage vs. Load Current

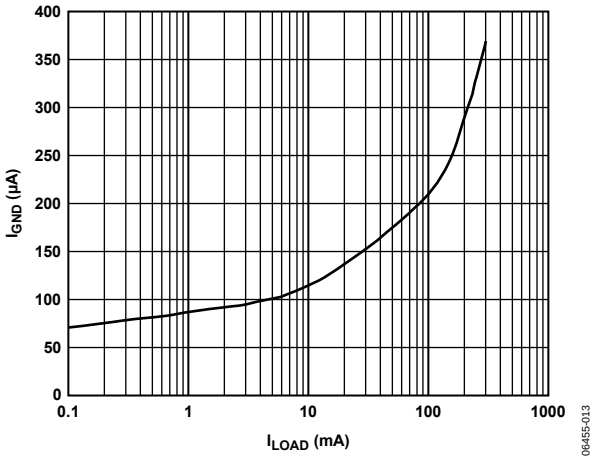

Figure 13. Ground Current vs. Load Current

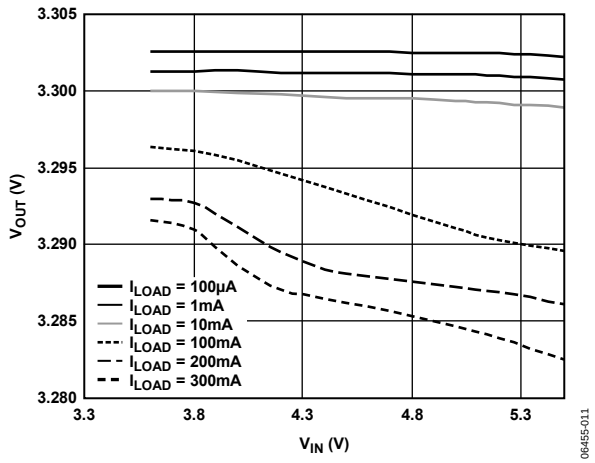

Figure 11. Output Voltage vs. Input Voltage

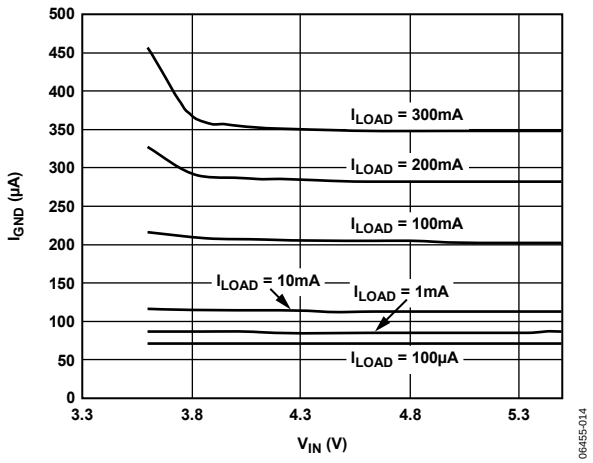

Figure 14. Ground Current vs. Input Voltage

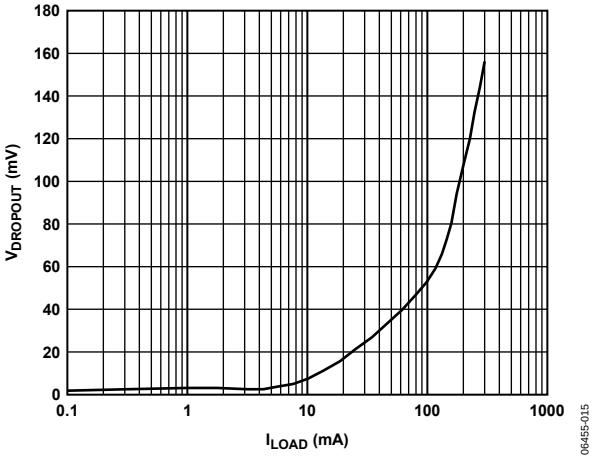

Figure 15. Dropout Voltage vs. Load Current

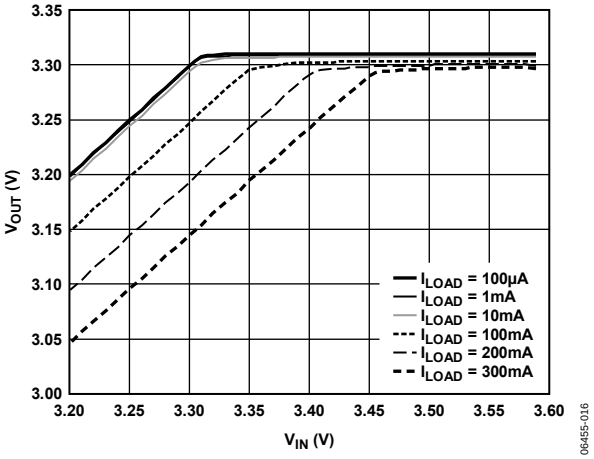

Figure 16. Output Voltage vs. Input Voltage (in Dropout)

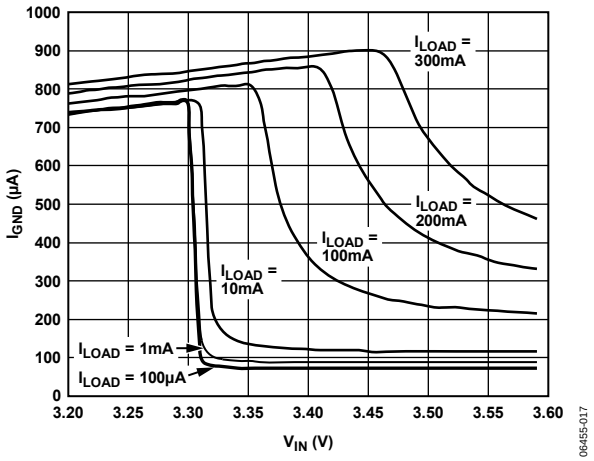

Figure 17. Ground Current vs. Input Voltage (in Dropout)

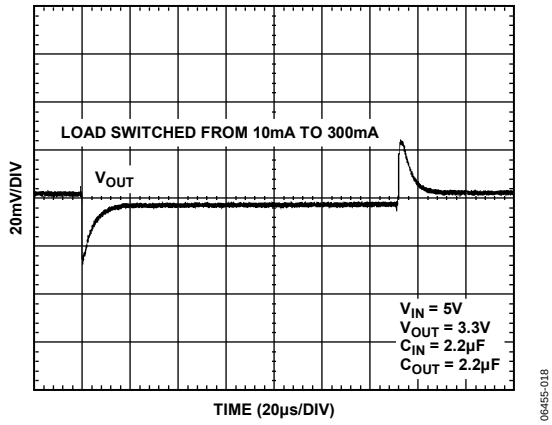

Figure 18. Load Transient Response

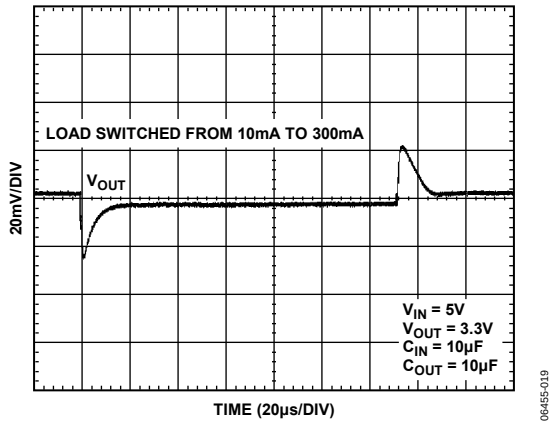

Figure 19. Load Transient Response

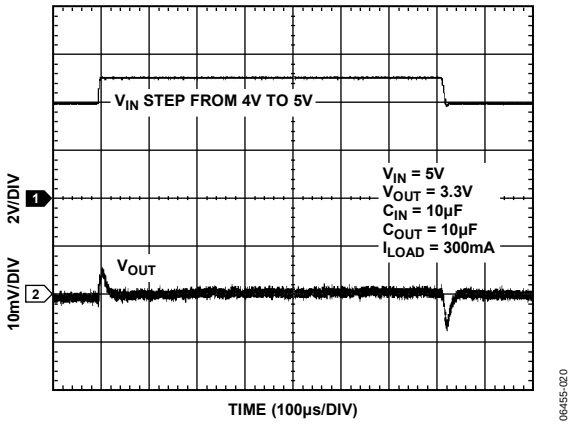

Figure 20. Line Transient Response

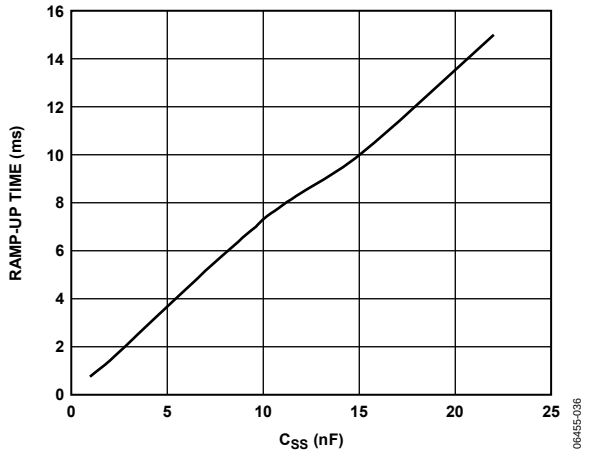

Figure 21. Output Voltage Ramp-Up Time vs. Soft-Start Capacitor Value

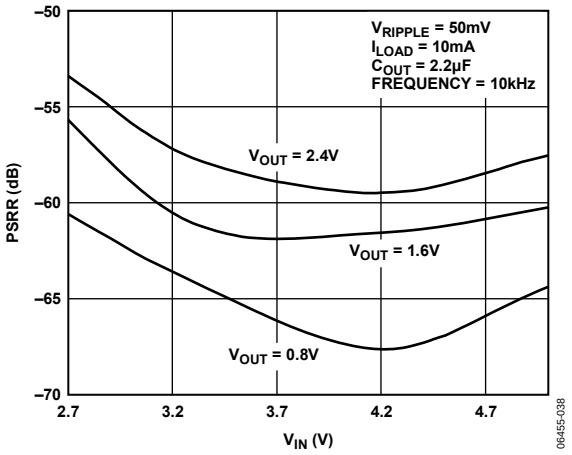

Figure 23. ADP1712 Adjustable Power Supply Rejection Ratio vs. Input Voltage

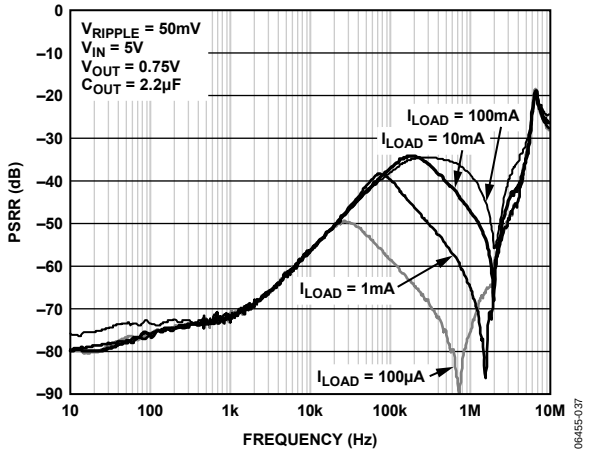

Figure 22. ADP1713 Power Supply Rejection Ratio vs. Frequency (10 nF Bypass Capacitor)

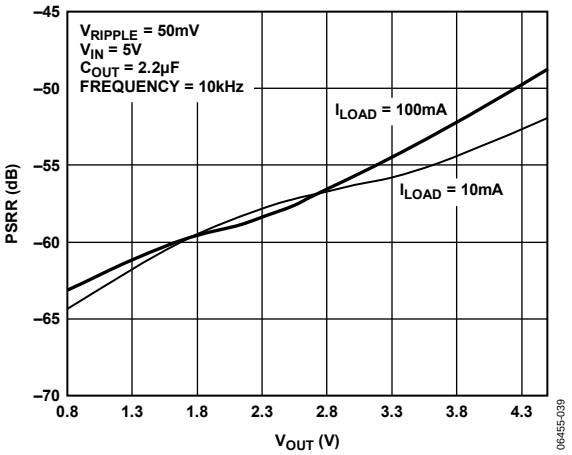

Figure 24. ADP1712 Adjustable Power Supply Rejection Ratio vs. Output Voltage

THEORY OF OPERATION

The ADP1712/ADP1713/ADP1714 are low dropout linear regulators that use an advanced, proprietary architecture to provide high power supply rejection ratio (PSRR) and excellent line and load transient response with just a small 2.2 µF ceramic output capacitor. All devices operate from a 2.5 V to 5.5 V input rail and provide up to 300 mA of output current. Incorporating a novel scaling architecture, ground current is very low when driving light loads. Ground current in the shutdown mode is typically less than 1 µA.

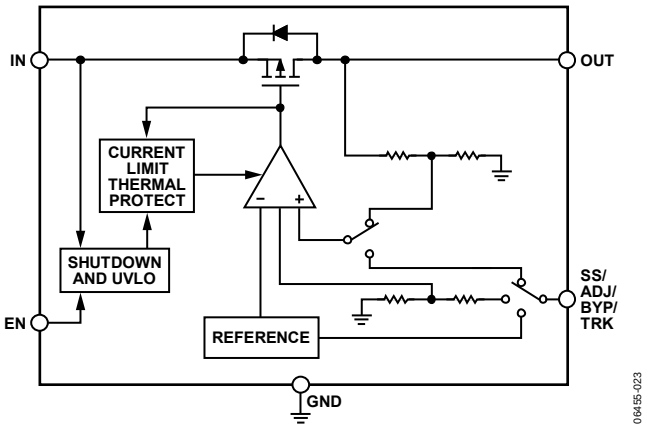

Figure 25. Internal Block Diagram

Internally, the ADP1712/ADP1713/ADP1714 each consist of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, which allows more current to pass and increases the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP1712 is available in two versions, one with a fixed output voltage and one with an adjustable output voltage. The fixed output voltage is set internally to one of sixteen values between 0.75 V and 3.3 V, using an internal feedback network. The adjustable output voltage can be set to between 0.8 V and 5.0 V by an external voltage divider connected from OUT to ADJ. The ADP1713 and ADP1714 are available in fixed output voltage options only. The ADP1712 fixed version allows an external soft-start capacitor to be connected between the SS pin and GND, which controls the output voltage ramp during startup. The ADP1713 allows a reference bypass capacitor to be connected between the BYP pin and GND, which reduces output voltage noise and improves power supply rejection. The ADP1714 features a track pin, which allows the output voltage to follow the voltage at the TRK pin.

A logic on the EN pin determines if the output is active. When EN is high, the output is on, and when EN is low, the output is off.

SOFT-START FUNCTION (ADP1712)

For applications that require a controlled startup, the ADP1712 provides a programmable soft-start function. Programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. To implement soft start, connect a small ceramic capacitor from SS to GND. Upon startup, a 1.2 µA current source charges this capacitor. The ADP1712 start-up output voltage is limited by the voltage at SS, providing a smooth ramp up to the nominal output voltage. The soft-start time is calculated by

$$T_{SS} = V_{REF} \times (C_{SS}/I_{SS}) \quad (1)$$

where:

T_{SS} is the soft-start period.
V_{REF} is the 0.8 V reference voltage.
C_{SS} is the soft-start capacitance from SS to GND.
I_{SS} is the current sourced from SS (1.2 µA).

When the ADP1712 is disabled (using EN), the soft-start capacitor is discharged to GND through an internal 100 Ω resistor.

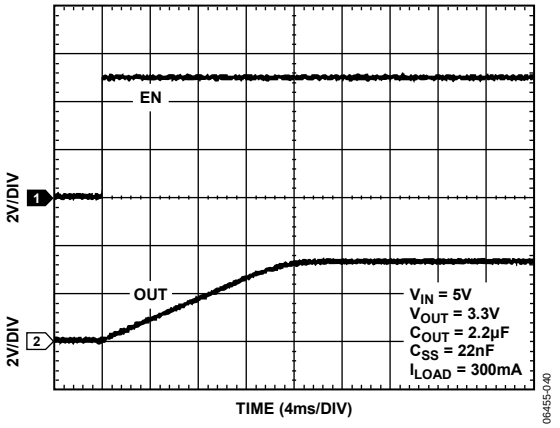

Figure 26. OUT Ramp-Up with External Soft-Start Capacitor

The ADP1712 adjustable version, ADP1713, and ADP1714 have no pins for soft start, so the function is switched to an internal soft-start capacitor. This sets the soft-start ramp-up period to approximately 24 µs.

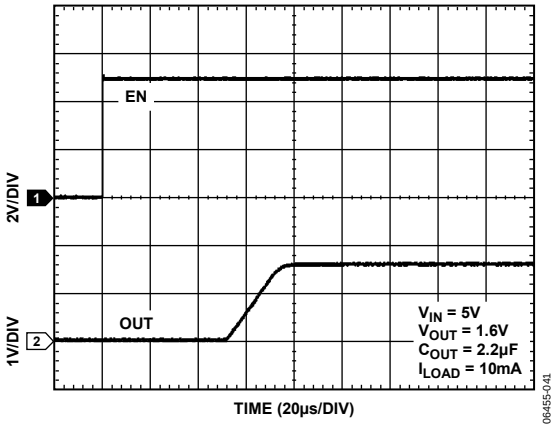

Figure 27. OUT Ramp-Up with Internal Soft-Start

ADJUSTABLE OUTPUT VOLTAGE (ADP1712 ADJUSTABLE)

The ADP1712 adjustable version can have its output voltage set over a 0.8 V to 5.0 V range. The output voltage is set by connecting a resistive voltage divider from OUT to ADJ. The output voltage is calculated using the equation

$$V_{OUT} = 0.8\ V\ (1 + R1/R2) \quad (2)$$

where:

R1 is the resistor from OUT to ADJ.
R2 is the resistor from ADJ to GND.

The maximum bias current into ADJ is 100 nA, so for less than 0.5% error due to the bias current, use values less than 60 kΩ for R2.

BYPASS CAPACITOR (ADP1713)

The ADP1713 allows for an external bypass capacitor to be connected to the internal reference, which reduces output voltage noise and improves power supply rejection. A low leakage capacitor of 1 nF or greater (10 nF is recommended) must be connected between the BYP and GND pins.

TRACK MODE (ADP1714)

The ADP1714 includes a tracking mode feature. As shown in Figure 28, if the voltage applied at the TRK pin is less than the nominal output voltage, OUT is equal to the voltage at TRK. Otherwise, OUT regulates to its nominal output value.

For example, consider an ADP1714 with a nominal output voltage of 3 V. If the voltage applied to its TRK pin is greater than 3 V, OUT maintains a nominal output voltage of 3 V. If the voltage applied to TRK is reduced below 3 V, OUT tracks this voltage. OUT can track the TRK pin voltage from the nominal value all the way down to 0 V. A voltage divider is present from TRK to the error amplifier input with a divider ratio equal to the divider from OUT to the error amplifier. This sets the output voltage equal to the tracking voltage. Both divider ratios are set by post-package trim, depending on the desired output voltage.

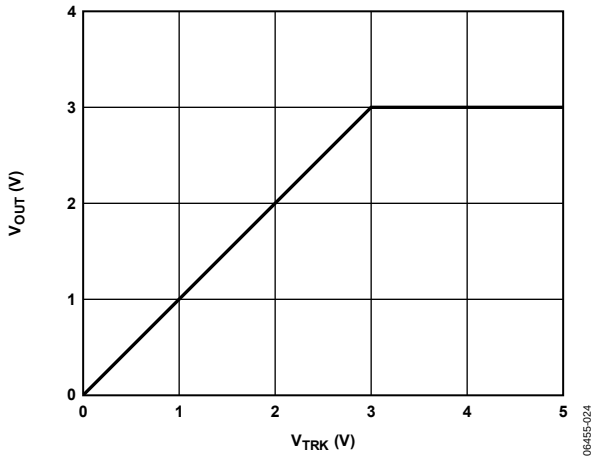

Figure 28. ADP1714 Output Voltage vs. Tracking Voltage with Nominal Output Voltage Set to 3 V

ENABLE FEATURE

The ADP1712/ADP1713/ADP1714 use the EN pin to enable and disable the OUT pin under normal operating conditions. As shown in Figure 29, when a rising voltage on EN crosses the active threshold, OUT turns on. When a falling voltage on EN crosses the inactive threshold, OUT turns off.

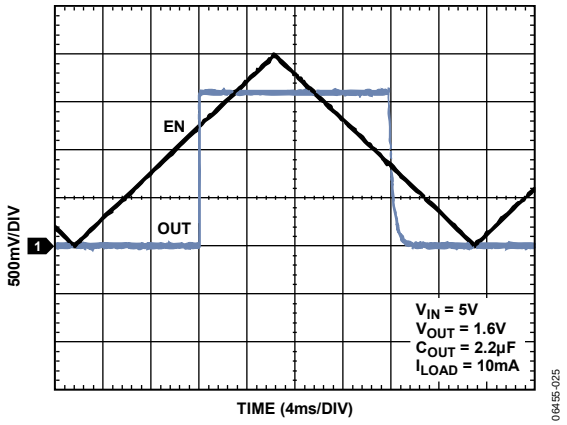

Figure 29. ADP1712 Adjustable Typical EN Pin Operation

As can be seen, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the IN voltage. Therefore, these thresholds vary with changing input voltage. Figure 30 shows typical EN active/inactive thresholds when the input voltage varies from 2.5 V to 5.5 V.

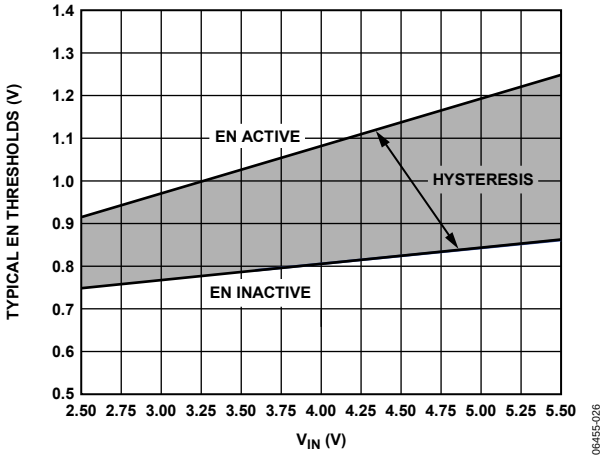

Figure 30. Typical EN Pin Thresholds vs. Input Voltage

UNDERVOLTAGE LOCKOUT (UVLO)

The ADP1712/ADP1713/ADP1714 have an undervoltage lockout circuit, which monitors the voltage on the IN pin. When the voltage on IN drops below 2 V (minimum), the circuit activates, disabling the OUT pin.

APPLICATION INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1712/ADP1713/ADP1714 are designed for operation with small, space-saving ceramic capacitors, but they function with most commonly used capacitors as long as care is taken about the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 2.2 µF capacitance with an ESR of 500 mΩ or less is recommended to ensure stability of the ADP1712/ADP1713/ADP1714. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1712/ADP1713/ADP1714 to large changes in load current. Figure 31 and Figure 32 show the transient responses for output capacitance values of 2.2 µF and 10 µF, respectively.

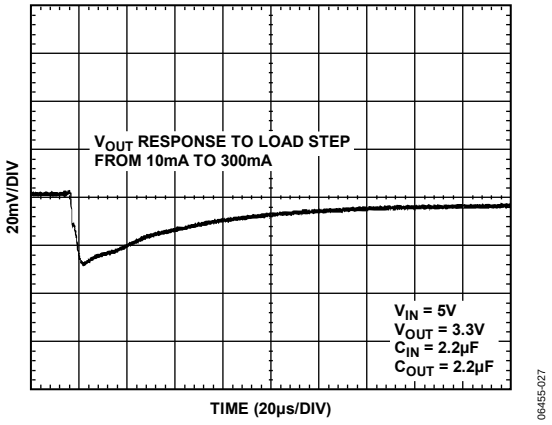

Figure 31. Output Transient Response, C_{OUT} = 2.2 µF

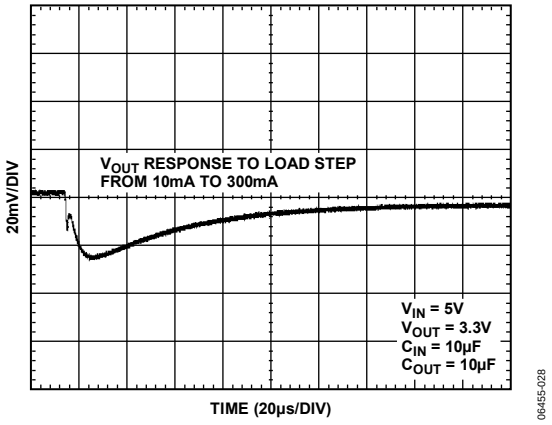

Figure 32. Output Transient Response, C_{OUT} = 10 µF

Input Bypass Capacitor

Connecting a 2.2 µF capacitor from the IN pin to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 2.2 µF of output capacitance is required, increasing the input capacitor to match is recommended.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP1712/ADP1713/ADP1714, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1712/ADP1713/ADP1714 are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP1712/ADP1713/ADP1714 are designed to current limit when the output load reaches 500 mA (typical). When the output load exceeds 500 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C (typical), the output is turned on again and output current is restored to its nominal value.

Consider the case where a hard short from OUT to ground occurs. At first the ADP1712/ADP1713/ADP1714 current limit, so that only 500 mA is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 500 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 500 mA and 0 mA, which continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation needs to be externally limited so junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP1712/ADP1713/ADP1714 must not exceed 125°C. To ensure the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds used and the amount of copper to which the GND pin of the package is soldered on the PCB. Table 5 shows typical θ_{JA} values of the 5-lead TSOT package for various PCB copper sizes.

Table 5.

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	170
50	152
100	146
300	134
500	131

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP1712/ADP1713/ADP1714 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (3)$$

where:

T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (4)$$

where:

I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input voltage and output voltage, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (5)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure the junction temperature does not rise above 125°C. The following figures show junction temperature calculations for different ambient temperatures, load currents, input-to-output voltage differentials, and areas of PCB copper.

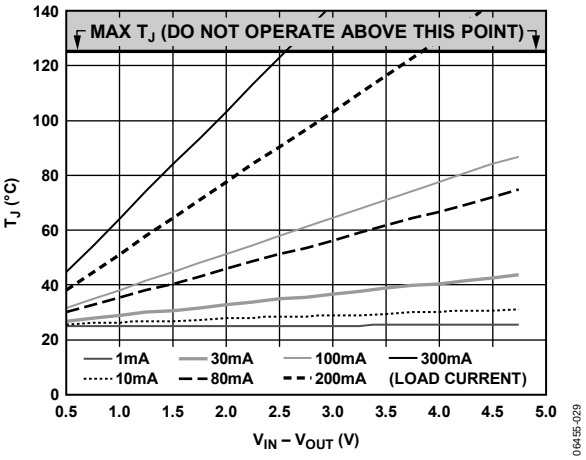

Figure 33. 500 mm² of PCB Copper, T_A = 25°C

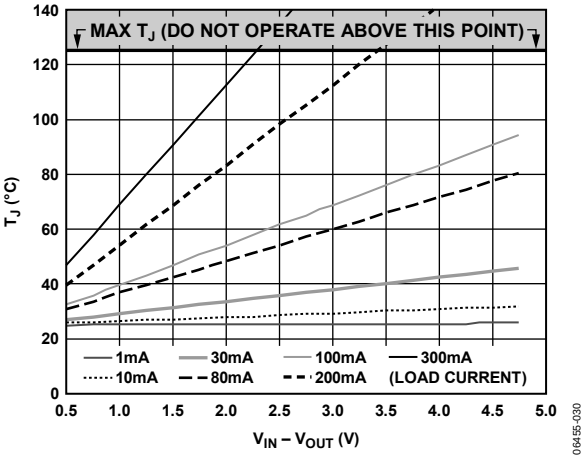

Figure 34. 100 mm² of PCB Copper, T_A = 25°C

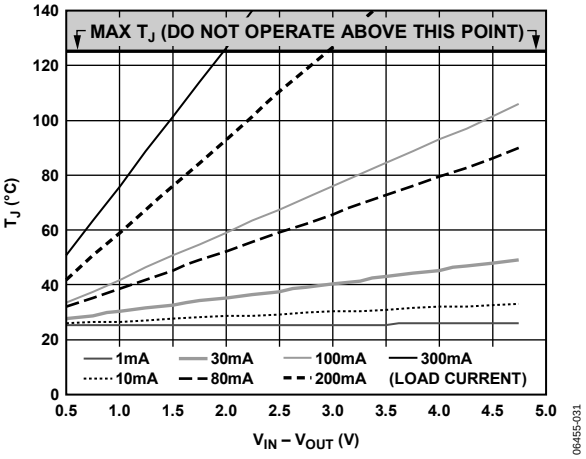

Figure 35. 0 mm² of PCB Copper, T_A = 25°C

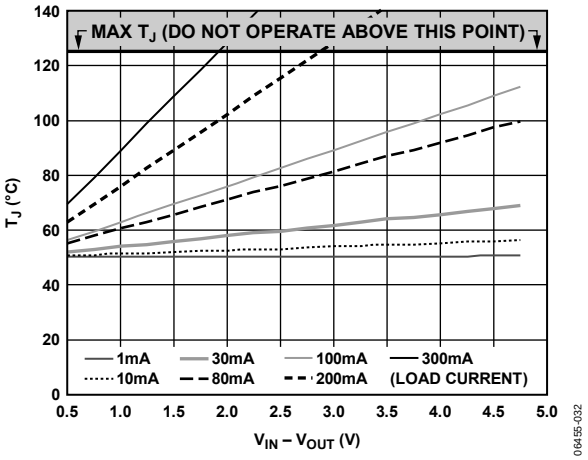

Figure 36. 500 mm² of PCB Copper, T_A = 50°C

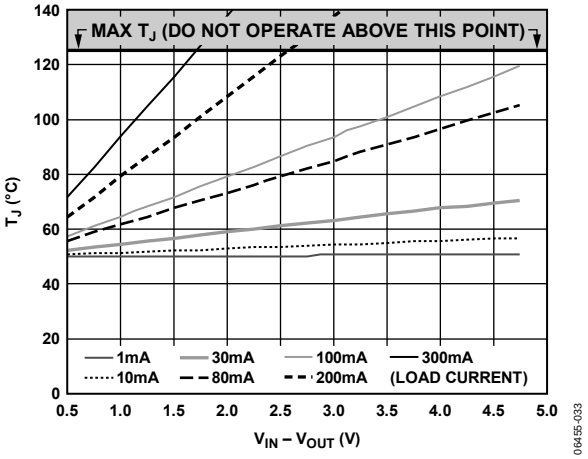

Figure 37. 100 mm² of PCB Copper, T_A = 50°C

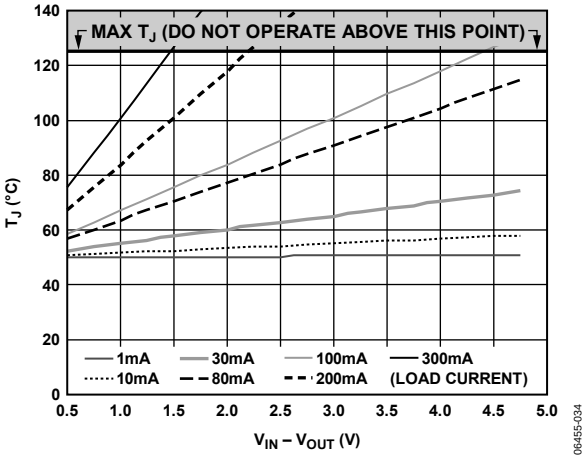

Figure 38. 0 mm² of PCB Copper, T_A = 50°C

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP1712/ADP1713/ADP1714. However, as can be seen from Table 5, a point of diminishing returns eventually is reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the IN and GND pins. Place the output capacitor as close as possible to the OUT and GND pins. For the ADP1712 adjustable version, place the soft-start capacitor as close as possible to the SS pin. For the ADP1713, place the internal reference bypass capacitor as close as possible to the BYP pin. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

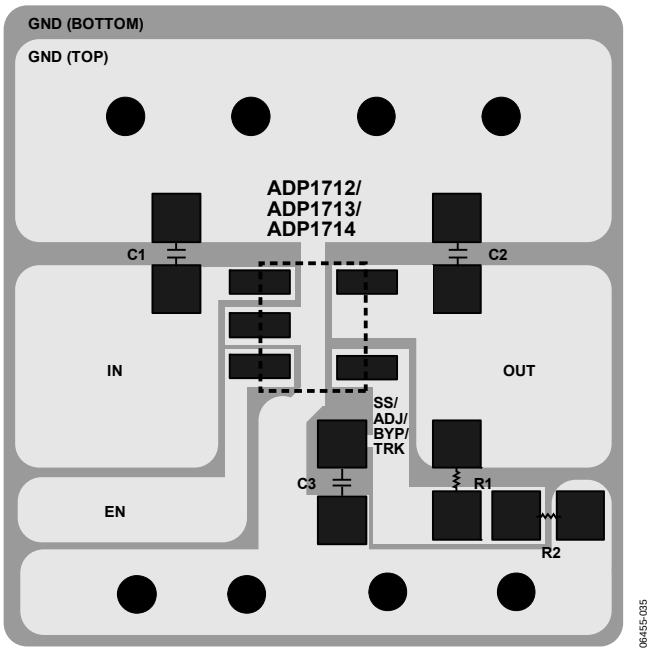

Figure 39. Example PCB Layout

OUTLINE DIMENSIONS

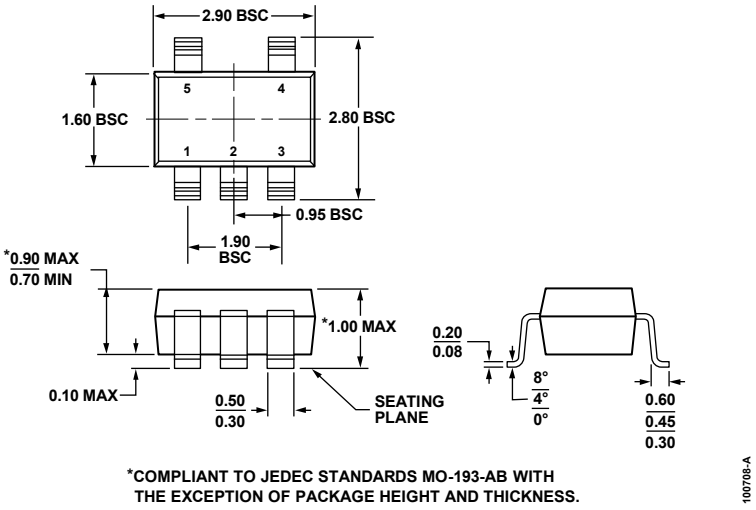

Figure 40. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP1712AUJZ-0.75R7[1]	–40°C to +125°C	0.75	5-Lead TSOT	UJ-5	L3S
ADP1712AUJZ-0.8-R7[1]	–40°C to +125°C	0.80	5-Lead TSOT	UJ-5	L3T
ADP1712AUJZ-0.85R7[1]	–40°C to +125°C	0.85	5-Lead TSOT	UJ-5	L3U
ADP1712AUJZ-0.9-R7[1]	–40°C to +125°C	0.90	5-Lead TSOT	UJ-5	L3V
ADP1712AUJZ-0.95R7[1]	–40°C to +125°C	0.95	5-Lead TSOT	UJ-5	L3W
ADP1712AUJZ-1.0-R7[1]	–40°C to +125°C	1.00	5-Lead TSOT	UJ-5	L3X
ADP1712AUJZ-1.05R7[1]	–40°C to +125°C	1.05	5-Lead TSOT	UJ-5	L3Y
ADP1712AUJZ-1.1-R7[1]	–40°C to +125°C	1.10	5-Lead TSOT	UJ-5	L3Z
ADP1712AUJZ-1.15R7[1]	–40°C to +125°C	1.15	5-Lead TSOT	UJ-5	L4H
ADP1712AUJZ-1.2-R7[1]	–40°C to +125°C	1.20	5-Lead TSOT	UJ-5	L4J
ADP1712AUJZ-1.3-R7[1]	–40°C to +125°C	1.30	5-Lead TSOT	UJ-5	L4K
ADP1712AUJZ-1.5-R7[1]	–40°C to +125°C	1.50	5-Lead TSOT	UJ-5	L4L
ADP1712AUJZ-1.8-R7[1]	–40°C to +125°C	1.80	5-Lead TSOT	UJ-5	L4M
ADP1712AUJZ-2.5-R7[1]	–40°C to +125°C	2.50	5-Lead TSOT	UJ-5	L4N
ADP1712AUJZ-3.0-R7[1]	–40°C to +125°C	3.00	5-Lead TSOT	UJ-5	L4P
ADP1712AUJZ-3.3-R7[1]	–40°C to +125°C	3.30	5-Lead TSOT	UJ-5	L4Q
ADP1712AUJZ-R7[1]	–40°C to +125°C	0.8 to 5	5-Lead TSOT	UJ-5	L4R
ADP1713AUJZ-0.75R7[1]	–40°C to +125°C	0.75	5-Lead TSOT	UJ-5	L4U
ADP1713AUJZ-0.8-R7[1]	–40°C to +125°C	0.80	5-Lead TSOT	UJ-5	L4V
ADP1713AUJZ-0.85R7[1]	–40°C to +125°C	0.85	5-Lead TSOT	UJ-5	L4W
ADP1713AUJZ-0.9-R7[1]	–40°C to +125°C	0.90	5-Lead TSOT	UJ-5	L4X
ADP1713AUJZ-0.95R7[1]	–40°C to +125°C	0.95	5-Lead TSOT	UJ-5	L4Y
ADP1713AUJZ-1.0-R7[1]	–40°C to +125°C	1.00	5-Lead TSOT	UJ-5	L4Z
ADP1713AUJZ-1.05R7[1]	–40°C to +125°C	1.05	5-Lead TSOT	UJ-5	L50
ADP1713AUJZ-1.1-R7[1]	–40°C to +125°C	1.10	5-Lead TSOT	UJ-5	L51
ADP1713AUJZ-1.15R7[1]	–40°C to +125°C	1.15	5-Lead TSOT	UJ-5	L52
ADP1713AUJZ-1.2-R7[1]	–40°C to +125°C	1.20	5-Lead TSOT	UJ-5	L53

Model	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP1713AUJZ-1.3-R7[1]	–40°C to +125°C	1.30	5-Lead TSOT	UJ-5	L54
ADP1713AUJZ-1.5-R7[1]	–40°C to +125°C	1.50	5-Lead TSOT	UJ-5	L55
ADP1713AUJZ-1.8-R7[1]	–40°C to +125°C	1.80	5-Lead TSOT	UJ-5	L56
ADP1713AUJZ-2.5-R7[1]	–40°C to +125°C	2.50	5-Lead TSOT	UJ-5	L57
ADP1713AUJZ-3.0-R7[1]	–40°C to +125°C	3.00	5-Lead TSOT	UJ-5	L58
ADP1713AUJZ-3.3-R7[1]	–40°C to +125°C	3.30	5-Lead TSOT	UJ-5	L59
ADP1714AUJZ-0.75R7[1]	–40°C to +125°C	0.75	5-Lead TSOT	UJ-5	L5A
ADP1714AUJZ-0.8-R7[1]	–40°C to +125°C	0.80	5-Lead TSOT	UJ-5	L5C
ADP1714AUJZ-0.85R7[1]	–40°C to +125°C	0.85	5-Lead TSOT	UJ-5	L5D
ADP1714AUJZ-0.9-R7[1]	–40°C to +125°C	0.90	5-Lead TSOT	UJ-5	L5E
ADP1714AUJZ-0.95R7[1]	–40°C to +125°C	0.95	5-Lead TSOT	UJ-5	L5F
ADP1714AUJZ-1.0-R7[1]	–40°C to +125°C	1.00	5-Lead TSOT	UJ-5	L5G
ADP1714AUJZ-1.05R7[1]	–40°C to +125°C	1.05	5-Lead TSOT	UJ-5	L5H
ADP1714AUJZ-1.1-R7[1]	–40°C to +125°C	1.10	5-Lead TSOT	UJ-5	L5J
ADP1714AUJZ-1.15R7[1]	–40°C to +125°C	1.15	5-Lead TSOT	UJ-5	L5K
ADP1714AUJZ-1.2-R7[1]	–40°C to +125°C	1.20	5-Lead TSOT	UJ-5	L5L
ADP1714AUJZ-1.3-R7[1]	–40°C to +125°C	1.30	5-Lead TSOT	UJ-5	L5M
ADP1714AUJZ-1.5-R7[1]	–40°C to +125°C	1.50	5-Lead TSOT	UJ-5	L5N
ADP1714AUJZ-1.8-R7[1]	–40°C to +125°C	1.80	5-Lead TSOT	UJ-5	L5P
ADP1714AUJZ-2.5-R7[1]	–40°C to +125°C	2.50	5-Lead TSOT	UJ-5	L5Q
ADP1714AUJZ-3.0-R7[1]	–40°C to +125°C	3.00	5-Lead TSOT	UJ-5	L5R
ADP1714AUJZ-3.3-R7[1]	–40°C to +125°C	3.30	5-Lead TSOT	UJ-5	L5S
ADP1712-3.3-EVALZ1[1]		3.3	ADP1712 Fixed 3.3 V Output with Soft Start Evaluation Board		
ADP1712-EVALZ1[1]		Adjustable, but set to 1.6	ADP1712 Adjustable Output Evaluation Board		
ADP1713-3.3-EVALZ1[1]		3.3	ADP1713 Fixed 3.3 V Output with Bypass Evaluation Board		
ADP1714-3.3-EVALZ1[1]		3.3	ADP1714 Fixed 3.3 V Output with Track Mode Evaluation Board		

[1] Z = RoHS Compliant Part.

D06455-0-6/09(A)