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REVISION HISTORY

4/06—Rev. C to Rev. D

Updated Outline Dimensions	15
Changes to Ordering Guide	16

11/04—Rev. B to Rev. C

Updated Format.....	Universal
Changes to Receiving Truth Table Inputs Data Section	11
Renamed General Information to Theory of Operation.....	12
Updated Outline Dimensions	15
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5/01—Rev. A to Rev. B

Changes to Absolute Maximum Ratings Section	3
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3/01—Rev. 0 to Rev. A

Changes to ESD Specification, Absolute Maximum Ratings.....	3
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6/97—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 10\%$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			5.0	V	$R = \infty$, see Figure 6
	2.0		5.0	V	$V_{CC} = 5\text{ V}$, $R = 50\ \Omega$ (RS-422), see Figure 6
	1.5		5.0	V	$R = 27\ \Omega$ (RS-485), see Figure 6
	1.5		5.0	V	$V_{TST} = -7\text{ V to }+12\text{ V}$, see Figure 7, $V_{CC} = 5\text{ V} \pm 5\%$
$\Delta V_{OD} $ for Complementary Output States			0.2	V	$R = 27\ \Omega$ or $50\ \Omega$, see Figure 6
Common-Mode Output Voltage, V_{OC}			3	V	$R = 27\ \Omega$ or $50\ \Omega$, see Figure 6
$\Delta V_{OC} $ for Complementary Output States			0.2	V	$R = 27\ \Omega$ or $50\ \Omega$
Output Short-Circuit Current ($V_{OUT} = \text{High}$)			250	mA	$-7\text{ V} \leq V_O \leq +12\text{ V}$
Output Short-Circuit Current ($V_{OUT} = \text{Low}$)			250	mA	$-7\text{ V} \leq V_O \leq +12\text{ V}$
CMOS Input Logic Threshold Low, V_{INL}		1.4	0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0	1.4		V	
Logic Input Current (DE, DI)			± 1.0	μA	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	-0.2		+0.2	V	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Voltage Hysteresis, ΔV_{TH}		70		mV	$V_{CM} = 0\text{ V}$
Input Resistance	12			k Ω	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Current (A, B)			1	mA	$V_{IN} = 12\text{ V}$
			-0.8	mA	$V_{IN} = -7\text{ V}$
Logic Enable Input Current (\overline{RE})			± 1	μA	
CMOS Output Voltage Low, V_{OL}			0.4	V	$I_{OUT} = +4.0\text{ mA}$
CMOS Output Voltage High, V_{OH}	4.0			V	$I_{OUT} = -4.0\text{ mA}$
Short-Circuit Output Current	7		85	mA	$V_{OUT} = \text{GND or } V_{CC}$
Three-State Output Leakage Current			± 1.0	μA	$0.4\text{ V} \leq V_{OUT} \leq +2.4\text{ V}$
POWER SUPPLY CURRENT					
I_{CC}		30	60	μA	Outputs unloaded, receivers enabled DE = 0 V (disabled)
		37	74	μA	DE = 5 V (enabled)

ADM488/ADM489

TIMING SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 10\%$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Propagation Delay Input to Output, T_{PLH} , T_{PHL}	250		2000	ns	R_L Differential = 54 Ω , $C_{L1} = C_{L2} = 100$ pF, see Figure 10
Driver O/P to \overline{OP} , T_{SKEW}		100	800	ns	R_L Differential = 54 Ω , $C_{L1} = C_{L2} = 100$ pF, see Figure 10
Driver Rise/Fall Time, T_R , T_F	250		2000	ns	R_L Differential = 54 Ω , $C_{L1} = C_{L2} = 100$ pF, see Figure 10
Driver Enable to Output Valid	250		2000	ns	$R_L = 500$ Ω , $C_L = 100$ pF, see Figure 7
Driver Disable Timing	300		3000	ns	$R_L = 500$ Ω , $C_L = 15$ pF, see Figure 7
Data Rate	250			kbps	
RECEIVER					
Propagation Delay Input to Output, T_{PLH} , T_{PHL}	250		2000	ns	$C_L = 15$ pF, see Figure 10
Skew $ T_{PLH} - T_{PHL} $		100		ns	
Receiver Enable, T_{EN1}		10	50	ns	$R_L = 1$ k Ω , $C_L = 15$ pF, see Figure 9
Receiver Disable, T_{EN2}		10	50	ns	$R_L = 1$ k Ω , $C_L = 15$ pF, see Figure 9
Data Rate	250			kbps	

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	7 V
Inputs	
Driver Input (DI)	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Control Inputs (DE, $\overline{\text{RE}}$)	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Receiver Inputs (A, B)	$-14\text{ V to }+14\text{ V}$
Outputs	
Driver Outputs	$-14\text{ V to }+12.5\text{ V}$
Receiver Output	$-0.5\text{ V to }V_{CC} + 0.5\text{ V}$
Power Dissipation 8-Lead PDIP	700 mW
θ_{JA} , Thermal Impedance	120°C/W
Power Dissipation 8-Lead SOIC	520 mW
θ_{JA} , Thermal Impedance	110°C/W
Power Dissipation 14-Lead PDIP	800 mW
θ_{JA} , Thermal Impedance	140°C/W
Power Dissipation 14-Lead SOIC	800 mW
θ_{JA} , Thermal Impedance	120°C/W
Power Dissipation 16-Lead TSSOP	800 mW
θ_{JA} , Thermal Impedance	150°C/W
Operating Temperature Range	
Industrial (A Version)	$-40^\circ\text{C to }+85^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Association S5.1 HBM Standard	3 kV
EFT Rating, IEC1000-4-4	2 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADM488/ADM489

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

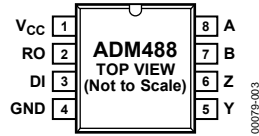


Figure 3. ADM488 8-Lead PDIP/SOIC Pin Configuration

Table 4. ADM488 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{CC}	Power Supply, 5 V ± 10%.
2	RO	Receiver Output. When A > B by 200 mV, RO = high. If A < B by 200 mV, RO = low.
3	DI	Driver Input. A logic low on DI forces Y low and Z high, while a logic high on DI forces Y high and Z low.
4	GND	Ground Connection, 0 V.
5	Y	Noninverting Driver, Output Y.
6	Z	Inverting Driver, Output Z.
7	B	Inverting Receiver, Input B.
8	A	Noninverting Receiver, Input A.

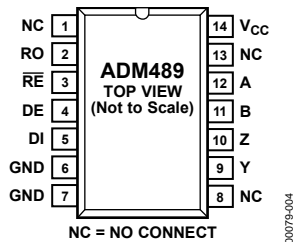


Figure 4. ADM489 14-Lead PDIP/SOIC Pin Configuration

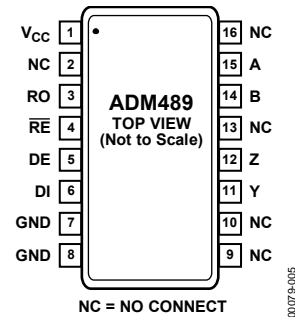


Figure 5. ADM489 16-Lead TSSOP Pin Configuration

Table 5. ADM489 Pin Function Descriptions

PDIP/SOIC Pin No.	TSSOP Pin No.	Mnemonic	Description
1, 8, 13	2, 9, 10, 13, 16	NC	No Connect. No connections are required to this pin.
2	3	RO	Receiver Output. When enabled, if A > B by 200 mV then RO = high. If A < B by 200 mV then RO = low.
3	4	\overline{RE}	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.
4	5	DE	Driver Output Enable. A high level enables the driver differential outputs, Y and Z. A low level places it in a high impedance state.
5	6	DI	Driver Input. When the driver is enabled, a logic low on DI forces Y low and Z high, while a logic high on DI forces Y high and Z low.
6, 7	7, 8	GND	Ground Connection, 0 V.
9	11	Y	Noninverting Driver, Output Y.
10	12	Z	Inverting Driver, Output Z.
11	14	B	Inverting Receiver, Input B.
12	15	A	Noninverting Receiver, Input A.
14	1	V _{CC}	Power Supply, 5 V ± 10%.

TEST CIRCUITS

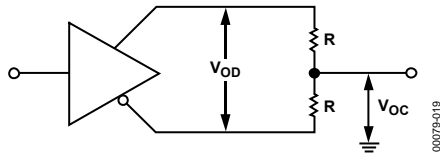


Figure 6. Driver Voltage Measurement Test Circuit

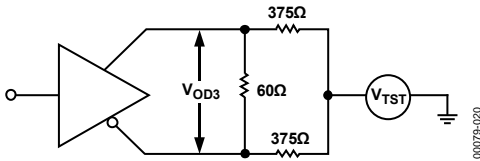


Figure 7. Driver Enable/Disable Test Circuit

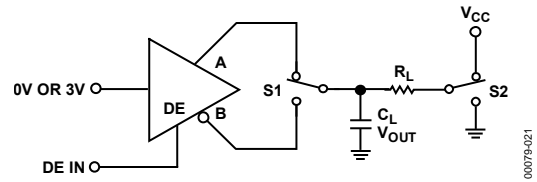


Figure 8. Driver Voltage Measurement Test Circuit 2

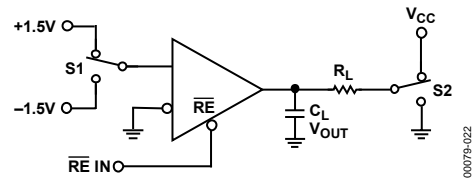


Figure 9. Receiver Enable/Disable Test Circuit

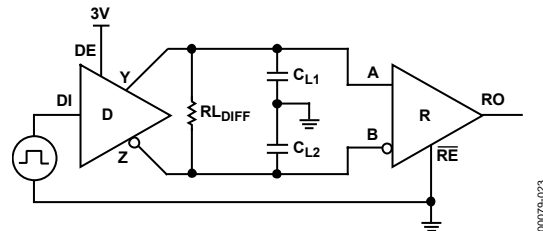


Figure 10. Driver/Receiver Propagation Delay Test Circuit

SWITCHING CHARACTERISTICS

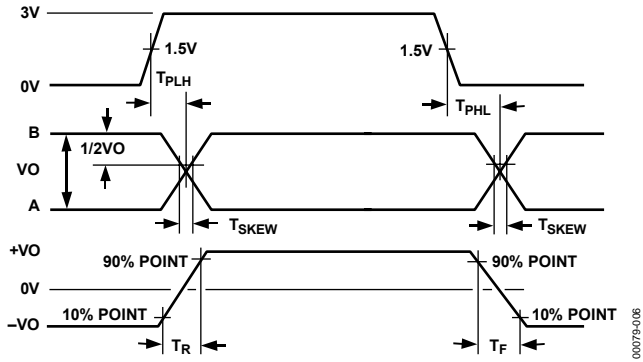


Figure 11. Driver Propagation Delay, Rise/Fall Timing

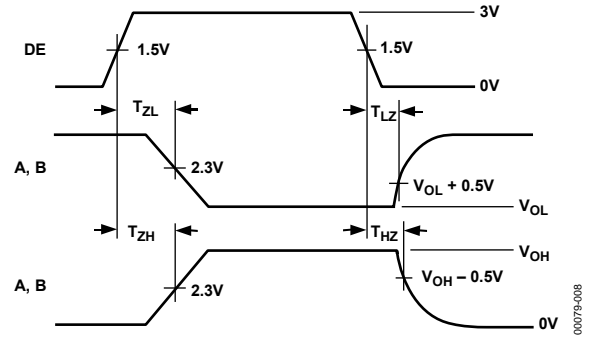


Figure 13. Driver Enable/Disable Timing

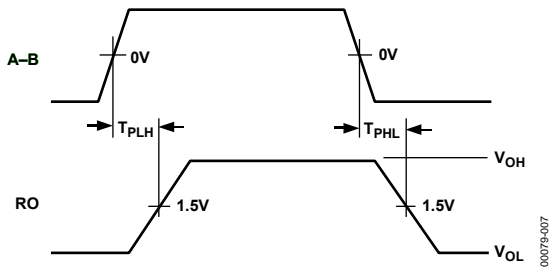


Figure 12. Receiver Propagation Delay

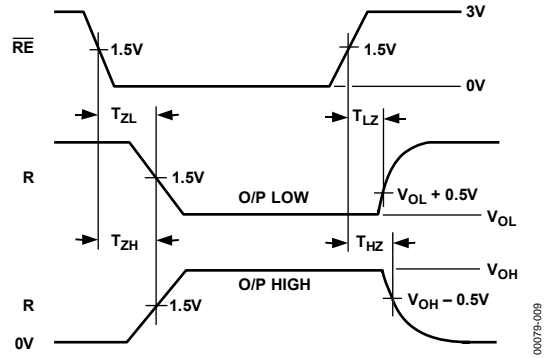


Figure 14. Receiver Enable/Disable Timing

TYPICAL PERFORMANCE CHARACTERISTICS

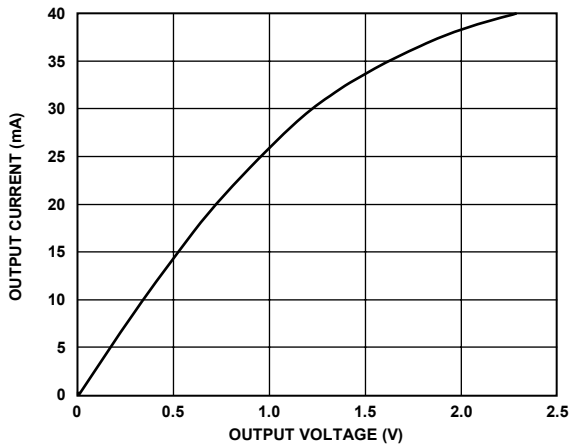


Figure 15. Output Current vs. Receiver Output Low Voltage

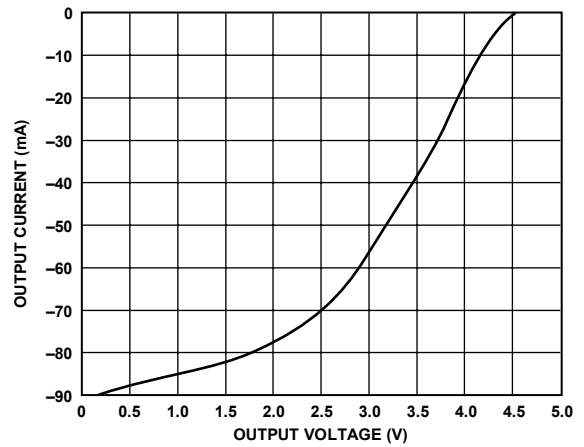


Figure 18. Output Current vs. Driver Output High Voltage

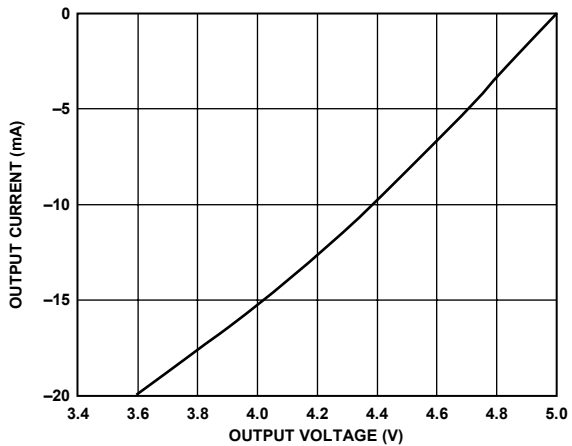


Figure 16. Output Current vs. Receiver Output High Voltage

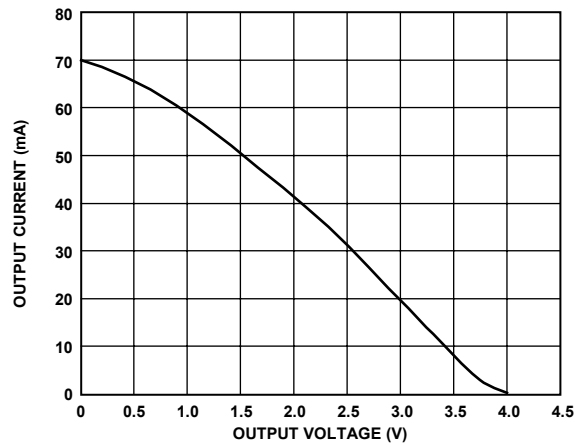


Figure 19. Output Current vs. Driver Differential Output Voltage

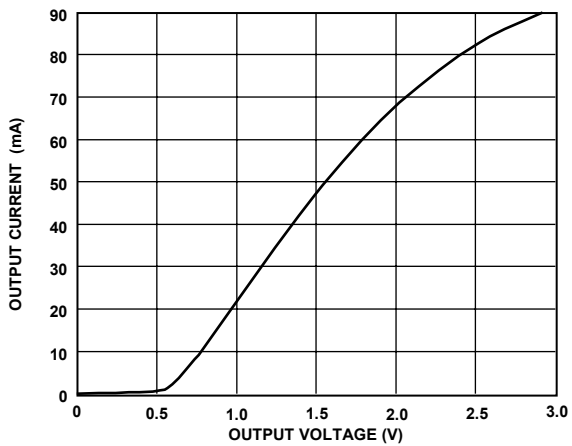


Figure 17. Output Current vs. Driver Output Low Voltage

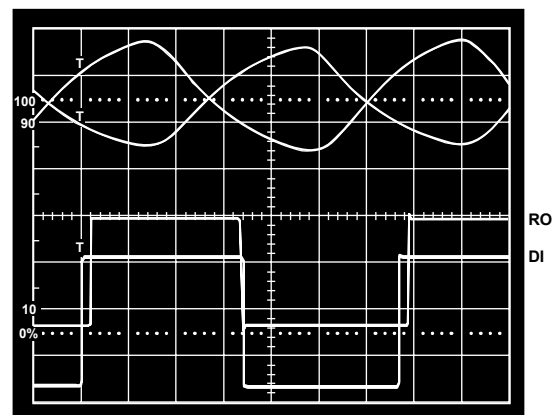


Figure 20. Driving 4000 Ft. of Cable

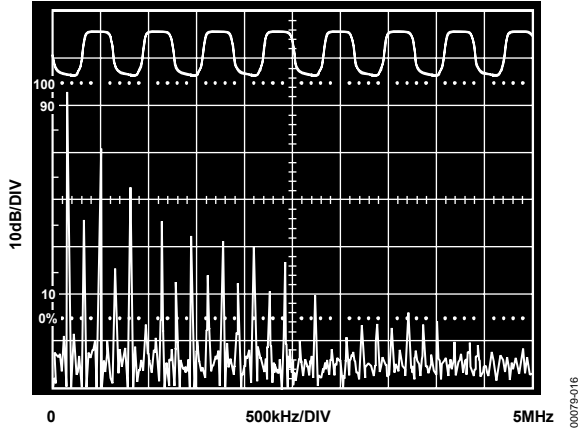


Figure 21. Driver Output Waveform and FFT Plot Transmitting at 150 kHz

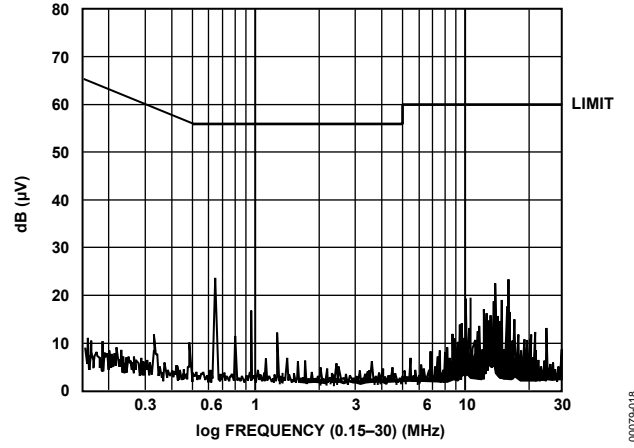


Figure 23. Conducted Emissions

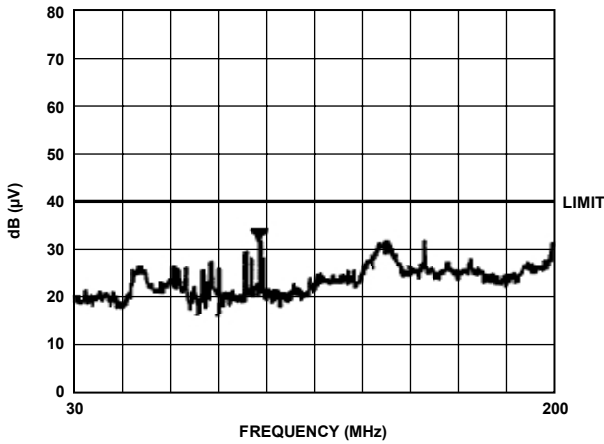


Figure 22. Radiated Emissions

ADM488/ADM489

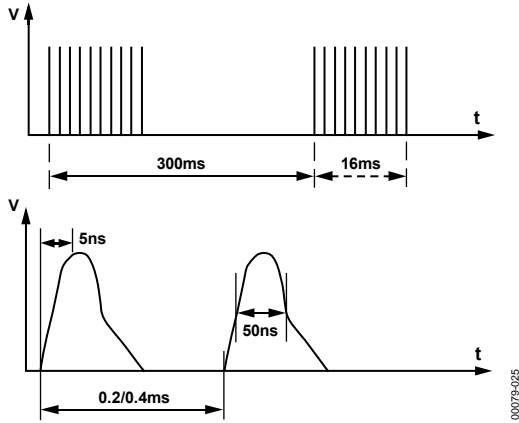


Figure 25. IEC1000-4-4 Fast Transient Waveform

Table 8 shows the peak voltages for each of the environments.

Table 8. Peak Voltages

Level	V _{PEAK} (kV) PSU	V _{PEAK} (kV) I/O
1	0.5	0.25
2	1	0.5
3	2	1
4	4	2

A simplified circuit diagram of the actual EFT generator is shown in Figure 26.

These transients are coupled onto the signal lines using an EFT coupling clamp. The clamp is 1 m long and completely surrounds the cable, providing maximum coupling capacitance (50 pF to 200 pF typical) between the clamp and the cable. High energy transients are capacitively coupled onto the signal lines. Fast rise times (5 ns), as specified by the standard, result in very effective coupling. This test is very severe because high voltages are coupled onto the signal lines. The repetitive transients often cause problems, while single pulses do not. Destructive latch-up can be induced due to the high energy content of the transients. Note that this stress is applied while the interface products are powered up and transmitting data. The EFT test applies hundreds of pulses with higher energy than ESD. Worst-case transient current on an I/O line can be as high as 40 A.

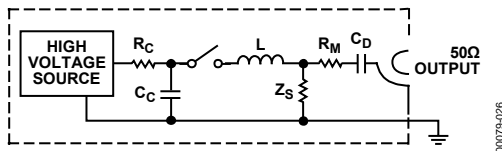


Figure 26. EFT Generator

Test results are classified according to the following:

- Normal performance within specification limits.
- Temporary degradation or loss of performance that is self-recoverable.
- Temporary degradation or loss of function or performance that requires operator intervention or system reset.
- Degradation or loss of function that is not recoverable due to damage.

The ADM488/ADM489 have been tested under worst-case conditions using unshielded cables, and meet Classification 2 at Severity Level 4. Data transmission during the transient condition is corrupted, but it can be resumed immediately following the EFT event without user intervention.

RADIATED IMMUNITY (IEC1000-4-3)

IEC1000-4-3 (previously IEC801-3) describes the measurement method and defines the levels of immunity to radiated electromagnetic fields. It was originally intended to simulate the electromagnetic fields generated by portable radio transceivers or any other device that generates continuous wave-radiated electromagnetic energy. Its scope has been broadened to include spurious EM energy, which can be radiated from fluorescent lights, thyristor drives, inductive loads, and so on.

Testing for immunity involves irradiating the device with an EM field. Test methods include the use of anechoic chamber, stripline cell, TEM cell, and GTEM cell. These consist of two parallel plates with an electric field developed between them. The device under test is placed between the plates and exposed to the electric field. The three severity levels have field strengths ranging from 1 V/m to 10 V/m. Results are classified as follows:

- Normal operation.
- Temporary degradation or loss of function that is self-recoverable when the interfering signal is removed.
- Temporary degradation or loss of function that requires operator intervention or system reset when the interfering signal is removed.
- Degradation or loss of function that is not recoverable due to damage.

The ADM488/ADM489 comfortably meet Classification 1 at the most stringent (Level 3) requirement. In fact, field strengths up to 30 V/m showed no performance degradation, and error-free data transmission continued even during irradiation.

Table 9. Field Strengths

Level V/m	Field Strength
1	1
2	3
3	10

EMI EMISSIONS

The ADM488/ADM489 contain internal slew rate limiting to minimize the level of electromagnetic interference generated. Figure 27 shows an FFT plot when transmitting a 150 kHz data stream.

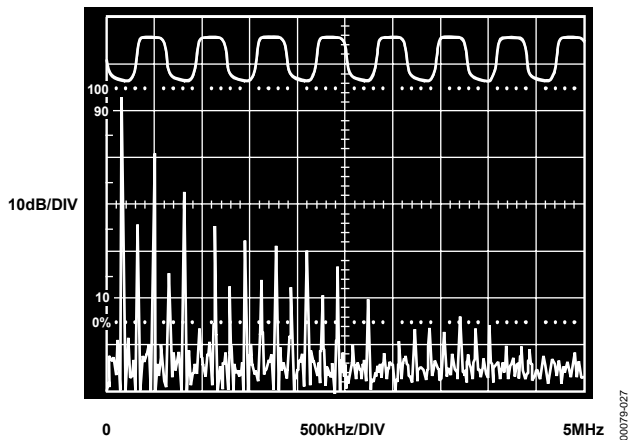


Figure 27. Driver Output Waveform and FFT Plot Transmitting at 150 kHz

The slew limiting attenuates the high frequency components. EMI is, therefore, reduced, as are reflections due to improperly terminated cables.

EN55022, CISPR22 defines the permitted limits of radiated and conducted interference from information technology equipment (ITE).

The objective is to control the level of both conducted and radiated emissions.

For ease of measurement and analysis, conducted emissions are assumed to predominate below 30 MHz, while radiated emissions predominate above this frequency.

CONDUCTED EMISSIONS

Conducted emissions are a measure of noise that is conducted onto the main power supply. The noise is measured using a LISN (line impedance stabilizing network) and a spectrum analyzer. The test setup is shown in Figure 28. The spectrum analyzer is set to scan the spectrum from 0 MHz to 30 MHz. Figure 29 shows that the level of conducted emissions from the ADM488/ADM489 is well below the maximum allowable limits.

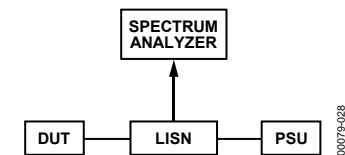


Figure 28. Conducted Emissions Test Setup

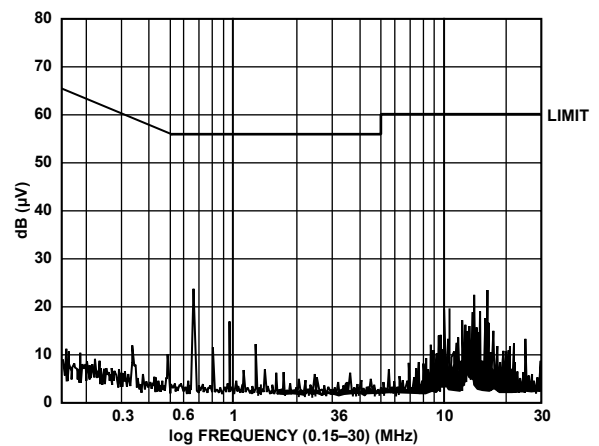


Figure 29. Conducted Emissions

APPLICATION INFORMATION

DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals, which appear as common-mode voltages on the line. Two main standards that specify the electrical characteristics of transceivers used in differential data transmission are approved by the EIA.

The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

To cater to true multipoint communications, the RS-485 standard was defined to meet or exceed the requirements of RS-422. It also allows up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of -7 V to $+12\text{ V}$ is defined. The most significant difference between the RS-422 and RS-485 is that the RS-485 drivers can be disabled, thereby allowing up to 32 receivers to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

CABLE AND DATA RATE

The transmission line of choice for RS-485 communications is a twisted pair. Twisted-pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM488/ADM489 are designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 30. An RS-485 transmission line can have up to 32 transceivers on the bus. Only one driver can transmit at a particular time, but multiple receivers can be simultaneously enabled.

As with any transmission line, it is important that reflections be minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

Table 10. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Data Rate	10 MB/s	10 MB/s
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	$\pm 2\text{ V}$	$\pm 1.5\text{ V}$
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 k Ω minimum	12 k Ω minimum
Receiver Input Sensitivity	$\pm 200\text{ mV}$	$\pm 200\text{ mV}$
Receiver Input Voltage Range	-7 V to $+7\text{ V}$	-7 V to $+12\text{ V}$
Number of Drivers/Receivers per Line	1/10	32/32

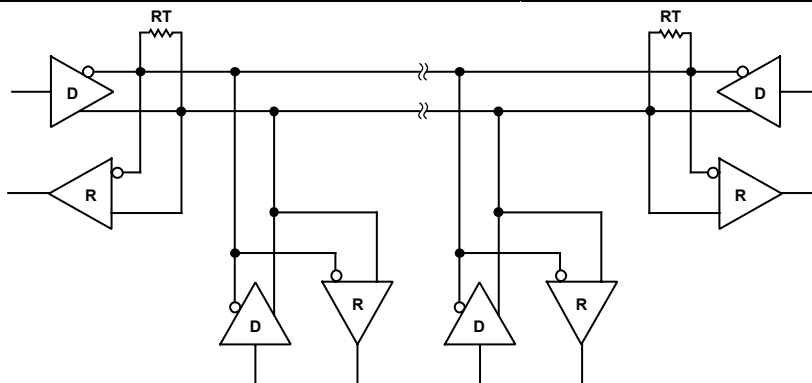
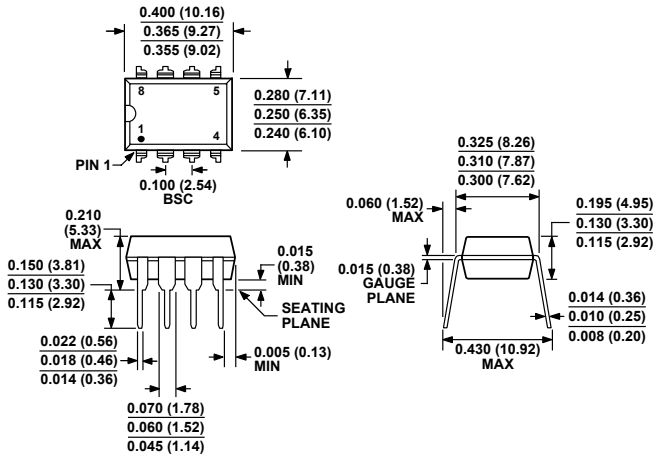


Figure 30. Typical RS-485 Network

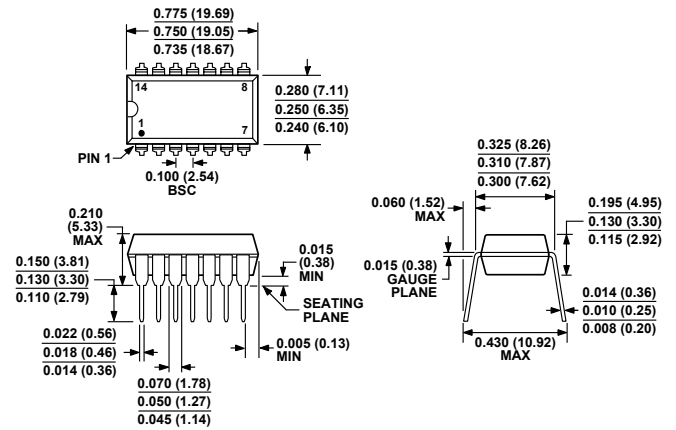
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OUTLINE DIMENSIONS



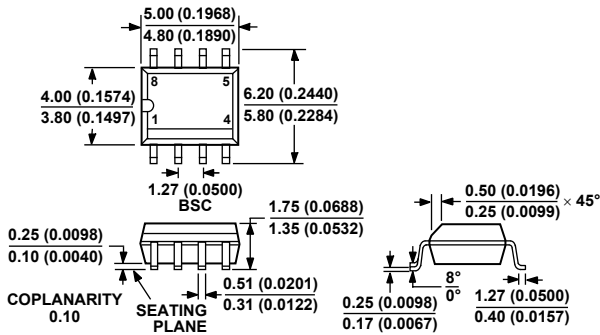
COMPLIANT TO JEDEC STANDARDS MS-001-BA
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Figure 31. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8)
 Dimensions shown in inches and (millimeters)



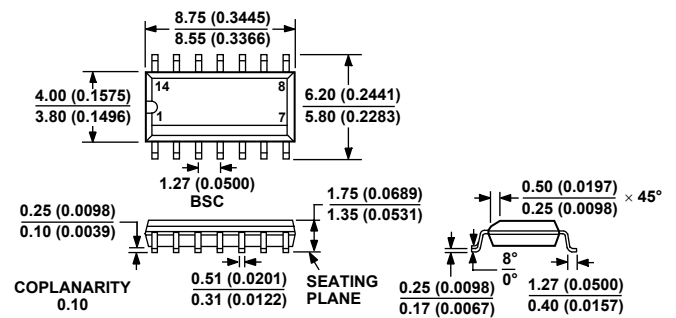
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Figure 33. 14-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-14)
 Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

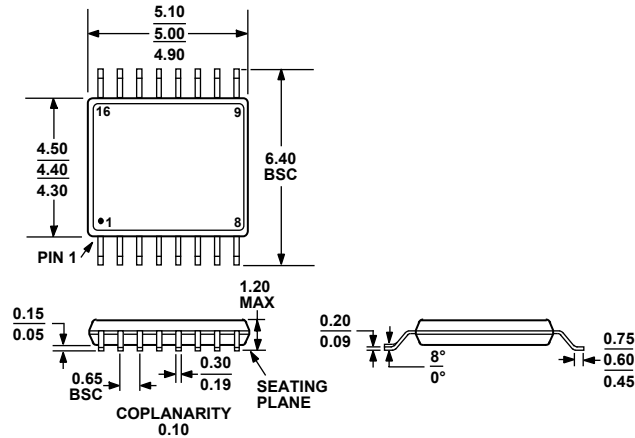
Figure 32. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)
 Dimensions show in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012-AB
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 34. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-14)
 Dimensions shown in millimeters and (inches)

ADM488/ADM489



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM488AN	-40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM488ANZ ¹	-40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM488AR	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488AR-REEL	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488AR-REEL7	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488ARZ ¹	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488ARZ-REEL ¹	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM488ARZ-REEL7 ¹	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM489AN	-40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
ADM489ANZ ¹	-40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
ADM489AR	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489AR-REEL	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489AR-REEL7	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489ARZ ¹	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489ARZ-REEL ¹	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489ARZ-REEL7 ¹	-40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM489ARU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARU-REEL	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARU-REEL7	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARUZ ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARUZ-REEL ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM489ARUZ-REEL7 ¹	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

¹ Z = Pb-free part.