All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in straight binary/offset binary or complementary binary/complementary offset binary by using the COMP BIN pin. An overflow pin indicates when inputs are below or above the normal full-scale range.

A novel feature of the ADC-530 is the provision of a Sample/Hold control pin for applications where a sample-hold is used in conjunction with the ADC-530. This feature allows the sample-and-hold device to go back into the sample mode a minimum of 30 nanoseconds before the conversion is complete, improving the overall conversion rate of the system.

ABSOLUTE MAXIMUM RATINGS

+15V Supply (Pin 13)	0 to +18V dc
-15V Supply (Pin 14)	0 to -18V dc
+5V Supply (Pin 11)	-0.5 to +7V dc
Digital Inputs (Pins 7, 9, 10, & 31)	-0.3 to +6V dc
Analog Input (Pin 3)	-15 to +15V dc
Lead temperature (10 Sec.)	300 °C max.

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V power supply voltages unless otherwise specified.

INPUTS	MIN.	TYP.	MAX.	UNIT
Input Voltage Range	–	0 to +10	–	V dc
(See Tech Note 9)	–	0 to +20	–	V dc
	–	±10	–	V dc
Logic Levels				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	2.5	µA
Logic 0	–	–	-100	µA
OUTPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	9.98	10.0	10.02	V dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Output Coding				
(Pin 7 High)	straight binary/offset binary			
(Pin 7 Low)	complementary binary complementary offset binary			
PERFORMANCE				
Integral Nonlinearity				
+25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1.5	LSB
Differential Nonlinearity				
+25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	±1/2	±1.5	LSB

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Full-Scale Abs. Accuracy				
+25 °C	–	±0.1	±0.25	%FSR
0 to +70 °C	–	±0.13	±0.32	%FSR
-55 to +125 °C	–	±0.2	±0.5	%FSR
Unipolar Zero Error				
+25 °C	–	±0.05	±0.13	%FSR
Unipolar Zero Tempco	–	±13	±25	ppm/ °C
Bipolar Zero Error				
+25 °C	–	±0.05	±0.13	%FSR
Bipolar Zero Tempco	–	±13	±25	ppm/ °C
Bipolar Offset Error				
+25 °C	–	±0.1	±0.2	%FSR
Bipolar Offset Error				
Tempco	–	±17.5	±35	ppm/ °C
Gain Error, +25 °C	–	±0.08	±0.17	%FSR
Gain Tempco	–	±17.5	±35	ppm/ °C
Conversion Times				
+25 °C	–	–	350	nSec.
0 to +70 °C	–	–	400	nSec.
-55 to +125 °C	–	–	400	nSec.
No Missing Codes (12 Bits)	Over the operating temp. range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	V dc
-15V dc Supply	-14.25	-15	-15.75	V dc
+5V dc Supply	+4.75	+5	+5.25	V dc
Power Supply Current				
+15V Supply	–	+60	+70	mA
-15V Supply	–	-30	-40	mA
+5V Supply *	–	+150	+180	mA
Power Dissipation	–	2.1	2.5	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range, Case				
-MC	0 to +70 °C			
-MM	-55 to +125 °C			
Storage Temp. Range	-65 to +150 °C			
Package Type	32-pin hermetic, ceramic DIP			
Weight	0.42 ounces (12 grams)			

*+5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, retun the analog and digital ground separately to the power supplies.

3. Bypass all the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 16).

4. Obtain straight binary/offset binary output coding by tieing COMP BIN (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 (ENABLE bits 1-5 & O.F.).

6. The sample-and-hold (S/H) control signal, pin 17, goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before EOC goes low. This indicates that the converter can accept a new analog input.

7. The drive requirements of the ADC-530 may be satisfied with a wide-bandwidth, low output impedance input source. Applications of these converters that require the use of a sample-and-hold may be satisfied by using DATEL's model SHM-45. Using this device with multiplexers or for test purposes will require an input buffer.

8. Over temperature, input capacitance is 50 pF maximum and input impedance is 1.75K minimum (2.5K typical) for 0 to +10V and 3.75K minimum (5K typical) for 0 to +20V, ±10V. These values are guaranteed by design.

9. Requirements for ±2.5V inputs can be satisfied using DATEL's AM-1435 amplifier in front of the SHM-45/ADC-530 configuration, shown in Figure 3, at the appropriate gain. The SHM-45's gain of 2 mode allows 0 to +5V or ±5V input ranges.

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

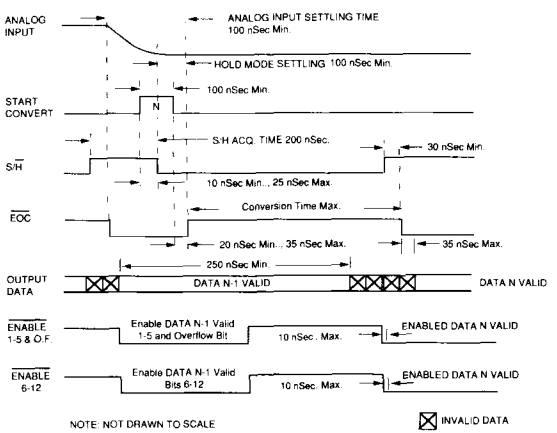


Figure 2. ADC-530 and SHM-45 Timing Diagram

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 100 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and ground (pin 16). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 7) tied high or between 1111 1111 1111 and 1111 1111 1110 with pin 7 tied low.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 7 tied high or between 0111 1111 1111 and 0111 1111 1110 with pin 7 tied low.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 7 tied high or between 0000 0000 0001 and 0000 0000 0000 for pin 7 tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

Table 2. Input Connections

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT PIN 2 (RANGE) TO PIN:
0 to +10V dc	3	3
0 to +20V dc	3	16
±10V dc	3	1

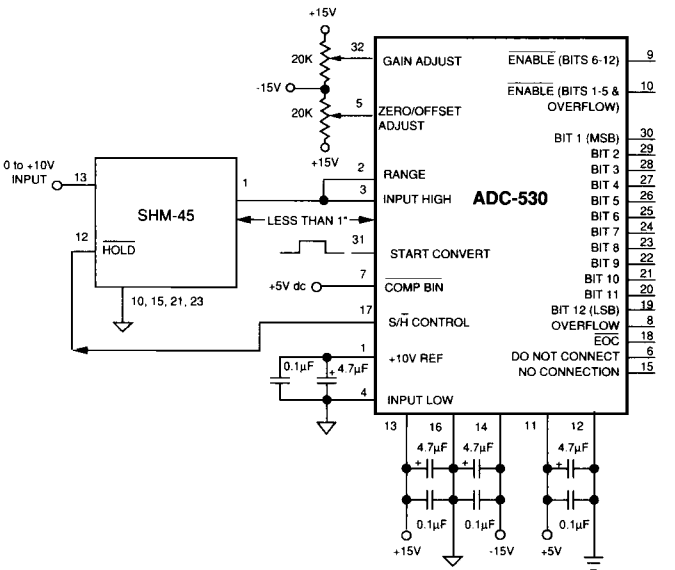
Table 3. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22 mV	+909963V dc
0 to +20V dc	+2.44 mV	+19.9927V dc
±10V dc	+2.44 mV	+9.9927V dc

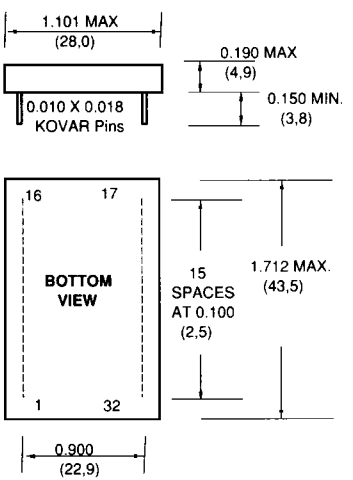
Table 4. Output Coding

			STRAIGHT BIN. COMP. BINARY			
UNIPOLAR	**INPUT RANGES, V dc**		**OUTPUT CODING**		**INPUT RANGE**	**BIPOLAR**
SCALE	**0 to +10V**	**0 to +20V**	**MSB LSB**	**MSB LSB**	**±10V dc**	**SCALE**
+FS -1 LSB	+9.9976V	+19.9951V	1111 1111 1111	0000 0000 0000	+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	17.500V	1110 0000 0000	0001 1111 1111	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	15.000V	1100 0000 0000	0011 1111 1111	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	+10.000V	1000 0000 0000	0111 1111 1111	0.0000V	0
1/4 FS	+2.5000V	+5.0000V	0100 0000 0000	1011 1111 1111	-5.0000V	-1/2 FS
1/8 FS	+1.2500V	+2.5000V	0010 0000 0000	1101 1111 1111	-7.5000V	-3/4 FS
1 LSB	+0.0024V	+0.0049V	0000 0000 0001	1111 1111 1110	-9.9951V	-FS +1 LSB
0	0.0000V	0.0000V	0000 0000 0000	1111 1111 1111	-10.000V	-FS
			OFF. BINARY COMP. OFF. BIN			

Figure 3. ADC-530 Calibration Setup



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
ADC-530 MC	0 to +70 °C	Hermetic
ADC-530 MM	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

For availability of MIL-STD-883B versions, contact DATEL.