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REVISION HISTORY

5/2016—Rev. C to Rev. D

Changed CP-8-2 to CP-8-13	Throughout
Changes to Figure 2	1
Changes to Table 4	5
Updated Outline Dimensions	13
Changes to Ordering Guide	15

4/2013—Rev. B to Rev. C

Changes to Figure 2	1
Added Exposed Pad Notation to Outline Dimensions	14
Changes to Ordering Guide	15

1/2008—Rev. A to Rev. B

Added TSSOP	Universal
Change to Table 4	5
Changes to Figure 8 and Figure 9	6
Changes to Figure 23 and Figure 26	9
Updated Outline Dimensions	13
Changes to Ordering Guide	15

Absolute Maximum Ratings	5
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10/2007—Rev. 0 to Rev. A

Added AD8667 and AD8669	Universal
Changes to Features	1
Changes to General Description	1
Inserted Figure 3 and Figure 4	1
Changes to Table 1, Power Supply Section	3
Changes to Table 2	4
Reformatted Typical Performance Characteristics Section	6
Changes to Figure 5	6
Changes to Figure 13	7
Changes to Figure 17 and Figure 20	8
Inserted Figure 35 through Figure 39	11
Inserted Figure 40 and Figure 41	12
Updated Outline Dimensions	13
Changes to Ordering Guide	15

7/2007—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_{SY} = 5.0\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		30	175	μV
Input Bias Current	I_B			0.3	450	μV
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			45	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			105	pA
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.2		pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			35	pA
Input Voltage Range			0.2		65	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0.2\text{ V to } 3.0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	76	100	3.0	V
Large Signal Voltage Gain	A_{VO}	$R_L = 100\text{ k}\Omega$, $V_{OUT} = 0.5\text{ V to } 4.5\text{ V}$	76	100		dB
		$R_L = 2\text{ k}\Omega$, $V_{OUT} = 0.5\text{ V to } 4.5\text{ V}$	115	140		dB
Offset Voltage Drift	TCV_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	106	114		dB
				1.5	5	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 100\text{ }\mu\text{A}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.95	4.97		V
			4.90			V
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.65	4.80		V
			4.60			V
Output Voltage Low	V_{OL}	$I_L = 100\text{ }\mu\text{A}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		17	25	mV
					35	mV
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		150	200	mV
					250	mV
Short-Circuit Current	I_{SC}			± 7		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 100\text{ kHz}$, $A_V = 1$		120		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 5\text{ V to } 16\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	105		dB
			95			dB
Supply Current per Amplifier	I_{SY}	$V_{OUT} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		210	275	μA
					325	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		0.26		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP	$C_L = 20\text{ pF}$		520		kHz
Phase Margin	Φ_M	$C_L = 20\text{ pF}$		60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		23		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$

$V_{SY} = 16.0\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		40	300	μV
Input Bias Current	I_B			0.3	500	μV
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			45	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			120	pA
Input Offset Current	I_{OS}			0.2		pA
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			35	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			65	pA
Input Voltage Range			0.2		14.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0.2\text{ V to }14.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	87	109		dB
			87	109		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 100\text{ k}\Omega$, $V_{OUT} = 0.5\text{ V to }15.5\text{ V}$	115	140		dB
		$R_L = 2\text{ k}\Omega$, $V_{OUT} = 0.5\text{ V to }15.5\text{ V}$	106	111		dB
Offset Voltage Drift	TCV_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	5	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 100\text{ }\mu\text{A}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	15.95	15.98		V
			15.90			V
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	15.85	15.92		V
			15.80			V
Output Voltage Low	V_{OL}	$I_L = 100\text{ }\mu\text{A}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		17	25	mV
					35	mV
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		70	100	mV
					125	mV
Short-Circuit Current	I_{SC}			± 50		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 100\text{ kHz}$, $A_V = 1$		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 5\text{ V to }16\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	105		dB
			95			dB
Supply Current per Amplifier	I_{SY}	$V_{OUT} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		230	285	μA
					355	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		0.3		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP	$C_L = 20\text{ pF}$		540		kHz
Phase Margin	Φ_M	$C_L = 20\text{ pF}$		64		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		2.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		23		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	−0.1 V to V_{SY}
Differential Input Voltage	18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R-8)	121	43	°C/W
8-Lead LFCSP (CP-8-13)	75 ¹	18 ¹	°C/W
8-Lead MSOP (RM-8)	145	45	°C/W
14-Lead SOIC (R-14)	90	45	°C/W
14-Lead TSSOP (RU-14)	180	35	°C/W

¹ Exposed pad soldered to application board.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

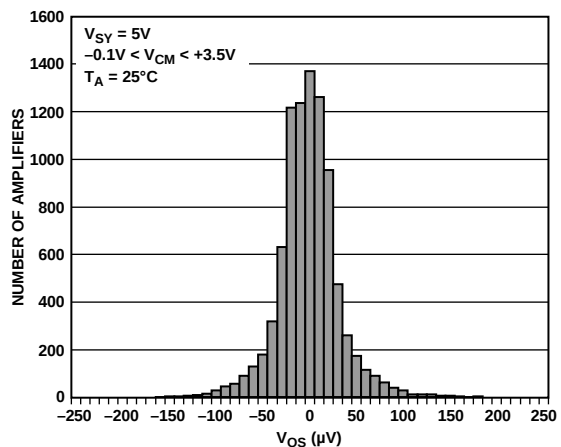


Figure 5. Input Offset Voltage Distribution

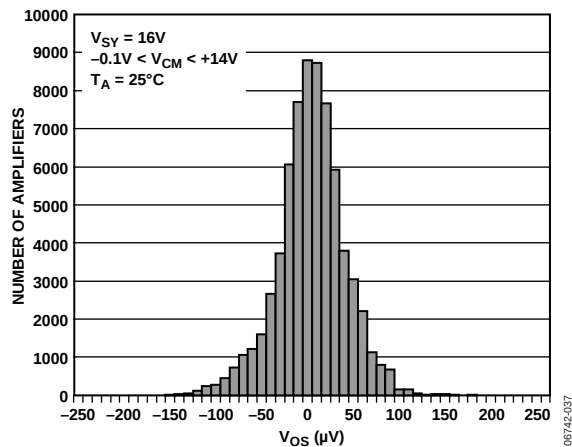


Figure 8. Input Offset Voltage Distribution

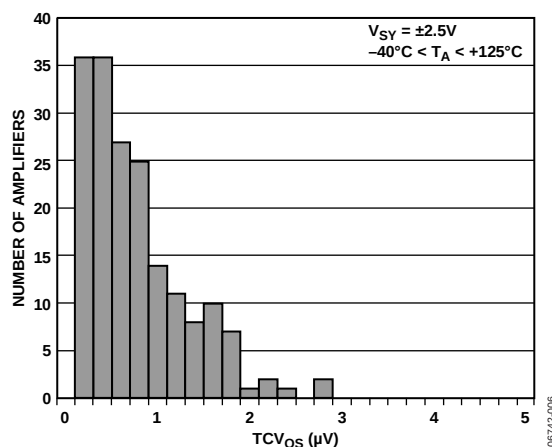


Figure 6. Offset Voltage Drift Distribution

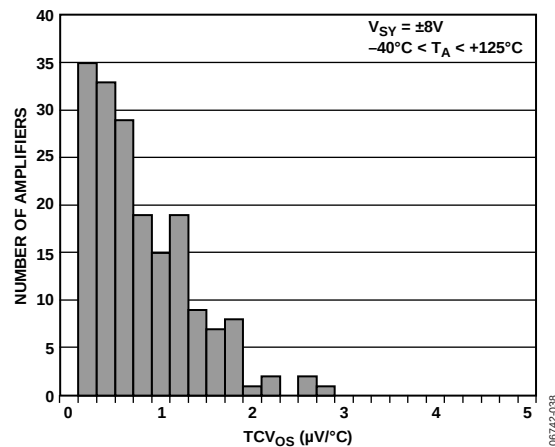


Figure 9. Offset Voltage Drift Distribution

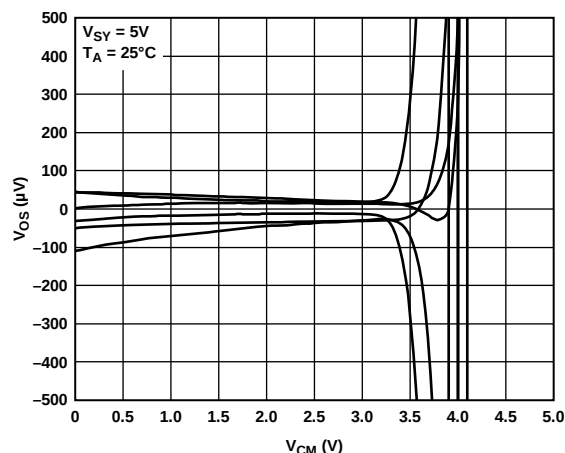


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

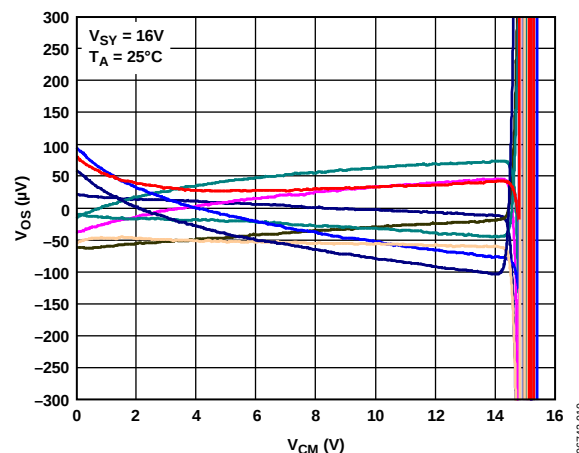


Figure 10. Input Offset Voltage vs. Common-Mode Voltage

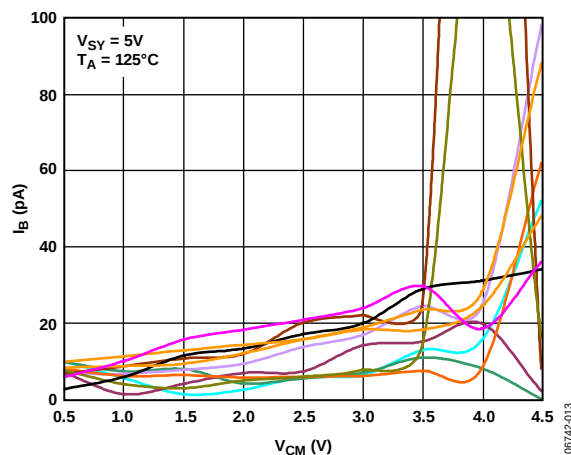


Figure 11. Input Bias Current vs. Common-Mode Voltage at 125°C

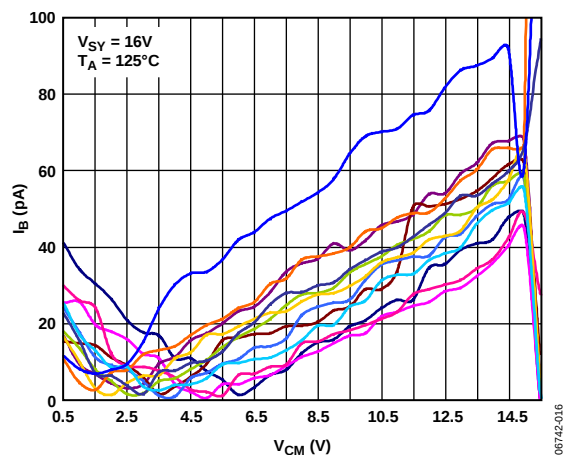


Figure 14. Input Bias Current vs. Common-Mode Voltage at 125°C

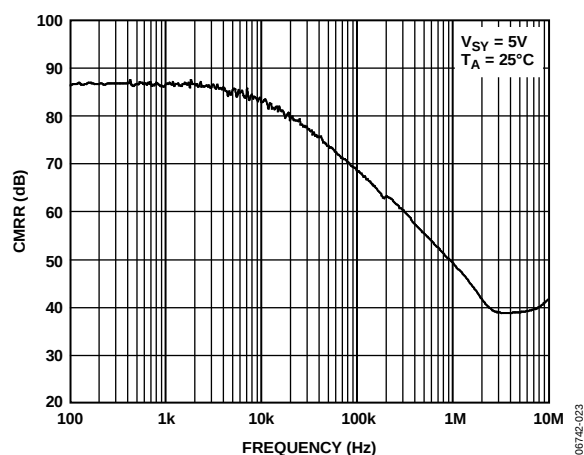
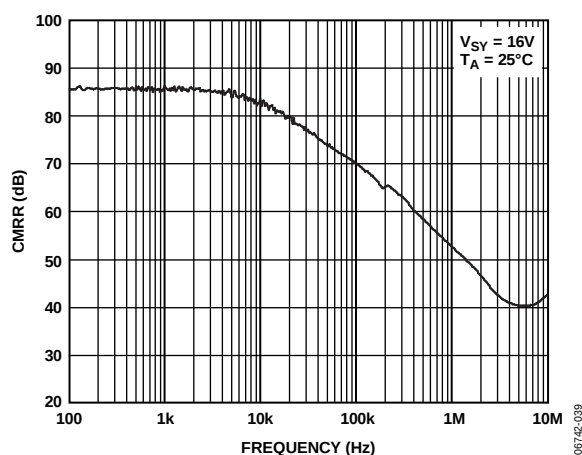
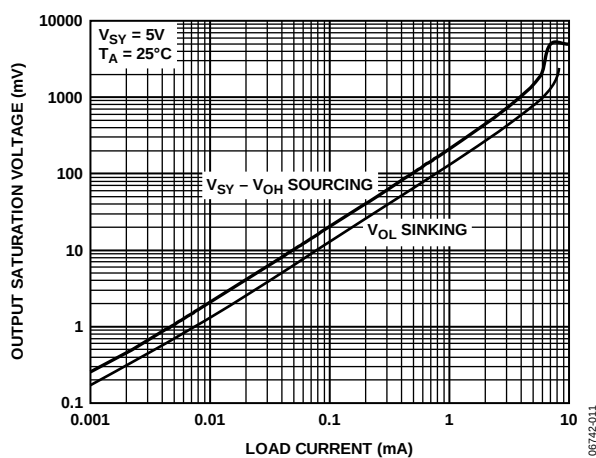
Figure 12. CMRR vs. Frequency, $V_{SY} = 5\text{ V}$ Figure 15. CMRR vs. Frequency, $V_{SY} = 16\text{ V}$ 

Figure 13. Output Swing Saturation Voltage vs. Load Current

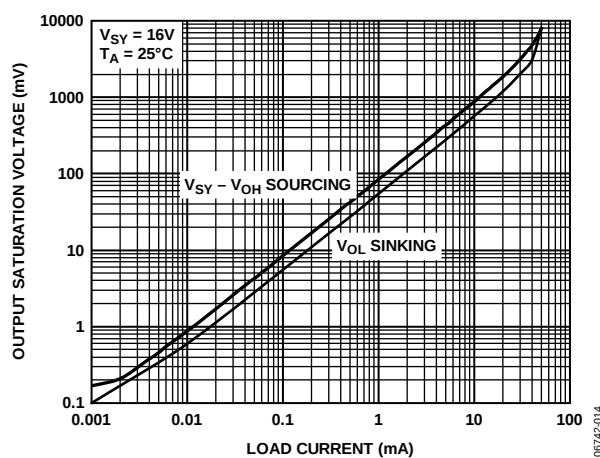


Figure 16. Output Swing Saturation Voltage vs. Load Current

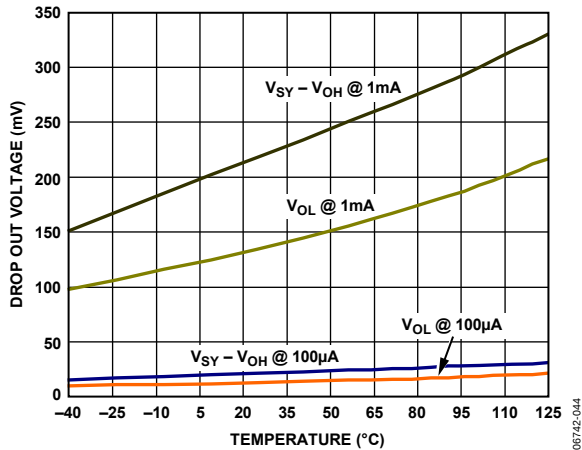


Figure 17. Output Voltage Saturation vs. Temperature

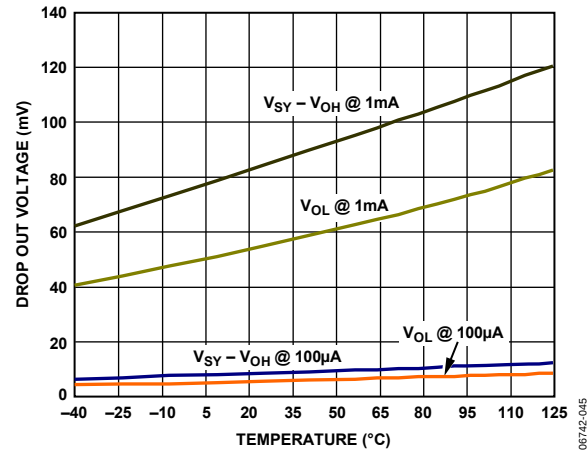


Figure 20. Output Voltage Saturation vs. Temperature

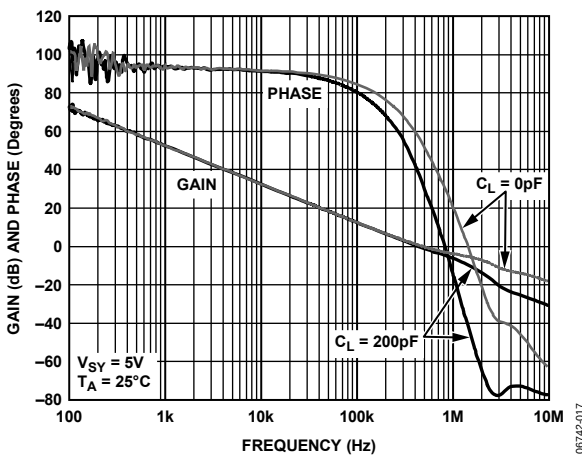


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

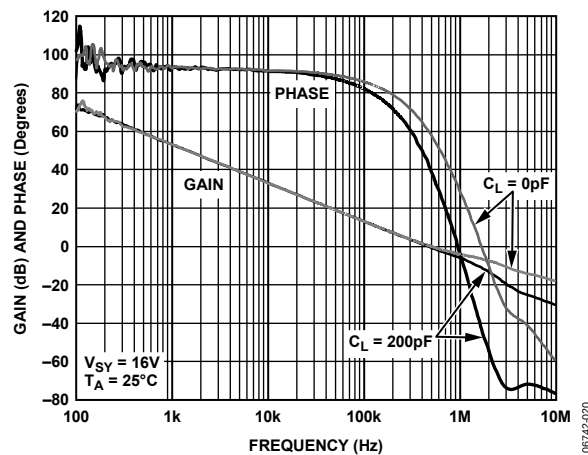


Figure 21. Open-Loop Gain and Phase Shift vs. Frequency

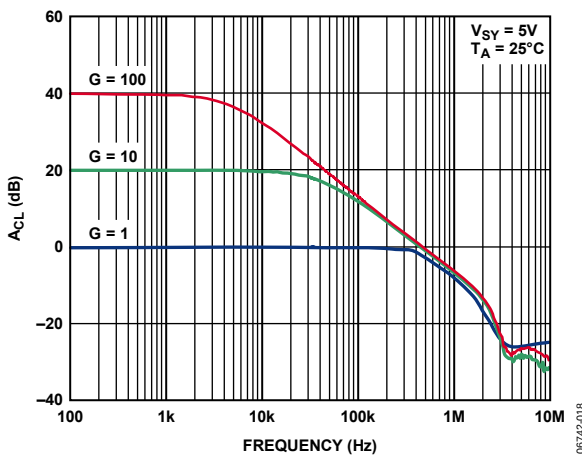
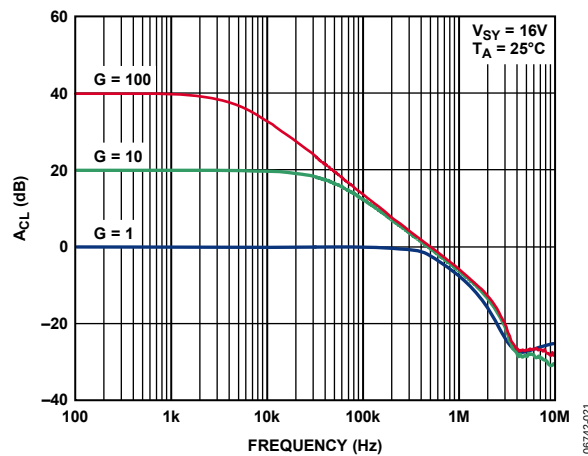
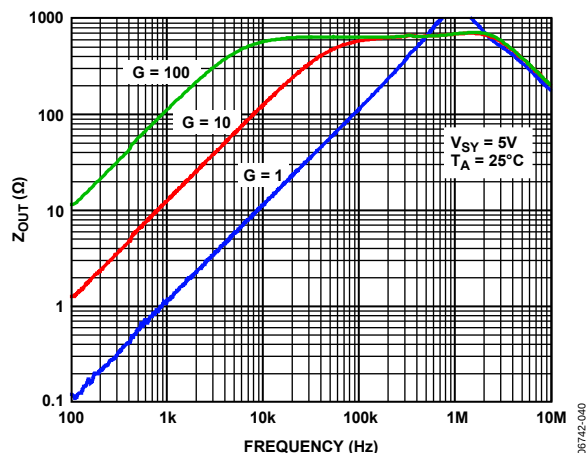
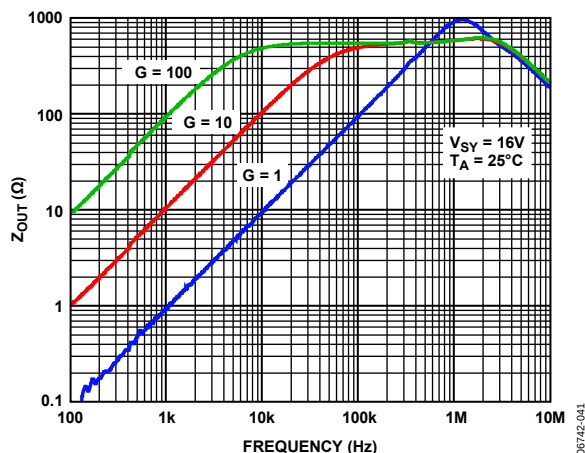
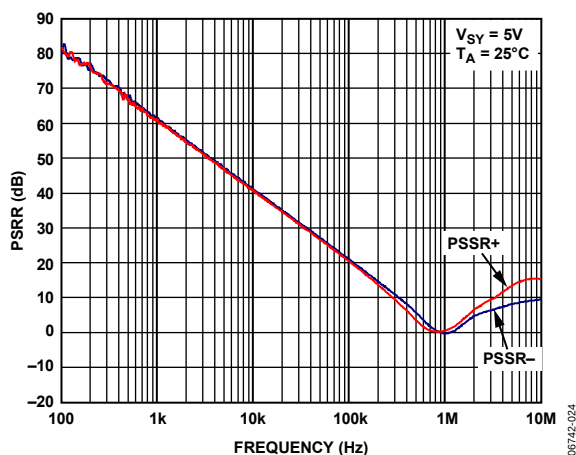
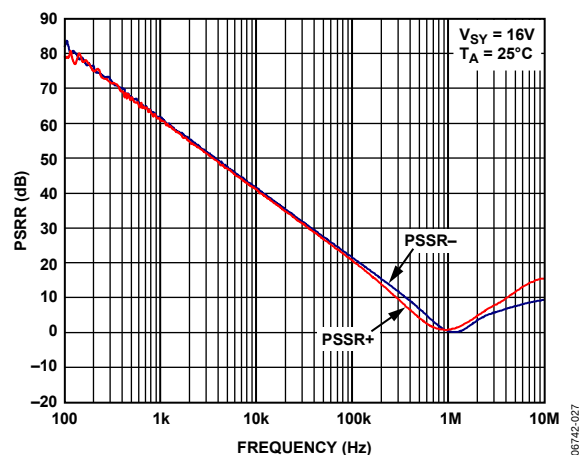
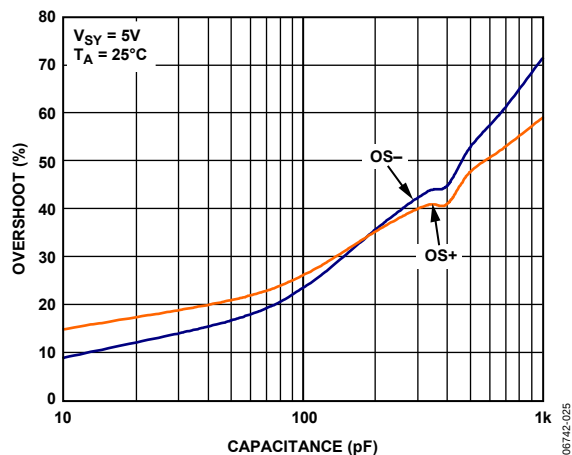
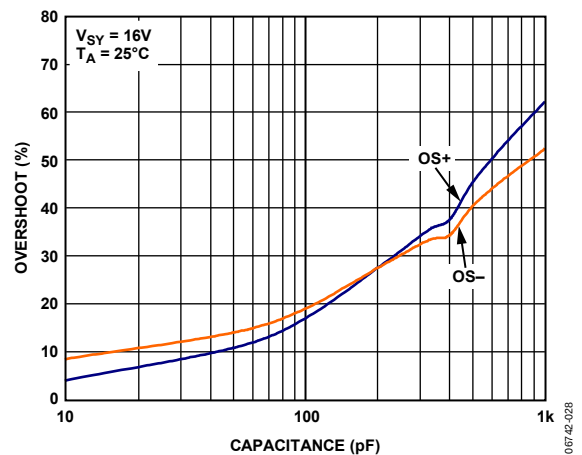


Figure 19. Closed-Loop Gain vs. Frequency

Figure 22. Closed-Loop Gain vs. Frequency, $V_{SY} = 16V$

Figure 23. Closed-Loop Output Impedance vs. Frequency, $V_{SV} = 5\text{ V}$ Figure 26. Closed-Loop Output Impedance vs. Frequency, $V_{SV} = 16\text{ V}$ Figure 24. PSRR vs. Frequency, $V_{SV} = 5\text{ V}$ Figure 27. PSRR vs. Frequency, $V_{SV} = 16\text{ V}$ Figure 25. Small-Signal Overshoot vs. Load Capacitance, $V_{SV} = 5\text{ V}$ Figure 28. Small-Signal Overshoot vs. Load Capacitance, $V_{SV} = 16\text{ V}$

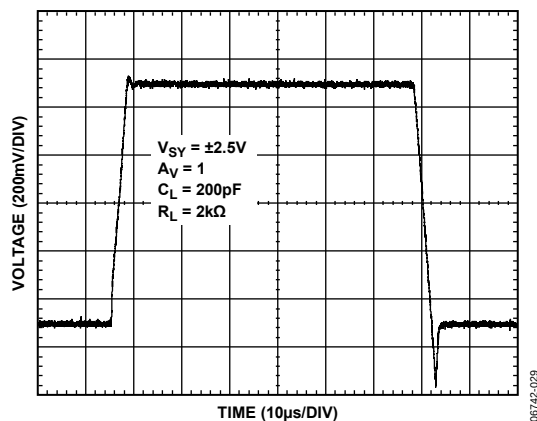
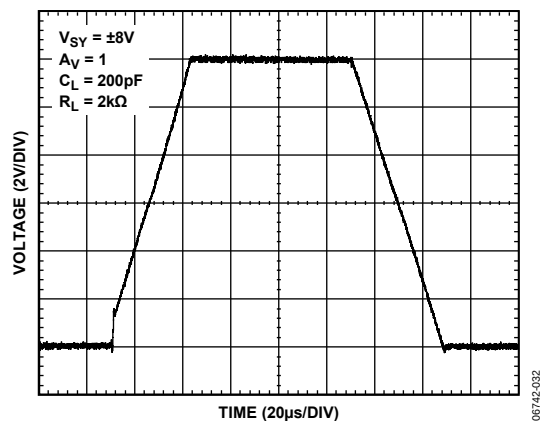
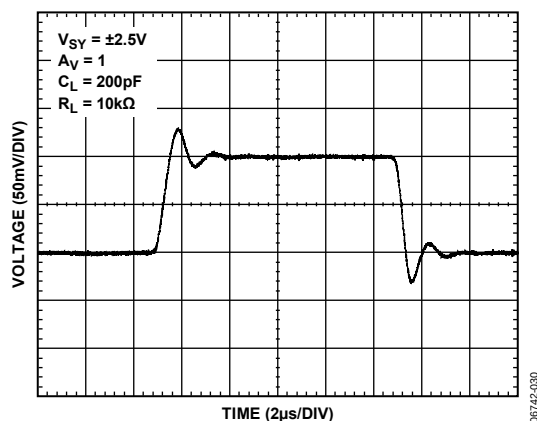
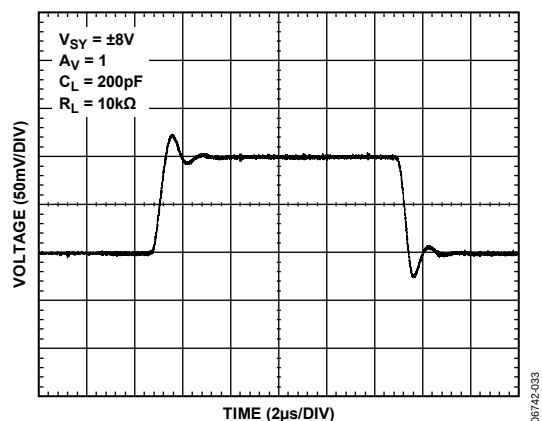
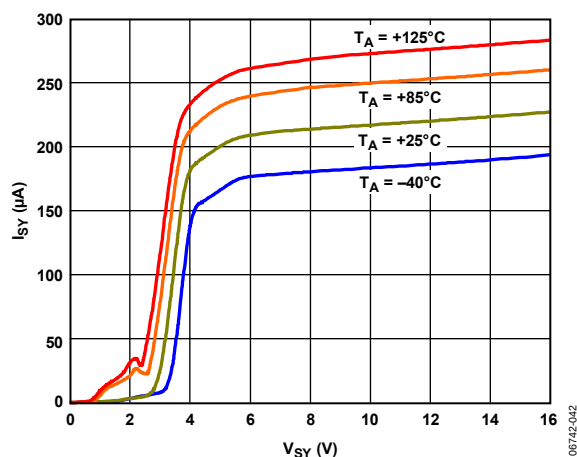
Figure 29. Large Signal Transient Response, $V_{SV} = \pm 2.5\text{ V}$ Figure 32. Large Signal Transient Response, $V_{SV} = \pm 8\text{ V}$ Figure 30. Small Signal Transient Response, $V_{SV} = \pm 2.5\text{ V}$ Figure 33. Small Signal Transient Response, $V_{SV} = \pm 8\text{ V}$ 

Figure 31. AD8663, Supply Current vs. Supply Voltage

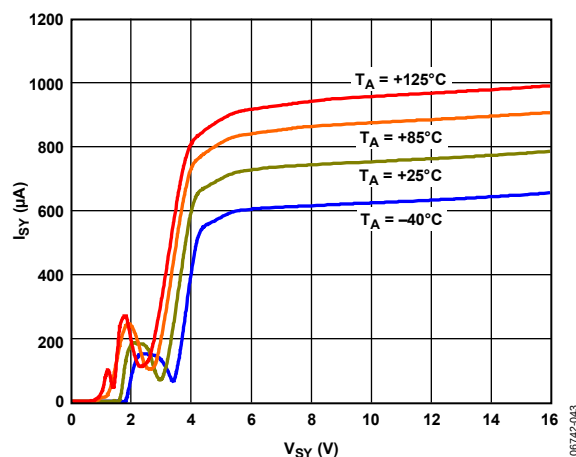


Figure 34. AD8669, Supply Current vs. Supply Voltage

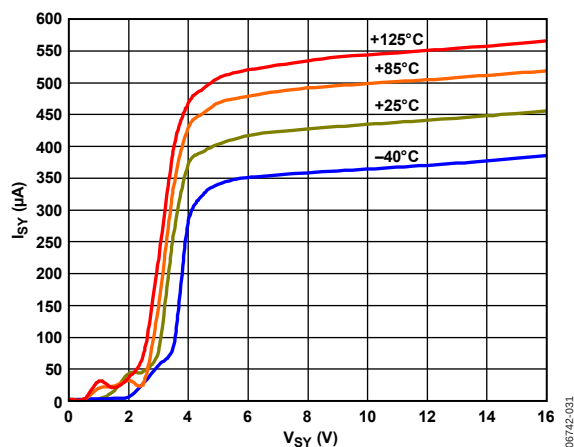


Figure 35. AD8667, Supply Current vs. Supply Voltage

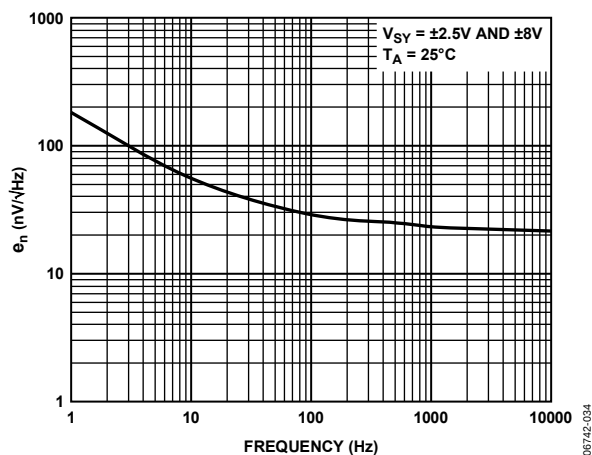


Figure 38. Voltage Noise Density

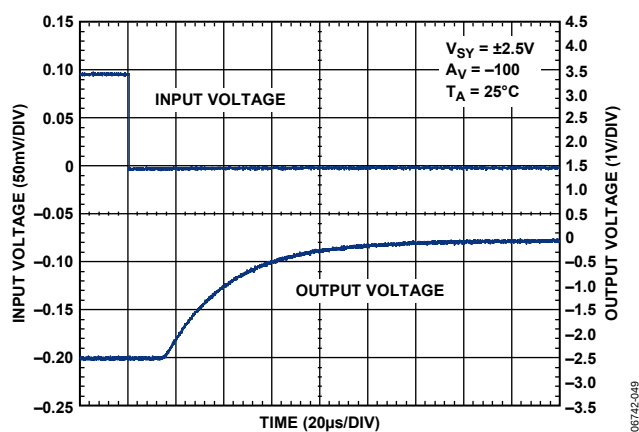


Figure 36. Positive Overload Recovery

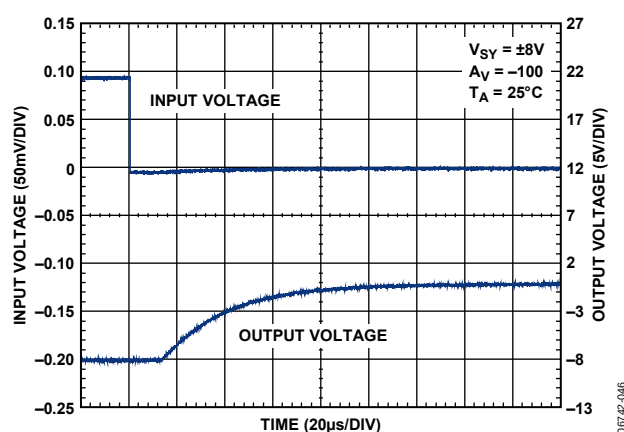


Figure 39. Positive Overload Recovery

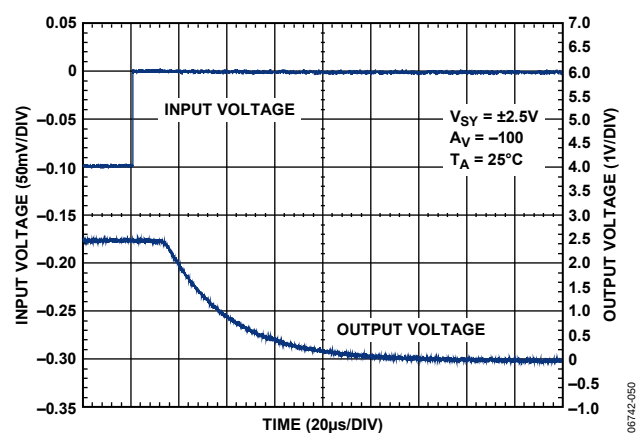


Figure 37. Negative Overload Recovery

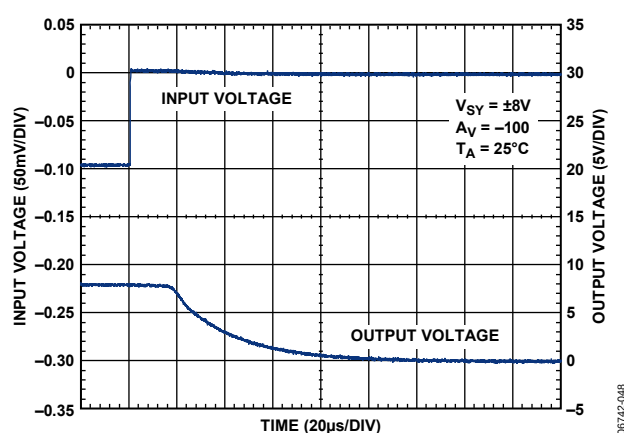


Figure 40. Negative Overload Recovery

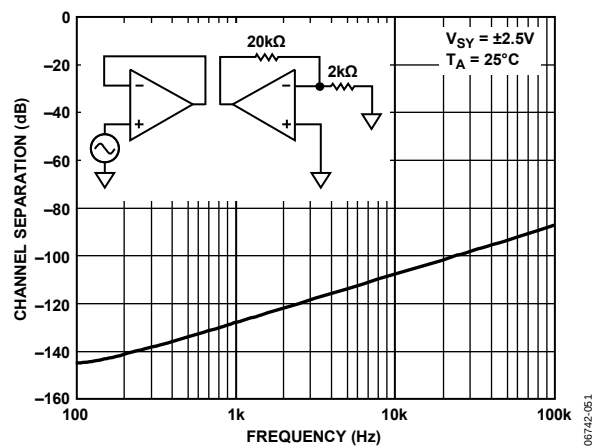


Figure 41. Channel Separation vs. Frequency

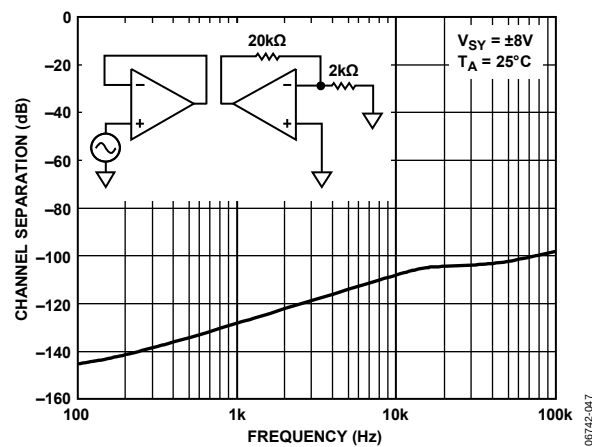


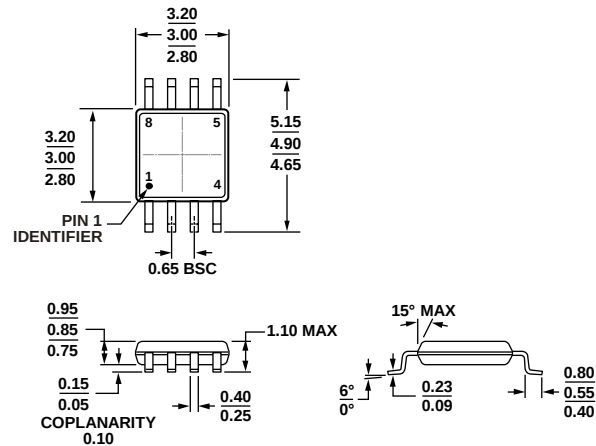
Figure 42. Channel Separation vs. Frequency

112407-A

Dimensions shown in millimeters and (inches)



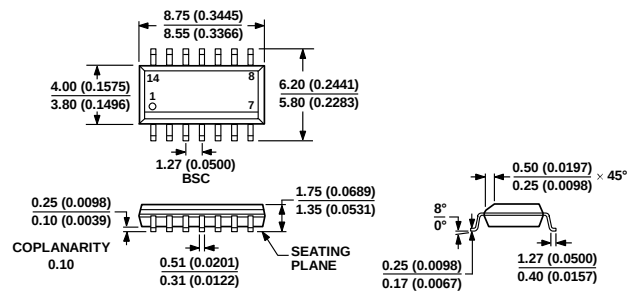
Figure 44. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm x 3 mm and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters



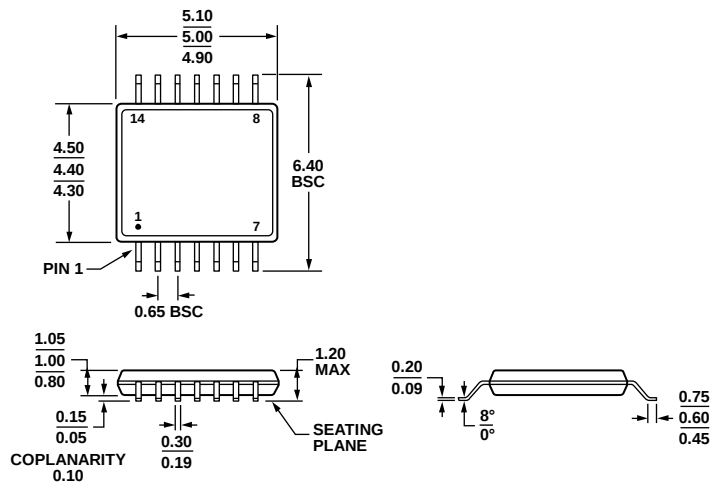
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 45. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.Figure 46. 14-Lead Small Outline Package [SOIC_N]
Narrow Body
(R-14)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 47. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
AD8663ARZ	–40°C to +125°C	8-Lead SOIC_N	R-8	A1U
AD8663ARZ-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8663ARZ-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8663ACPZ-R2	–40°C to +125°C	8-Lead LFCSP	CP-8-13	
AD8663ACPZ-REEL7	–40°C to +125°C	8-Lead LFCSP	CP-8-13	
AD8667ARZ	–40°C to +125°C	8-Lead SOIC_N	R-8	A1E
AD8667ARZ-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8667ARZ-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8667ARMZ	–40°C to +125°C	8-Lead MSOP	RM-8	
AD8667ARMZ-REEL	–40°C to +125°C	8-Lead MSOP	RM-8	
AD8669ARZ	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8669ARZ-REEL	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8669ARZ-REEL7	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8669ARUZ	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8669ARUZ-REEL	–40°C to +125°C	14-Lead TSSOP	RU-14	

¹ Z = RoHS Compliant Part.