AD829* Product Page Quick Links

Last Content Update: 08/30/2016

Comparable Parts

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Evaluation Kits

- AD829 Evaluation Board
- Universal Evaluation Board for Single High Speed Operational Amplifiers

Documentation

Application Notes

- AN-402: Replacing Output Clamping Op Amps with Input Clamping Amps
- AN-417: Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems
- AN-581: Biasing and Decoupling Op Amps in Single Supply Applications

Data Sheet

- AD829: High Speed, Low Noise Video Op Amp Data Sheet
- AD829: Military Data Sheet

User Guides

- UG-101: Evaluation Board User Guide
- UG-135: Evaluation Board for Single, High Speed Operational Amplifiers (8-Lead SOIC and Exposed Paddle)

Tools and Simulations

- Analog Filter Wizard
- Analog Photodiode Wizard
- Op Amp Stability with Capacitive Load
- Power Dissipation vs Die Temp
- VRMS/dBm/dBu/dBV calculators
- AD829 SPICE Macro-Model

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- High Speed Amplifiers Selection Table

Tutorials

- MT-032: Ideal Voltage Feedback (VFB) Op Amp
- MT-033: Voltage Feedback Op Amp Gain and Bandwidth
- MT-047: Op Amp Noise
- MT-048: Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth
- MT-049: Op Amp Total Output Noise Calculations for Single-Pole System
- MT-052: Op Amp Noise Figure: Don't Be Misled
- MT-053: Op Amp Distortion: HD, THD, THD + N, IMD, SFDR, MTPR
- MT-056: High Speed Voltage Feedback Op Amps
- MT-058: Effects of Feedback Capacitance on VFB and CFB Op Amps
- MT-060: Choosing Between Voltage Feedback and Current Feedback Op Amps

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- AD829 Material Declaration
- PCN-PDN Information
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Discussions

View all AD829 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

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SPECIFICATIONS

T_A = 25°C and V_S = ±15 V dc, unless otherwise noted.

Table 1.

Parameter	Conditions	V_S	AD829JR			AD829AR			AD829AQ/AD829S			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE	t_{MIN} to t_{MAX}	±5 V, ±15 V		0.2	1		0.2	1		0.1	0.5	mV
					1			1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7		3.3	7	µA
	t_{MIN} to t_{MAX}				8.2			9.5			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500		50	500	nA
	t_{MIN} to t_{MAX}				500			500			500	nA
Offset Current Drift		± 5 V, ±15 V		0.5			0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V, R_L = 500 Ω	±5 V	30	65		30	65		30	65		V/mV
	R_L = 150 Ω			40			40			40		V/mV
	t_{MIN} to t_{MAX}		20			20			20			V/mV
	V_O = ±10 V, R_L = 1 kΩ	±15 V	50	100		50	100		50	100		V/mV
	R_L = 500 Ω			85			85			85		V/mV
	t_{MIN} to t_{MAX}		20			20			20			V/mV
DYNAMIC PERFORMANCE												
Gain Bandwidth Product		±5 V		600			600			600		MHz
		±15 V		750			750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p-p, R_L = 500 Ω	±5 V		25			25			25		MHz
	V_O = 20 V p-p, R_L = 1 kΩ	±15 V		3.6			3.6			3.6		MHz
Slew Rate[2]	R_L = 500 Ω	±5 V		150			150			150		V/µs
	R_L = 1 kΩ	±15 V		230			230			230		V/µs
Settling Time to 0.1%	A_V = −19											
	−2.5 V to +2.5 V	±5 V		65			65			65		ns
	10 V step	±15 V		90			90			90		ns
Phase Margin[2]	C_L = 10 pF	±15 V										
	R_L = 1 kΩ			60			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_L = 100 Ω, C_{COMP} = 30 pF	±15 V		0.02			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_L = 100 Ω, C_{COMP} = 30 pF	±15 V		0.04			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		100	120		dB
	t_{MIN} to t_{MAX}		96			96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		98	120		dB
	t_{MIN} to t_{MAX}		94			94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		1.7	2		1.7	2		1.7	2	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5			1.5		pA/√Hz

Parameter	Conditions	V_S	AD829JR Min	AD829JR Typ	AD829JR Max	AD829AR Min	AD829AR Typ	AD829AR Max	AD829AQ/AD829S Min	AD829AQ/AD829S Typ	AD829AQ/AD829S Max	Unit
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3			+4.3		V
				−3.8			−3.8			−3.8		V
		±15 V		+14.3			+14.3			+14.3		V
				−13.8			−13.8			−13.8		V
OUTPUT VOLTAGE SWING	R_L = 500 Ω	±5 V	±3.0	±3.6		±3.0	±3.6		±3.0	±3.6		V
	R_L = 150 Ω	±5 V	±2.5	±3.0		±2.5	±3.0		±2.5	±3.0		V
	R_L = 50 Ω	±5 V		±1.4			±1.4			±1.4		V
	R_L = 1 kΩ	±15 V	±12	±13.3		±12	±13.3		±12	±13.3		V
	R_L = 500 Ω	±15 V	±10	±12.2		±10	±12.2		±10	±12.2		V
Short-Circuit Current		±5 V, ±15 V		32			32			32		mA
INPUT CHARACTERISTICS												
Input Resistance (Differential)				13			13			13		kΩ
Input Capacitance (Differential)[4]				5			5			5		pF
Input Capacitance (Common Mode)				1.5			1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2			2		mΩ
POWER SUPPLY												
Operating Range			±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		5	6.5		5	6.5		5	6.5	mA
	t_{MIN} to t_{MAX}				8.0			8.0			8.7	mA
		±15 V		5.3	6.8		5.3	6.8		5.3	6.8	mA
	t_{MIN} to t_{MAX}				8.3			9.0			9.0	mA
TRANSISTOR COUNT	Number of transistors			46			46			46		

[1] Full power bandwidth = slew rate/2 π V_{PEAK}.
[2] Tested at gain = 20, C_{COMP} = 0 pF.
[3] 3.58 MHz (NTSC) and 4.43 MHz (PAL and SECAM).
[4] Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	
8-Lead PDIP (N)	1.3 W
8-Lead SOIC (R)	0.9 W
8-Lead CERDIP (Q)	1.3 W
20-Terminal LCC (E)	0.8 W
Differential Input Voltage[2]	±6 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
8-Lead CERDIP (Q) and 20-Terminal LCC (E)	−65°C to +150°C
8-Lead PDIP (N) and 8-Lead SOIC (R)	−65°C to +125°C
Operating Temperature Range	
AD829J	0°C to 70°C
AD829A	−40°C to +125°C
AD829S	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Maximum internal power dissipation is specified so that T_J does not exceed 150°C at an ambient temperature of 25°C.

[2] If the differential voltage exceeds 6 V, external series protection resistors should be added to limit the input current.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Table 3.

Package Type	θ_{JA}	Unit
8-Lead PDIP (N)	100 (derates at 8.7 mW/°C)	°C/W
8-Lead CERDIP (Q)	110 (derates at 8.7 mW/°C)	°C/W
20-Lead LCC (E)	77	°C/W
8-Lead SOIC (R)	125 (derates at 6 mW/°C)	°C/W

METALLIZATION PHOTO

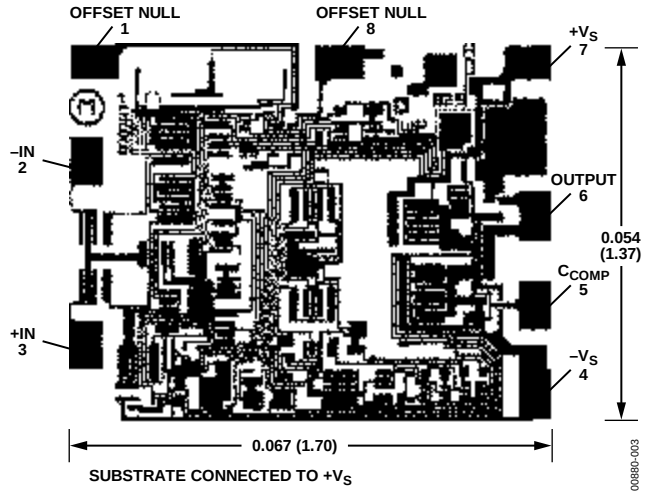


Figure 3. Metallization Photo; Contact Factory for Latest Dimensions, Dimensions Shown in Inches and (Millimeters)

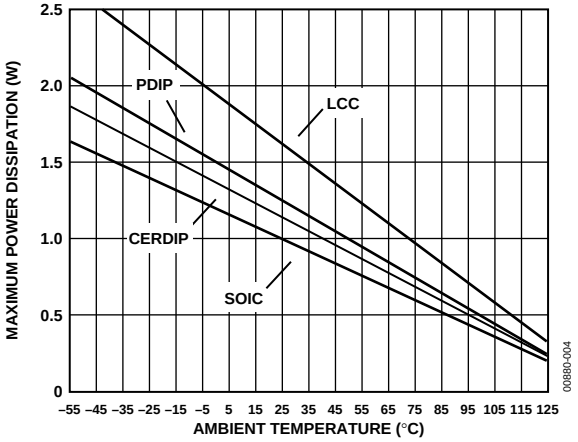


Figure 4. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

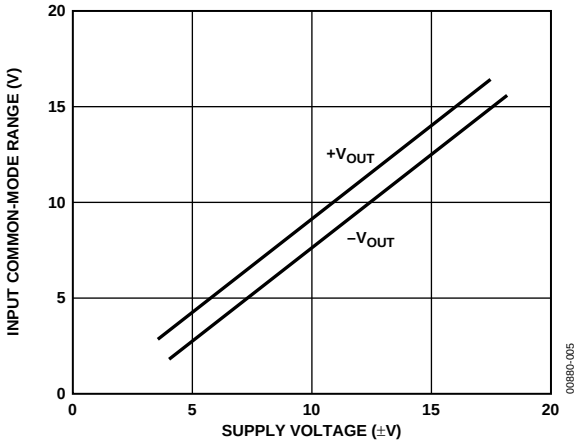


Figure 5. Input Common-Mode Range vs. Supply Voltage

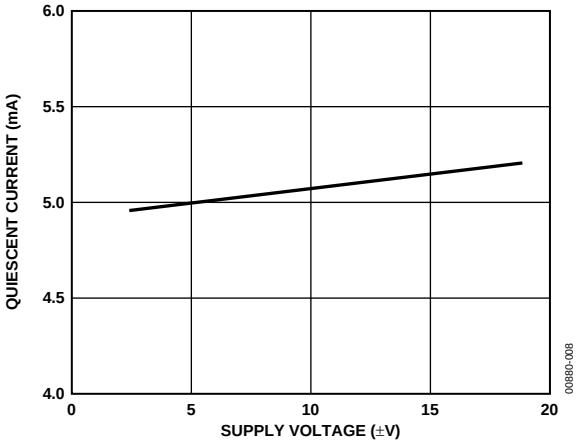


Figure 8. Quiescent Current vs. Supply Voltage

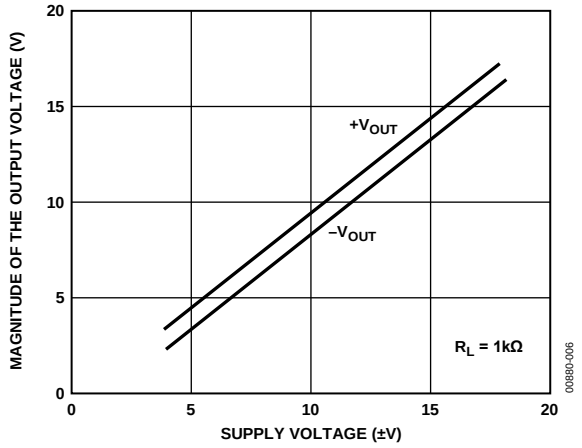


Figure 6. Output Voltage Swing vs. Supply Voltage

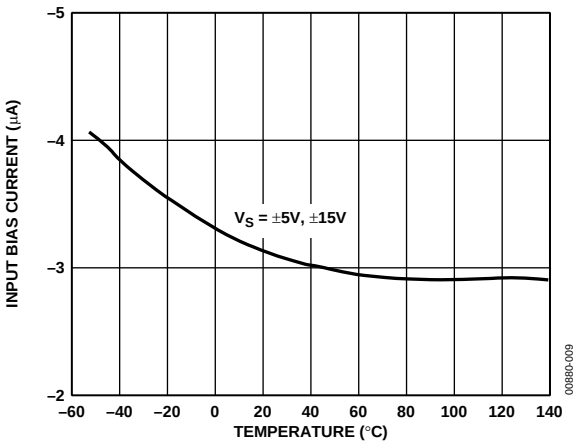


Figure 9. Input Bias Current vs. Temperature

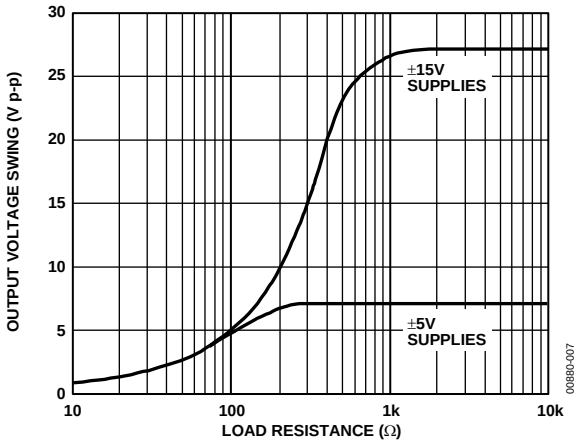


Figure 7. Output Voltage Swing vs. Resistive Load

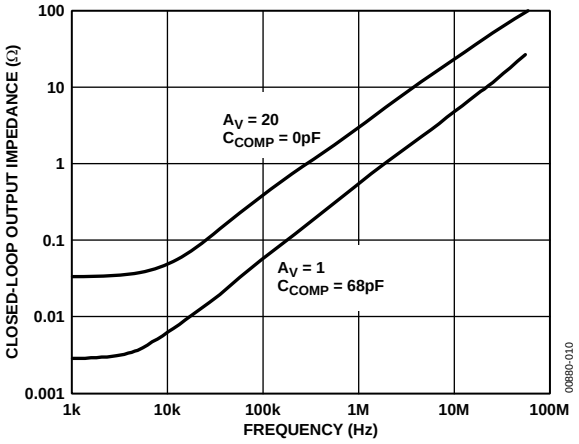
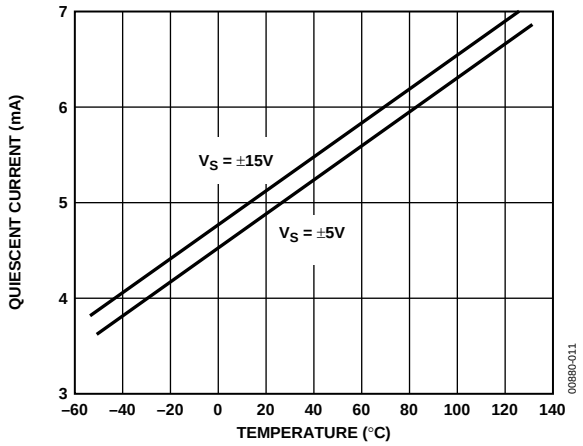


Figure 10. Closed-Loop Output Impedance vs. Frequency



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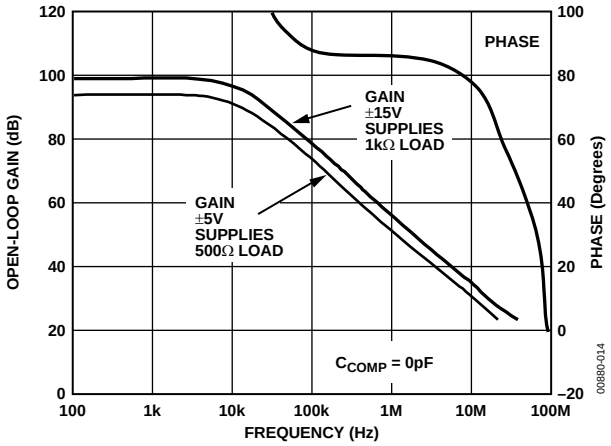


Figure 14. Open-Loop Gain and Phase vs. Frequency

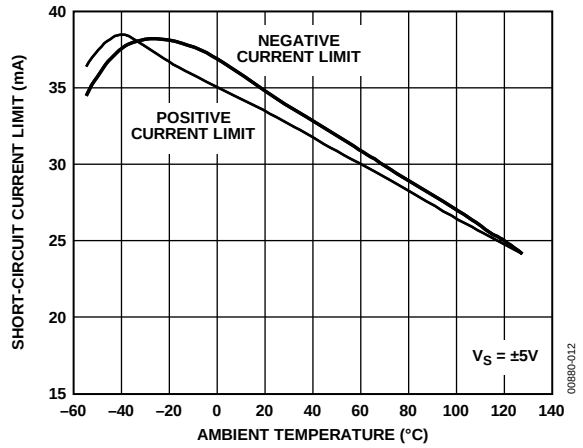


Figure 12. Short-Circuit Current Limit vs. Ambient Temperature

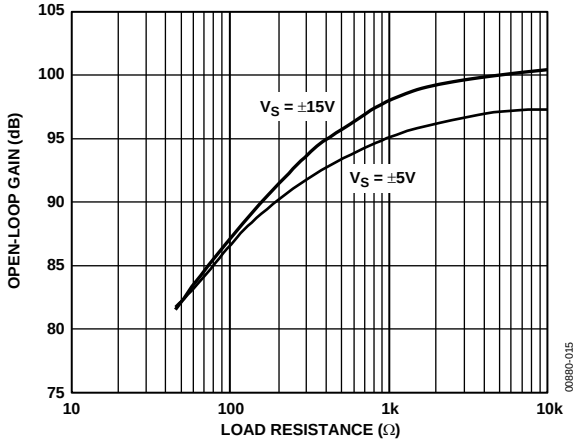


Figure 15. Open-Loop Gain vs. Resistive Load

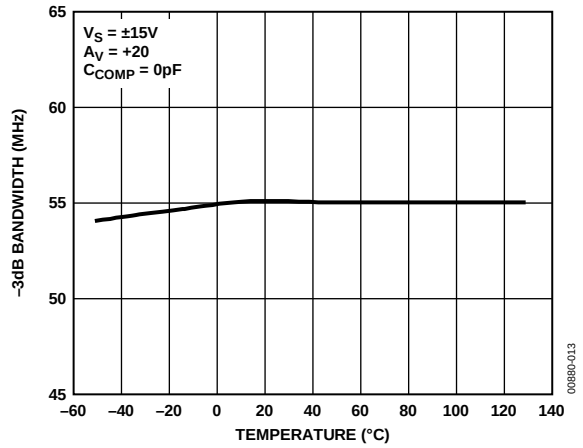
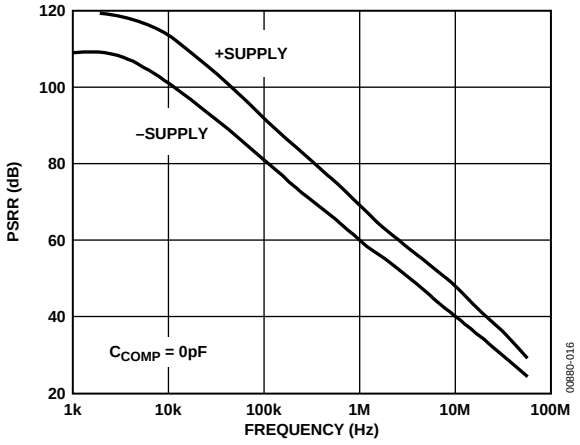


Figure 13. –3 dB Bandwidth vs. Temperature



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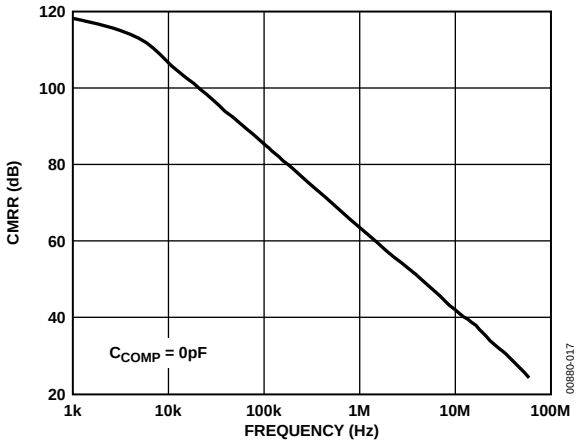
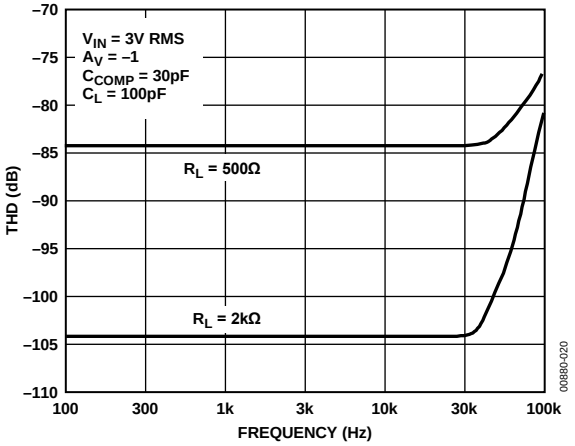


Figure 17. Common-Mode Rejection Ratio (CMRR) vs. Frequency



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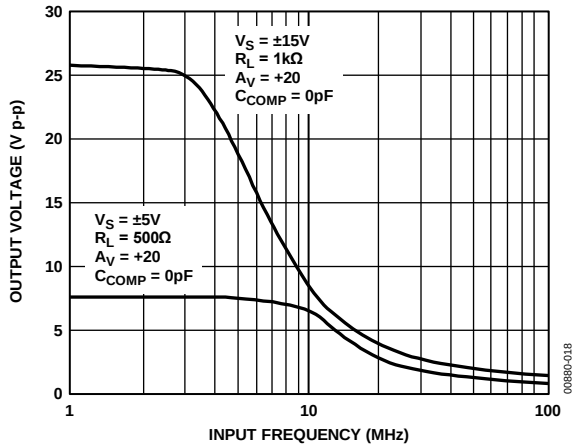


Figure 18. Large Signal Frequency Response

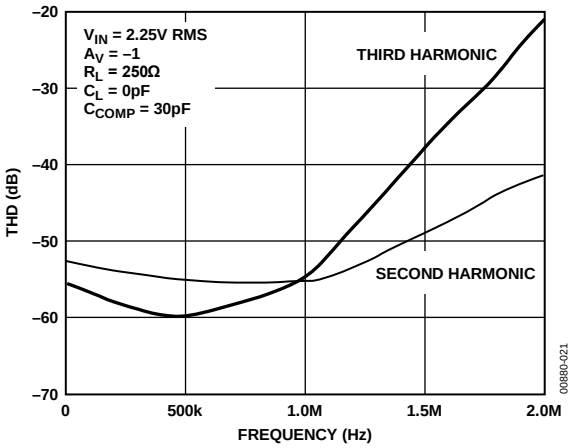


Figure 21. Second and Third THD vs. Frequency

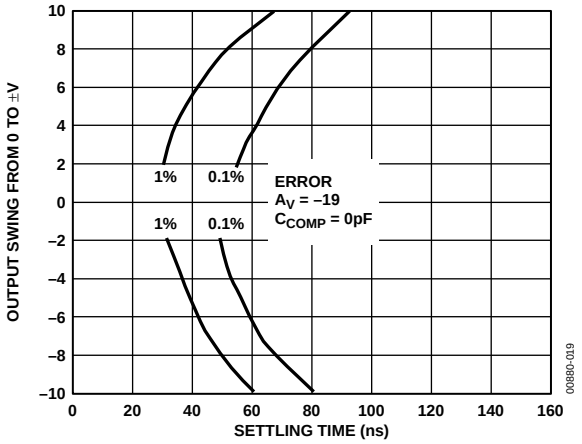


Figure 19. Output Swing and Error vs. Settling Time

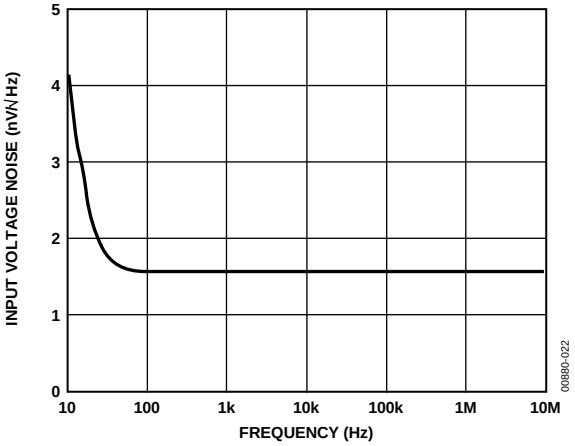


Figure 22. Input Voltage Noise Spectral Density

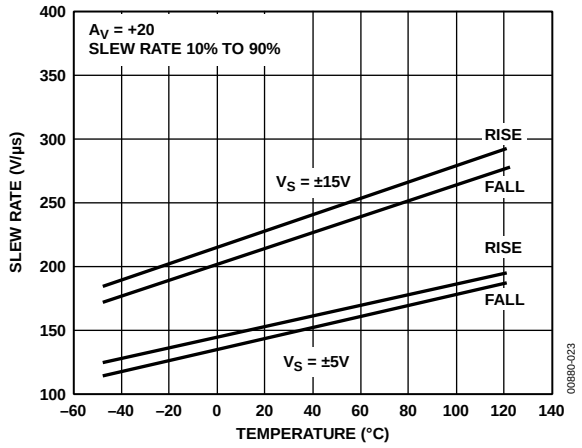


Figure 23. Slew Rate vs. Temperature

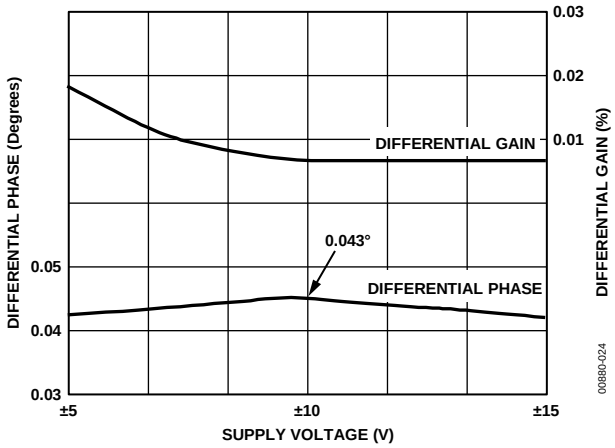


Figure 24. Differential Phase and Gain vs. Supply Voltage

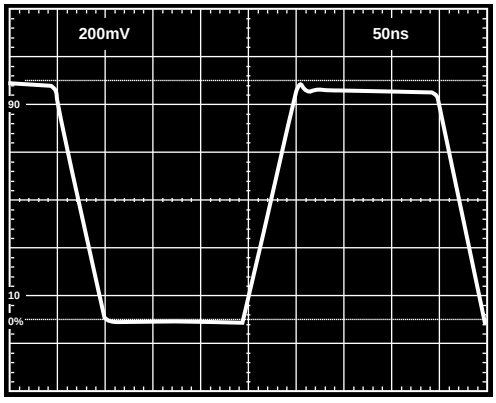


Figure 25. Gain-to-2 Follower Large Signal Pulse Response (See Figure 32)

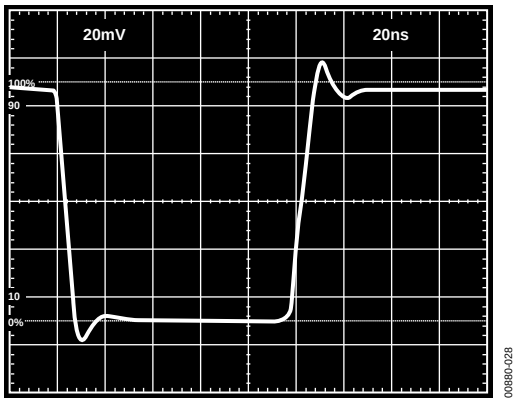


Figure 26. Gain-of-2 Follower Small Signal Pulse Response (See Figure 32)

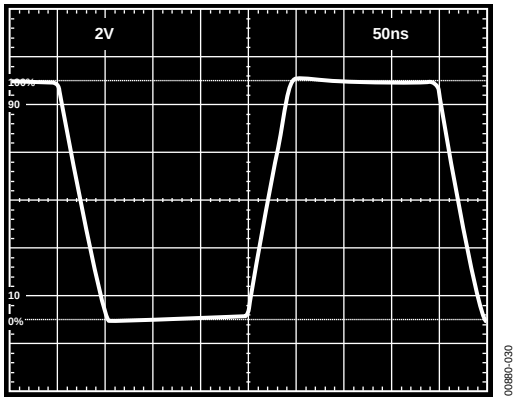


Figure 27. Gain-of-20 Follower Large Signal Pulse Response (See Figure 33)

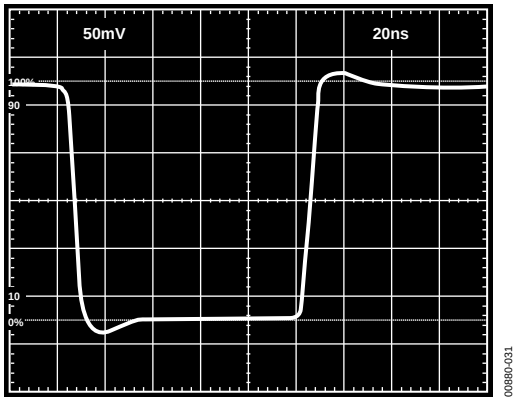


Figure 28. Gain-of-20 Follower Small Signal Pulse Response (See Figure 33)

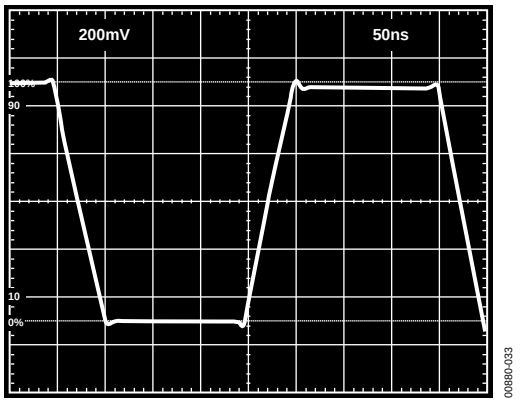


Figure 29. Unity-Gain Inverter Large Signal Pulse Response (See Figure 34)

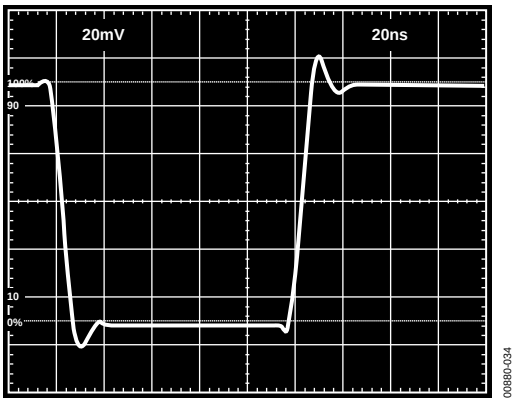


Figure 30. Unity-Gain Inverter Small Signal Pulse Response (See Figure 34)

TEST CIRCUITS

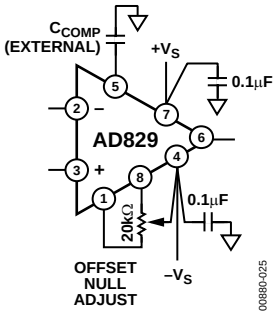


Figure 31. Offset Null and External Shunt Compensation Connections

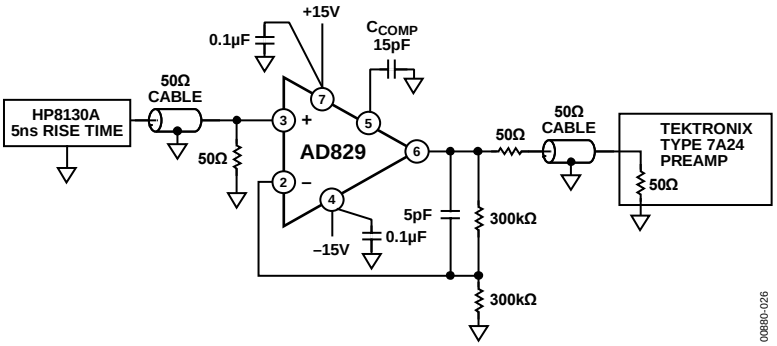


Figure 32. Follower Connection, Gain = 2

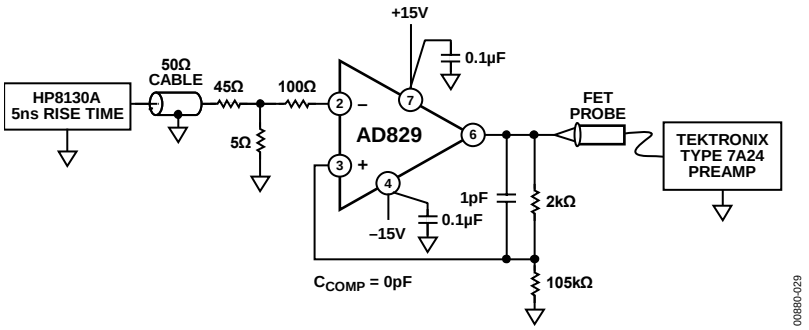


Figure 33. Follower Connection, Gain = 20

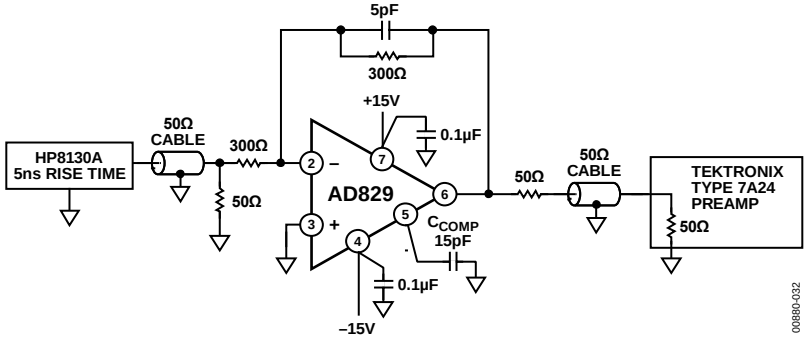


Figure 34. Unity-Gain Inverter Connection

THEORY OF OPERATION

The AD829 is fabricated on the Analog Devices, Inc., proprietary complementary bipolar (CB) process, which provides PNP and NPN transistors with similar f_Ts of 600 MHz. As shown in Figure 35, the AD829 input stage consists of an NPN differential pair in which each transistor operates at a 600 µA collector current. This gives the input devices a high transconductance, which in turn gives the AD829 a low noise figure of 2 nV/√Hz at 1 kHz.

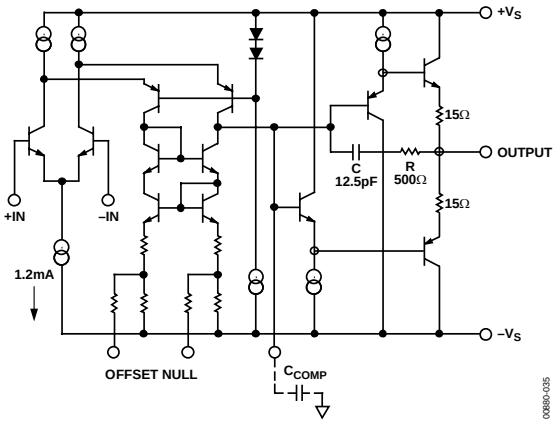


Figure 35. Simplified Schematic

The input stage drives a folded cascode that consists of a fast pair of PNP transistors. These PNPs drive a current mirror that provides a differential-input-to-single-ended-output conversion. The high speed PNPs are also used in the current-amplifying output stage, which provides a high current gain of 40,000. Even under heavy loading conditions, the high f_Ts of the NPN and PNPs, produced using the CB process, permit cascading two stages of emitter followers while maintaining 60 phase margin at closed-loop bandwidths greater than 50 MHz.

Two stages of complementary emitter followers also effectively buffer the high impedance compensation node (at the C_{COMP} pin) from the output so that the AD829 can maintain a high dc open-loop gain, even into low load impedances (92 dB into a 150 Ω load and 100 dB into a 1 kΩ load). Laser trimming and PTAT biasing ensure low offset voltage and low offset voltage drift, enabling the user to eliminate ac coupling in many applications.

For added flexibility, the AD829 provides access to the internal frequency compensation node. This allows users to customize the frequency response characteristics for a particular application.

Unity-gain stability requires a compensation capacitance of 68 pF (Pin 5 to ground), which yields a small signal bandwidth of 66 MHz and slew rate of 16 V/µs. The slew rate and gain bandwidth product varies inversely with compensation capacitance. Table 4 and Figure 37 show the optimum compensation capacitance and the resulting slew rate for a desired noise gain.

For gains between 1 and 20, choose C_{COMP} to keep the small signal bandwidth relatively constant. The minimum gain that will still provide stability depends on the value of the external compensation capacitance.

An RC network in the output stage (see Figure 35) completely removes the effect of capacitive loading when the amplifier compensates for closed-loop gains of 10 or higher. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C is bootstrapped and does not contribute to the compensation capacitance of the device. As the capacitive load increases, a pole forms with the output impedance of the output stage, which reduces the gain, and subsequently, C is incompletely bootstrapped. Therefore, some fraction of C contributes to the compensation capacitance, and the unity-gain bandwidth falls. As the load capacitance is further increased, the bandwidth continues to fall, and the amplifier remains stable.

EXTERNALLY COMPENSATING THE AD829

The AD829 is stable with no external compensation for noise gains greater than 20. For lower gains, two different methods of frequency compensating the amplifier can be used to achieve closed-loop stability: shunt and current feedback compensation.

SHUNT COMPENSATION

Figure 36 and Figure 37 show that shunt compensation has an external compensation capacitor, C_{COMP}, connected between the compensation pin and ground. This external capacitor is tied in parallel with approximately 3 pF of internal capacitance at the compensation node. In addition, a small capacitance, C_{LEAD}, in parallel with resistor R2, compensates for the capacitance at the inverting input of the amplifier.

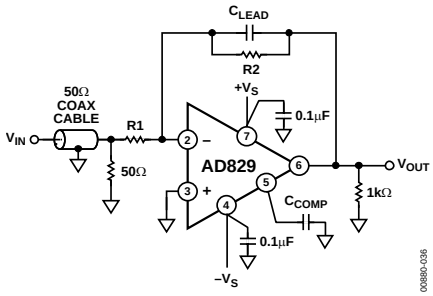


Figure 36. Inverting Amplifier Connection Using External Shunt Compensation

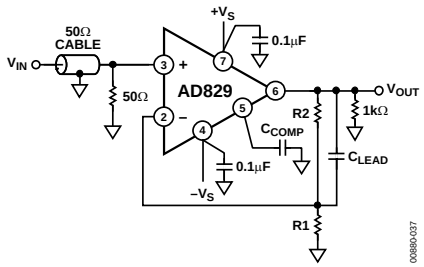


Figure 37. Noninverting Amplifier Connection Using External Shunt Compensation

Table 4 gives the recommended C_{COMP} and C_{LEAD} values, as well as the corresponding slew rates and bandwidth. The capacitor values were selected to provide a small signal frequency response with <1 dB of peaking and <10% overshoot. For Table 4, ±15 V

supply voltages should be used. Figure 38 is a graphical extension of Table 4, which shows the slew rate/gain trade-off for lower closed-loop gains, when using the shunt compensation scheme.

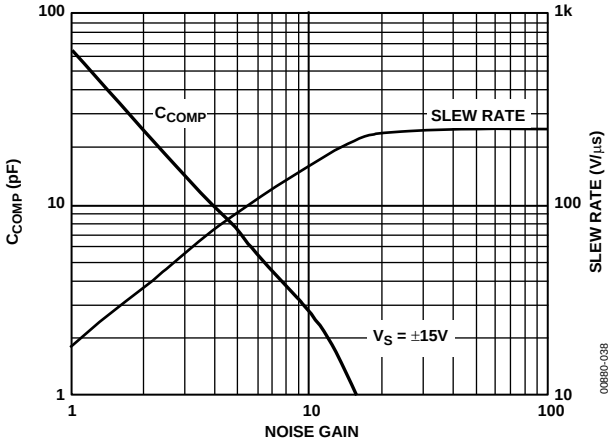


Figure 38. Value of C_{COMP} and Slew Rate vs. Noise Gain

CURRENT FEEDBACK COMPENSATION

Bipolar, nondegenerated, single-pole, and internally compensated amplifiers have their bandwidths defined as

$$f_T = \frac{1}{2\pi r_e C_{COMP}} = \frac{I}{2\pi \frac{kT}{q} C_{COMP}}$$

where:
f_T is the unity-gain bandwidth of the amplifier.
I is the collector current of the input transistor.
C_{COMP} is the compensation capacitance.
r_e is the inverse of the transconductance of the input transistors.
kT/q approximately equals 26 mV at 27°C.

Because both f_T and slew rate are functions of the same variables, the dynamic behavior of an amplifier is limited. Because

$$Slew\ Rate = \frac{2I}{C_{COMP}}$$

then

$$\frac{Slew\ Rate}{f_T} = 4\pi\frac{kT}{q}$$

This shows that the slew rate is only 0.314 V/µs for every megahertz of bandwidth. The only way to increase the slew rate is to increase the f_T, and that is difficult because of process limitations. Unfortunately, an amplifier with a bandwidth of 10 MHz can only slew at 3.1 V/µs, which is barely enough to provide a full power bandwidth of 50 kHz.

The AD829 is especially suited to a form of current feedback compensation that allows for the enhancement of both the full power bandwidth and the slew rate of the amplifier. The voltage gain from the inverting input pin to the compensation pin is large; therefore, if a capacitance is inserted between these pins, the bandwidth of the amplifier becomes a function of its feedback resistor and the capacitance. The slew rate of the amplifier is now a function of its internal bias (2I) and the compensation capacitance.

Table 4. Component Selection for Shunt Compensation

Follower Gain	Inverter Gain	R1 (Ω)	R2 (Ω)	C_{LEAD} (pF)	C_{COMP} (pF)	Slew Rate (V/µs)	−3 dB Small Signal Bandwidth (MHz)
1		Open	100	0	68	16	66
2	−1	1 k	1 k	5	25	38	71
5	−4	511	2.0 k	1	7	90	76
10	−9	226	2.05 k	0	3	130	65
20	−19	105	2 k	0	0	230	55
25	−24	105	2.49	0	0	230	39
100	−99	20	2 k	0	0	230	7.5

Because the closed-loop bandwidth is a function of R_F and C_{COMP} (see Figure 39), it is independent of the amplifier closed-loop gain, as shown in Figure 41. To preserve stability, the time constant of R_F and C_{COMP} needs to provide a bandwidth of <65 MHz. For example, with C_{COMP} = 15 pF and R_F = 1 kΩ, the small signal bandwidth of the AD829 is 10 MHz. Figure 40 shows that the slew rate is in excess of 60 V/µs. As shown in Figure 41, the closed-loop bandwidth is constant for gains of −1 to −4; this is a property of the current feedback amplifiers.

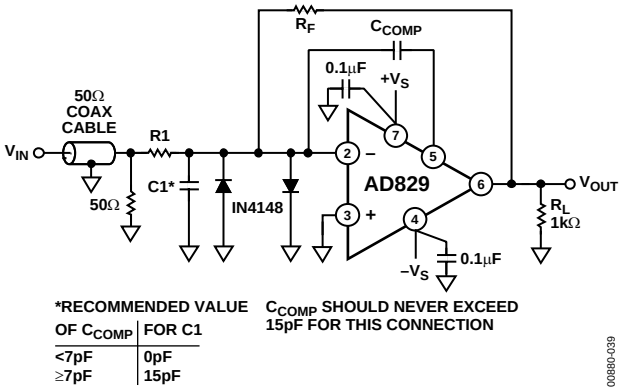


Figure 39. Inverting Amplifier Connection Using Current Feedback Compensation

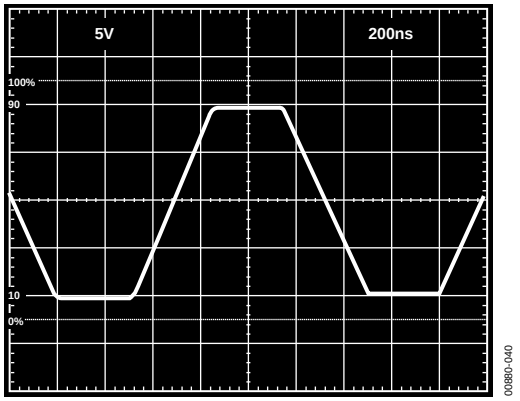


Figure 40. Large Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation, C_{COMP} = 15 pF, C1 = 15 pF R_F = 1 kΩ, R1 = 1 kΩ

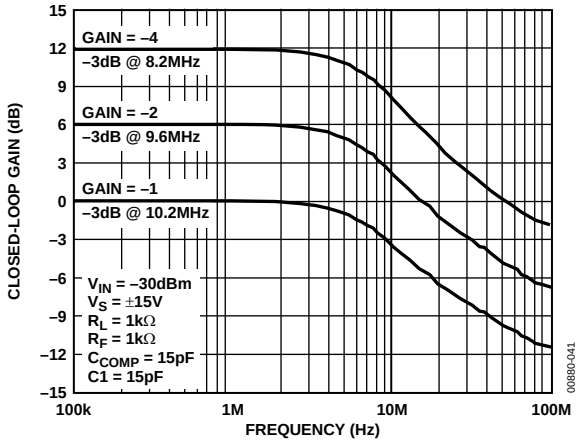


Figure 41. Closed-Loop Gain vs. Frequency for the Circuit of Figure 38

Figure 42 is an oscilloscope photo of the pulse response of a unity-gain inverter that has been configured to provide a small signal bandwidth of 53 MHz and a subsequent slew rate of 180 V/µs; R_F = 3 kΩ and C_{COMP} = 1 pF. Figure 43 shows the excellent pulse response as a unity-gain inverter, this using component values of R_F = 1 kΩ and C_{COMP} = 4 pF.

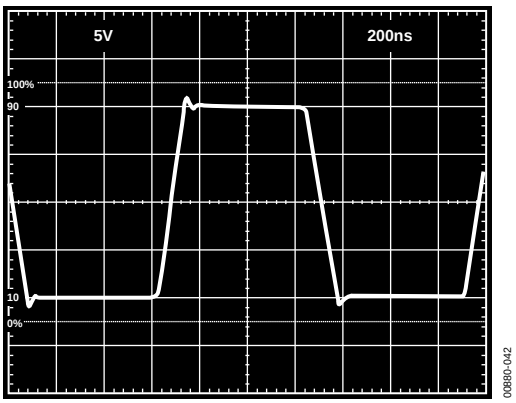


Figure 42. Large Signal Pulse Response of the Inverting Amplifier Using Current Feedback Compensation, C_{COMP} = 1 pF, R_F = 3 kΩ, R1 = 3 kΩ

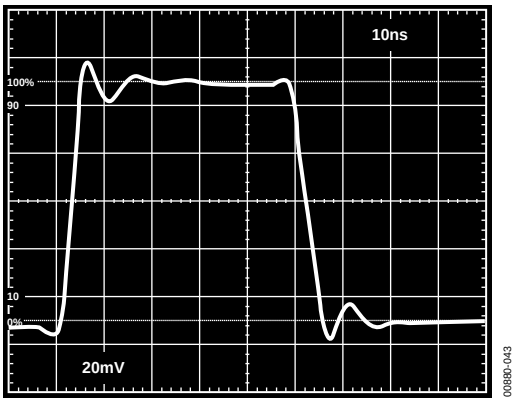


Figure 43. Small Signal Pulse Response of Inverting Amplified Using Current Feedback Compensation, C_{COMP} = 4 pF, R_F = 1 kΩ, R1 = 1 kΩ

Figure 44 and Figure 45 show the closed-loop frequency response of the AD829 for different closed-loop gains and different supply voltages.

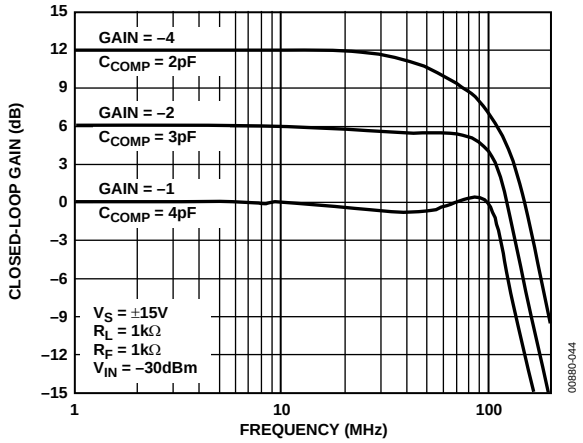


Figure 44. Closed-Loop Frequency Response for the Inverting Amplifier Using Current Feedback Compensation

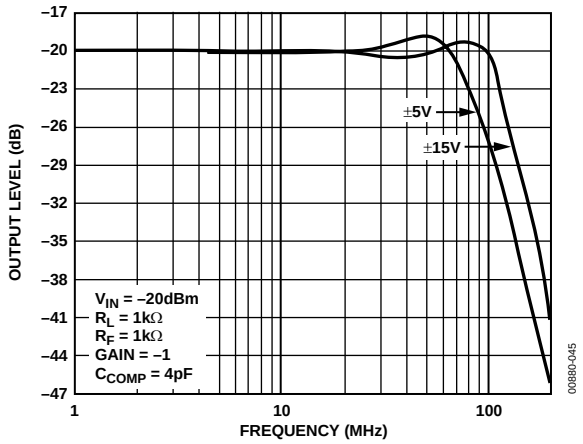


Figure 45. Closed-Loop Frequency Response vs. Supply for the Inverting Amplifier Using Current Feedback Compensation

When a noninverting amplifier configuration using a current feedback compensation is needed, the circuit shown in Figure 46 is recommended. This circuit provides a slew rate twice that of the shunt compensated noninverting amplifier of Figure 47 at the expense of gain flatness. Nonetheless, this circuit delivers 95 MHz bandwidth with 1 dB flatness into a back-terminated cable, with a differential gain error of only 0.01% and a differential phase error of only 0.015 at 4.43 MHz.

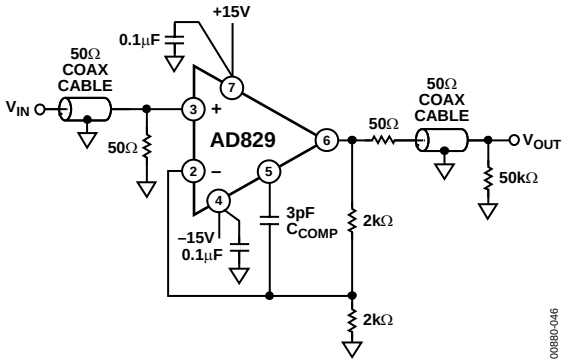


Figure 46. Noninverting Amplifier Connection Using Current Feedback Compensation

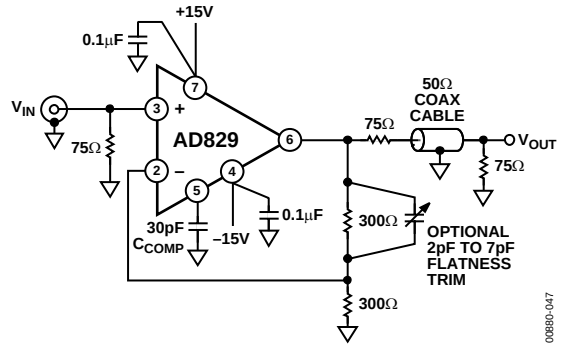


Figure 47. Video Line Driver with a Flatness over Frequency Adjustment

LOW ERROR VIDEO LINE DRIVER

The buffer circuit shown in Figure 47 drives a back-terminated 75 Ω video line to standard video levels (1 V p-p), with 0.1 dB gain flatness to 30 MHz and with only 0.04° and 0.02% differential phase and gain at the 4.43 MHz PAL color subcarrier frequency. This level of performance, which meets the requirements for high definition video displays and test equipment, is achieved using only 5 mA quiescent current.

HIGH GAIN VIDEO BANDWIDTH, 3-OP-AMP INSTRUMENTATION AMPLIFIER

Figure 48 shows a 3-op-amp instrumentation amplifier circuit that provides a gain of 100 at video bandwidths. At a circuit gain of 100, the small signal bandwidth equals 18 MHz into a FET probe. Small signal bandwidth equals 6.6 MHz with a 50 Ω load. The 0.1% settling time is 300 ns.

The input amplifiers operate at a gain of 20, while the output op amp runs at a gain of 5. In this circuit, the main bandwidth limitation is the gain/bandwidth product of the output amplifier. Extra care should be taken while breadboarding this circuit because even a couple of extra picofarads of stray capacitance at the compensation pins of A1 and A2 will degrade circuit bandwidth.

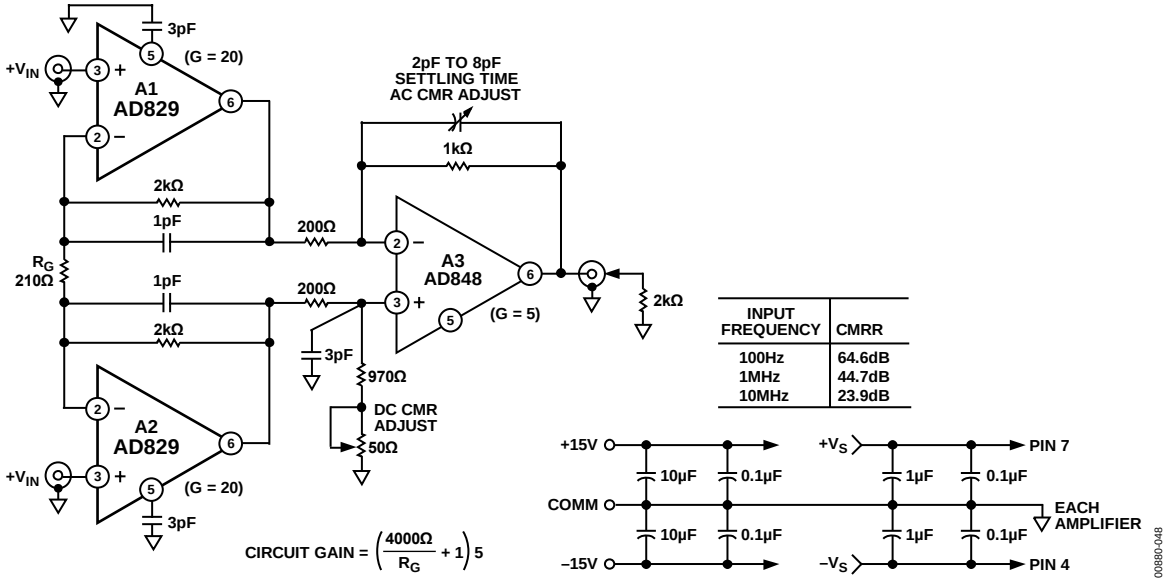
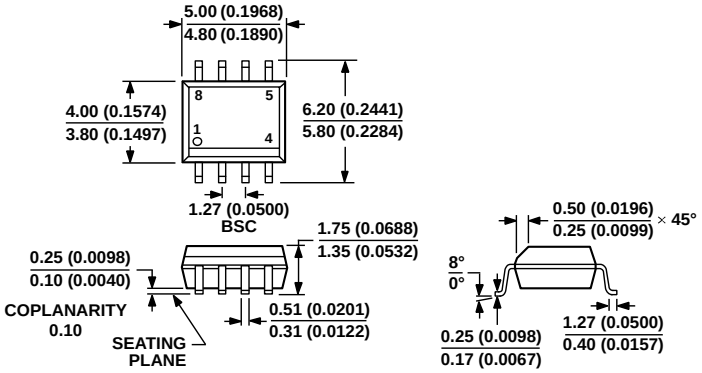


Figure 48. High Gain Video Bandwidth, 3-Op-Amp In-Amp Circuit

OUTLINE DIMENSIONS

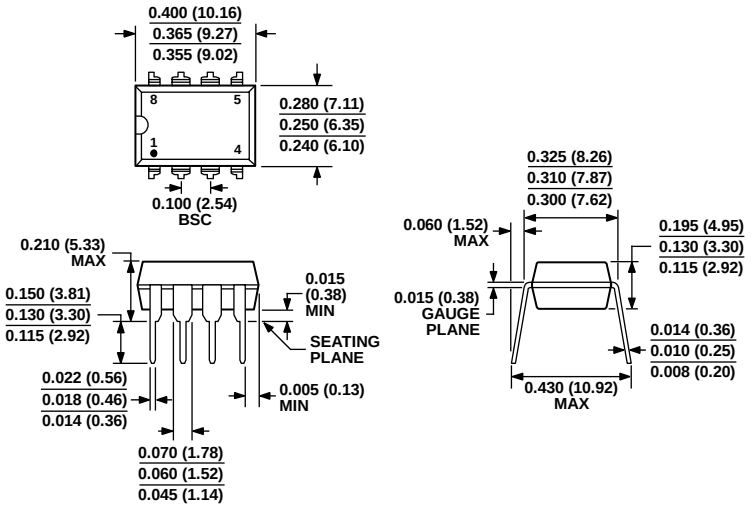


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 49. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

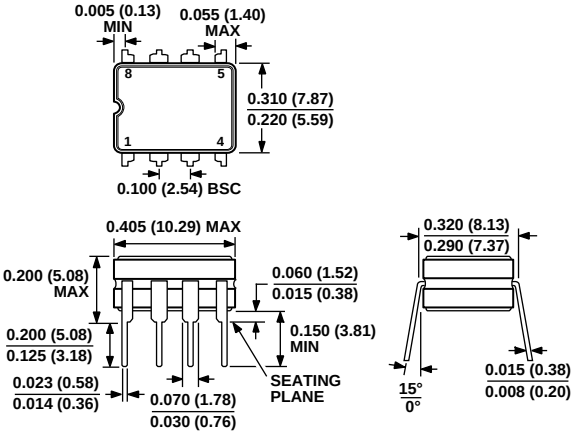


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

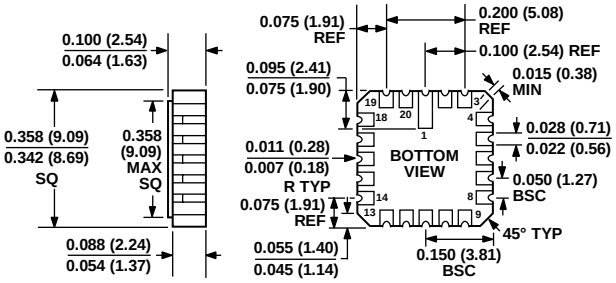
070606-A

Figure 50. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 51. 8-Lead Ceramic Dual In-Line [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

022106-A

Figure 52. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20-1)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD829AR	−40°C to +125°C	8-Lead SOIC_N	R-8
AD829AR-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8
AD829AR-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8
AD829ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8
AD829ARZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8
AD829ARZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8
AD829JN	0°C to 70°C	8-Lead PDIP	N-8
AD829JNZ	0°C to 70°C	8-Lead PDIP	N-8
AD829JR	0°C to 70°C	8-Lead SOIC_N	R-8
AD829JR-REEL	0°C to 70°C	8-Lead SOIC_N	R-8
AD829JR-REEL7	0°C to 70°C	8-Lead SOIC_N	R-8
AD829JRZ	0°C to 70°C	8-Lead SOIC_N	R-8
AD829JRZ-REEL	0°C to 70°C	8-Lead SOIC_N	R-8
AD829JRZ-REEL7	0°C to 70°C	8-Lead SOIC_N	R-8
AD829AQ	−40°C to +125°C	8-Lead CERDIP	Q-8
AD829SQ	−55°C to +125°C	8-Lead CERDIP	Q-8
AD829SQ/883B	−55°C to +125°C	8-Lead CERDIP	Q-8
5962-9312901MPA	−55°C to +125°C	8-Lead CERDIP	Q-8
AD829SE/883B	−55°C to +125°C	20-Lead LCC	E-20-1
5962-9312901M2A	−55°C to +125°C	20-Lead LCC	E-20-1
AD829JCHIPS		Die	
AD829SCHIPS		Die	
AD829AR-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES