AD5162* PRODUCT PAGE QUICK LINKS

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- AD5162 Evaluation Board

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- AN-1291: Digital Potentiometers: Frequently Asked Questions
- AN-686: Implementing an $I^2C^®$ Reset

Data Sheet

- AD5162: Dual, 256-Position, SPI Digital Potentiometer Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5162 - Microcontroller No-OS Driver
- AD5162 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- BeMicro FPGA Project for AD5162 with Nios driver

DESIGN RESOURCES

- AD5162 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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11/03—Rev. 0 to Rev. A

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11/03—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS: 2.5 kΩ VERSION

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−2	±0.1	+2	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−14	±2	+14	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
Wiper Resistance	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE[4]						
Differential Nonlinearity[5]	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity[5]	INL		−2	±0.6	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−14	−5.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	4.5	12	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, B[7]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[7]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[7]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[9]						
Bandwidth, −3 dB	BW	Code = 0x80		4.8		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 1.25 kΩ, R_S = 0		3.2		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, V_B = 0 V, wiper (V_W) = no connect.
[4] Specifications apply to all VRs.
[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[7] Guaranteed by design, but not subject to production test.
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[9] All dynamic characteristics use V_{DD} = 5 V.

ELECTRICAL CHARACTERISTICS: 10 kΩ, 50 kΩ, AND 100 kΩ VERSIONS

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < 125°C; unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2.5	±0.25	+2.5	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
Wiper Resistance	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE[4]						
Differential Nonlinearity[5]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[5]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2.5	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2.5	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, B[7]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[7]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	μA
Input Capacitance	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	μA
Power Dissipation	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	μW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS						
Bandwidth, −3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		μs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, V_B = 0 V, wiper (V_W) = no connect.
[4] Specifications apply to all VRs.
[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[7] Guaranteed by design, but not subject to production test.

TIMING CHARACTERISTICS: ALL VERSIONS

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SPI INTERFACE TIMING CHARACTERISTICS[1]						
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		40			ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

[1] See the timing diagrams for the locations of measured values (that is, see Figure 42 and Figure 43).

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx[1]	
Pulsed	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance, θ_{JA} for 10-Lead MSOP[2]	230°C/W

[1] The maximum terminal current is bound by the maximum current handling of the switches, the maximum power dissipation of the package, and the maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] The package power dissipation is $(T_{JMAX} - T_A)/\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

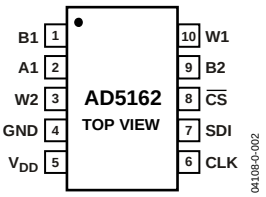

Figure 2.

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	B1 Terminal.
2	A1	A1 Terminal.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply.
6	CLK	Serial Clock Input. Positive-edge triggered.
7	SDI	Serial Data Input.
8	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data is loaded into the DAC register.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

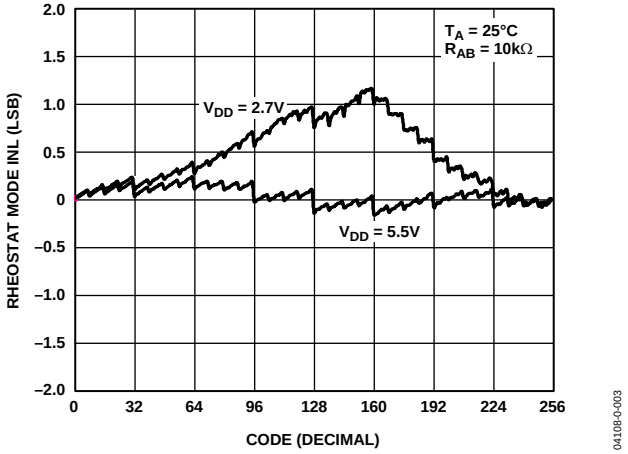

Figure 3. R-INL vs. Code vs. Supply Voltages

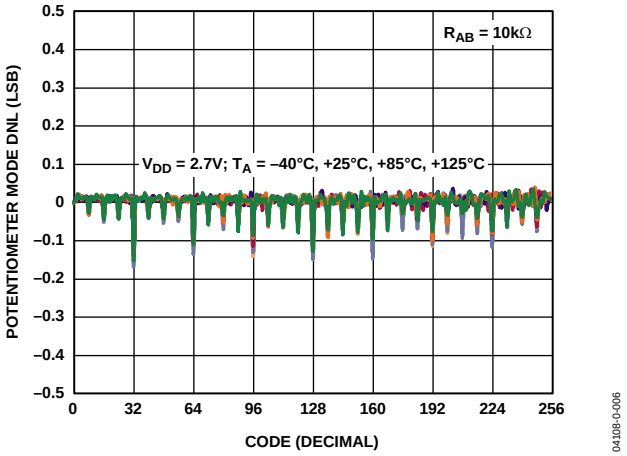

Figure 6. DNL vs. Code vs. Temperature

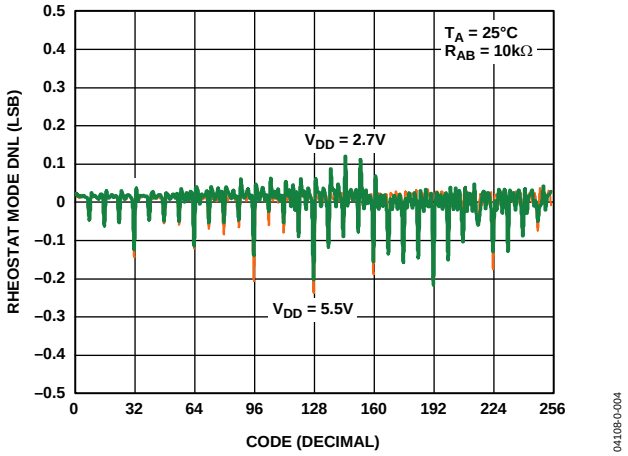

Figure 4. R-DNL vs. Code vs. Supply Voltages

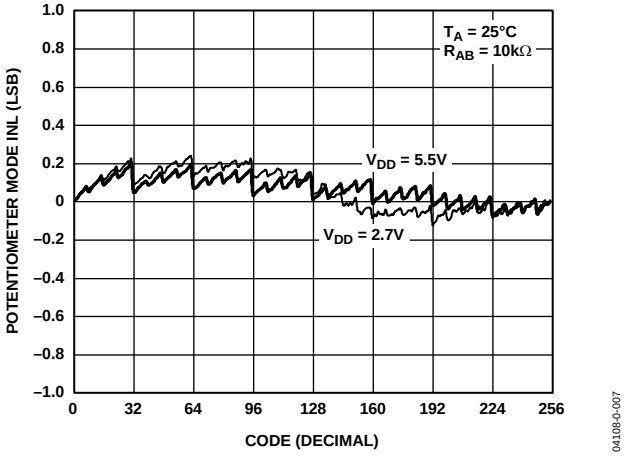

Figure 7. INL vs. Code vs. Supply Voltages

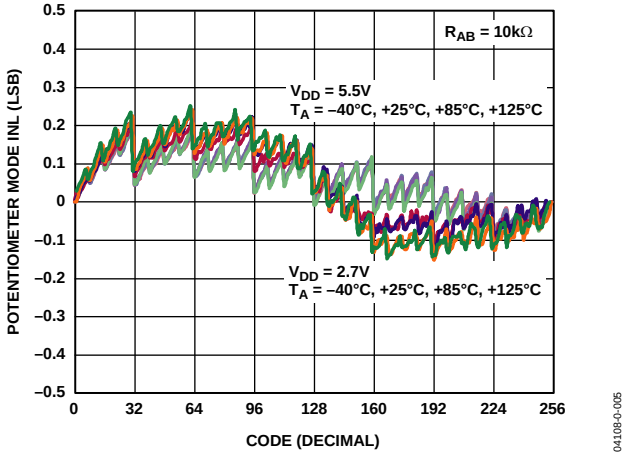

Figure 5. INL vs. Code vs. Temperature

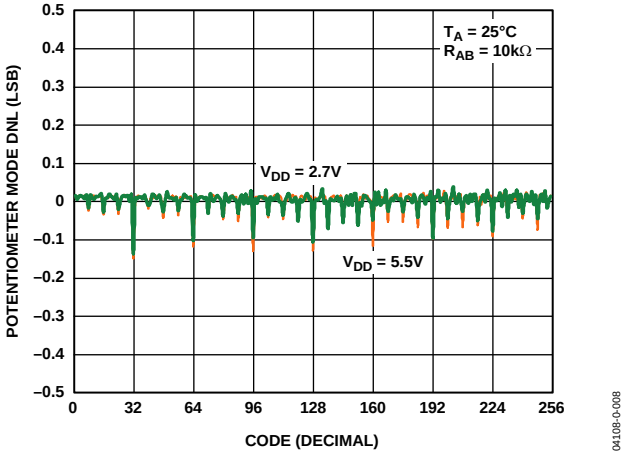

Figure 8. DNL vs. Code vs. Supply Voltages

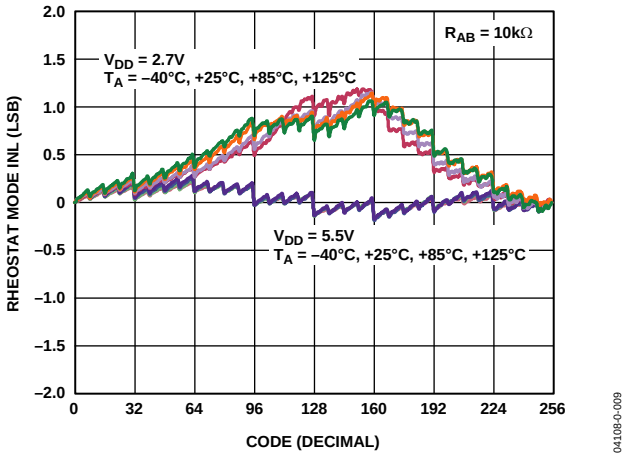

Figure 9. R-INL vs. Code vs. Temperature

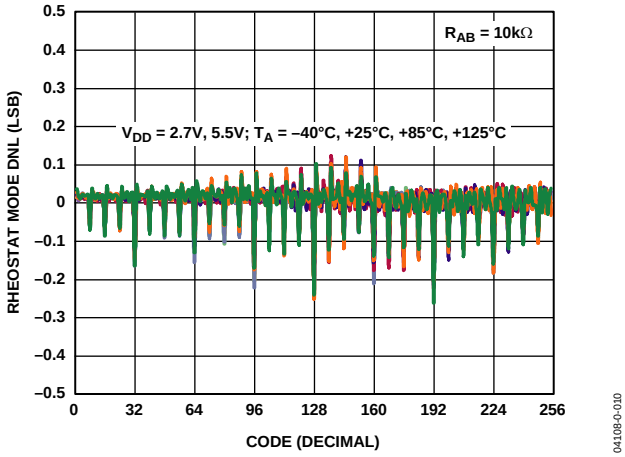

Figure 10. R-DNL vs. Code vs. Temperature

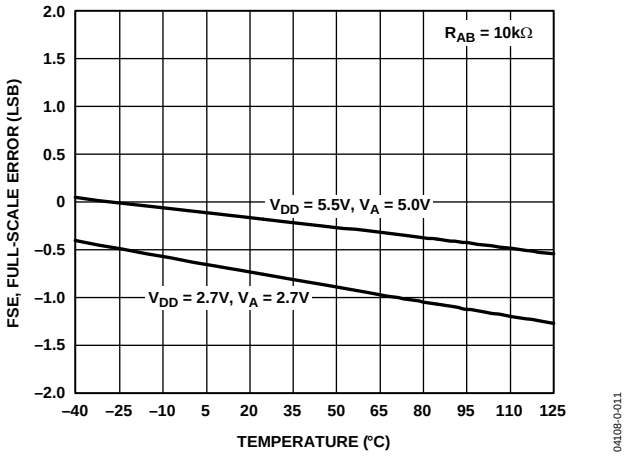

Figure 11. Full-Scale Error vs. Temperature

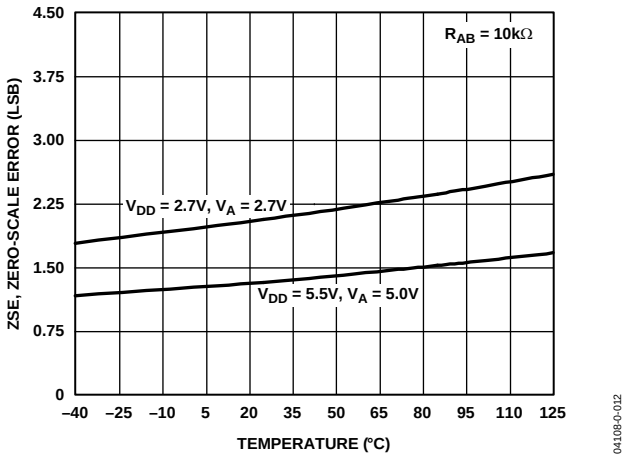

Figure 12. Zero-Scale Error vs. Temperature

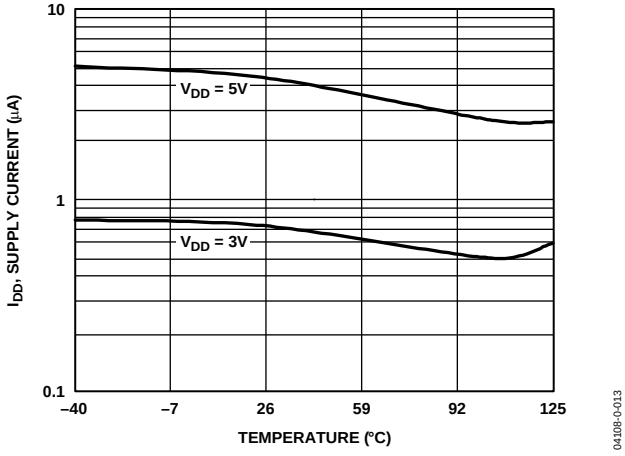

Figure 13. Supply Current vs. Temperature

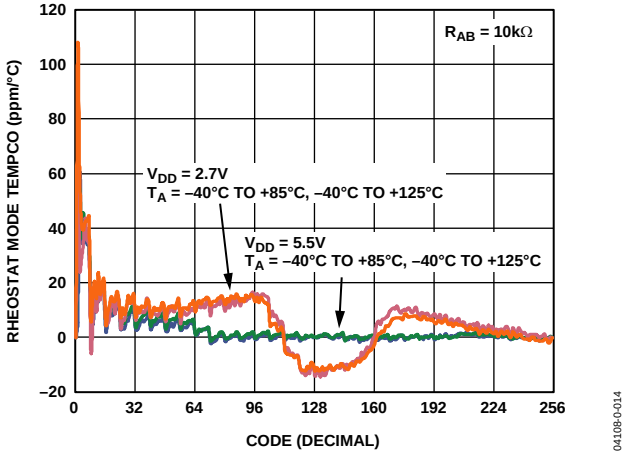

Figure 14. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

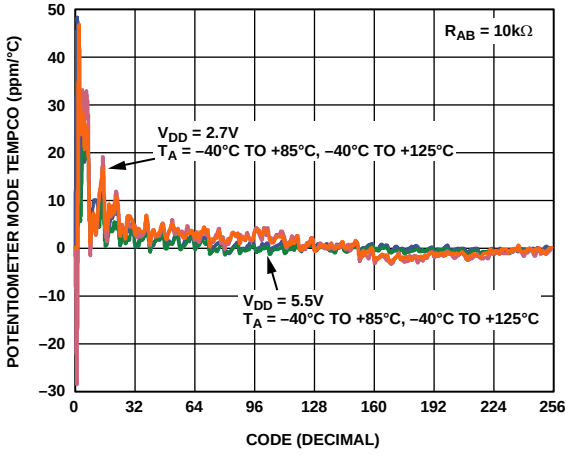

Figure 15. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

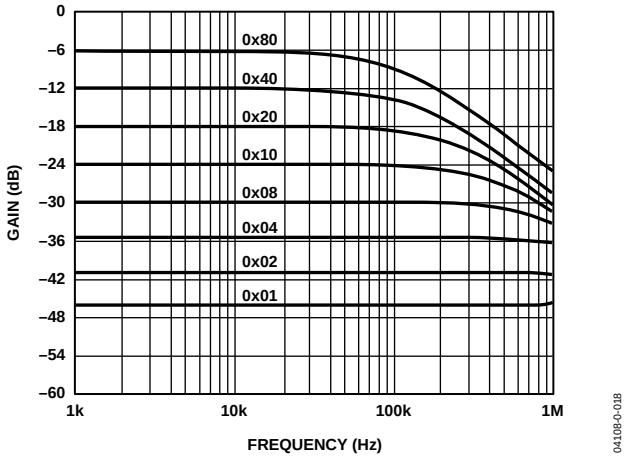

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

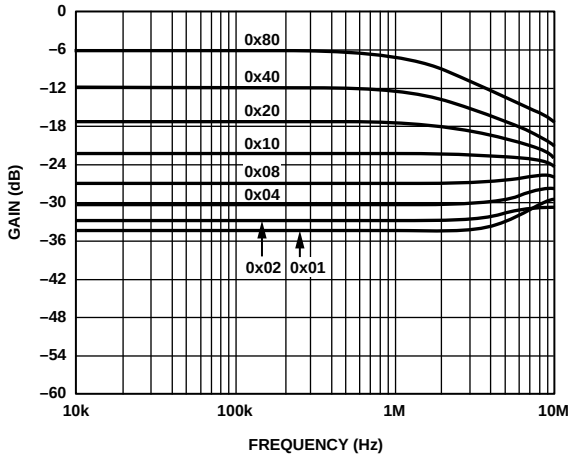

Figure 16. Gain vs. Frequency vs. Code, R_{AB} = 2.5 kΩ

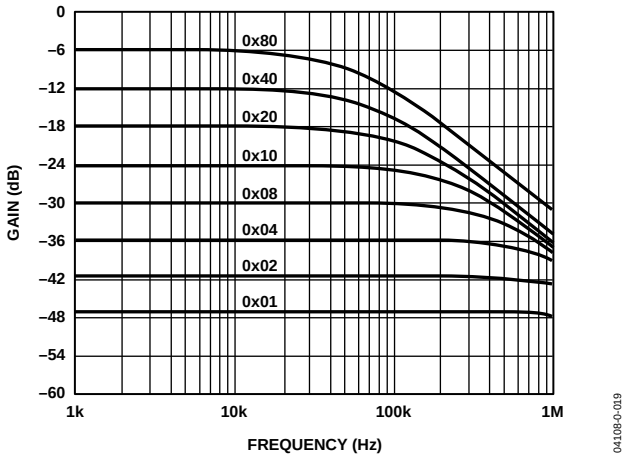

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

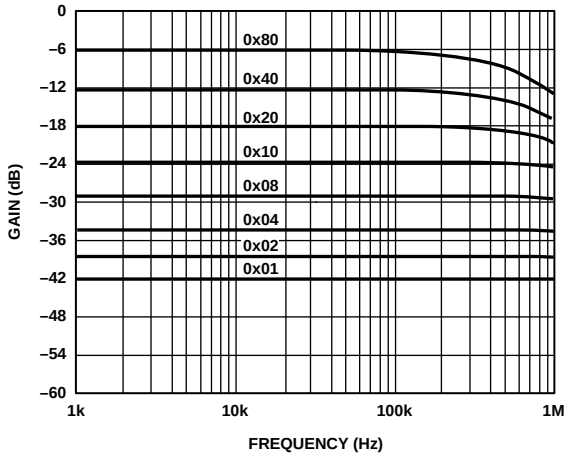

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

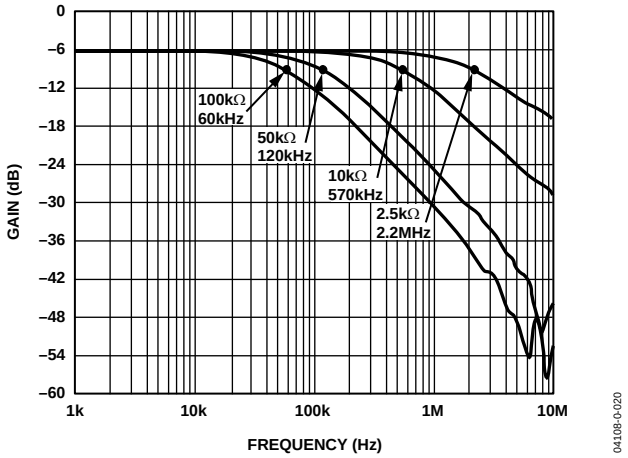

Figure 20. –3 dB Bandwidth at Code = 0x80

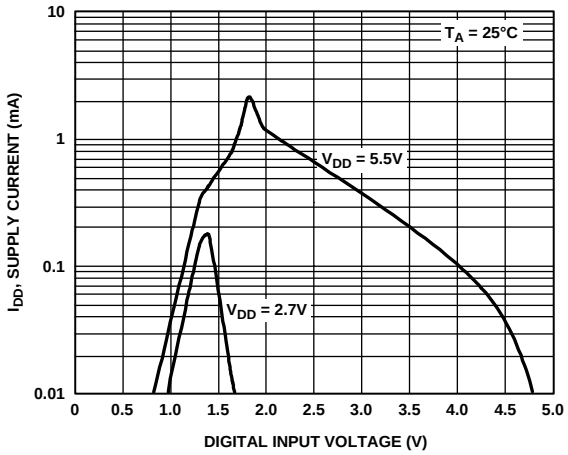

Figure 21. Supply Current vs. Digital Input Voltage

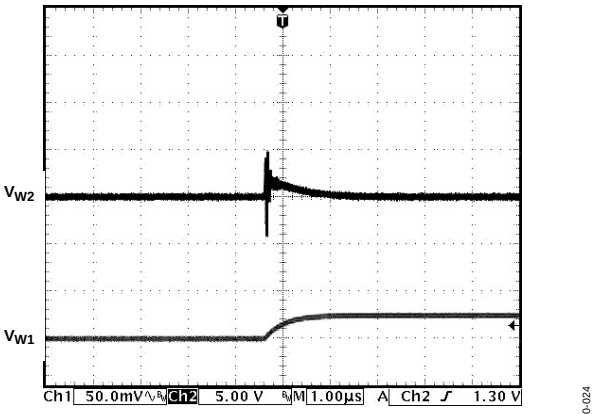

Figure 24. Analog Crosstalk

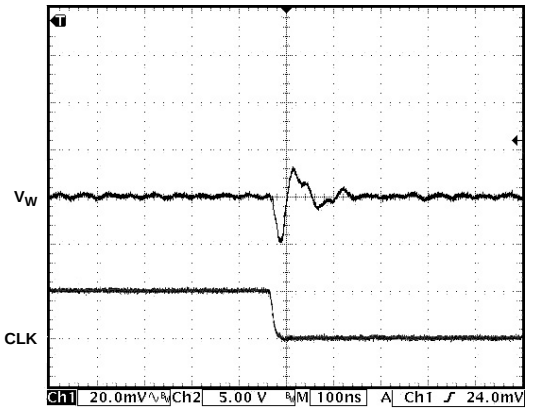

Figure 22. Digital Feedthrough

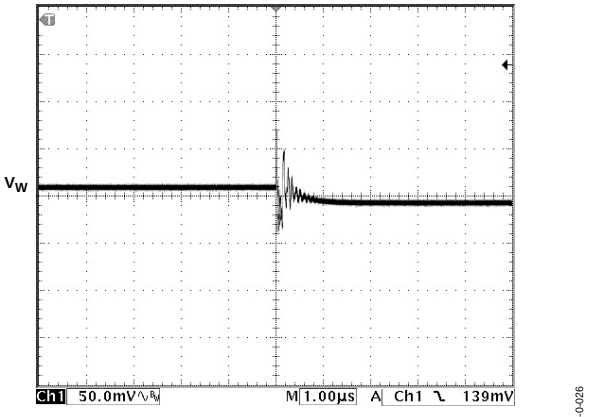

Figure 25. Midscale Glitch, Code 0x80 to Code 0x7F

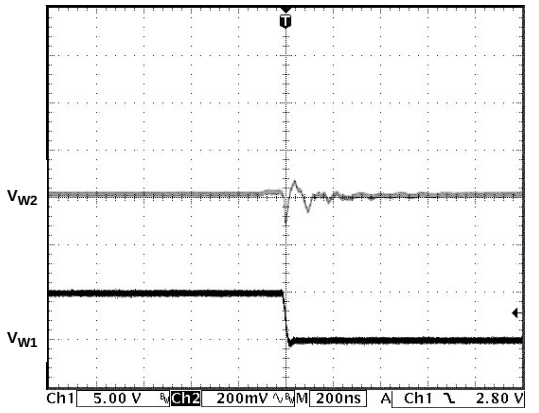

Figure 23. Digital Crosstalk

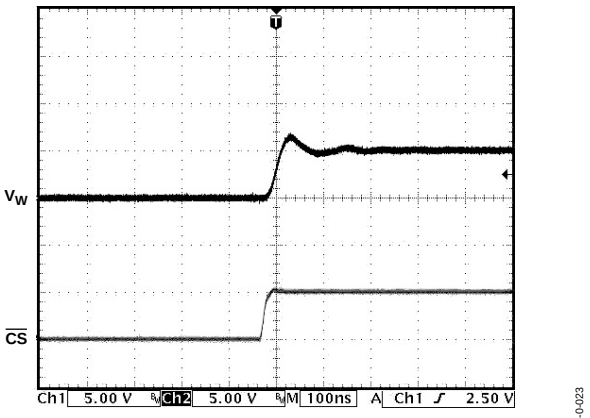

Figure 26. Large-Signal Settling Time

TEST CIRCUITS

Figure 27 through Figure 32 illustrate the test circuits that define the test conditions used in the product specification tables (see Table 1 and Table 2).

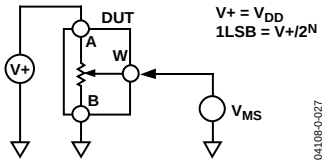

Figure 27. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

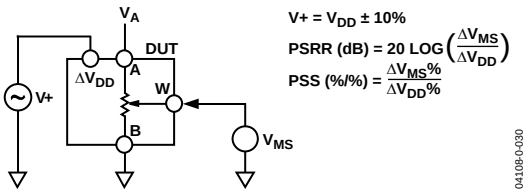

Figure 30. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

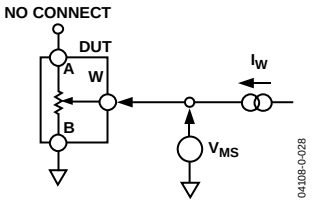

Figure 28. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

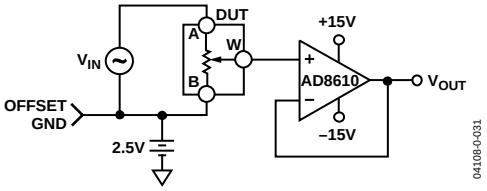

Figure 31. Test Circuit for Gain vs. Frequency

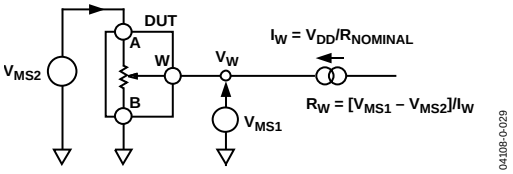

Figure 29. Test Circuit for Wiper Resistance

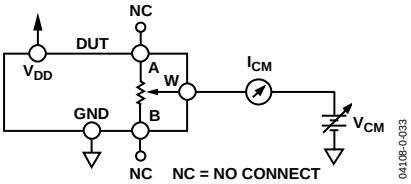

Figure 32. Test Circuit for Common-Mode Leakage Current

THEORY OF OPERATION

The AD5162 is a 256-position, digitally controlled variable resistor (VR) device.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal and the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

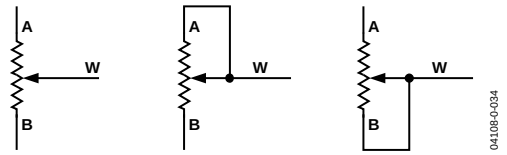

Figure 33. Rheostat Mode Configuration

Assuming that a 10 kΩ part is used, the first connection of the wiper starts at the B terminal for Data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between Terminal W and Terminal B. The second connection is the first tap point, which corresponds to 139 Ω (R_{WB} = R_{AB}/256 + 2 × R_W = 39 Ω + 2 × 50 Ω) for Data 0x01. The third connection is the next tap point, representing 178 Ω (2 × 39 Ω + 2 × 50 Ω) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100 Ω (R_{AB} + 2 × R_W).

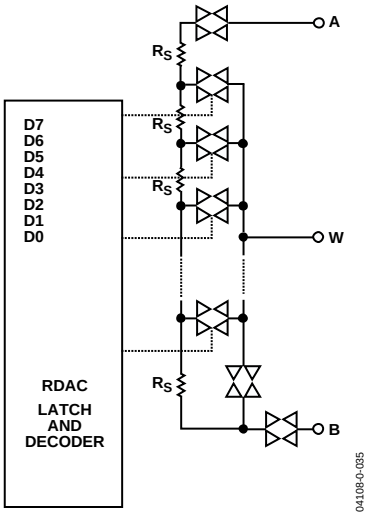

Figure 34. AD5162 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} is 10 kΩ and the A terminal is open circuited, the output resistance, R_{WB}, is set according to the RDAC latch codes, as listed in Table 6.

Table 6. Codes and Corresponding R_{WB} Resistance

D (Dec)	R_{WB} (Ω)	Output State
255	9961	Full scale (R_{AB} − 1 LSB + R_W)
128	5060	Midscale
1	139	1 LSB
0	100	Zero scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of 100 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact may occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

When R_{AB} is 10 kΩ and the B terminal is open circuited, the output resistance, R_{WA}, is set according to the RDAC latch codes, as listed in Table 7.

Table 7. Codes and Corresponding R_{WA} Resistance

D (Dec)	R_{WA} (Ω)	Output State
255	139	Full scale
128	5060	Midscale
1	9961	1 LSB
0	10,060	Zero scale

Typical device-to-device matching is process-lot dependent and may vary by up to ±30%. Because the resistance element is processed in thin-film technology, the change in R_{AB} with temperature has a very low temperature coefficient of 35 ppm/°C.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A, proportional to the input voltage at A to B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

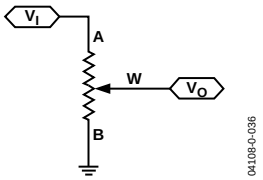

Figure 35. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper to B, starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across the A and B terminals divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256-D}{256}V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, V_W, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Unlike in the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB}, not on the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

ESD PROTECTION

All digital inputs are protected with a series of input resistors and parallel Zener ESD structures, as shown in Figure 36 and Figure 37. This applies to the SDI, CLK, and $\overline{CS}$ digital input pins.

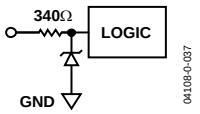

Figure 36. ESD Protection of Digital Pins

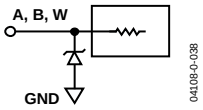

Figure 37. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5162 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on the A, B, and W terminals that exceed V_{DD} or GND are clamped by the internal forward-biased diodes (see Figure 38).

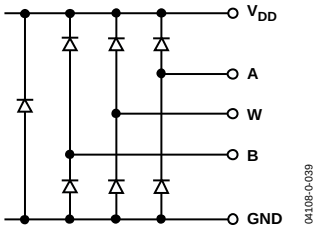

Figure 38. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at the A, B, and W terminals (see Figure 38), it is important to power V_{DD}/GND before applying voltage to the A, B, and W terminals; otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then V_A, V_B, V_W. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important, as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 39). In addition, note that the digital ground should be joined remotely to the analog ground at one point to minimize the ground bounce.

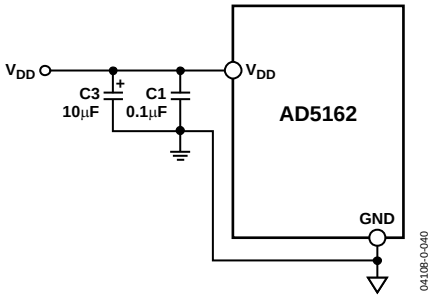

Figure 39. Power Supply Bypassing

CONSTANT BIAS TO RETAIN RESISTANCE SETTING

For users who desire nonvolatility but cannot justify the additional cost of the EEMEM, the AD5162 can be considered a low cost alternative by maintaining a constant bias to retain the wiper setting. The AD5162 is designed specifically for low power applications, allowing low power consumption even in battery-operated systems. The graph in Figure 40 demonstrates the power consumption from a 3.4 V, 450 mAhr Li-Ion cell phone battery connected to the AD5162. The measurement over time shows that the device draws approximately 1.3 µA and consumes negligible power. Over a course of 30 days, the battery is depleted by less than 2%, the majority of which is due to the intrinsic leakage current of the battery itself.

This demonstrates that constantly biasing the potentiometer can be a practical approach. Most portable devices do not require the removal of batteries for the purpose of charging. Although the resistance setting of the AD5162 is lost when the battery needs replacement, such events occur rather infrequently such that this inconvenience is justified by the lower cost and smaller size offered by the AD5162. If total power is lost, the user should be provided with a means to adjust the setting accordingly.

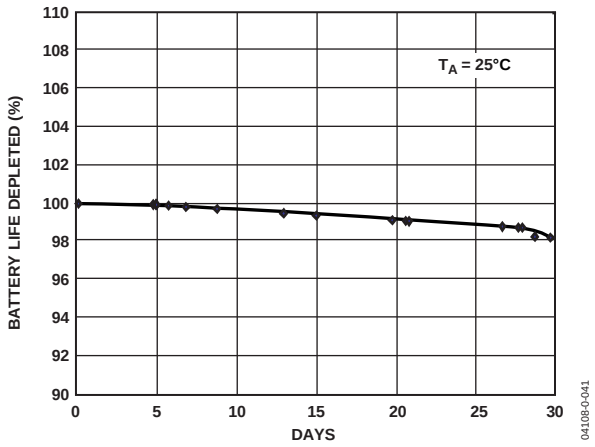

Figure 40. Battery Operating Life Depletion

EVALUATION BOARD

An evaluation board, along with all necessary software, is available to program the AD5162 from any PC running Windows® 98/2000/XP. The graphical user interface, as shown in Figure 41, is straightforward and easy to use. More detailed information is available in the user manual, which is supplied with the board.

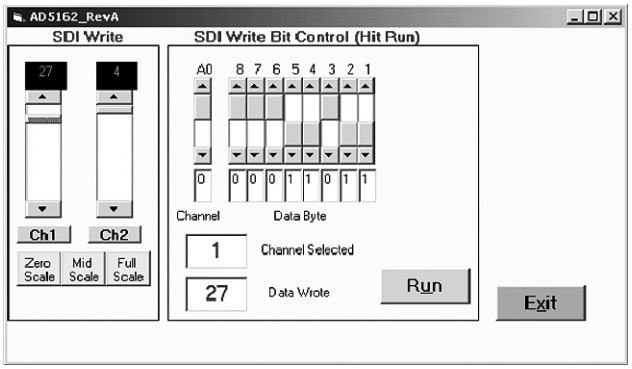

Figure 41. AD5162 Evaluation Board Software

The AD5162 starts at midscale upon power-up. To increment or decrement the resistance, simply move the scrollbars in the left of the software window (see Figure 41). To write a specific value, use the bit pattern in the upper part of the **SDI Write Bit Control (Hit Run)** box and then click **Run**. The format of writing data to the device is shown in Table 8.

SPI INTERFACE

SPI-COMPATIBLE, 3-WIRE SERIAL BUS

The AD5162 contains a 3-wire, SPI-compatible digital interface (SDI, $\overline{CS}$, and CLK). The 9-bit serial word must be loaded MSB first. The format of the word is shown in Table 8.

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or another suitable means. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (see Figure 42).

The data setup and data hold times in Table 3 determine the valid timing requirements. The AD5162 uses a 9-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

Table 8. Serial Data-Word Format[1]

MSB								LSB
B8	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A0 (2^8)	D7 (2^7)	D6	D5	D4	D3	D2	D1	D0 (2^0)

[1] The values of bits are shown in parentheses.

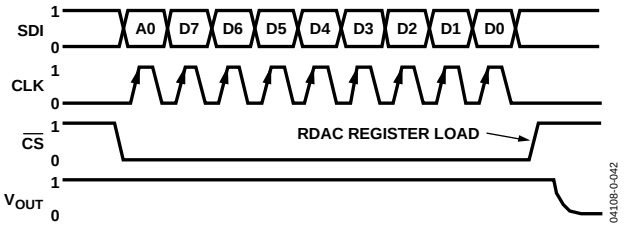

Figure 42. SPI Interface Timing Diagram (V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

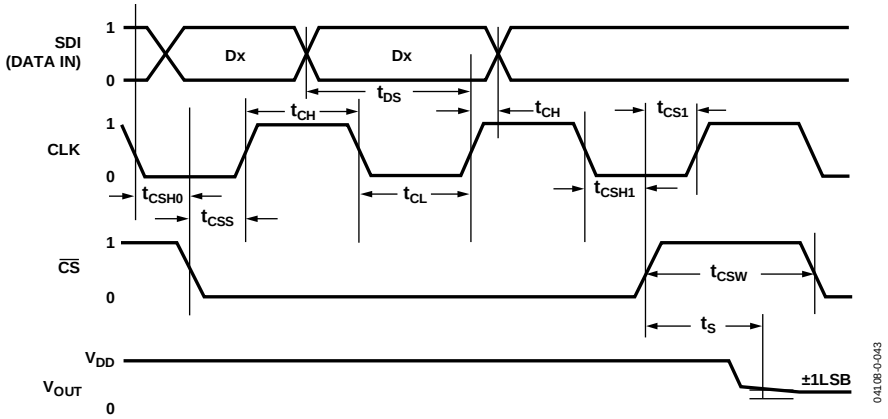

Figure 43. SPI Interface Detailed Timing Diagram (V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

OUTLINE DIMENSIONS

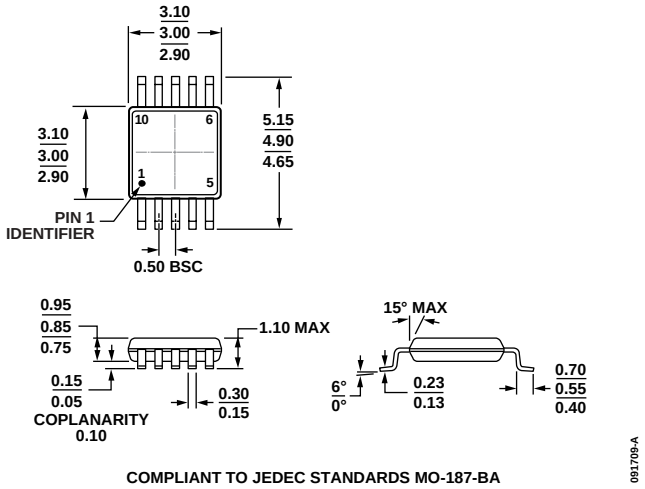

Figure 44. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	R_{AB} (kΩ)	Temperature	Package Description	Package Option	Branding
AD5162BRM2.5	2.5	–40°C to +125°C	10-Lead MSOP	RM-10	D0Q
AD5162BRM2.5-RL7	2.5	–40°C to +125°C	10-Lead MSOP	RM-10	D0Q
AD5162BRM10	10	–40°C to +125°C	10-Lead MSOP	RM-10	D0R
AD5162BRM50	50	–40°C to +125°C	10-Lead MSOP	RM-10	D0S
AD5162BRM50-RL7	50	–40°C to +125°C	10-Lead MSOP	RM-10	D0S
AD5162BRM100	100	–40°C to +125°C	10-Lead MSOP	RM-10	D0T
AD5162BRM100-RL7	100	–40°C to +125°C	10-Lead MSOP	RM-10	D0T
AD5162BRMZ2.5	2.5	–40°C to +125°C	10-Lead MSOP	RM-10	D74
AD5162BRMZ2.5-RL7	2.5	–40°C to +125°C	10-Lead MSOP	RM-10	D74
AD5162BRMZ10	10	–40°C to +125°C	10-Lead MSOP	RM-10	D9K
AD5162BRMZ10-RL7	10	–40°C to +125°C	10-Lead MSOP	RM-10	D9K
AD5162BRMZ50	50	–40°C to +125°C	10-Lead MSOP	RM-10	D0S#
AD5162BRMZ50-RL7	50	–40°C to +125°C	10-Lead MSOP	RM-10	D0S#
AD5162BRMZ100	100	–40°C to +125°C	10-Lead MSOP	RM-10	D0T#
AD5162BRMZ100-RL7	100	–40°C to +125°C	10-Lead MSOP	RM-10	D0T#
AD5162WBRMZ100-RL7	100	–40°C to +125°C	10-Lead MSOP	RM-10	D0T#
AD5162EVAL			Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] The evaluation board is shipped with the 10 k Ω R_{AB} resistor option; however, the board is compatible with all available resistor value options.

AUTOMOTIVE PRODUCTS

The AD5162W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

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