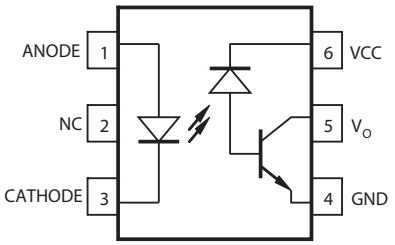
Functional Diagram

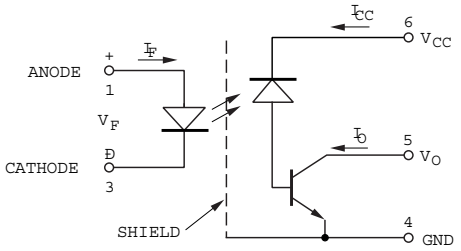


TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

A 0.1 µF bypass capacitor between pins 4 and 6 is recommended.

Schematic



Ordering Information

ACPL-P454 and ACPL-W454 are UL Recognized with 3750V_{RMS} (5000V_{RMS} under ACPL-W454) for 1 minute per UL1577 and are approved under CSA Component Accep tance Notice #5, File CA 88324.

Part Number	Option RoHS Compliant	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-P454 ACPL-W454	-000E	Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P454-560E to order product of Stretched SO-6 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

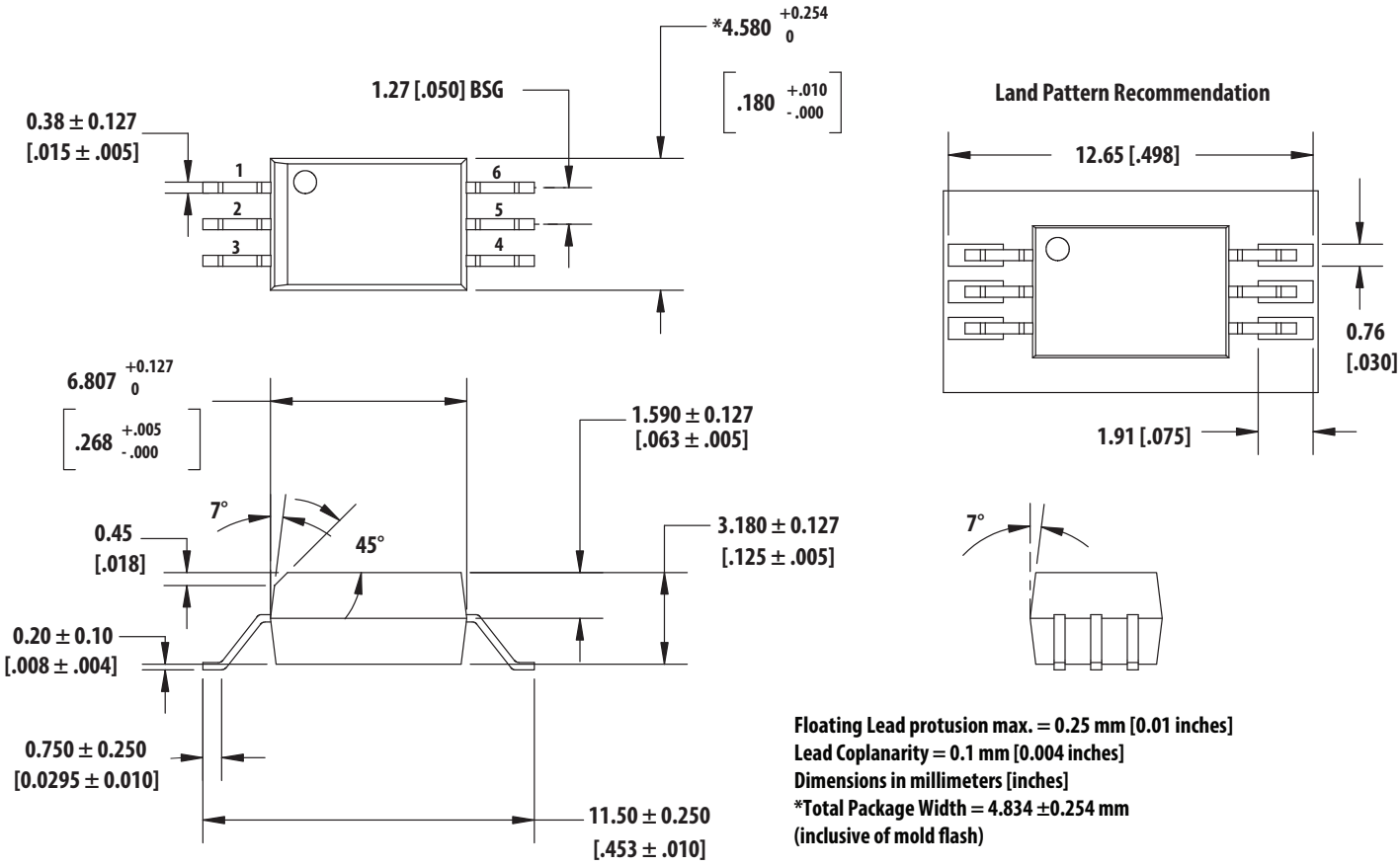
Example 2:

ACPL-P454-000E to order product of Stretched SO-6 package in tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

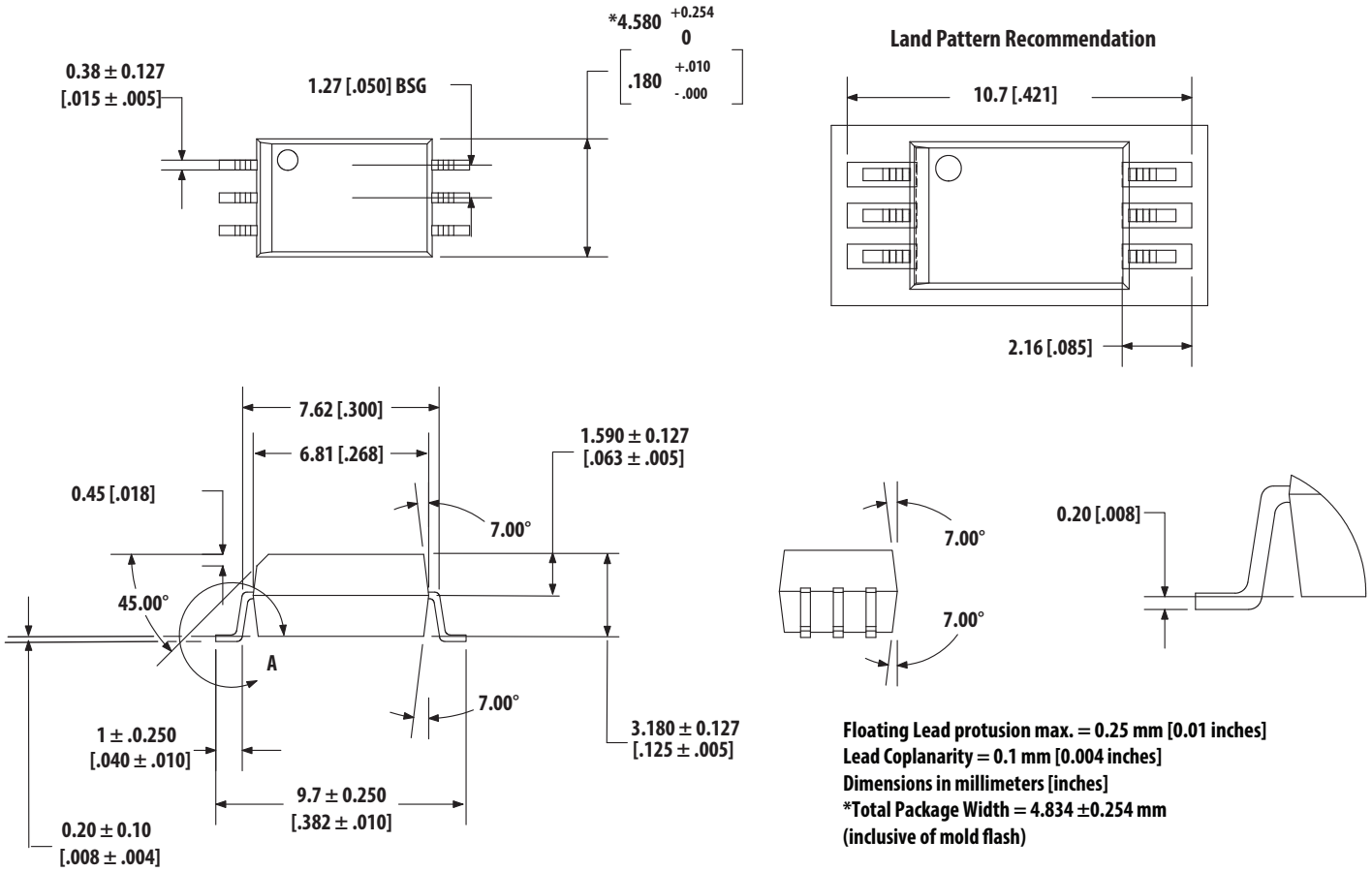
Package Outline Drawings

ACPL-W454 (Stretched SO-6, 8 mm Clearance)



Floating Lead protusion max. = 0.25 mm [0.01 inches]
Lead Coplanarity = 0.1 mm [0.004 inches]
Dimensions in millimeters [inches]
*Total Package Width = 4.834 ±0.254 mm
(inclusive of mold flash)

ACPL-P454 (Stretched SO-6, 7 mm Clearance)



Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Use non-halide flux.

Regulatory Information

The ACPL-W454/P454 are approved by the following organizations:

- **IEC/EN/DIN EN 60747-5-5 (Option 060 only)**
- **UL** – Approval under UL 1577, component recognition program up to V_{ISO} = 3750V_{RMS} (5000V_{RMS} for ACPL-W454). File E55361.
- **CSA** – Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation Related Specifications

Parameter	Symbol	ACPL-W454	ACPL-P454	Units	Conditions
Min External Air Gap (Clearance)	L(IO1)	8	7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	8	8	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa	—	—	Material Group DIN VDE 0109

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	ACPL-P454 Option 060	ACPL-W454 Option 060	Unit
Installation classification per DIN VDE 0110/39, Table 1				
for rated mains voltage ≤ 150V_{RMS}		I-IV	I-IV	
for rated mains voltage ≤ 300V_{RMS}		I-IV	I-IV	
for rated mains voltage ≤ 600V_{RMS}		I-III	I-III	
for rated mains voltage ≤1000V_{RMS}			I-III	
Climatic Classification		55/85/21	55/85/21	—
Pollution Degree (DIN VDE 0110/39)		2	2	—
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{peak}
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1671	2137	V_{peak}
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1426	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting values - maximum values allowed in the event of a failure.				
Case Temperature	T_S	175	175	°C
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at TS, V_{IO} = 500V	R_S	$\geq 10^9$	$\geq 10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

Absolute Maximum Ratings

Parameter	Value
Storage Temperature	–55°C to +125°C
Operating Temperature	–55°C to +100°C
Average Input Current – I_F	25 mA[a]
Peak Input Current – I_F	50 mA[b] (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F	1.0A (≤ 1 ms pulse width, 300 pps)
Reverse Input Voltage – V_R (Pin 3-1)	5V
Input Power Dissipation	45 mW[c]
Average Output Current – I_O (Pin 5)	8 mA
Peak Output Current	16 mA
Output Voltage – V_O (Pin 5-4)	–0.5V to +20V
Supply Voltage – V_{CC} (Pin 6-4)	–0.5V to +30V
Output Power Dissipation	100 mW[d]
Solder Reflow Temperature Profile	See Package Outline Drawings section

a. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
b. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
c. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
d. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.

DC Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.[a]	Max.	Unit	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	25	32	60	%	T_A = 25°C	V_O = 0.4V	I_F = 16 mA, V_{CC} = 4.5V	1, 2, 4	b
		21	34	—		—	V_O = 0.5V			
Current Transfer Ratio	CTR	26	35	65	%	T_A = 25°C	V_O = 0.4V	I_F = 12 mA, V_{CC} = 4.5V		b
		22	37	—		—	V_O = 0.5V			
Logic Low Output Voltage	V_{OL}	—	0.2	0.4	V	T_A = 25°C	I_O = 3.0 mA	I_F = 16 mA, V_{CC} = 4.5V	1	
			0.2	0.5		—	I_O = 2.4 mA			
Logic High Output Current	I_{OH}	—	0.003	0.5	µA	T_A = 25°C	V_O = V_{CC}= 5.5V	I_F = 0 mA	5	
			0.01	1		T_A = 25°C	V_O = V_{CC} = 15.0V			
			—	50		—				
Logic Low Supply Current	I_{CCL}	—	50	200	µA	I_F = 16 mA,	V_{CC} = 15V	V_O = Open		c
Logic High Supply Current	I_{CCH}	—	0.02	1	µA	T_A = 25°C	I_F = 0 mA, V_O = Open	V_{CC} = 15V		c
			0.02	2		—				
Input Forward Voltage	V_F	—	1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
			1.5	1.8		—				
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 10A				
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, V_F = 0				

a. All typicals at T_A = 25°C.

b. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O), to the forward LED input current (I_F), times 100.

c. Use of a 0.1 µF bypass capacitor connected between pins 4 and 6 is recommended.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified

Parameter	Symbol	Min.	Typ.[a]	Max.	Unit	Test Conditions		Fig.	Notes
Propagation Delay Time to Logic Low at Output	t_{PHL}	—	0.2	0.3	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10% I_F = 16 mA, V_{CC} = 5.0V R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V	6, 8, 9	b
		—	0.2	0.5		—			
		0.2	0.5	0.7		T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50% I_F = 12 mA, $_{VCC}$ = 15.0V R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5V	6, 10–14	c
		0.1	0.5	1.0		—			
Propagation Delay Time to Logic High at Output	t_{PLH}	—	0.3	0.5	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10% I_F = 16 mA, V_{CC} = 5.0V R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V	6, 8, 9	b
		—	0.3	0.7		—			
		0.3	0.8	1.1		T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50% I_F = 12 mA, V_{CC} = 15.0V R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 2.0V	6, 10–14	c
		0.2	0.8	1.4		—			
Propagation Delay Difference Between Any 2 Parts	$t_{PLH} - t_{PHL}$	–0.4	+0.3	+0.9	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50% I_F = 12 mA, V_{CC} = 15.0V R_L = 20 kΩ, C_L = 100 pF V_{THHL} = 1.5V, V_{THLH} = 2.0V	6, 10–14	d
		–0.7	+0.3	+1.3	µs	—			
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	15	30	—	kV/s	T_A = 25°C	V_{CC} = 5.0V, R_L = 1.9 kΩ C_L = 15 pF, I_F = 0 mA, V_{CM} = 1500 V_{P-P}	7	b, e
		15	30	—		T_A = 25°C	V_{CC} = 15.0V, R_L = 20 kΩ C_L = 100 pF, I_F = 0 mA V_{CM} = 1500 V_{P-P}	7	c, f
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	15	30	—	kV/µs	T_A = 25°C	V_{CC} = 5.0V, R_L = 1.9 kΩ C_L = 15 pF, I_F = 16 mA V_{CM} = 1500 V_{P-P}	7	b, e
		15	30	—		T_A = 25°C	V_{CC} = 15.0V, R_L = 20 kΩ C_L = 100 pF, I_F = 12 mA V_{CM} = 1500 V_{P-P}	7	c, f
		15	30	—		T_A = 25°C	V_{CC} = 15.0V, R_L = 20 kΩ C_L = 100 pF, I_F = 16 mA V_{CM} = 1500 V_{P-P}	7	c, f

a. All typicals at T_A = 25°C.

b. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.

c. The RL = 20 kΩ, C_L = 100 pF load represents an IPM (Intelligent Power Mode) load.

d. The difference between t_{PLH} and t_{PHL}, between any two ACPL-W454/P454 parts under the same test condition. (See Power Inverter Dead Time and Propagation Delay Specifications section).

e. Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (that is, V_O > 2.0V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (that is, V_O < 0.8V).

f. Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (that is, V_O > 3.0V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state that is, V_O < 1.0V).

Package Characteristics

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	3750	—	—	Vrms	RH ≤ 50%, t = 1 min, T_A = 25°C		b, c
		5000 (For "ACPL-W454)						
Input-Output Resistance	R_{I-O}	—	10^{12}	—	Ω	V_{I-O} = 500V_{DC}		b
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz; V_{I-O} = 0V_{DC}		b

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable).

b. Device considered a two-terminal device: Pins 1 and 3 shorted together and Pins 4, 5, and 6 shorted together.

c. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA); each optocoupler under ACPL-W454 is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).

Figure 1 DC and Pulsed Transfer Characteristics

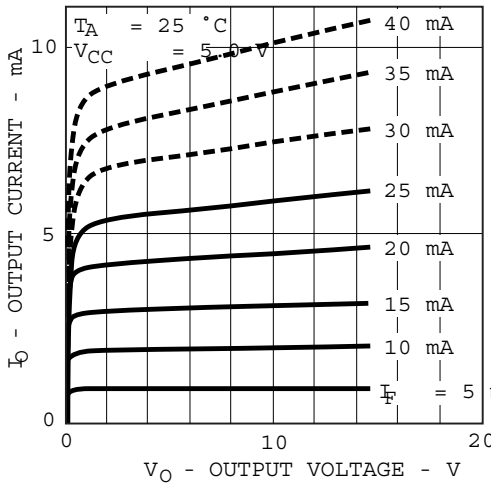


Figure 2 Current Transfer Ratio vs. Input Current

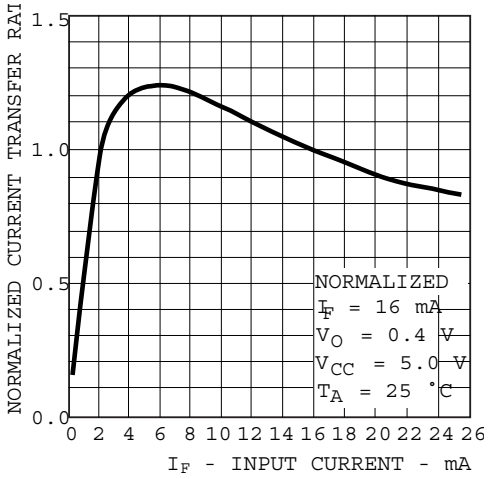


Figure 3 Input Current vs. Forward Voltage

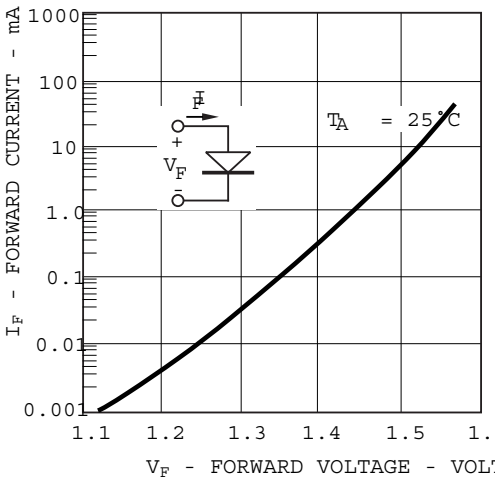


Figure 4 Current Transfer Ratio vs. Temperature

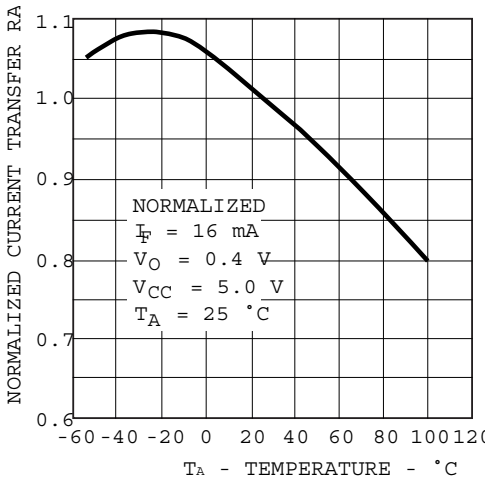


Figure 5 Logic High Output Current vs. Temperature

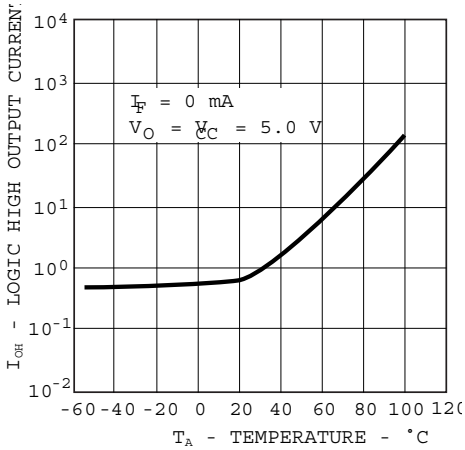


Figure 6 Switching Test Circuit

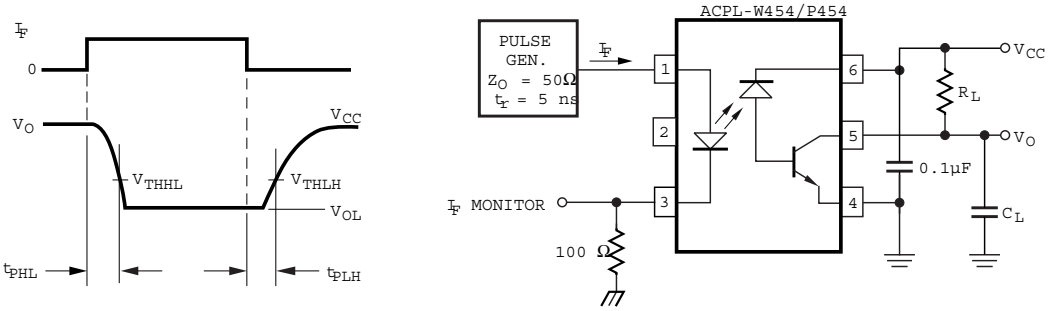


Figure 7 Test Circuit for Transient Immunity and Typical Waveforms

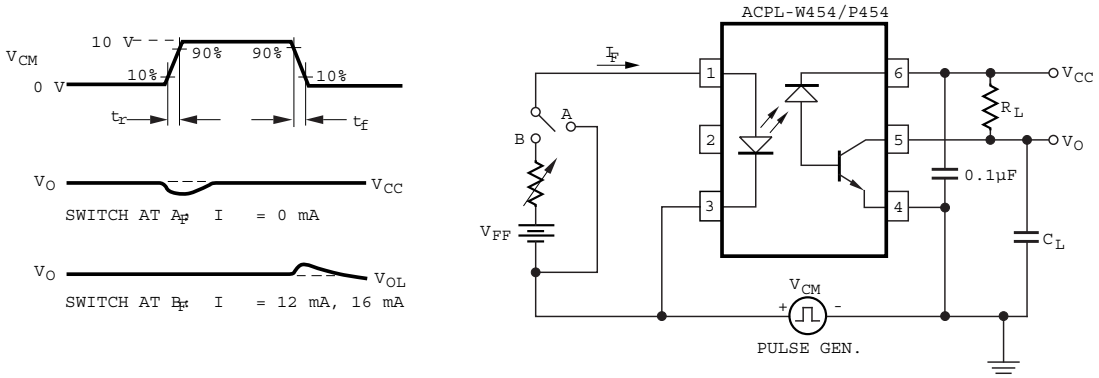


Figure 8 Propagation Delay Time vs. Temperature

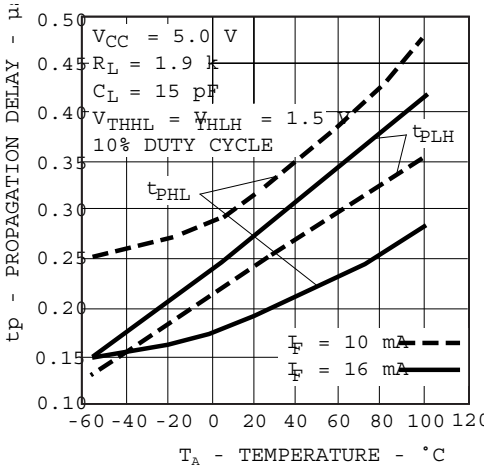


Figure 9 Propagation Delay Time vs. Load Resistance

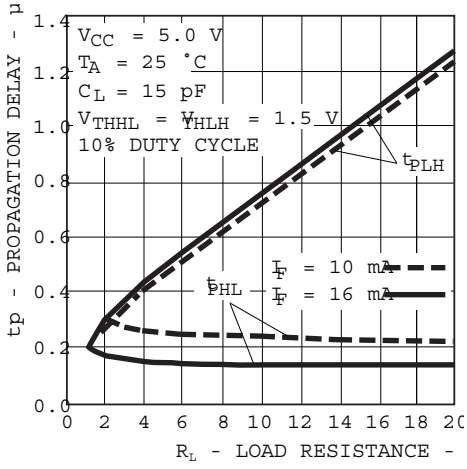


Figure 10 Propagation Delay Time vs. Load Resistance

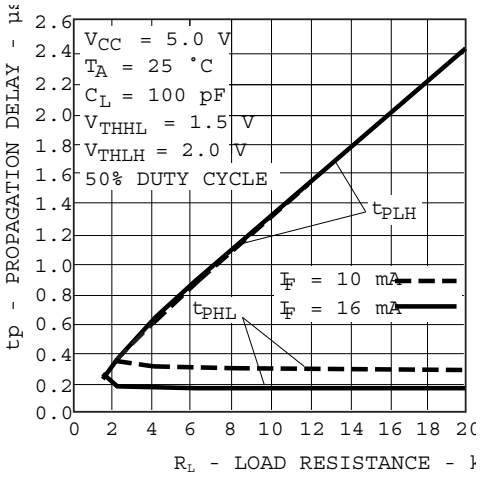


Figure 11 Propagation Delay Time vs. Temperature

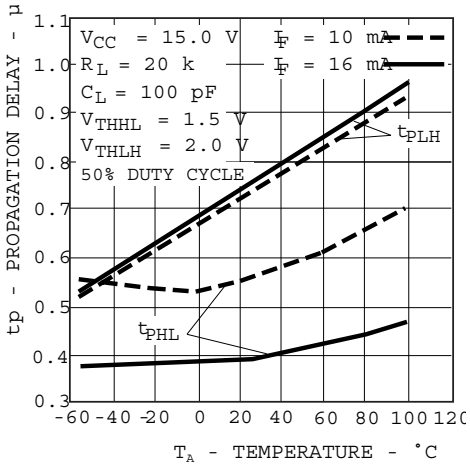


Figure 12 Propagation Delay Time vs. Load Resistance

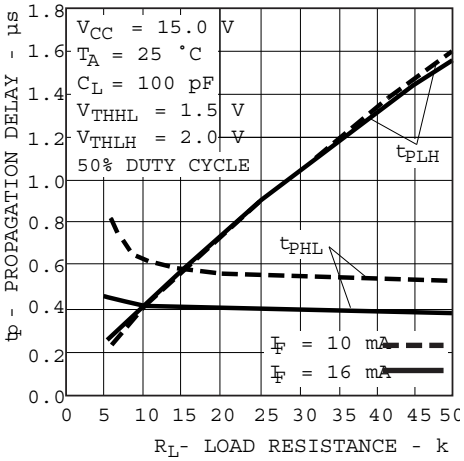


Figure 13 Propagation Delay Time vs. Load Capacitance

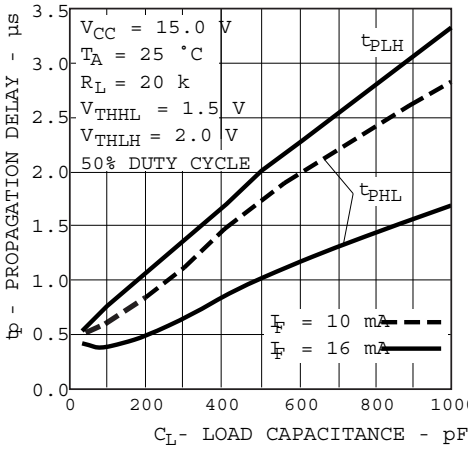
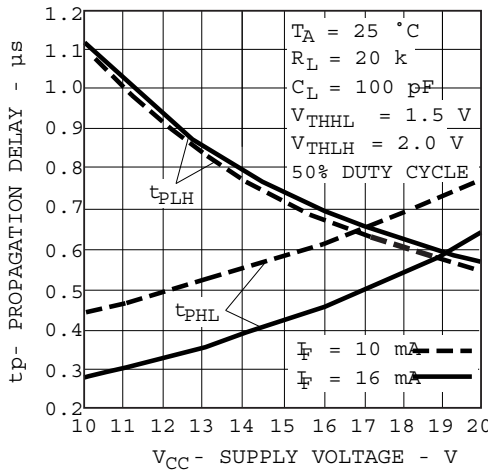


Figure 14 Propagation Delay Time vs. Supply Voltage



For product information and a complete list of distributors, please go to our web site: www.broadcom.com

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