Table 1. Pin Description

Pin No.	Symbol	Description
1	V_{DD1}	Supply voltage for input side (4.5 V to 5.5 V), relative to GND1
2	V_{IN+}	Positive input (± 200 mV recommended)
3	V_{IN-}	Negative input (normally connected to GND1)
4	GND1	Input side ground
5	GND2	Output side ground
6	V_{OUT-}	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Supply voltage for output side (3 V to 5.5 V), relative to GND2

Table 2. Ordering Information

ACPL-C79B/C79A/C790 is UL recognized with 5000 Vrms/1 minute rating per UL 1577.

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-C79B	-000E	Stretched SO-8	X		X	80 per tube
ACPL-C79A ACPL-C790	-500E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

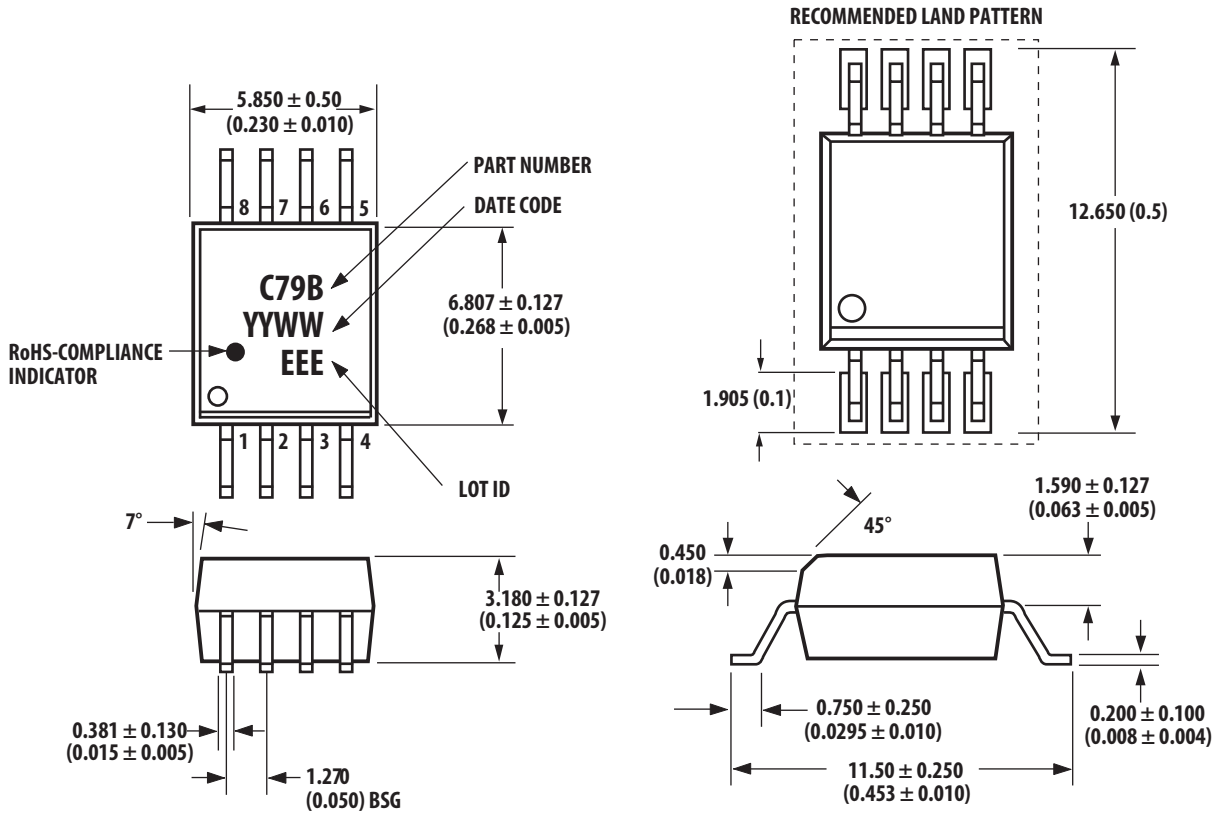
Example:

ACPL-C79B-500E to order product of Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliance.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

Stretched SO-8 Package (SSO-8)



Dimensions in millimeters and (inches).
Lead coplanarity = 0.1 mm (0.004 inches).

Figure 2. SSO-8 package.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-C79B/C79A/C790 is approved by the following organizations:

IEC/EN/DIN EN 60747-5-5

Approved with Maximum Working Insulation Voltage V_{IORM} = 1414 Vpeak.

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 5000 Vrms/1min. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 3. Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (External Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 4. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics [1]

Description	Symbol	Value	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 Vrms		I-IV	
for rated mains voltage ≤ 300 Vrms		I-IV	
for rated mains voltage ≤ 450 V rms		I-IV	
for rated mains voltage ≤ 600 Vrms		I-IV	
for rated mains voltage ≤ 1000 Vrms		I-III	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	Vpeak
Input to Output Test Voltage, Method b V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	Vpeak
Input to Output Test Voltage, Method a V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	2262	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	8000	Vpeak
Safety-limiting values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current [2]	$I_{S,INPUT}$	230	mA
Output Power [2]	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

Notes:
1. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.
2. Safety-limiting parameters are dependent on ambient temperature. The Input Current, $I_{S,INPUT}$, derates linearly above 25°C free-air temperature at a rate of 2.53 mA/°C; the Output Power, $P_{S,OUTPUT}$, derates linearly above 25°C free-air temperature at a rate of 4 mW/°C.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	+125	°C
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD1}, V_{DD2}	–0.5	6.0	V
Steady-State Input Voltage [1, 3]	V_{IN+}, $V_{IN–}$	–2	V_{DD1} + 0.5	V
Two-Second Transient Input Voltage [2]	V_{IN+}, $V_{IN–}$	–6	V_{DD1} + 0.5	V
Output Voltages	V_{OUT+}, $V_{OUT–}$	–0.5	V_{DD2} + 0.5	V
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane			

Notes:
1. DC voltage of up to –2 V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.
2. Transient voltage of 2 seconds up to –6 V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.
3. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+105	°C
VDD1 Supply Voltage	V_{DD1}	4.5	5.5	V
VDD2 Supply Voltage	V_{DD2}	3	5.5	V
Input Voltage Range [1]	V_{IN+}, $V_{IN–}$	–200	+200	mV

Notes:
1. ±200 mV is the nominal input range. Full scale input range (FSR) is ±300 mV. Functional input range is ±2 V.

Table 7. Electrical Specifications

Unless otherwise noted, T_A = –40°C to +105°C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, V_{IN}+ = –200 mV to +200 mV, and V_{IN}– = 0 V (single-ended connection).

Parameter		Symbol	Min.	Typ.[1]	Max.	Unit	Test Conditions/Notes	Fig.
DC CHARACTERISTICS								
Input Offset Voltage		V_{OS}	–1	0.4	2	mV	T_A = 25°C	3, 4
Magnitude of Input Offset Change vs. Temperature		$\lvert dV_{OS}/dT_A \rvert$		-0.8	4	µV/°C	T_A = –40°C to +105°C; absolute value	5
Gain (ACPL-C79B, ±0.5%)		G0	8.16	8.2	8.24	V/V	T_A = 25°C; Note 2	6, 7
Gain (ACPL-C79A, ±1%)		G1	8.12	8.2	8.28	V/V	T_A = 25°C; Note 2	6, 7
Gain (ACPL-C790, ±3%)		G3	7.95	8.2	8.44	V/V	T_A = 25°C; Note 2	6, 7
Magnitude of Gain Change vs. Temperature		dG/dT_A		–0.00041		V/V/°C	T_A = –40°C to +105°C; Note 3	8
Nonlinearity over ±200 mV Input Voltage		NL_{200}		0.05	0.13	%	V_{IN+} = –200 mV to +200 mV, T_A = 25°C; Note 2	9, 10
Magnitude of NL_{200} Change vs. Temperature		dNL_{200}/dT_A		0.0003		%/°C	T_A = –40°C to +105°C	11
Nonlinearity over ±100 mV Input Voltage		NL_{100}		0.013	0.06	%	V_{IN+} = –100 mV to +100 mV, T_A = 25°C; Note 2	9, 10, 11
INPUTS AND OUTPUTS								
Full-Scale Differential Voltage Input Range		FSR		±300		mV	$V_{IN} = V_{IN+} - V_{IN–}$; Note 4	12
Input Bias Current		I_{IN+}	–1	–0.1		µA	V_{IN+} = 0 V, $V_{IN–}$ = 0 V; Note 5	13
Magnitude of I_{IN+} Change vs. Temperature		dI_{IN+}/dT_A		–0.05		nA/°C		
Equivalent Input Impedance		R_{IN}		27		kΩ	V_{IN+} or $V_{IN–}$, single-ended	14
Output Common-Mode Voltage		V_{OCM}		1.23		V	V_{OUT+} or $V_{OUT–}$; Note 6	
Output Voltage Range		OVR		0 to 2.5		V	V_{OUT+} or $V_{OUT–}$; Note 4	12
Output Short-Circuit Current		$\lvert I_{OSC} \rvert$		11		mA	V_{OUT+} or $V_{OUT–}$, shorted to GND2 or V_{DD2}	
Output Resistance		R_{OUT}		21		Ω	V_{OUT+} or $V_{OUT–}$	
Input DC Common-Mode Rejection Ratio		$CMRR_{IN}$		76		dB	Note 2	
AC CHARACTERISTICS								
Signal-to-Noise Ratio		SNR		62		dB	V_{IN+} = 300 mVpp 10 kHz sine wave; Note 7	15, 16
Signal-to-(Noise + Distortion) Ratio		SNDR		59		dB	V_{IN+} = 300 mVpp 10 kHz sine wave; Note 8	15, 16
Small-Signal Bandwidth (-3 dB)		$f_{–3\ dB}$	140	200		kHz		17, 18
Input to Output Propagation Delay	10%-10%	t_{PD10}		1.6	2.3	µs	200 mV/µs step input	19
	50%-50%	t_{PD50}		2	2.6	µs	200 mV/µs step input	19
	90%-90%	t_{PD90}		2.6	3.3	µs	200 mV/µs step input	19
Output Rise/Fall Time (10%-90%)		$t_{R/F}$		1.7		µs	Step input	19
Common Mode Transient Immunity		CMTI	10	15		kV/µs	V_{CM} = 1 kV, T_A = 25°C; Note 2	
Power Supply Rejection		PSR		–78		dB	1 Vpp 1 kHz sine wave ripple on V_{DD1}, differential output; Note 9	
POWER SUPPLIES								
Input Side Supply Current		I_{DD1}		11	18.5	mA	V_{IN+} = 400 mV; see Note 10	20
Output Side Supply Current		I_{DD2}		7	12	mA	5 V supply	20
				6.8	11	mA	3.3 V supply	20

Notes:
1. All Typical values are under Typical Operating Conditions at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V.
2. See Definitions section.
3. Gain temperature drift can be normalized and expressed as Temperature Coefficient of Gain (TCG) of –50 ppm/°C.
4. When FSR is exceeded, outputs saturate.
5. Because of the switched-capacitor nature of the input sigma-delta converter, time-averaged values are shown.
6. Under Typical Operating Conditions, part-to-part variation ±0.04 V.
7. Under Typical Operating Conditions, part-to-part variation ±1 dB.
8. Under Typical Operating Conditions, part-to-part variation ±1 dB.
9. Ripple voltage applied to V_{DD1} with a 0.1 µF bypass capacitor connected; differential amplitude of the ripple outputs measured. See Definitions section.
10. The input supply current decreases as the differential input voltage (V_{IN}+ – V_{IN}–) decreases.

Table 8. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			Vrms	RH < 50%, t = 1 min., T_A = 25°C	1, 2
Resistance (Input-Output)	R_{I-O}		$>10^{12}$		Ω	V_{I-O} = 500 V_{DC}	3
Capacitance (Input-Output)	C_{I-O}		0.5		pF	f = 1 MHz	3

Notes:
1. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
2. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 insulation characteristics table and your equipment level safety specification.
3. This is a two-terminal measurement: pins 1–4 are shorted together and pins 5–8 are shorted together.

Typical Performance Plots

Unless otherwise noted, T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V.

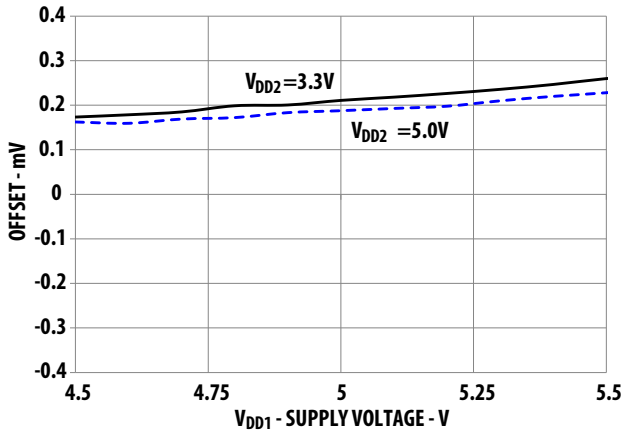


Figure 3. Input offset vs. supply V_{DD1}.

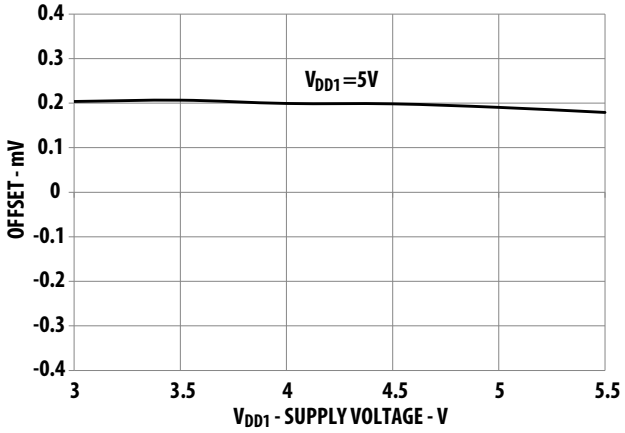


Figure 4. Input offset vs. supply V_{DD2}.

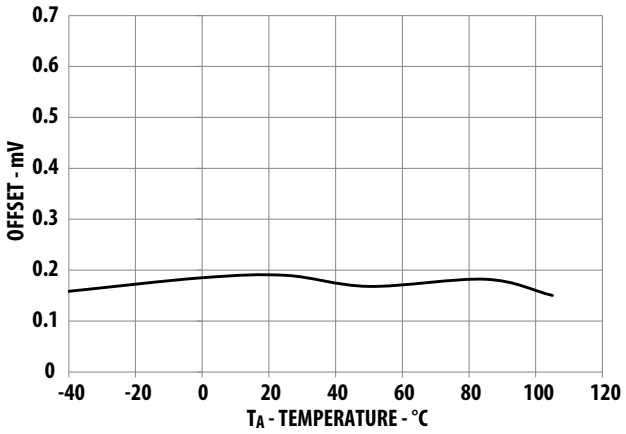


Figure 5. Input offset vs. temperature.

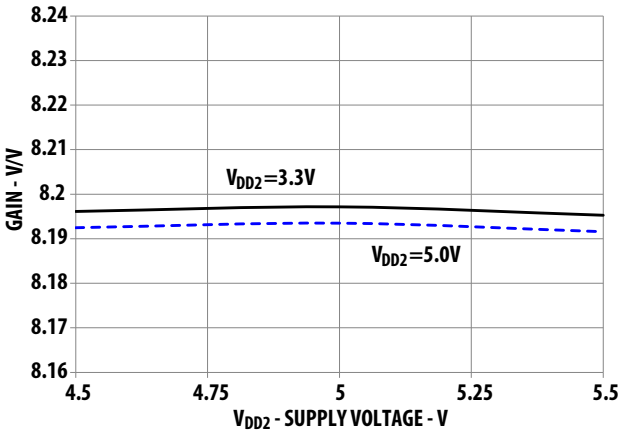


Figure 6. Gain vs. supply V_{DD1}.

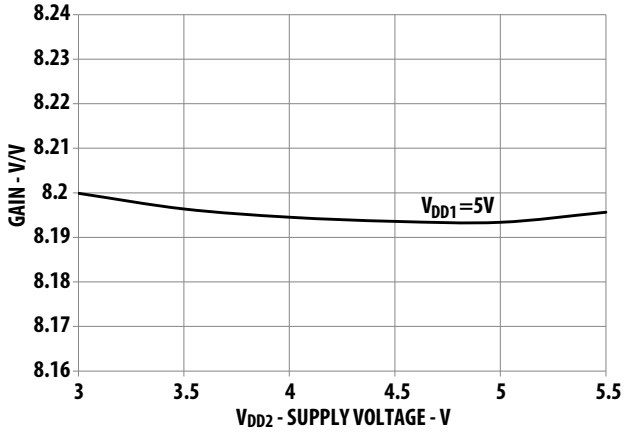


Figure 7. Gain vs. supply V_{DD2}.

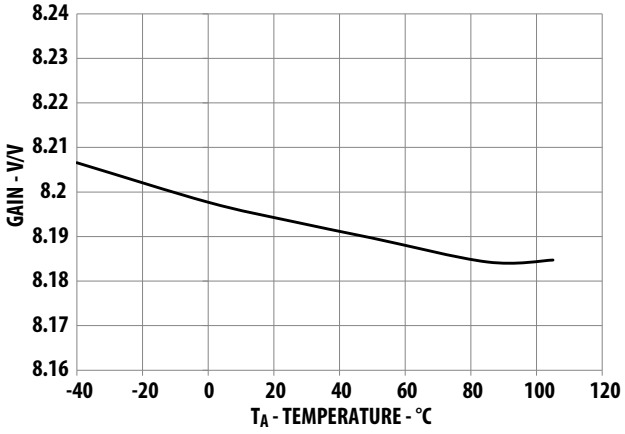


Figure 8. Gain vs. temperature.

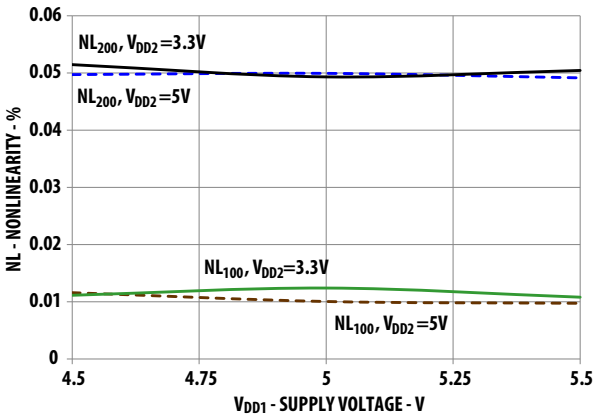


Figure 9. Nonlinearity vs. supply V_{DD1}.

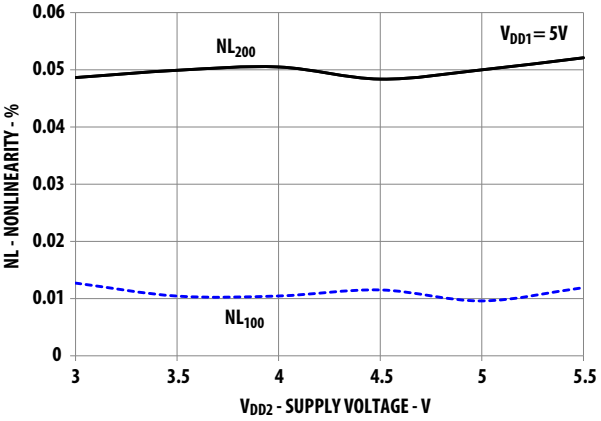


Figure 10. Nonlinearity vs. supply V_{DD2}.

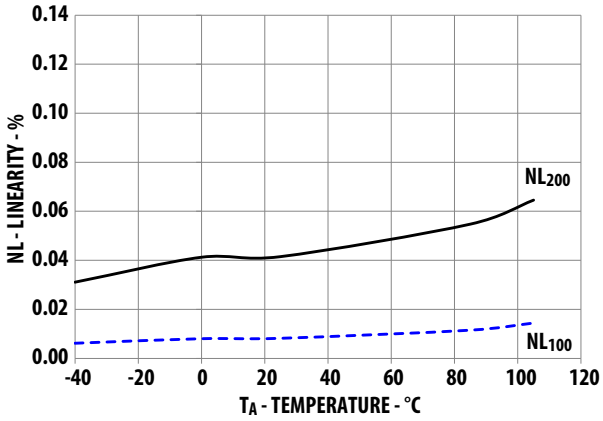


Figure 11. Nonlinearity vs. temperature.

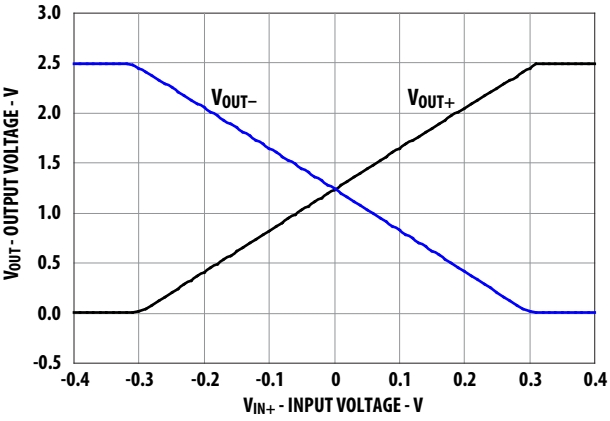


Figure 12. Output voltage vs. input voltage.

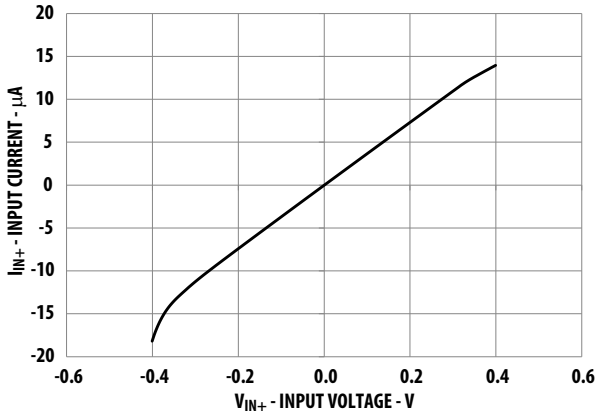


Figure 13. Input current vs. input voltage.

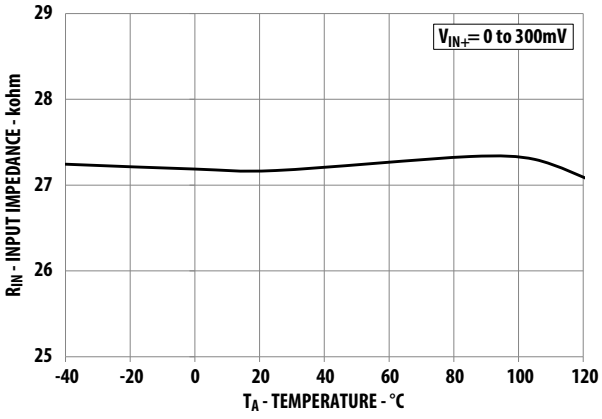


Figure 14. Input impedance vs. temperature.

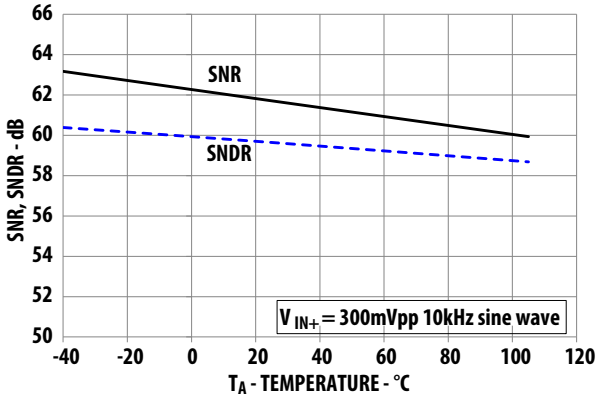


Figure 15. SNR, SNDR vs. temperature.

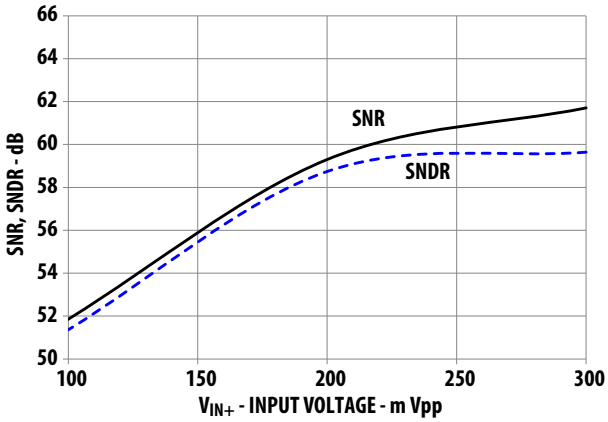


Figure 16. SNR, SNDR vs. input voltage.

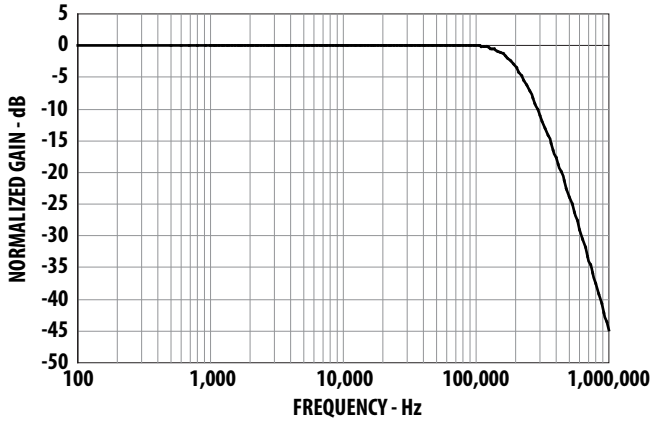


Figure 17. Gain frequency response.

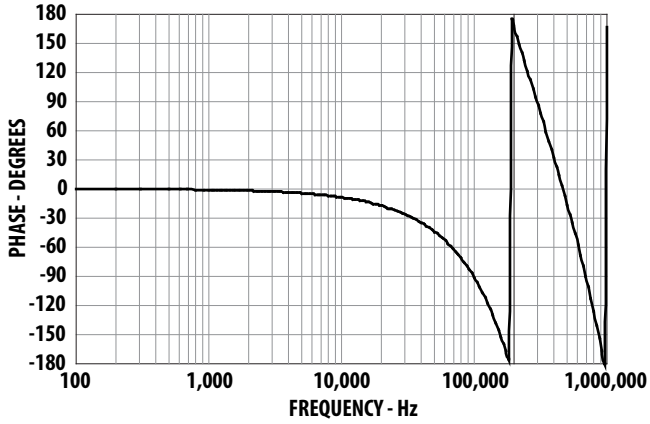


Figure 18. Phase frequency response.

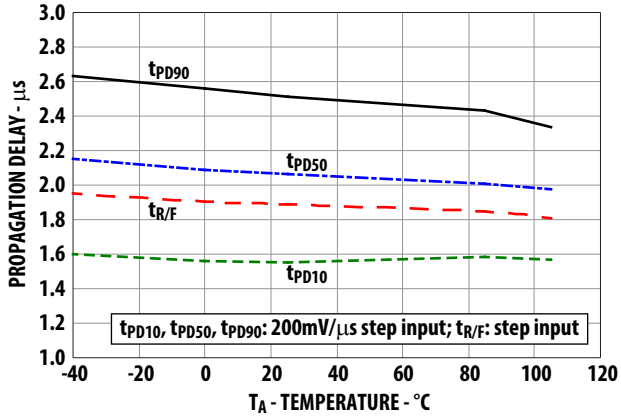


Figure 19. Propagation delay, output rise/fall time vs. temperature.

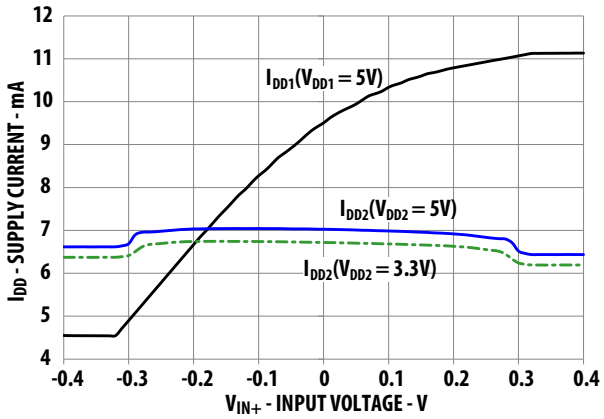


Figure 20. Supply current vs. input voltage.

Definitions

Gain

Gain is defined as the slope of the best-fit line of differential output voltage ($V_{OUT}+ - V_{OUT}-$) vs. differential input voltage ($V_{IN}+ - V_{IN}-$) over the nominal input range, with offset error adjusted out.

Nonlinearity

Nonlinearity is defined as half of the peak-to-peak output deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.

Input DC Common Mode Rejection Ratio, $CMRR_{IN}$

$CMRR_{IN}$ is defined as the ratio of the differential signal gain (signal applied differentially between pins $V_{OUT}+$ and $V_{OUT}-$) to the input side common-mode gain (input pins tied together and the signal applied to both inputs with respect to pin GND1), expressed in dB.

Common Mode Transient Immunity, CMTI, also known as Common Mode Rejection

CMTI is tested by applying an exponentially rising/falling voltage step on pin 4 (GND1) with respect to pin 5 (GND2). The rise time of the test waveform is set to approximately 50 ns. The amplitude of the step is adjusted until the differential output ($V_{OUT}+ - V_{OUT}-$) exhibits more than a 200 mV deviation from the average output voltage for more than 1μs. The ACPL-C79B/C79A/C790 will continue to function if more than 10 kV/μs common mode slopes are applied, as long as the breakdown voltage limitations are observed.

Power Supply Rejection, PSR

PSR is the ratio of differential amplitude of the ripple outputs over power supply ripple voltage, referred to the input, expressed in dB.

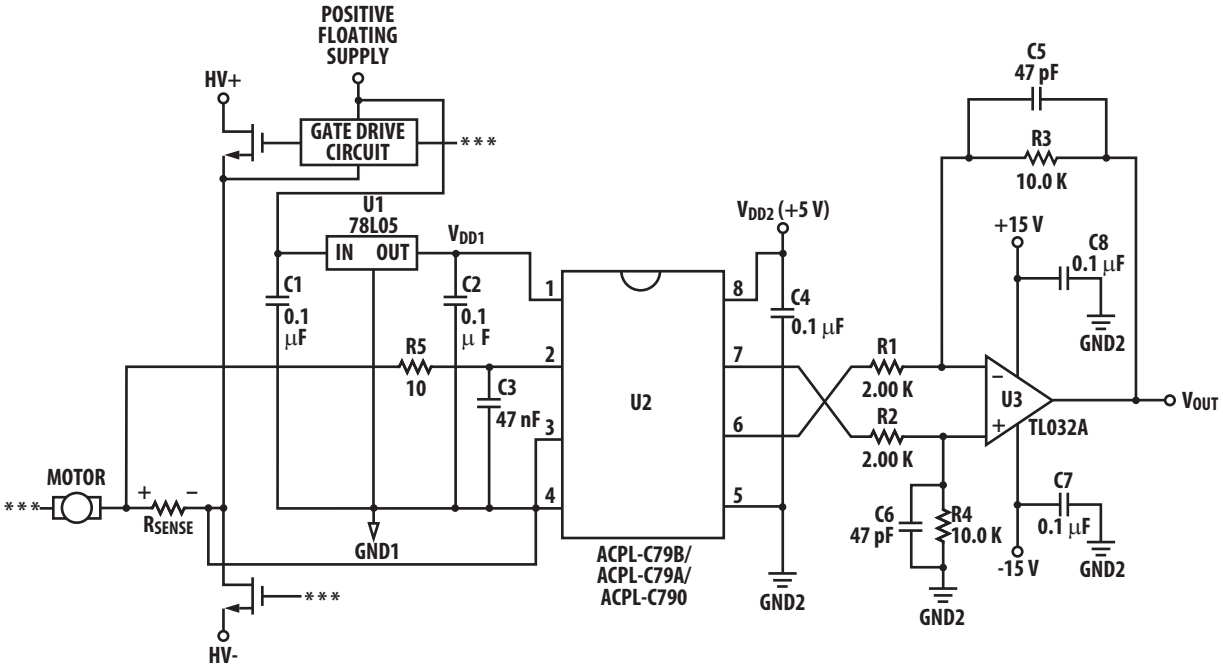


Figure 21. Typical application circuit for motor phase current sensing.

Application Information

Application Circuit

The typical application circuit is shown in Figure 21. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator (U1). The voltage from the current sensing resistor, or shunt (R_{SENSE}), is applied to the input of the ACPL-C79B/C79A/C790 through an RC anti-aliasing filter (R5 and C3). And finally, the differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit (U3 and associated components). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

Power Supplies and Bypassing

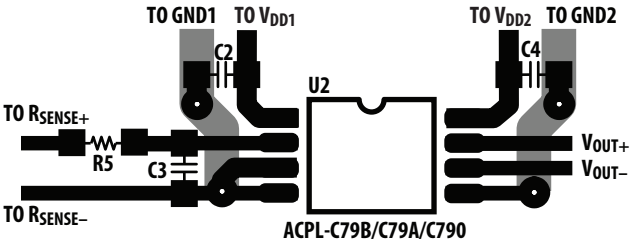
As mentioned above, an inexpensive 78L05 three-terminal regulator can be used to reduce the gate-drive power supply voltage to 5 V. To help attenuate high frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

The power supply for the isolation amplifier is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

As shown in Figure 21, 0.1 µF bypass capacitors (C2, C4) should be located as close as possible to the pins of the isolation amplifier. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. A 47 nF bypass capacitor (C3) is also recommended at the input pins due to the switched-capacitor nature of the input circuit. The input bypass capacitor also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal. The input filter also performs an important reliability function – it reduces transient spikes from ESD events flowing through the current sensing resistor.

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. In addition, the layout of the PCB can also affect the isolation transient immunity (CMTI) of the ACPL-C79B/C79A/C790, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMTI performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the ACPL-C79B/C79A/C790. Figure 22 shows an example PCB layout.



Note: Drawing not to scale

Figure 22. Example printed circuit board layout.

Shunt Resistor Selection

The current sensing resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistance decreases power dissipation, while larger sense resistance can improve circuit accuracy by utilizing the full input range of the ACPL-C79B/C79A/C790.

The first step in selecting a sense resistor is determining how much current the resistor will be sensing. The graph in Figure 23 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the sense resistor is determined by the current being measured and the maximum recommended input voltage of the isolation amplifier. The maximum sense resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the sense resistor should see during normal operation. For example, if a motor will have a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (=10 x 1.414 x 1.5). Assuming a maximum input voltage of 200 mV, the maximum value of sense resistance in this case would be about 10 mΩ.

The maximum average power dissipation in the sense resistor can also be easily calculated by multiplying the sense resistance times the square of the maximum RMS current, which is about 1 W in the previous example. If the power dissipation in the sense resistor is too high, the resistance can be decreased below the maximum value to decrease power dissipation. The minimum value of the sense resistor is limited by precision and accuracy requirements of the design. As the resistance value is reduced, the output voltage across the resistor is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the sense resistor will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the sense resistor, the temperature coefficient (tempco) of the resistor can introduce nonlinearity due to the signal dependent temperature rise of the resistor. The effect increases as the resistor-to-ambient thermal resistance increases. This effect can be minimized by reducing the thermal resistance of the current sensing resistor or by using a resistor with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the current sensing resistor on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

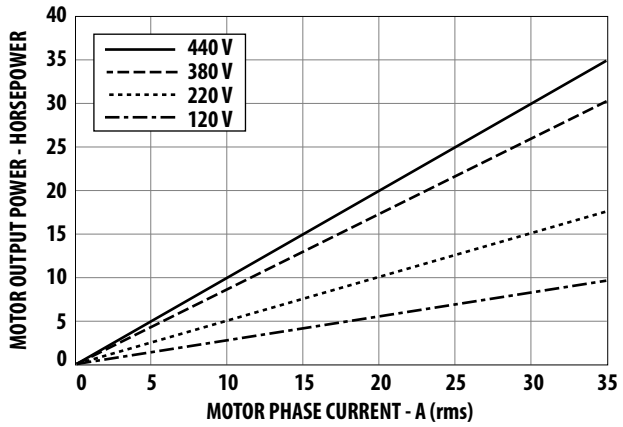


Figure 23. Motor output horsepower vs. motor phase current and supply voltage.

For a two-terminal current sensing resistor, as the value of resistance decreases, the resistance of the leads become a significant percentage of the total resistance. This has two primary effects on resistor accuracy. First, the effective resistance of the sense resistor can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the leads during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material, such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco overall.

Both of these effects are eliminated when a four-terminal current sensing resistor is used. A four-terminal resistor has two additional terminals that are Kelvin connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

When laying out a PC board for the current sensing resistors, a couple of points should be kept in mind. The Kelvin connections to the resistor should be brought together under the body of the resistor and then run very close to each other to the input of the ACPL-C79B/C79A/C790; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the sense resistor is not located on the same PC board as the isolation amplifier circuit, a tightly twisted pair of wires can accomplish the same thing.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the sense resistor to help distribute the current between the layers of the PC board. The PC board should use 2 or 4 oz. copper for the layers, resulting in a current carrying capacity in excess of 20 A. Making the current carrying traces on the PC board fairly large can also improve the sense resistor's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

Shunt Resistor Connections

The typical method for connecting the ACPL-C79B/C79A/C790 to the current sensing resistor is shown in Figure 21. V_{IN}+ (pin 2) is connected to the positive terminal of the sense resistor, while V_{IN}– (pin 3) is shorted to GND1 (pin 4), with the power-supply return path functioning as the sense line to the negative terminal of the current sense resistor. This allows a single pair of wires or PC board traces to connect the isolation amplifier circuit to the sense resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the resistor are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current sensing resistor.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the ACPL-C79B/C79A/C790 to the sense resistor be the **only** return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the ACPL-C79B/C79A/C790 circuit and the gate drive circuit should be the positive power supply line.

Differential Input Connection

The differential analog inputs of the ACPL-C79B/C79A/C790 are implemented with a fully-differential, switched-capacitor circuit. In the typical application circuit (Figure 21), the isolation amplifier is connected in a single-ended input mode. Given the fully differential input structure, a differential input connection method (balanced input mode as shown in Figure 24) is recommended to achieve better performance. The input currents created by the switching actions on both of the pins are balanced on the filter resistors and cancelled out each other. Any noise induced on one pin will be coupled to the other pin by the capacitor C and creates only common mode noise which is rejected by the device. Typical value for Ra and Rb is 10 Ω and 22 nF for C.

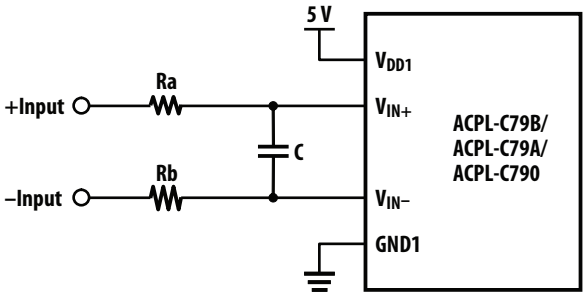


Figure 24. Simplified differential input connection diagram.

Output Side

The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

Voltage Sensing

The ACPL-C79B/C79A/C790 can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (22 kΩ) and input bias current (0.1 μA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 10 Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth.

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