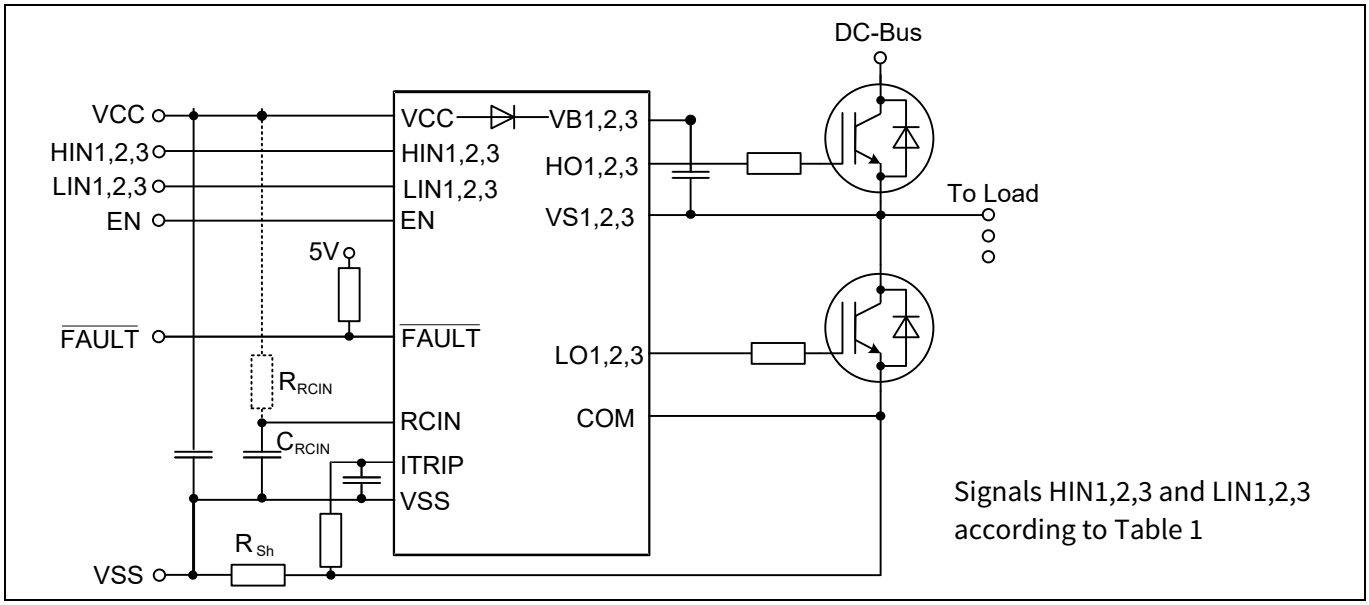

Figure 1 Typical application diagram

Ordering information

Table 1 Members of 6EDL04 family – 2nd generation

Sales Name	High side control input HIN1,2,3 and LIN1,2,3	Target transistor	Typ. UVLO-Thresholds	Bootstrap diode	Package	Evaluation board
6EDL04I06NT	negative logic	IGBT	11.7 V / 9.8 V	Yes	DSO-28	
6EDL04I06PT	positive logic	IGBT	11.7 V / 9.8 V	Yes	DSO-28	EVAL-6EDL04I06PT
6EDL04N06PT	positive logic	MOSFET	9 V / 8.1 V	Yes	DSO-28	
6EDL04N02PR	positive logic	MOSFET	9 V / 8.1 V	Yes	TSSOP-28	EVAL-6EDL04N02PR

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Table of contents

1 Block diagram

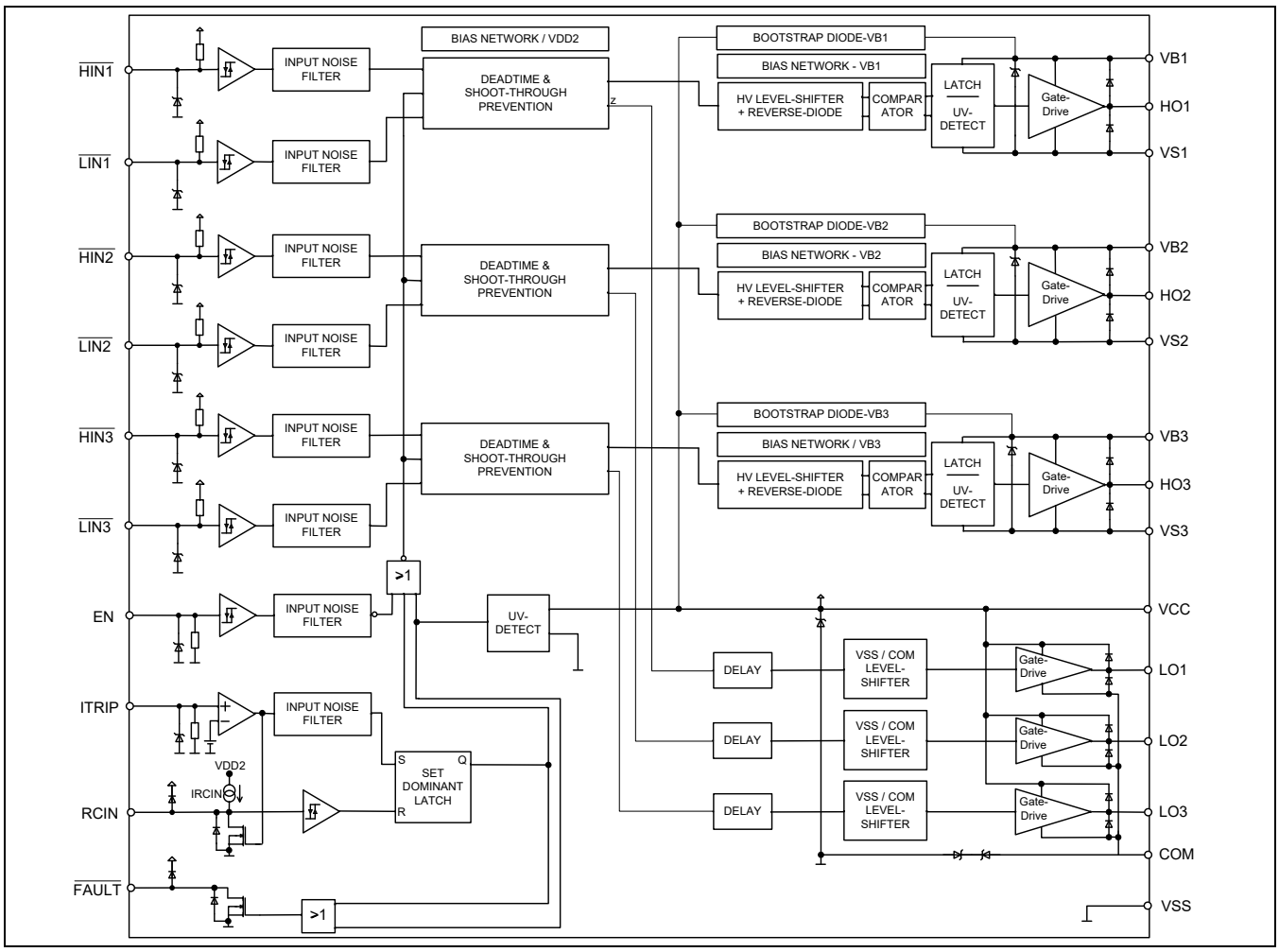


Figure 2 Functional block diagram for 6EDL04I06NT

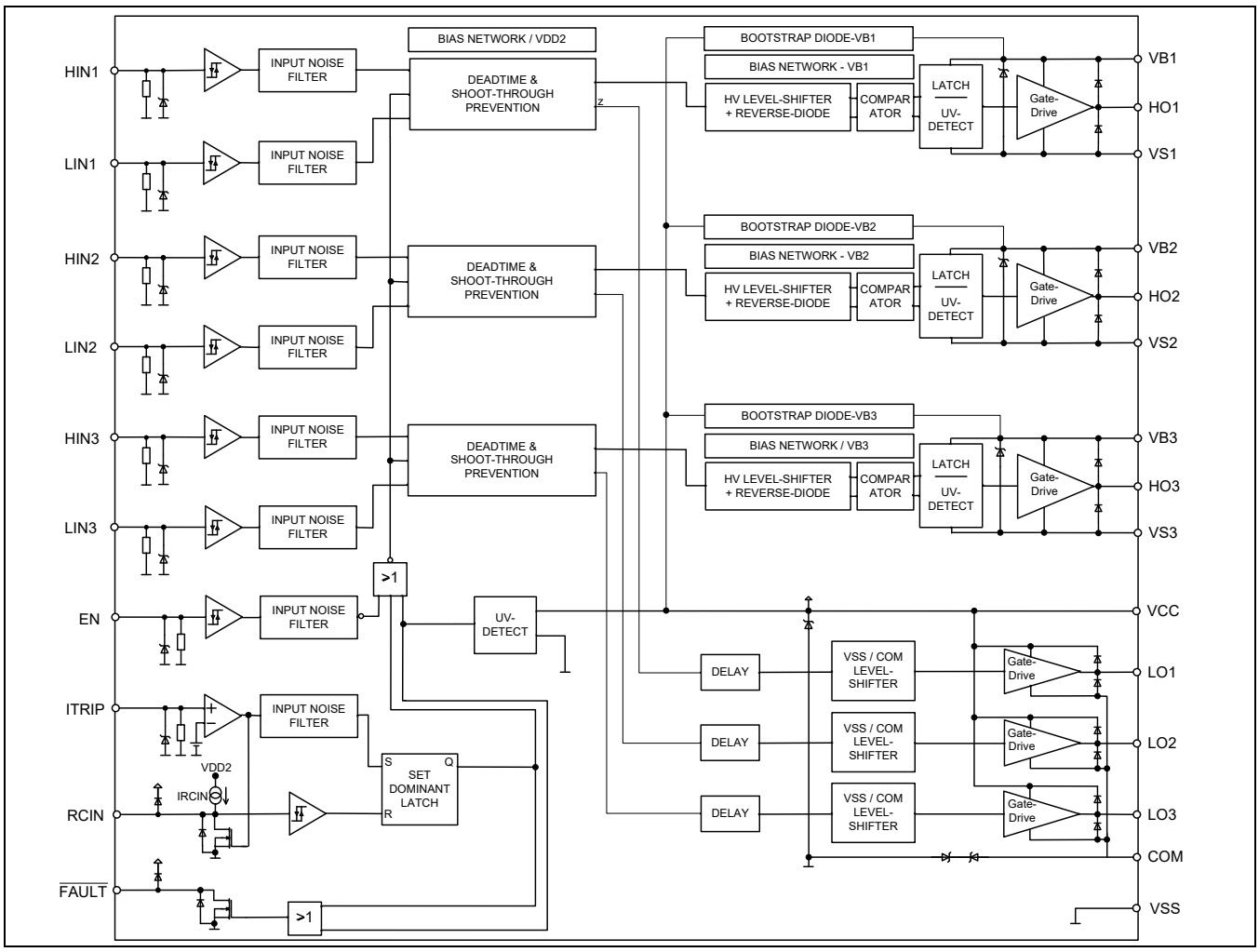


Figure 3 Functional block diagram for 6EDL04I06PT, and 6EDL04N06PT / 6EDL04N02PR

2 Lead definitions

Table 2 6EDL04 family lead definitions

Pin no.	Name	Function
1	VCC	Low side power supply
2,3,4	HIN1,2,3	High side logic input (positive or negative logic according to Table 1)
5,6,7	LIN1,2,3	Low side logic input (positive or negative logic according to Table 1)
8	/FAULT	Indicates over-current and under-voltage (negative logic, open-drain output)
9	ITRIP	Analog input for over-current shut down, activates FAULT and RCIN to VSS
10	EN	Enable I/O functionality (positive logic)
11	RCIN	External RC-network to define FAULT clear delay after FAULT-Signal (T_{FLTCLR})
12	VSS	Logic ground
13	COM	Low side gate driver reference
28,24,20	VB1,2,3	High side positive power supply
27,23,19	HO1,2,3	High side gate driver output
26,22,18	VS1,2,3	High side negative power supply
16,15,14	LO1,2,3	Low side gate driver output

Pin no.	Name	Function
21,25	nc	Not connected

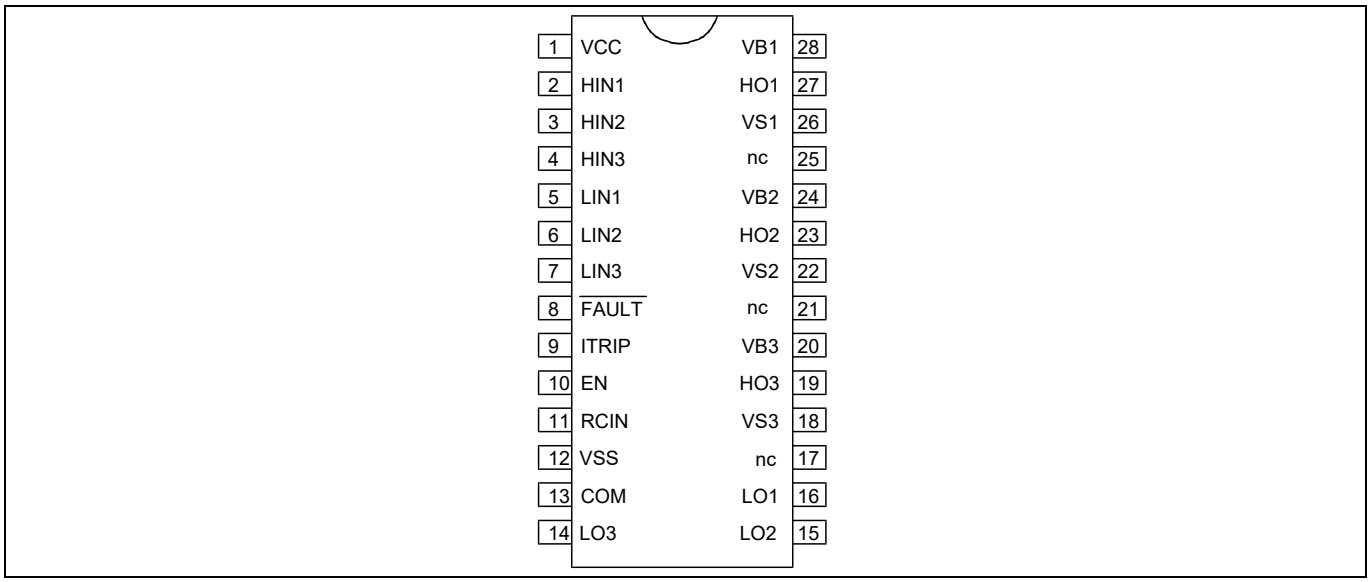


Figure 4 Pin Configuration of 6ED family (signals HIN1,2,3 and LIN1,2,3 according to Table 1)

3 Functional description

3.1 Low Side and High Side Control Pins (Pin 2, 3, 4, 5, 6, 7)

The Schmitt trigger input threshold of them is such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 5 and Figure 6.

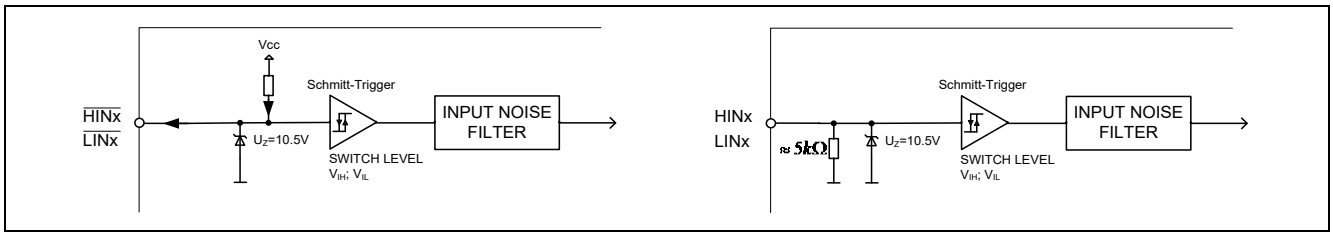


Figure 5 Input pin structure for negative logic (left) and positive logic (right)

An internal pull-up of about 75 kΩ (negative logic) pre-biases the input during supply start-up and a ESD zener clamp is provided for pin protection purposes. The zener diodes are therefore designed for single pulse stress only and not for continuous voltage stress over 10V. For versions with positive, a 5 kΩ pull-down resistor is used for this function.

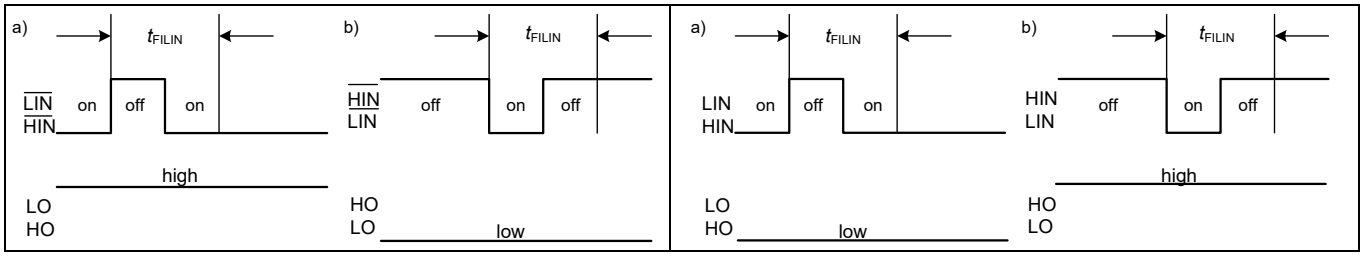


Figure 6 Input filter timing diagram for negative logic (left) and positive logic (right)

It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 1 µs.

The 6ED family – 2nd generation provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two channels of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only one leg output is activated, so that the leg is kept steadily in a safe state.

A minimum dead time insertion of typ. 310 ns is also provided, in order to reduce cross-conduction of the external power switches.

3.2 EN (Gate Driver Enable, Pin 10)

The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. The internal structure of the pin is given in Figure 7. The switching levels of the Schmitt-Trigger are here $V_{EN,TH+}$ = 2.1 V and $V_{EN,TH-}$ = 1.3 V. The typical propagation delay time is t_{EN} = 780 ns. There is an internal pull down resistor (75 kΩ), which keeps the gate outputs off in case of broken PCB connection.

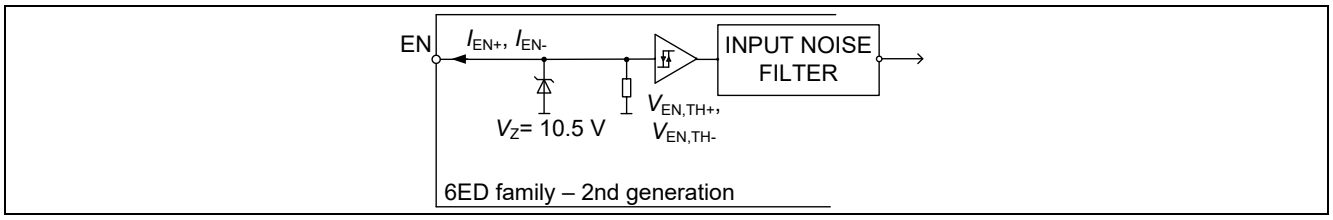


Figure 7 EN pin structures

3.3 /FAULT (Fault Feedback, Pin 8)

/Fault pin is an active low open-drain output indicating the status of the gate driver (see Figure 8). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VCC supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VCC pin description for more details).
- Over-current detection (ITRIP): The fault condition is latched until current trip condition is finished and RCIN input is released (please refer to ITRIP pin).

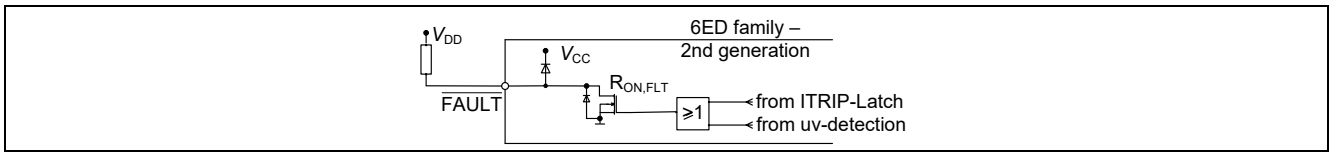


Figure 8 /FAULT pin structures

3.4 ITRIP and RCIN (Over-Current Detection Function, Pin 9, 11)

The 6ED family – 2nd generation provides an over-current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ 0.44 V) is referenced to VSS ground. An input noise filter (typ. $t_{ITRIPMIN}$ = 230 ns) prevents the driver to detect false over-current events.

Over-current detection generates a hard shut down of all outputs of the gate driver and provides a latched fault feedback at /FAULT pin. RCIN input/output pin is used to determine the reset time of the fault condition. As soon as ITRIP threshold is exceeded the external capacitor connected to RCIN is fully discharged. The capacitor is then recharged by the RCIN current generator when the over-current condition is finished. As soon as RCIN

voltage exceeds the rising threshold of typ $V_{RCIN,TH}$ = 5.2 V, the fault condition releases and the driver returns operational following the ontrol input pins according to Section 3.1.

3.5 VCC, VSS and COM (Low Side Supply, Pin 1, 12, 13)

VCC is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit. Output power stage is referenced to COM ground. COM ground is floating respect to VSS ground with a maximum range of operation of +/-5.7 V. A back-to-back zener structure protects grounds from noise spikes.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage higher than V_{CCUV+} is present.

The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below V_{CCUV-} = 9.8 V respectively 8.1 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

3.6 VB1, 2, 3 and VS1, 2, 3 (High Side Supplies, Pin 18, 20, 22, 24, 26, 28)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage. Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VCC.

The device operating area as a function of the supply voltage is given in Figure 15 and Figure 16.

3.7 LO1,2,3 and HO1,2,3 (Low and High Side Outputs, Pin 14, 15, 16, 19, 23, 27)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive of IGBT and MOSFET devices. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are edge triggered by the respective inputs. In particular, after an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after a under voltage condition of the VCC supply, the low side outputs switch to the state of their respective inputs.

4 Electrical parameters

4.1 Absolute maximum ratings

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 3 Absolute maximum ratings

Parameter		Symbol	Min.	Max.	Unit
High side offset voltage[1]	DSO28 TSSOP28	V_S	V_{CC}- V_{BS}-6	600 180	V
High side offset voltage (t_p<500ns)[1]			V_{CC} - V_{BS} – 50	–	
High side offset voltage[1]	DSO28 TSSOP28	V_B	V_{CC} – 6	620 200	
High side offset voltage (t_p<500ns) [1]			V_{CC} – 50	–	
High side floating supply voltage (V_B vs. V_S) (internally clamped)		V_{BS}	-1	20	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	-0.5	V_B + 0.5	
Low side supply voltage (internally clamped)		V_{CC}	-1	20	
Low side supply voltage (V_{CC} vs. V_{COM})		V_{CCOM}	-0.5	25	
Gate driver ground		V_{COM}	-5.7	5.7	
Low side output voltage (V_{LO} vs. V_{COM})		V_{LO}	-0.5	V_{CCOM} + 0.5	
Input voltage LIN,HIN,EN,ITRIP		V_{IN}	-1	10	
FAULT output voltage		V_{FLT}	-0.5	V_{CC} + 0.5	
RCIN output voltage		V_{RCIN}	-0.5	V_{CC} + 0.5	
Power dissipation (to package)[2]	DSO28 TSSOP28	P_D	– –	1.3 0.6	W
Thermal resistance (junction to ambient, see section 6)	DSO28 TSSOP28	$R_{th(j-a)}$	– –	75 165	K/W
Junction temperature		T_J	–	125	°C
Storage temperature		T_S	- 40	150	
offset voltage slew rate[3]		d V_S/dt		50	V/ns

Note: The minimum value for ESD immunity in PG-DSO-28 is 2.0 kV (Human Body Model). ESD immunity inside pins connected to the low side (VCC, HINx, LINx, FAULT, EN, RCIN, ITRIP, VSS, COM, LOx) and pins connected inside each high side itself (VBx, HOx, VSx) is guaranteed up to 2.0 kV (Human Body Model). See *section 7*.

The minimum value for ESD immunity in PG-TSSOP-28 is 1.0 kV (Human Body Model). ESD immunity inside pins connected to the low side (VCC, HINx, LINx, FAULT, EN, RCIN, ITRIP, VSS, COM, LOx) and pins connected inside each high side itself (VBx, HOx, VSx) is guaranteed up to 1.5 kV (Human Body Model). See *section 7.*

[1] In case V_{CC} > V_B there is an additional power dissipation in the internal bootstrap diode between pins VCC and VBx. Insensitivity of bridge output to negative transient voltage up to –50 V is not subject to production test – verified by design / characterization.

[2] Consistent power dissipation of all outputs. All parameters inside operating range.

[3] Not subject of production test, verified by characterisation

4.2 Required operation conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 4 Required Operation Conditions

Parameter		Symbol	Min.	Max.	Unit
High side offset voltage[1]	DSO28 TSSOP28	V_B	7	620 200	V
Low side supply voltage (V_{CC} vs. V_{COM})	DSO28 TSSOP28	V_{CCOM}	10	25	

4.3 Operating Range

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 5 Operating range

Parameter		Symbol	Min.	Max.	Unit
High side floating supply offset voltage		V_S	V_{CC} - V_{BS} -1	500	V
High side floating supply offset voltage (V_B vs. V_{CC}, statically)		V_{BCC}	-1.0	500	
High side floating supply voltage (V_B vs. V_S, Note 1)	6EDL04I06NT 6EDL04I06PT	V_{BS}	13	17.5	V
	6EDL04N06PT 6EDL04N02PR		10	17.5	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	0	V_{BS}	
Low side output voltage (V_{LO} vs. V_{COM})		V_{LO}	0	V_{CC}	
Low side supply voltage	6EDL04I06NT 6EDL04I06PT	V_{CC}	13	17.5	
	6EDL04N06PT 6EDL04N02PR		10	17.5	
Low side ground voltage		V_{COM}	-2.5	2.5	
Logic input voltages LIN,HIN,EN,ITRIP[2]		V_{IN}	0	5	
FAULT output voltage		V_{FLT}	0	V_{CC}	
RCIN input voltage		V_{RCIN}	0	V_{CC}	
Pulse width for ON or OFF[3]		t_{IN}	1	–	µs
Ambient temperature		T_a	-40	105	°C

[1] Logic operational for V_B (V_B vs. V_S) > 7.0 V

[2] All input pins (HINx, LINx) and EN, ITRIP pin are internally clamped (see abs. maximum ratings)

[3] In case of input pulse width at LINx and HINx below 1µ the input pulse may not be transmitted properly

4.4 Static logic function table

VCC	VBS	RCIN	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
< V_{CCUV-}	X	X	X	X	0	0	0
15 V	< V_{BSUV-}	X	0	3.3 V	High imp	LIN1,2,3*	0
15 V	15 V	<3.2 V ↓	0	3.3 V	0	0	0
15 V	15 V	X	> $V_{IT,TH+}$	3.3 V	0	0	0
15 V	15 V	> $V_{RCIN,TH}$	0	3.3 V	High imp	LIN1,2,3*	HIN1,2,3*
15 V	15 V	> $V_{RCIN,TH}$	0	0	High imp	0	0

* according to Table 1

4.5 Static parameters

V_{CC} = V_{BS} = 15V unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
High level input voltage		V_{IH}	1.7	2.1	2.4	V	
Low level input voltage		V_{IL}	0.7	0.9	1.1		
EN positive going threshold		$V_{EN,TH+}$	1.9	2.1	2.3		
EN negative going threshold		$V_{EN,TH-}$	1.1	1.3	1.5		
ITRIP positive going threshold		$V_{IT,TH+}$	380	445	510	mV	
ITRIP input hysteresis		$V_{IT,HYS}$	45	70			
RCIN positive going threshold		$V_{RCIN,TH}$	-	5.2	6.4	V	
RCIN input hysteresis		$V_{RCIN,HYS}$	-	2.0	-		
Input clamp voltage (HIN and LIN acc. Table 1, EN, ITRIP)		$V_{IN,CLMAP}$	9	10.3	12		I_{IN} = 4mA
Input clamp voltage at high impedance (/HIN, /LIN negative logic only)		$V_{IN,FLOAT}$	-	5.3	5.8		controller output pin floating
High level output voltage	LO1,2,3 HO1,2,3	V_{OH}	- -	V_{CC} -0.7 V_B -0.7	V_{CC} -1.4 V_B -1.4		I_O = 20mA
Low level output voltage	LO1,2,3 HO1,2,3	V_{OL}	- -	V_{COM}+ 0.2 V_S+ 0.2	V_{COM}+ 0.6 V_S + 0.6		I_O = -20mA
V_{CC} and V_{BS} supply undervoltage positive going threshold	6EDL04I06NT 6EDL04I06PT	V_{CCUV+} V_{BSUV+}	11	11.7	12.5		
	6EDL04N06PT 6EDL04N02PR		8.3	9	9.8		
V_{CC} and V_{BS} supply undervoltage negative going threshold	6EDL04I06NT 6EDL04I06PT	V_{CCUV-} V_{BSUV-}	9.5	9.8	10.8	V	
	6EDL04N06PT 6EDL04N02PR		7.5	8.1	8.8		

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
V_{CC} and V_{BS} supply undervoltage lockout hysteresis	6EDL04I06NT 6EDL04I06PT	V_{CCUVH} V_{BSUVH}	1.2	1.9	-	V	
	6EDL04N06PT 6EDL04N02PR		0.5	0.9	-		
High side leakage current betw. VS and VSS		I_{LVS+}		1	12.5	µA	V_S = 600V
High side leakage current betw. VS and VSS		I_{LVS+}[1]	-	10	-		T_J=125°C, V_S=600V
High side leakage current between VSx and VSy (x=1,2,3 and y=1,2,3)		I_{LVS-}[1]	-	10	-		T_J = 125°C V_{Sx} - V_{Sy} = 600V
Quiescent current V_{BS} supply (VB only)		I_{QBS1}	-	210	400		HO=low
Quiescent current V_{BS} supply (VB only)		I_{QBS2}	-	210	400		HO=high
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NT	I_{QCC1}	-	1.1	1.8	mA	V_{LIN}=float. (all) V_{Sx}=50V (only bootstrap types)
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR		-	0.75	1.5		
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NT	I_{QCC2}	-	1.3	2		V_{LIN}=0, V_{HIN}=3.3 V V_{Sx}=50V
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR			0.75	1.5		V_{LIN}=3.3 V, V_{HIN}=0 V_{Sx}=50V
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NT	I_{QCC3}	-	1.3	2		V_{LIN}=3.3 V, V_{HIN}=0 V_{Sx}=50V
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR			0.75	1.5		V_{LIN}=0, V_{HIN}=3.3 V V_{Sx}=50V
Input bias current	6EDL04I06NT	I_{LIN+}	-	70	100	µA	V_{LIN}=3.3 V
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR		400	700	1100		
Input bias current	6EDL04I06NT	I_{LIN-}	-	110	200	µA	V_{LIN}=0
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR			0			
Input bias current	6EDL04I06NT	I_{HIN+}	-	70	100		V_{HIN}=3.3 V
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR		400	700	1100		
Input bias current	6EDL04I06NT	I_{HIN-}	-	110	200		V_{HIN}=0
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR			0			

[1] Not subject of production test, verified by characterisation

Table 6 Static parameters

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Input bias current (ITRIP=high)	I_{ITRIP+}		45	120	µA	V_{ITRIP}=3.3 V
Input bias current (EN=high)	I_{EN+}	-	45	120		V_{ENABLE}=3.3 V
Input bias current RCIN (internal current source)	I_{RCIN}		2.8			V_{RCIN} = 2 V
Mean output current for load capacity charging in range from 3 V (20%) to 6 V (40%)	I_{O+}	120	165	-	mA	C_L=10 nF
Peak output current turn on (single pulse)	I_{Opk+}[1]		240			R_L = 0 , t_p<10 µs
Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%)	I_{O-}	250	375	-		C_L=10 nF
Peak output current turn off (single pulse)	I_{Opk-}[1]		420			R_L = 0 , t_p<10 µs
Bootstrap diode forward voltage between VCC and VB	$V_{F,BSD}$	-	1.0	1.3	V	I_F=0.5 mA
Bootstrap diode forward current between VCC and VB	$I_{F,BSD}$	27	51	75	mA	V_F=4 V
Bootstrap diode resistance	R_{BSD}	24	40	60	Ω	V_{F1}=4 V, V_{F2}=5 V
RCIN low on resistance of the pull down transistor	$R_{on,RCIN}$	-	40	100		V_{RCIN}=0.5 V
FAULT low on resistance of the pull down transistor	$R_{on,FLT}$	-	45	100		V_{FAULT}=0.5 V

[1] Not subject of production test, verified by characterisation

4.6 Dynamic parameters

V_{CC} = V_{BS} = 15 V, V_S = V_{SS} = V_{COM} unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 7 Dynamic parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
Turn-on propagation delay		t_{on}	400	530	800	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
Turn-off propagation delay	6EDL04I06NT 6EDL04I06PT	t_{off}	360	490	760		
	6EDL04N06PT 6EDL04N02PR		400	530	800		
Turn-on rise time		t_r	-	60	100		$V_{LIN/HIN}$ = 0 or 3.3 V C_L = 1 nF
Turn-off fall time		t_f	-	26	45		
Shutdown propagation delay ENABLE		t_{EN}	-	780	1100		V_{EN}=0
Shutdown propagation delay ITRIP		t_{ITRIP}	400	670	1000		V_{ITRIP}=1 V
Input filter time ITRIP		$t_{ITRIPMIN}$	155	230	380		
Propagation delay ITRIP to FAULT		t_{FLT}	-	420	700		
Input filter time at LIN/HIN for turn on and off		t_{FILIN}	120	300	-		$V_{LIN/HIN}$ = 0 & 3.3 V
Input filter time EN		t_{FILEN}	300	600	-		
Fault clear time at RCIN after ITRIP-fault, (C_{RCin}=1nF)		t_{FLTCLR}	1.0	1.9	3.0	ms	$V_{LIN/HIN}$ = 0 & 3.3 V V_{ITRIP} = 0
Dead time		DT	150	310	-	ns	$V_{LIN/HIN}$ = 0 & 3.3 V
Matching delay ON, max(ton)-min(ton), ton are applicable to all 6 driver outputs		MT_{ON}	-	20	100		external dead time > 500 ns
Matching delay OFF, max(toff)-min(toff), toff are applicable to all 6 driver outputs		MT_{OFF}	-	40	100		external dead time >500 ns
Output pulse width matching. Pw_{in}-PW_{out}	6EDL04I06NT 6EDL04I06PT	PM		40	100		PW_{in} > 1 µs
	6EDL04N06PT 6EDL04N02PR			10	100		

5 Timing diagrams

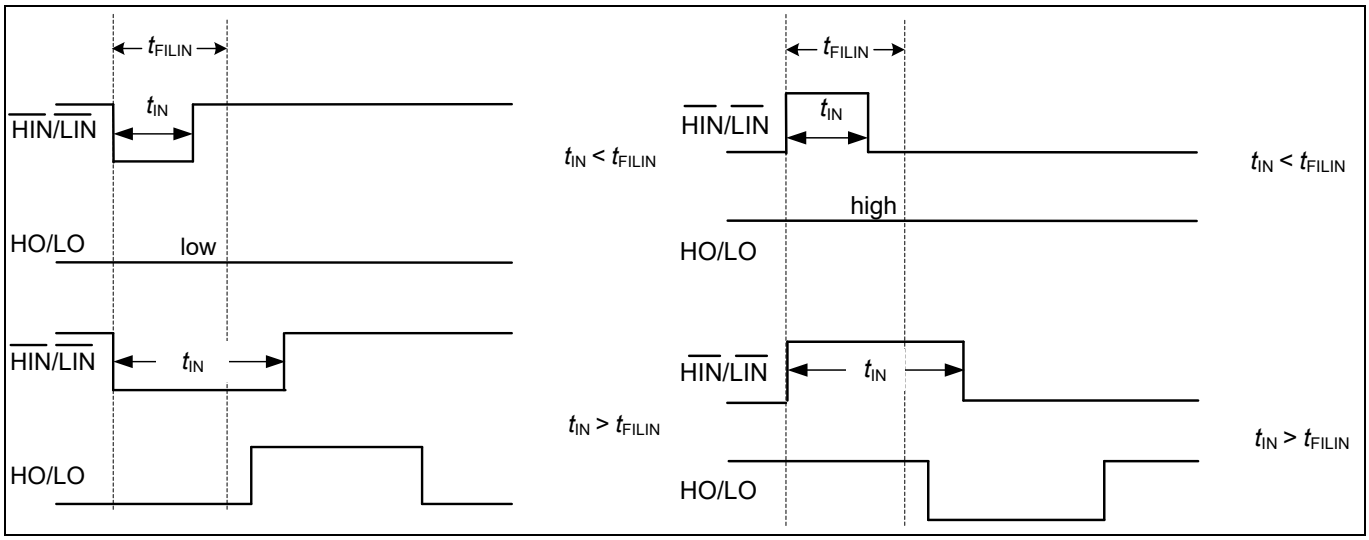


Figure 9 Timing of short pulse suppression (6EDL04I06NT)

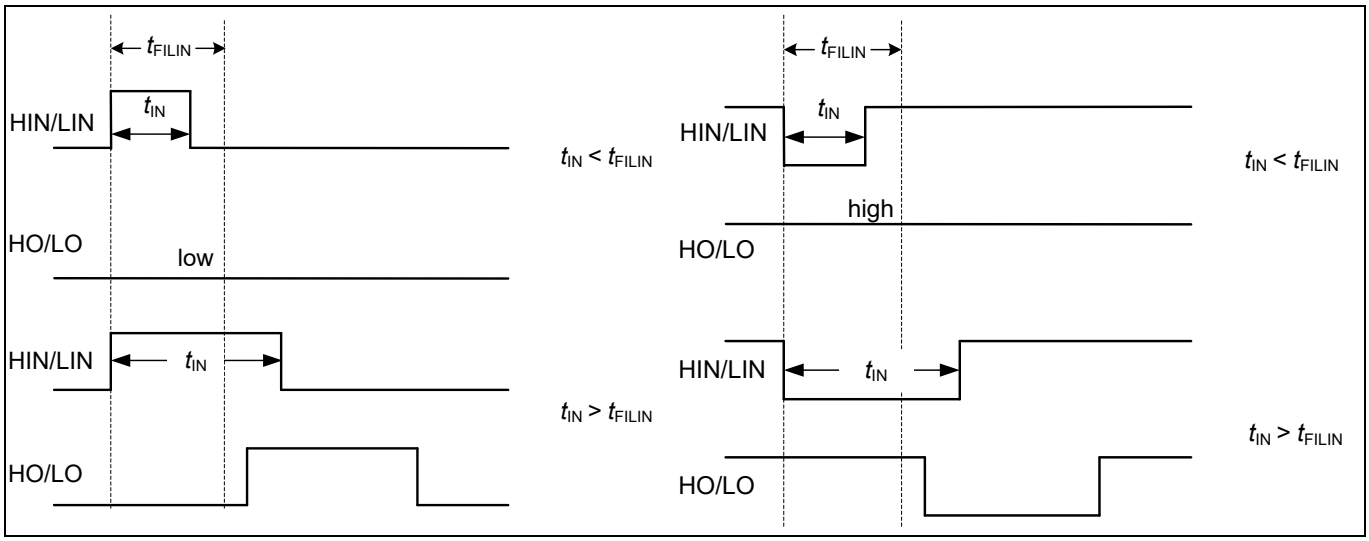


Figure 10 Timing of short pulse suppression (6EDL04I06PT, 6EDL04N06PT, 6EDL04N02PR)

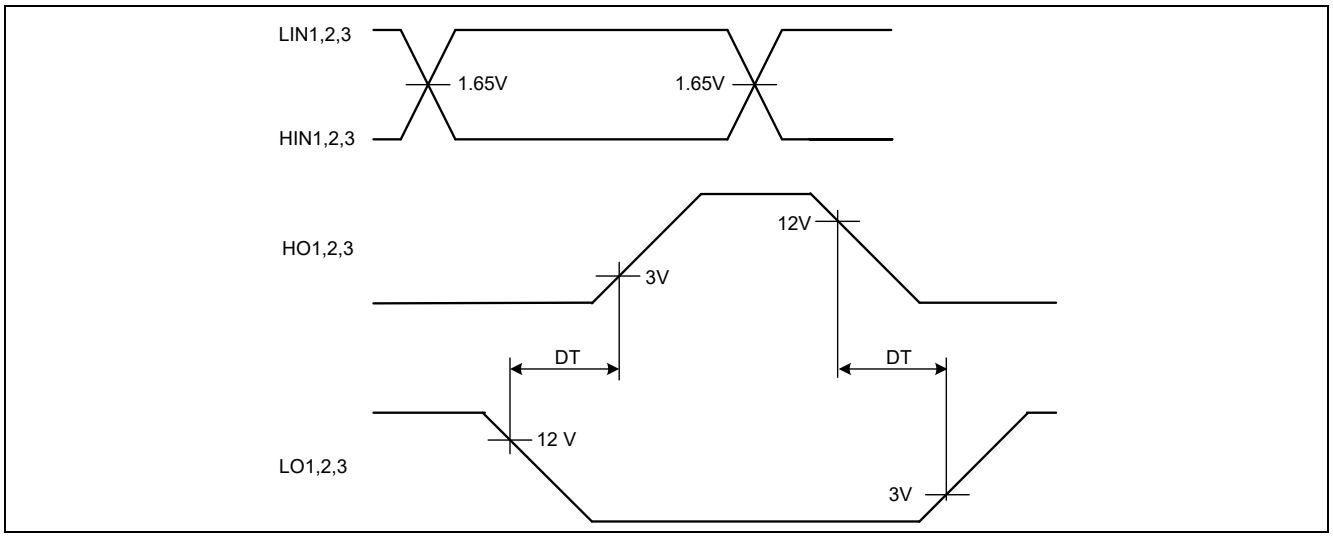


Figure 11 Timing of of internal deadtime (input logic according to Table 1)

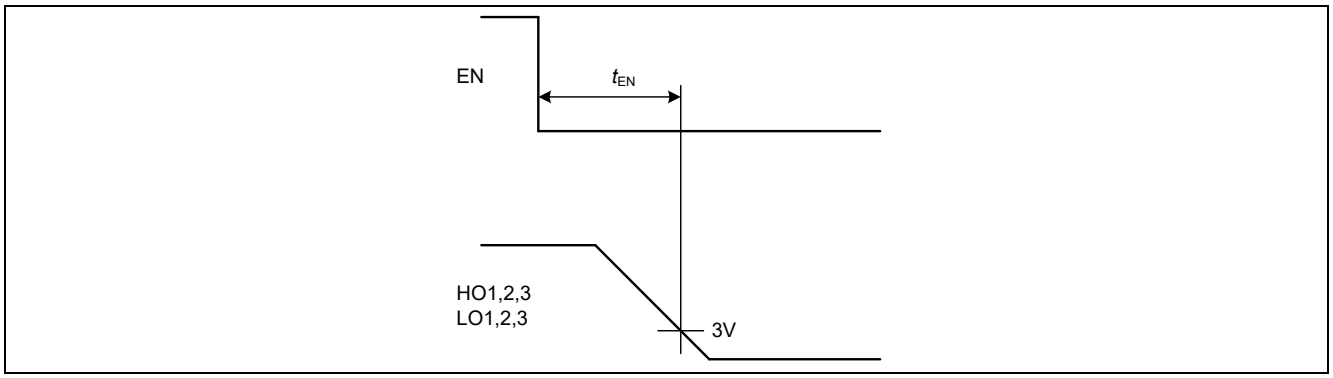


Figure 12 Enable delay time definition

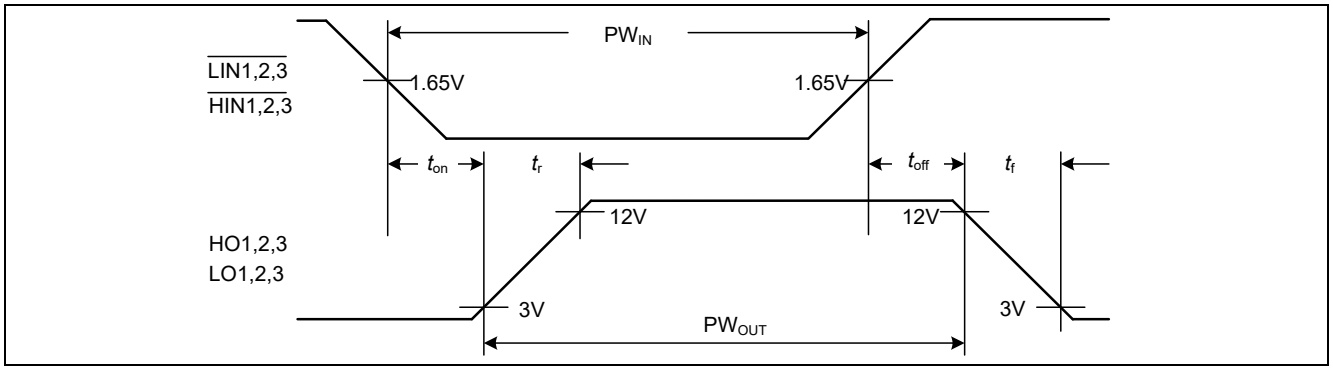


Figure 13 Input to output propagation delay times and switching times definition (6EDL04I06NT)

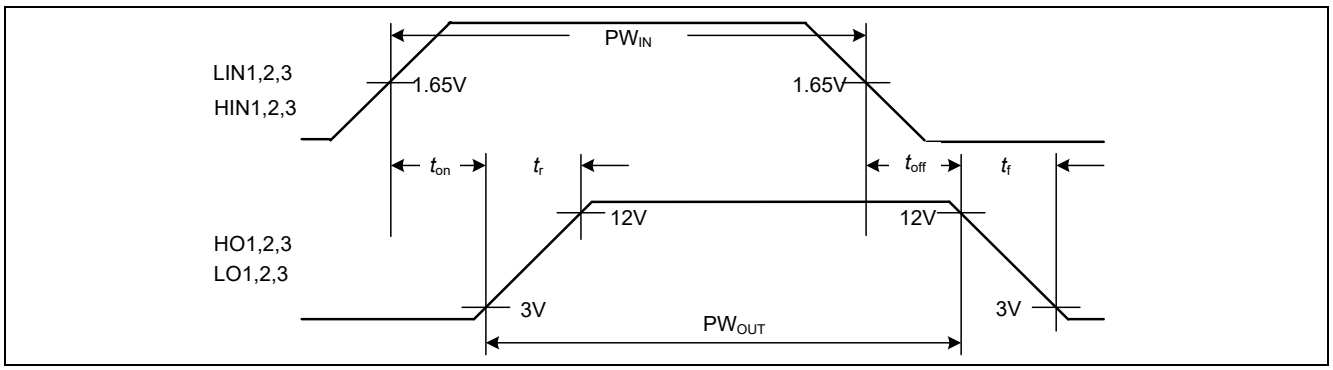


Figure 14 Input to output propagation delay times and switching times definition (6EDL04I06PT, 6EDL04N06PT, 6EDL04N02PR)

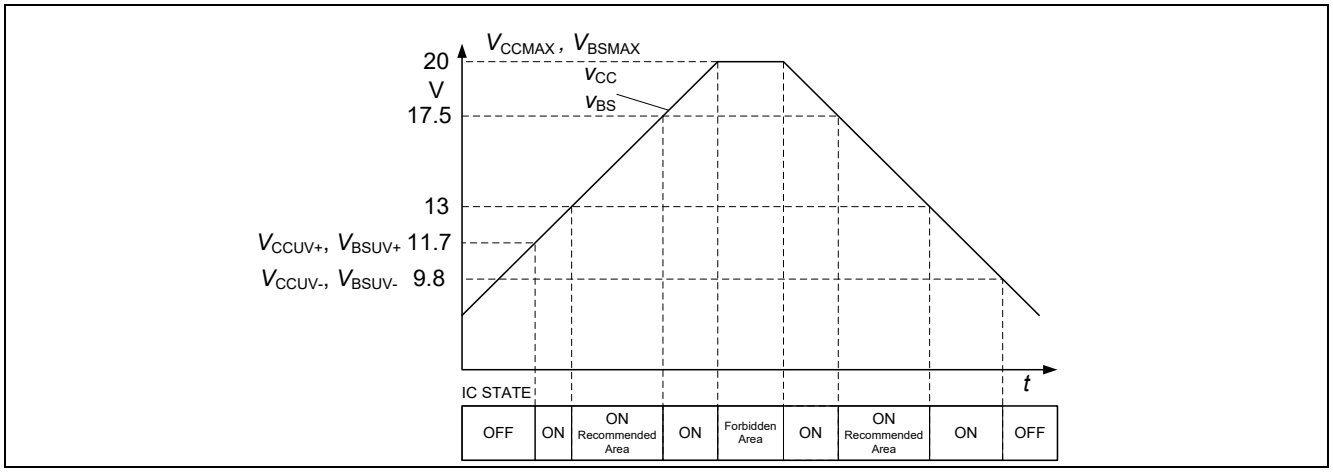


Figure 15 Operating areas (6EDL04I06NT, 6EDL04I06PT)

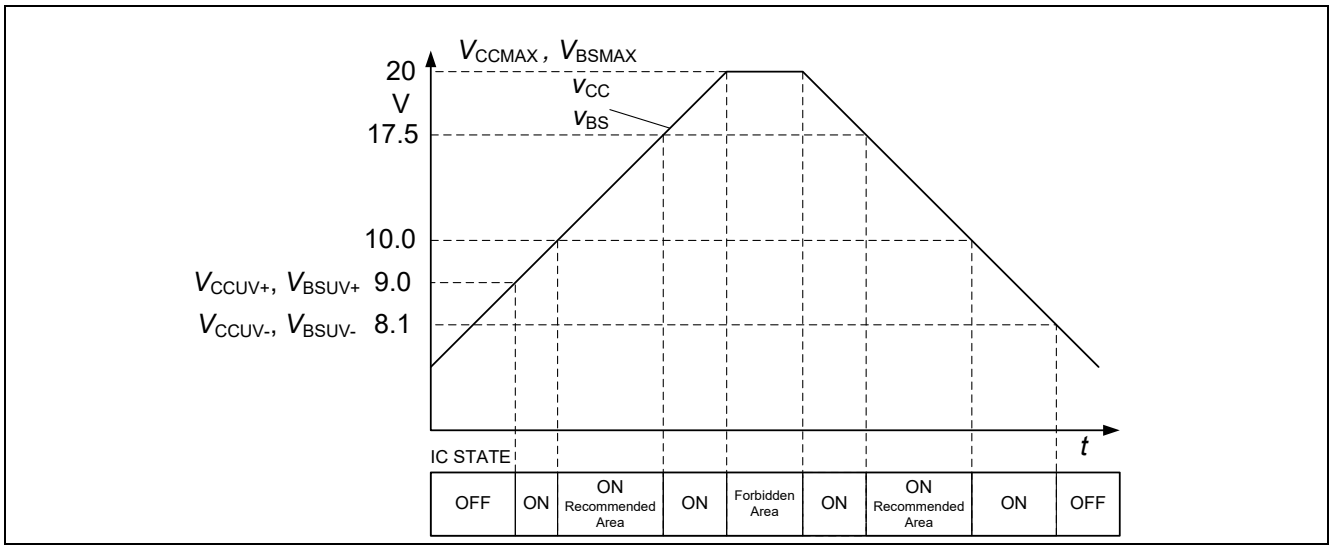


Figure 16 Operating Areas (6EDL04N06PT, 6EDL04N02PR)

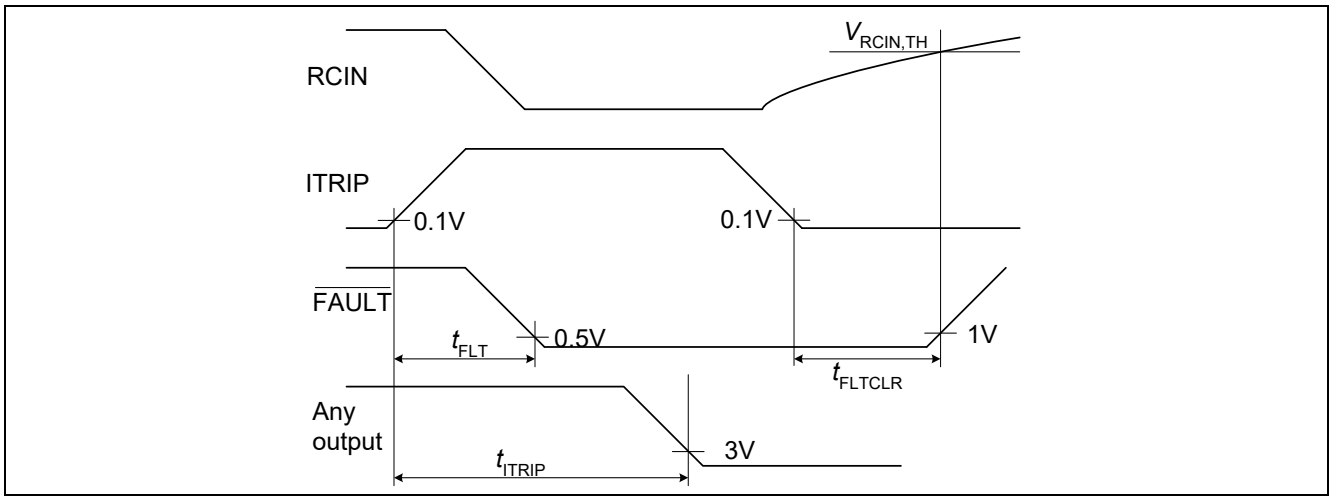


Figure 17 ITRIP-Timing

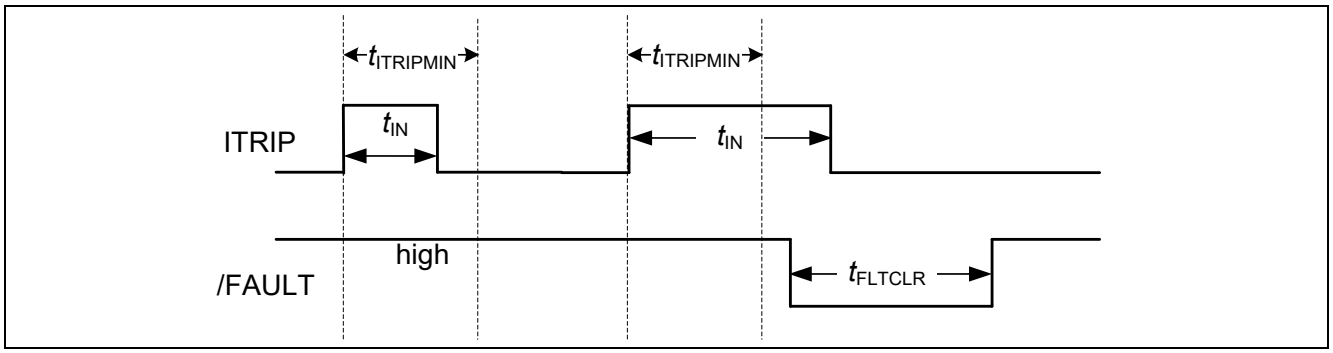
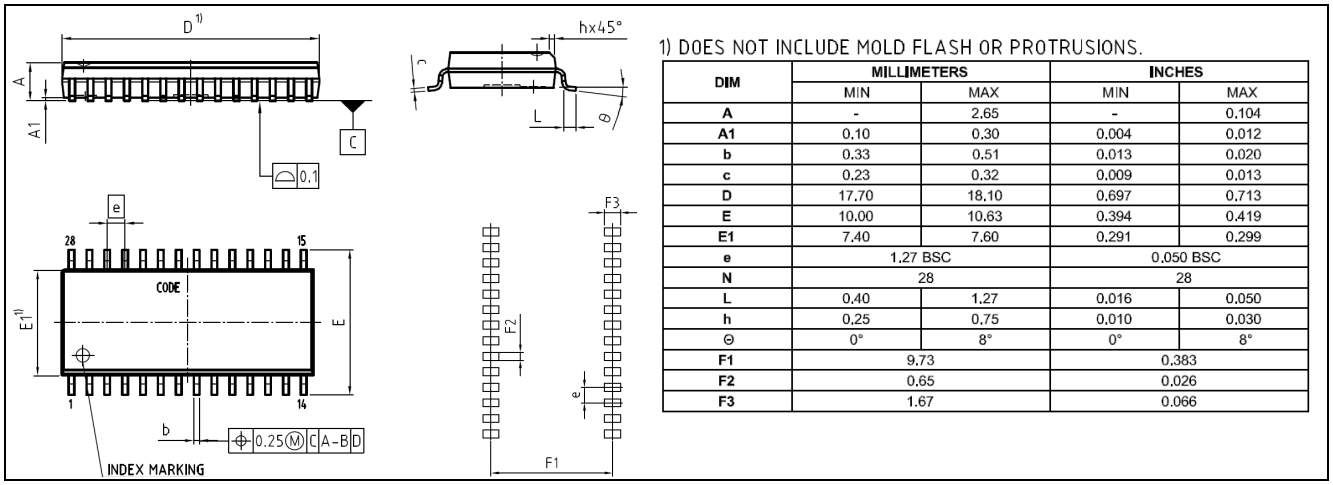


Figure 18 ITRIP Input Timing

6 Package information

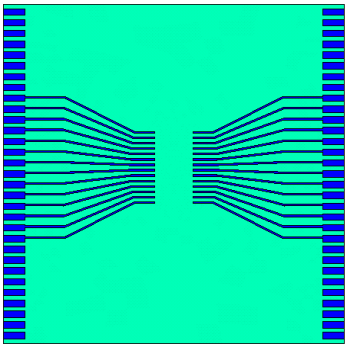
6.1 PG-DSO-28



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	2.65	-	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	17.70	18.10	0.697	0.713
E	10.00	10.63	0.394	0.419
E1	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
N	28		28	
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.030
Θ	0°	8°	0°	8°
F1	9.73		0.383	
F2	0.65		0.026	
F3	1.67		0.066	

Figure 19 Package drawing



Dimensions	80.0 × 80.0 × 1.5 mm³	λ_{therm} [W/m·K]
Material	FR4	0.3
Metal (Copper)	70µm	388

Figure 20 PCB reference layout

6.2 PG-TSSOP-28

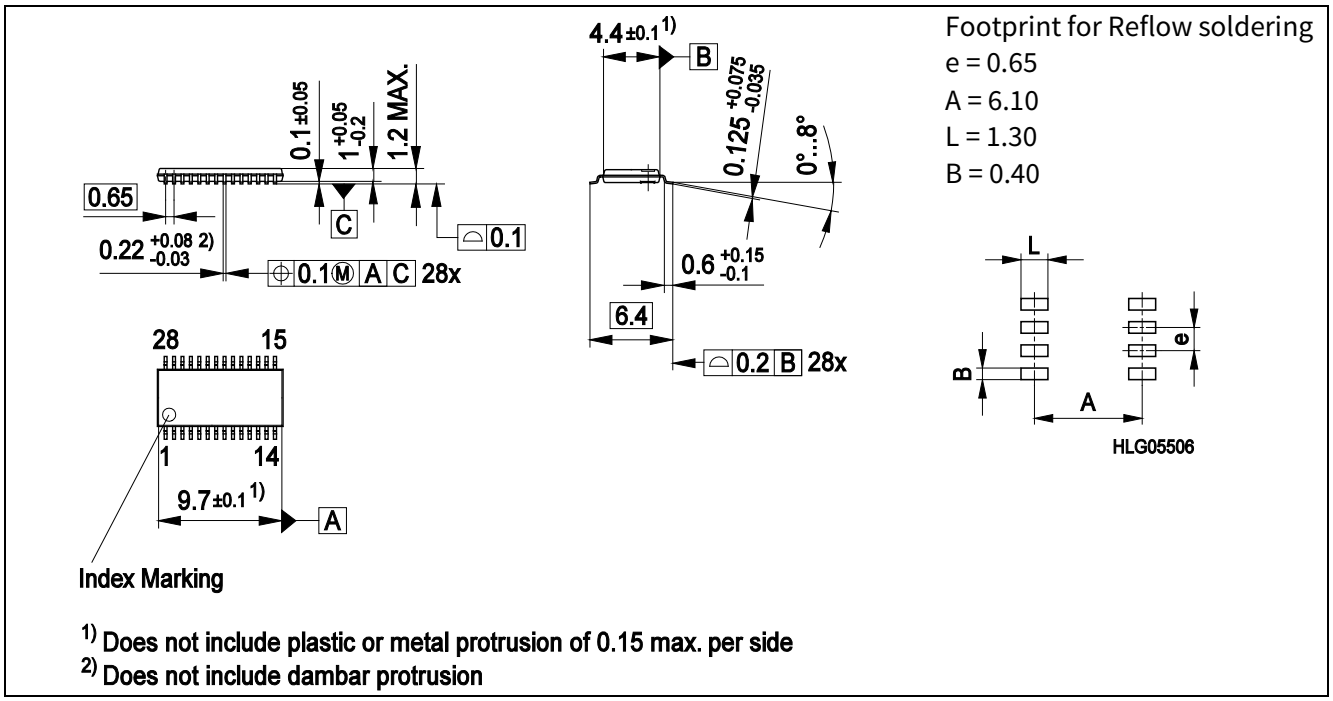


Figure 21 Package drawing

6.3 PG-TSSOP-28 (according to PCN 2018-165-A)

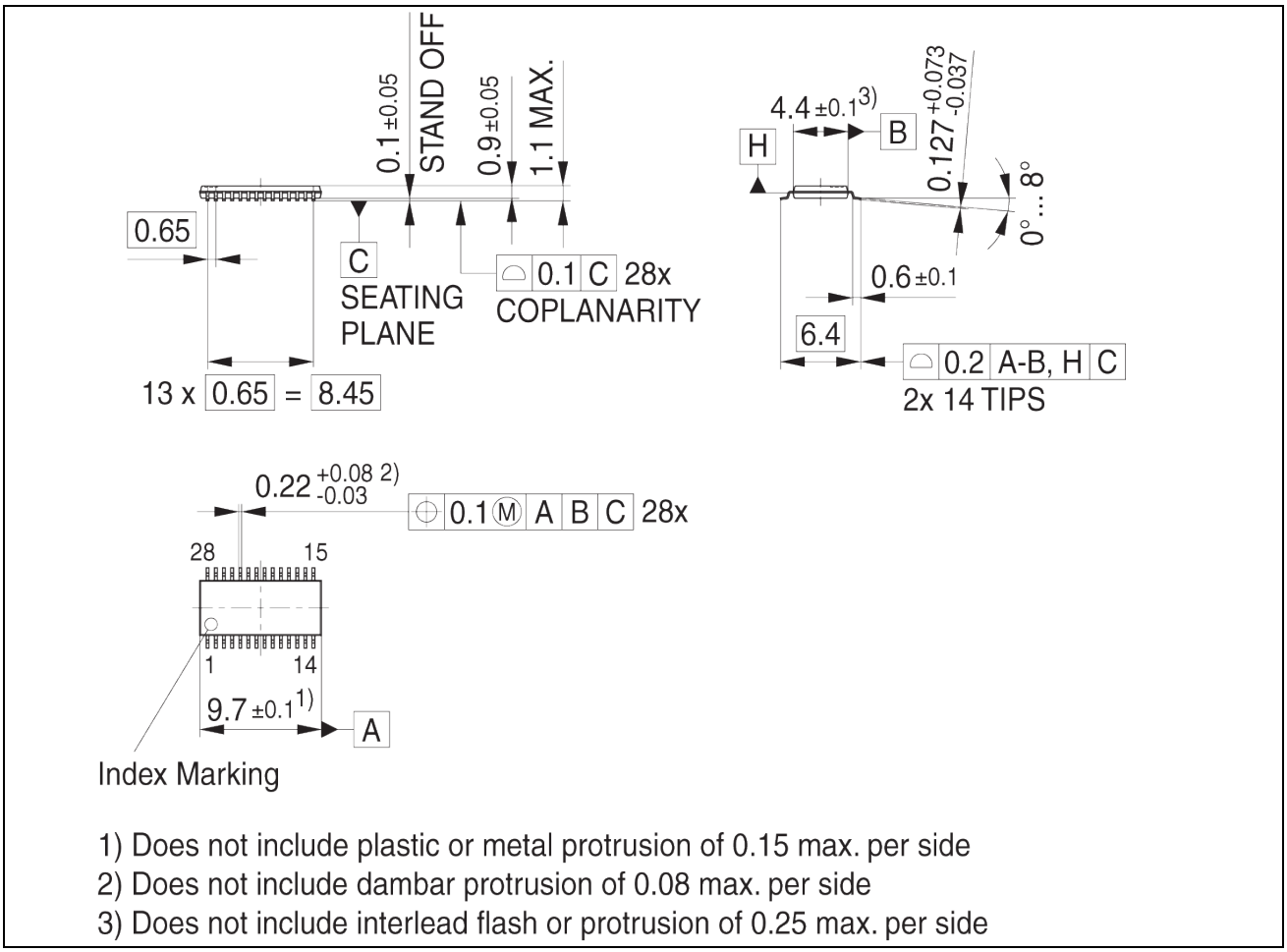


Figure 22 Package drawing

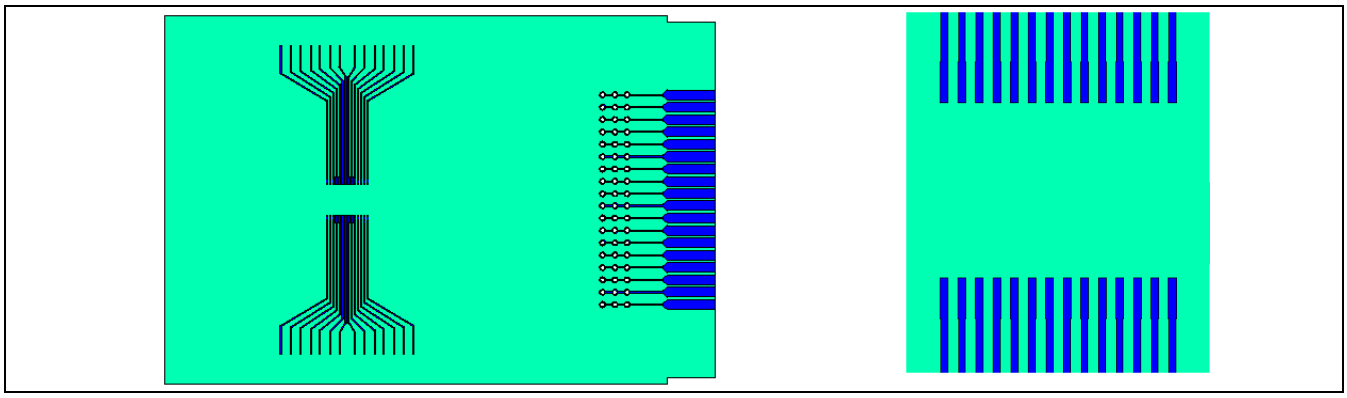


Figure 23 PCB reference layout (according to JEDEC 1s0P)
left: Reference layout
right: detail of footprint

Table 8 Data of reference layout

Dimensions	Material	Metal (Copper)
76.2 × 114.3 × 1.5 mm^3	FR4 (λ_{therm} = 0.3 W/mK)	70µm (λ_{therm} = 388 W/mK)

7 Qualification information[1]

Table 9 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		TSSOP-28/DSO-28	MSL3[3], 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (> 1.0 kV) (per JESD22-C101)	
	Human body model	6EDL04x06xT	Class 2 (per JEDEC standard JESD22-A114)
		6EDL04N02PR	Class 1C (per JEDEC standard JESD22-A114)
RoHS compliant		Yes	

8 Related products

Table 10

Gate Driver ICs	
2EDL05I06 / 2EDL05N06	600 V, half-bridge thin-film SOI level shift gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diode, 0.36/0.7 A source/sink current driver, 8pins/14pins package, for MOSFET or IGBT.
2EDL23I06 / 2EDL23N06	600 V, half-bridge thin-film SOI level shift gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diode, with over-current protection (OCP), 2.3/2.8 A source/sink current driver, and one pin Enable/Fault function for MOSFET or IGBT.
Power Switches	
IKD04N60R / RF	600 V TRENCHSTOP™ IGBT with integrated diode in PG-TO252-3 package
IKD06N65ET6	650 V TRENCHSTOP™ IGBT with integrated diode in DPAK
IPD65R950CFD	650 V CoolMOS CFD2 with integrated fast body diode in DPAK
IPN50R950CE	500 V CoolMOS CE Superjunction MOSFET in PG-SOT223 package
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

Revision history

Document version	Date of release	Description of changes
2.6	2016-08-05	Increased the maximum operating ambient temperature to 105 °C
		Updated disclaimer, Delete links to application note
		Corrected parameter V_{HO} in section 4.3
2.7	2019-01-11	Updated ESD HBM information, and add package drawing PG-TSSOP-28. Editorial change in table 6

[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
[3] Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

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Edition 2019-03-21

Published by

Infineon Technologies AG

81726 Munich, Germany

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