

Contents

1	Block diagram and pin description	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	8
2.4	Waveforms	19
2.5	Electrical characteristics curves	22
3	Application information	25
3.1	GND protection network against reverse battery	25
3.1.1	Solution 1: resistor in the ground line (RGND only)	25
3.1.2	Solution 2: diode (DGND) in the ground line	26
3.2	Load dump protection	26
3.3	MCU I/Os protection	26
3.4	Current sense and diagnostic	27
3.4.1	Short to V_{CC} and off-state open-load detection	28
3.5	Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)	29
4	Package and thermal data	30
4.1	PowerSSO-24 thermal data	30
5	Package and packing information	33
5.1	ECOPACK® packages	33
5.2	Package mechanical data	33
5.3	Packing information	35
6	Order codes	36
7	Revision history	37

List of tables

Table 1.	Pin functions	5
Table 2.	Suggested connections for unused and not connected pins	6
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data.	8
Table 5.	Power section	8
Table 6.	Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$)	9
Table 7.	Logic inputs.	10
Table 8.	Protections and diagnostics	10
Table 9.	Current sense ($8\text{ V} < V_{CC} < 18\text{ V}$)	11
Table 10.	Open-load detection ($8\text{ V} < V_{CC} < 18\text{ V}$)	12
Table 11.	Truth table.	17
Table 12.	Electrical transient requirements (part 1/3)	18
Table 13.	Electrical transient requirements (part 2/3)	18
Table 14.	Electrical transient requirements (part 3/3)	18
Table 15.	Thermal parameters	32
Table 16.	PowerSSO-24™ mechanical data	34
Table 17.	Device summary	36
Table 18.	Document revision history	37

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	6
Figure 3.	Current and voltage conventions	7
Figure 4.	Current sense delay characteristics	13
Figure 5.	Openload off-state delay timing	13
Figure 6.	Switching characteristics	14
Figure 7.	Delay response time between rising edge of output current and rising edge of current sense (CS enabled)	15
Figure 8.	Output voltage drop limitation	15
Figure 9.	I_{OUT}/I_{SENSE} vs I_{OUT}	16
Figure 10.	Maximum current sense ratio drift vs load current	16
Figure 11.	Normal operation	19
Figure 12.	Overload or short to GND	19
Figure 13.	Intermittent overload	20
Figure 14.	Off-state open-load with external circuitry	20
Figure 15.	Short to V_{CC}	21
Figure 16.	T_J evolution in overload or short to GND	21
Figure 17.	Off-state output current	22
Figure 18.	High level input current	22
Figure 19.	Input clamp voltage	22
Figure 20.	Input high level voltage	22
Figure 21.	Input low level voltage	22
Figure 22.	Input hysteresis voltage	22
Figure 23.	On-state resistance vs T_{case}	23
Figure 24.	On-state resistance vs V_{CC}	23
Figure 25.	Undervoltage shutdown	23
Figure 26.	I_{LIMH} vs T_{case}	23
Figure 27.	Turn-on voltage slope	23
Figure 28.	Turn-off voltage slope	23
Figure 29.	CS_DIS high level voltage	24
Figure 30.	CS_DIS low level voltage	24
Figure 31.	CS_DIS clamp voltage	24
Figure 32.	Application schematic ⁽¹⁾	25
Figure 33.	Current sense and diagnostic	27
Figure 34.	Maximum turn-off current versus inductance (for each channel) ⁽¹⁾	29
Figure 35.	PowerSSO-24 PC board ⁽¹⁾	30
Figure 36.	$R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)	30
Figure 37.	PowerSSO-24 thermal impedance junction to ambient single pulse (one channel on)	31
Figure 38.	Thermal fitting model of a double channel HSD in PowerSSO-24 ⁽¹⁾	31
Figure 39.	PowerSSO-24 package dimensions	33
Figure 40.	PowerSSO-24 tube shipment (no suffix)	35
Figure 41.	PowerSSO-24 tape and reel shipment (suffix "TR")	35

1 Block diagram and pin description

Figure 1. Block diagram

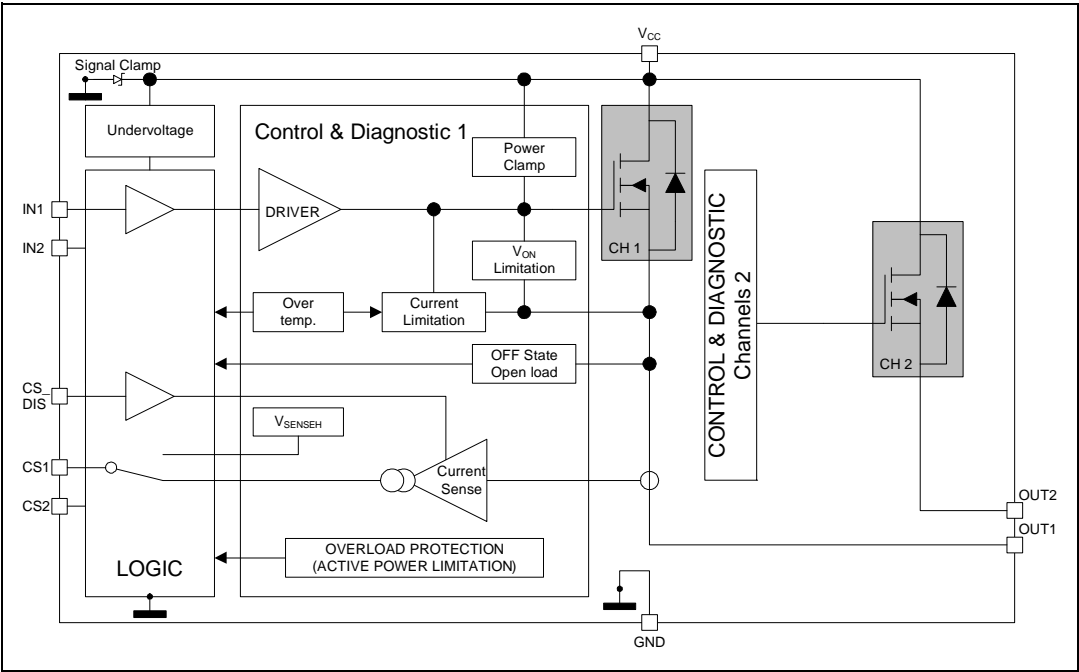


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT _{1,2}	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT _{1,2}	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE _{1,2}	Analog current sense pin; delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin to disable the current sense pin.

Figure 2. Configuration diagram (top view)

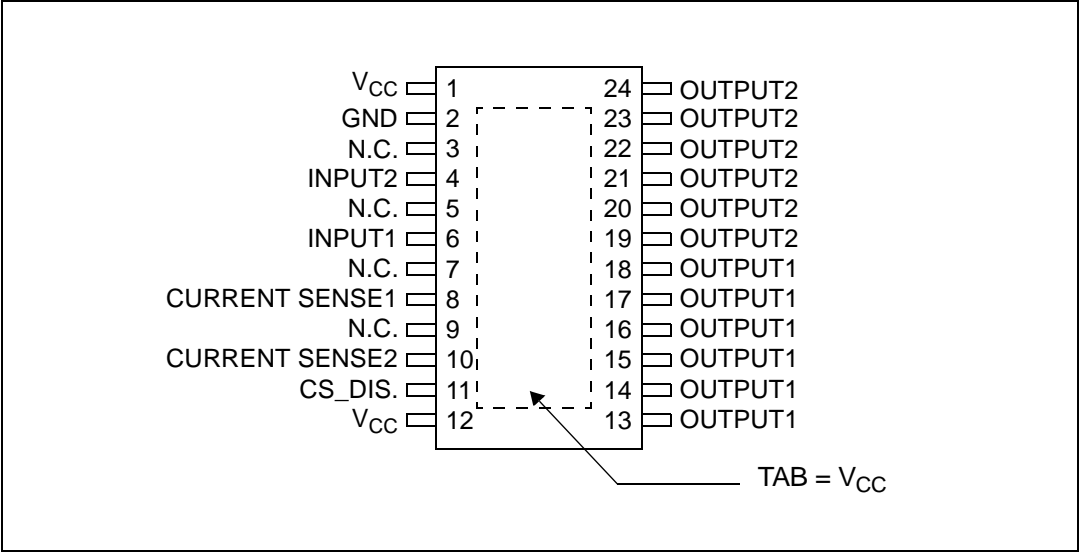
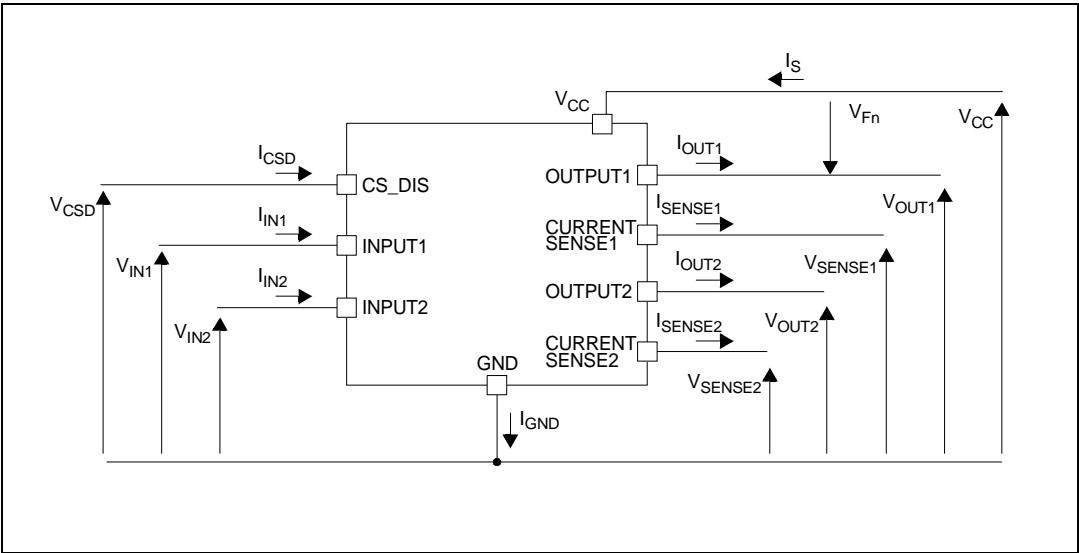


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1kΩ resistor	X	Through 22kΩ resistor	Through 10kΩ resistor	Through 10kΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	24	
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current		
$-I_{CSENSE}$	DC reverse CS pin current		
V_{CSENSE}	Current sense maximum voltage	$V_{CC} - 41$ to $+V_{CC}$	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) ($L = 0.8 \text{ mH}$; $R_L = 0 \text{ }\Omega$; $V_{bat} = 13.5 \text{ V}$; $T_{jstart} = 150 \text{ }^\circ\text{C}$; $I_{OUT} = I_{limL}(Typ.)$)	140	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: $R = 1.5 \text{ k}\Omega$; $C = 100 \text{ pF}$)		
	– Input	4000	V
	– Current sense	2000	V
	– CS_DIS	4000	V
	– Output	5000	V
	– V_{CC}	5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	- 40 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	- 55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	1.35	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	See Figure 36	

2.3 Electrical characteristics

Values specified in this section are for $8 \text{ V} < V_{CC} < 28 \text{ V}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		
R_{ON}	On-state resistance ⁽¹⁾	$I_{OUT} = 3 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$			25	m Ω
		$I_{OUT} = 3 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$			50	
		$I_{OUT} = 3 \text{ A}$; $V_{CC} = 5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$			35	
V_{clamp}	Clamp voltage	$I_S = 20 \text{ mA}$	41	46	52	V

Table 5. Power section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	Off-state; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0\text{ V}$		2 ⁽²⁾	5 ⁽²⁾	μA
		On-state; $V_{CC} = 13\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		3	6	mA
$I_{L(off1)}$	Off-state output current ⁽¹⁾	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	0		5	
V_F	Output - V_{CC} diode voltage ⁽¹⁾	$-I_{OUT} = 4\text{ A}$; $T_j = 150\text{ }^\circ\text{C}$			0.7	V

1. For each channel.

2. PowerMOS leakage included.

Table 6. Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On delay time	$R_L = 4.3\text{ }\Omega$ (see Figure 6)		20		μs
$t_{d(off)}$	Turn-Off delay time			40		
$(dV_{OUT}/dt)_{on}$	Turn-On voltage slope	$R_L = 4.3\text{ }\Omega$		See Figure 27		$\text{V}/\mu\text{s}$
$(dV_{OUT}/dt)_{off}$	Turn-Off voltage slope			See Figure 28		
W_{ON}	Switching energy losses during t_{WON}	$R_L = 4.3\text{ }\Omega$ (see Figure 6)		0.6		mJ
W_{OFF}	Switching energy losses during t_{WOFF}			0.35		

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	
		$I_{IN} = -1\text{ mA}$		-0.7		
V_{CSDL}	CS_DIS low level voltage				0.9	
I_{CSDL}	Low level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD} = 2.1\text{ V}$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD} = 1\text{ mA}$	5.5		7	
		$I_{CSD} = -1\text{ mA}$		-0.7		

Table 8. Protections and diagnostics ⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIMH}	DC short circuit current	$V_{CC} = 13\text{ V}$	43	60	85	A
		$5\text{ V} < V_{CC} < 28\text{ V}$				
I_{LIML}	Short circuit current during thermal cycling	$V_{CC} = 13\text{ V};$ $T_R < T_j < T_{TSD}$		15		
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		
T_{RS}	Thermal reset of STATUS		135			
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		
V_{DEMAG}	Turn-Off output voltage clamp	$I_{OUT} = 2\text{ A}; V_{IN} = 0;$ $L = 6\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.1\text{ A};$ $T_j = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$ (see Figure 8)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K _{LED}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.05 A; V _{SENSE} = 0.5 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	1240	3350	4960	
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 0.5 A; V _{SENSE} = 0.5 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	1860	3150	4600	
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C T _j = 25 °C to 150 °C	2100 2250	3100 3100	4400 3850	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	-13		13	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 3 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C T _j = 25 °C to 150 °C	2200 2450	3000 3000	4100 3550	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 3 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	-12		12	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 10 A; V _{SENSE} = 4V; V _{CSD} = 0V; T _j = -40°C to 150°C T _j = 25°C to 150°C	2550 2650	2850 2850	3280 3180	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 10 A; V _{SENSE} = 4V; V _{CSD} = 0V; T _j = -40°C to 150°C	-6		+6	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{CSD} = 5 V; V _{IN} = 0V; T _j = -40°C to 150°C V _{CSD} = 0 V; V _{IN} = 5 V; T _j = -40 °C to 150 °C I _{OUT} = 2A; V _{SENSE} = 0V; V _{CSD} = 5V; V _{IN} = 5V; T _j = -40°C to 150°C	0 0		1 2	μA μA
I _{OL}	Open-load on-state current detection threshold	V _{IN} = 5 V, 8 V < V _{CC} < 18 V I _{SENSE} = 5 μA	5		30	mA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 3 A; V _{CSD} = 0 V	5			V
V _{SENSEH}	Analog sense output voltage in fault condition ⁽¹⁾	V _{CC} = 13 V; R _{SENSE} = 3.9 kΩ		8		

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SENSEH}	Analog sense output current in fault condition ⁽²⁾	V _{CC} = 13 V; V _{SENSE} = 5 V		9		mA
t _{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} < 4 V, 0.5 < I _{OUT} < 10 A I _{SENSE} = 90% of I _{SENSEMAX} (see Figure 4)		30	100	μs
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} < 4 V, 0.5 < I _{OUT} < 10 A I _{SENSE} = 10 % of I _{SENSEMAX} (see Figure 4)		5	20	
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} < 4 V, 0.5 < I _{OUT} < 10 A I _{SENSE} = 90% of I _{SENSEMAX} (see Figure 4)		80	300	
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4 V, I _{SENSE} = 90 % of I _{SENSEMAX} , I _{OUT} = 90 % of I _{OUTMAX} , I _{OUTMAX} = 3 A (see Figure 7)			110	
t _{DSENSE2L}	Delay response time from falling edge of INPUT pin	V _{SENSE} < 4 V, 0.5 < I _{OUT} < 10 A I _{SENSE} = 10 % of I _{SENSEMAX} (see Figure 4)		70	250	

1. Fault condition includes: power limitation, overtemperature and open-load off-state detection.

Table 10. Open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _{OL}	Open-load off-state voltage detection threshold	V _{IN} = 0 V	2	See Figure 5	4	V
t _{DSTKON}	Output short circuit to V _{CC} detection delay at turn-off	See Figure 5	180		1200	μs
I _{L(off2)r}	Off-state output current at V _{OUT} = 4 V	V _{IN} = 0 V; V _{SENSE} = 0 V V _{OUT} rising from 0 V to 4 V	-120		0	μA

Table 10. Open-load detection ($8\text{ V} < V_{CC} < 18\text{ V}$) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{L(off2)f}$	Off-state output current at $V_{OUT} = 2\text{ V}$	$V_{IN} = 0\text{ V}$; $V_{SENSE} = V_{SENSEH}$ V_{OUT} falling from V_{CC} to 2 V	-50		90	μA
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in openload	$V_{OUT} = 4\text{ V}$; $V_{IN} = 0\text{ V}$ $V_{SENSE} = 90\%$ of V_{SENSEH}			20	μs

Figure 4. Current sense delay characteristics

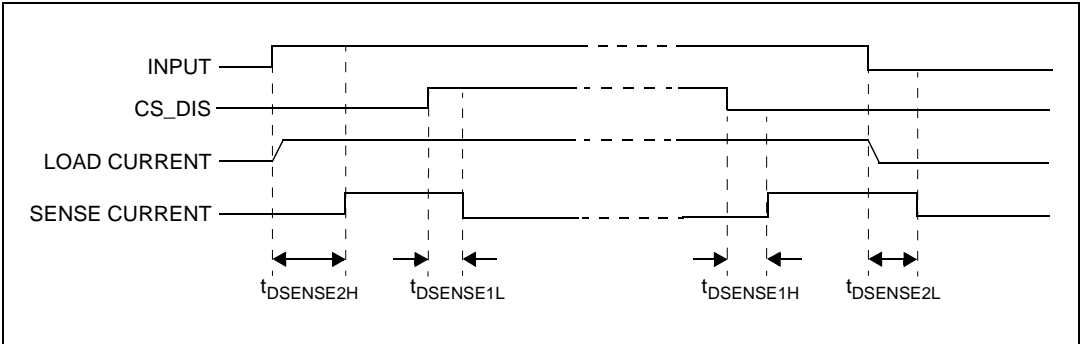


Figure 5. Openload off-state delay timing

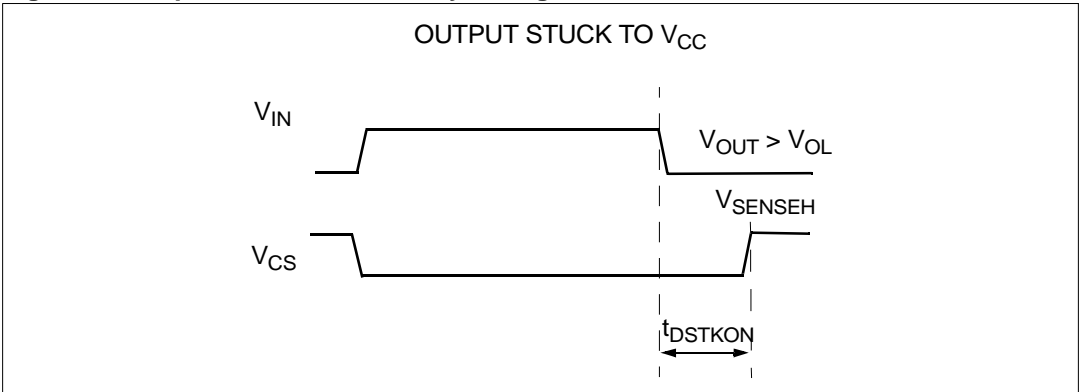


Figure 6. Switching characteristics

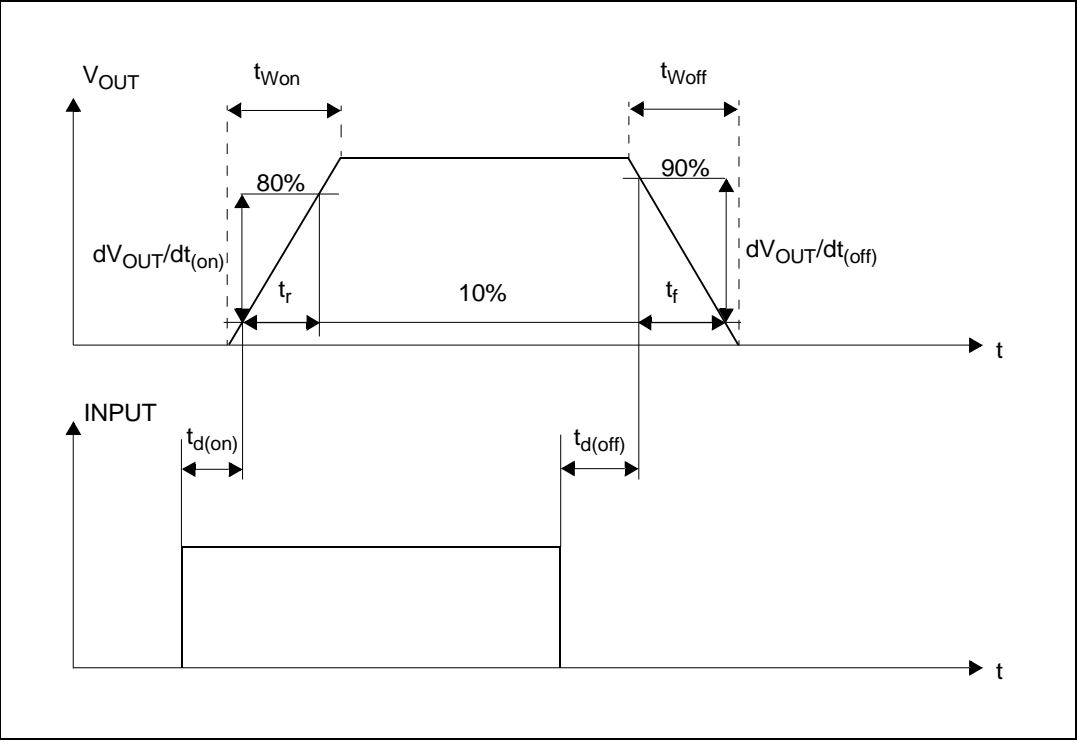


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

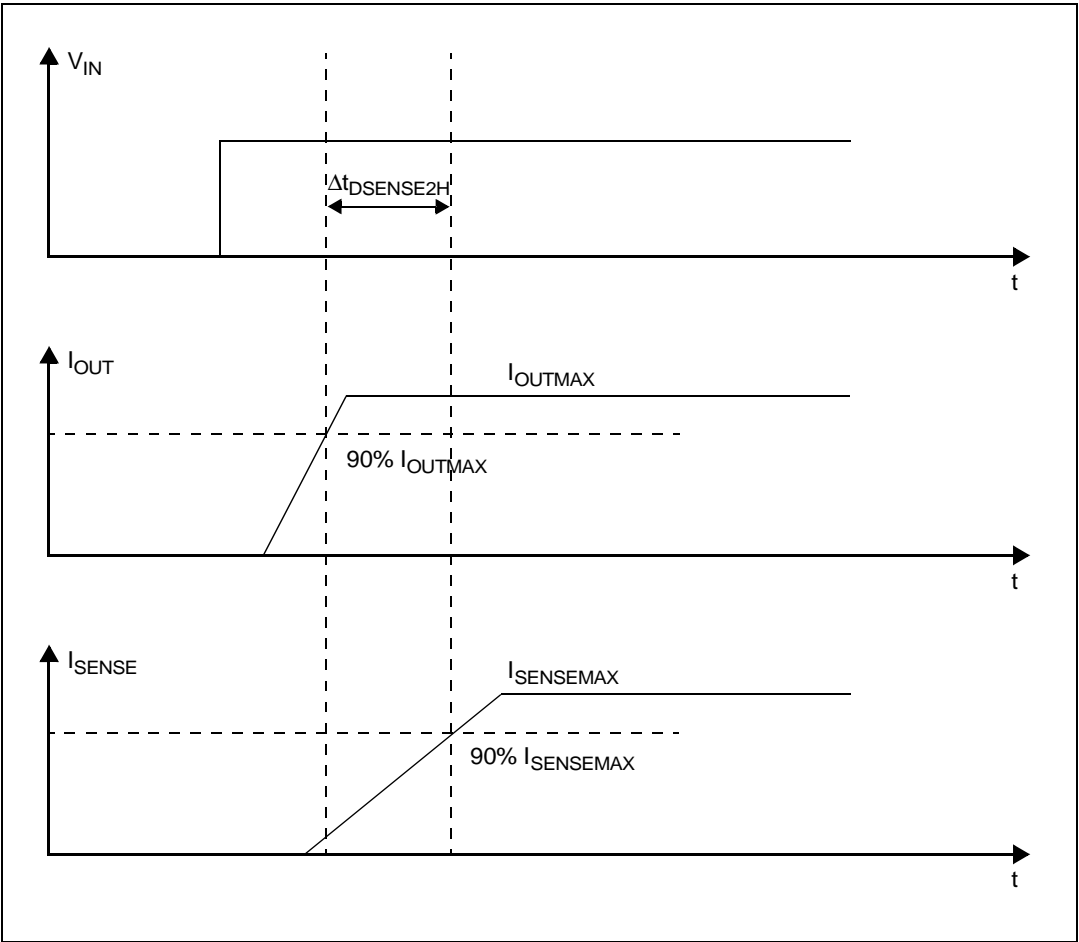


Figure 8. Output voltage drop limitation

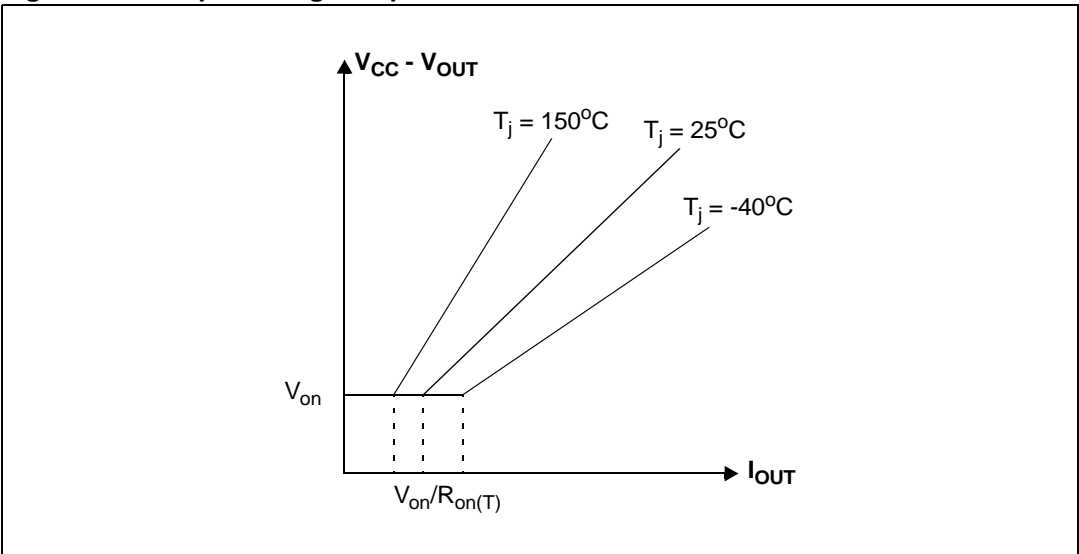


Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}

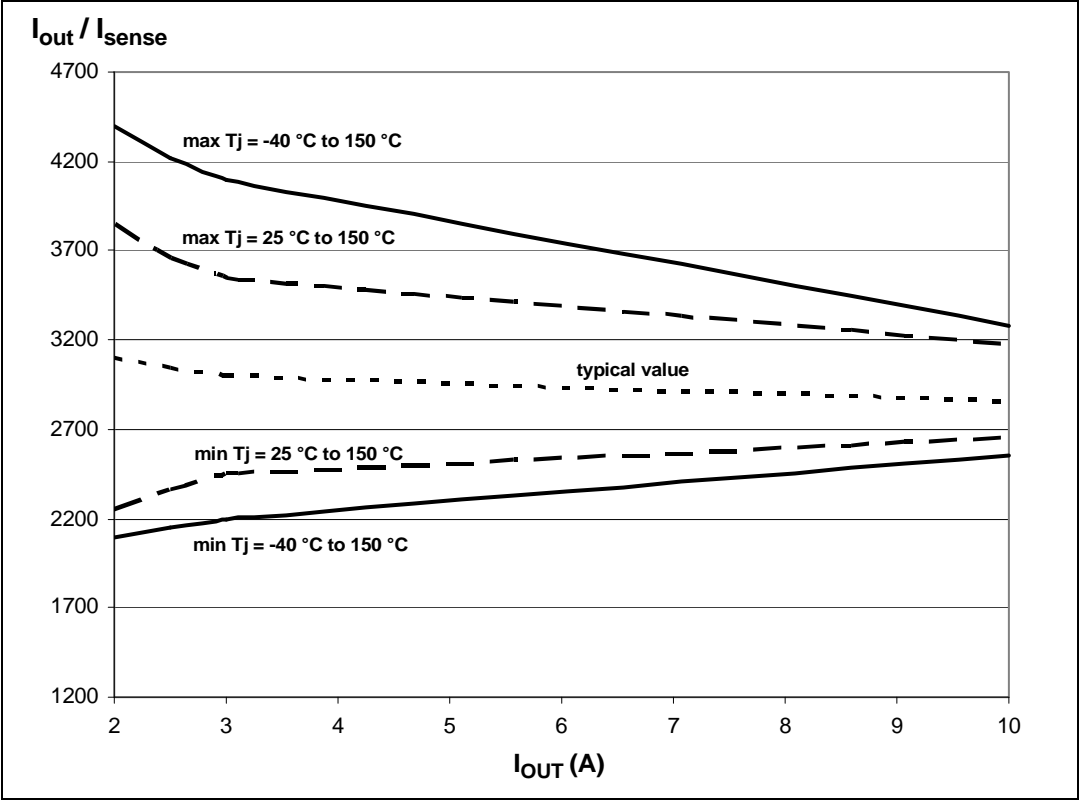
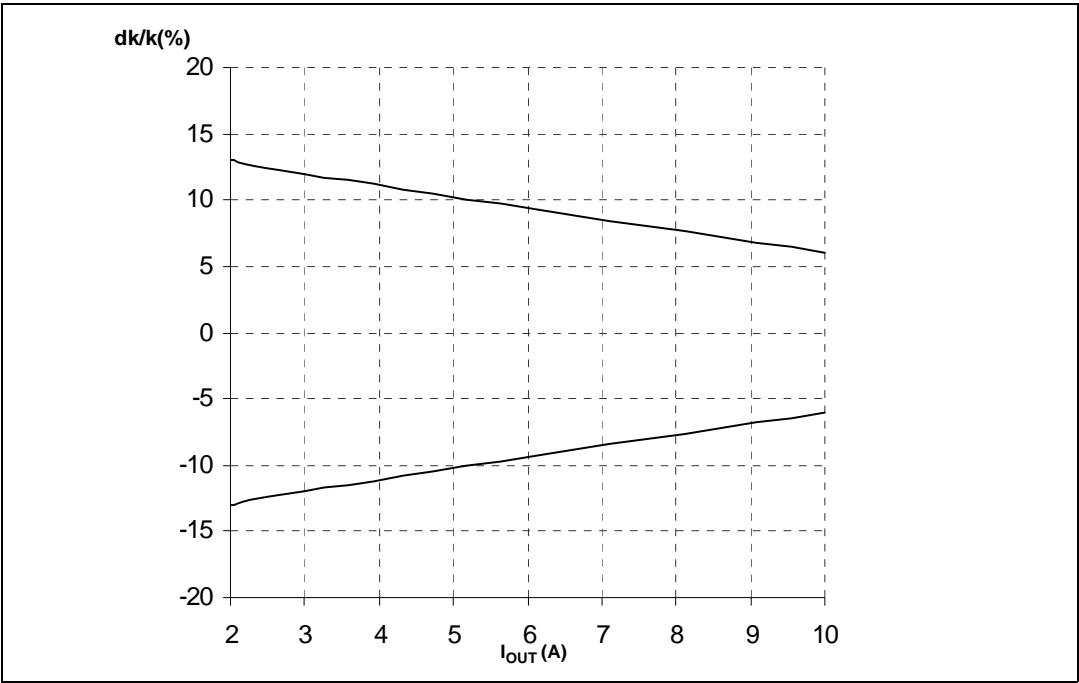


Figure 10. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense ($V_{CSD} = 0\text{ V}$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overload	H	X (no power limitation)	Nominal
	H	Cycling (power limitation)	V_{SENSEH}
Short circuit to GND (Power limitation)	L	L	0
	H	L	V_{SENSEH}
Open-load off-state (with external pull up)	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	L	H	V_{SENSEH}
	H	H	V_{SENSEH} < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1μs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1μs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b ⁽²⁾	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to $V_{CC} = 13.5V$ except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004E Test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽¹⁾	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

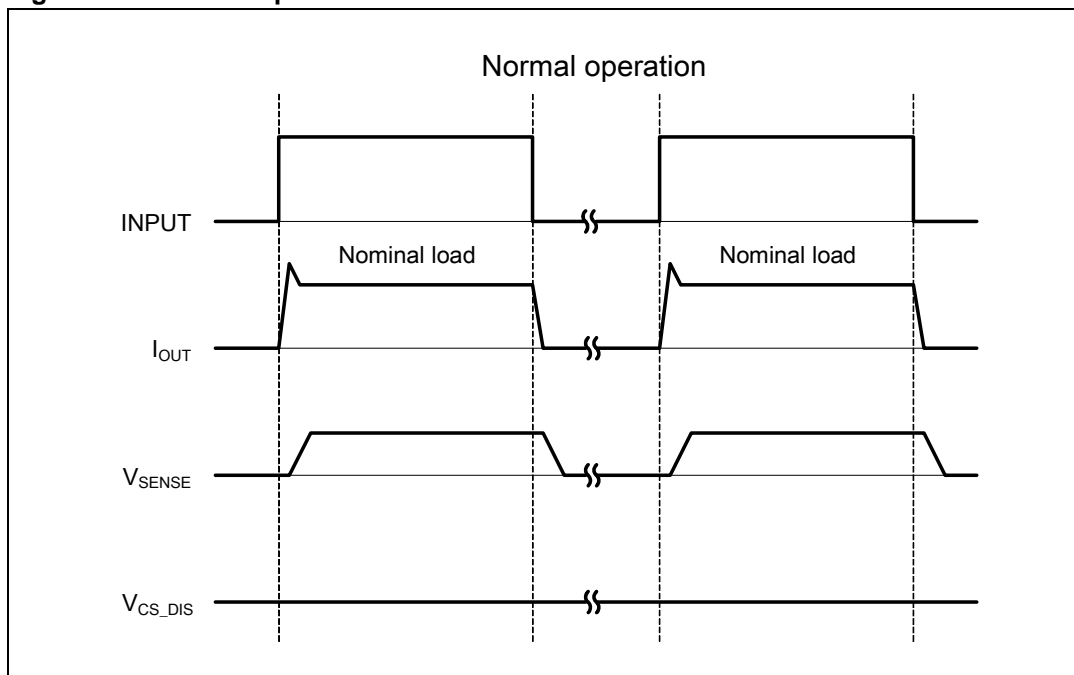


Figure 12. Overload or short to GND

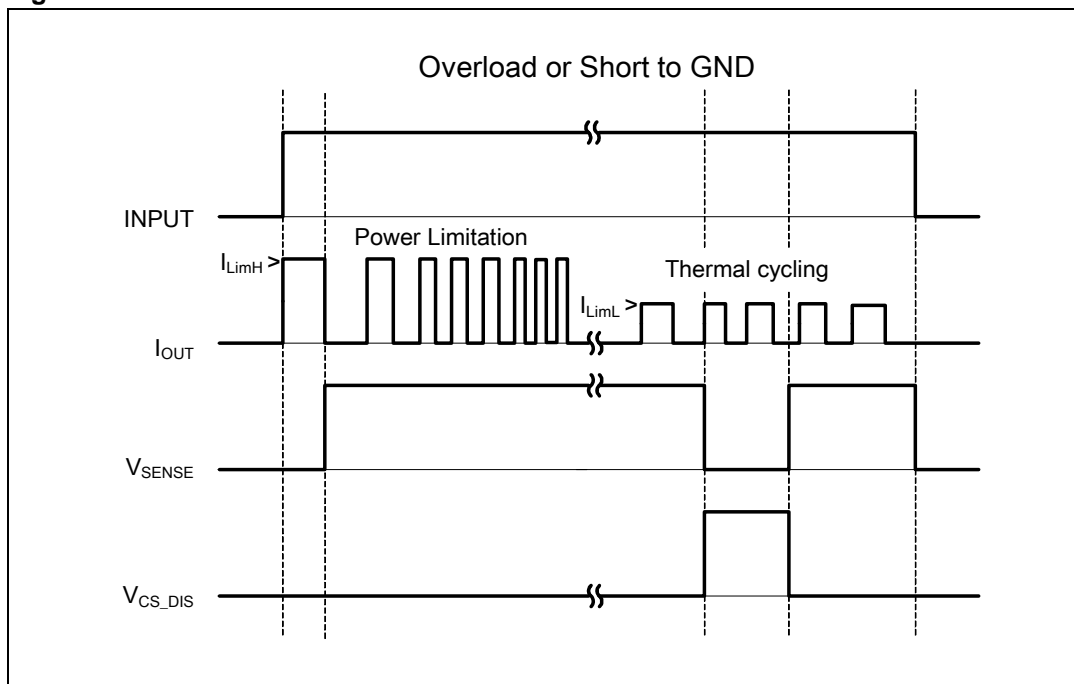


Figure 13. Intermittent overload

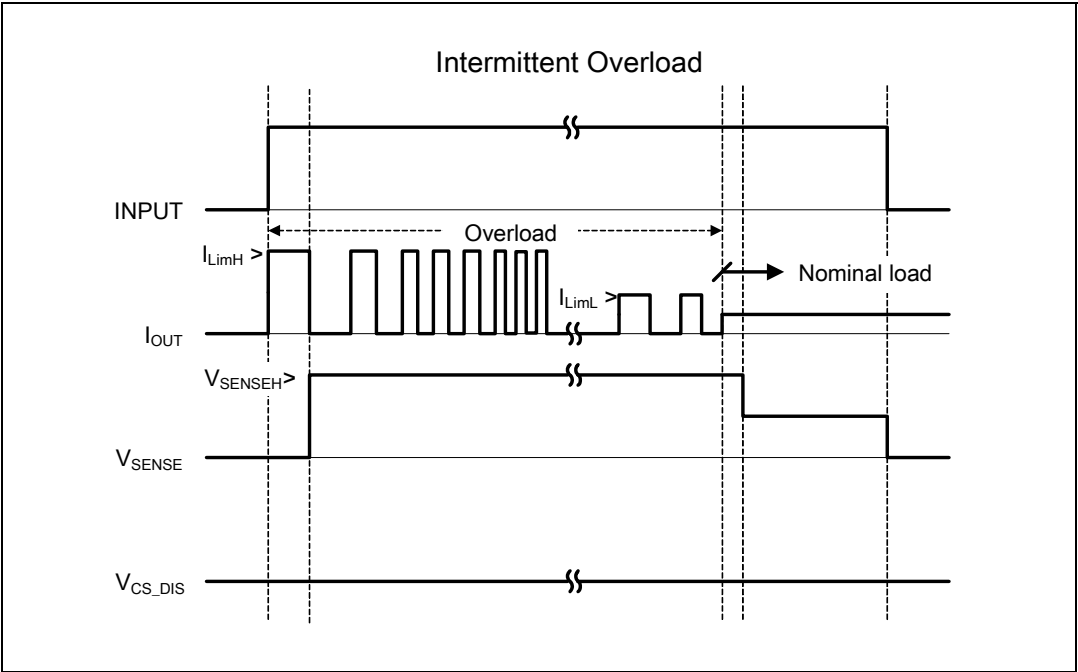


Figure 14. Off-state open-load with external circuitry

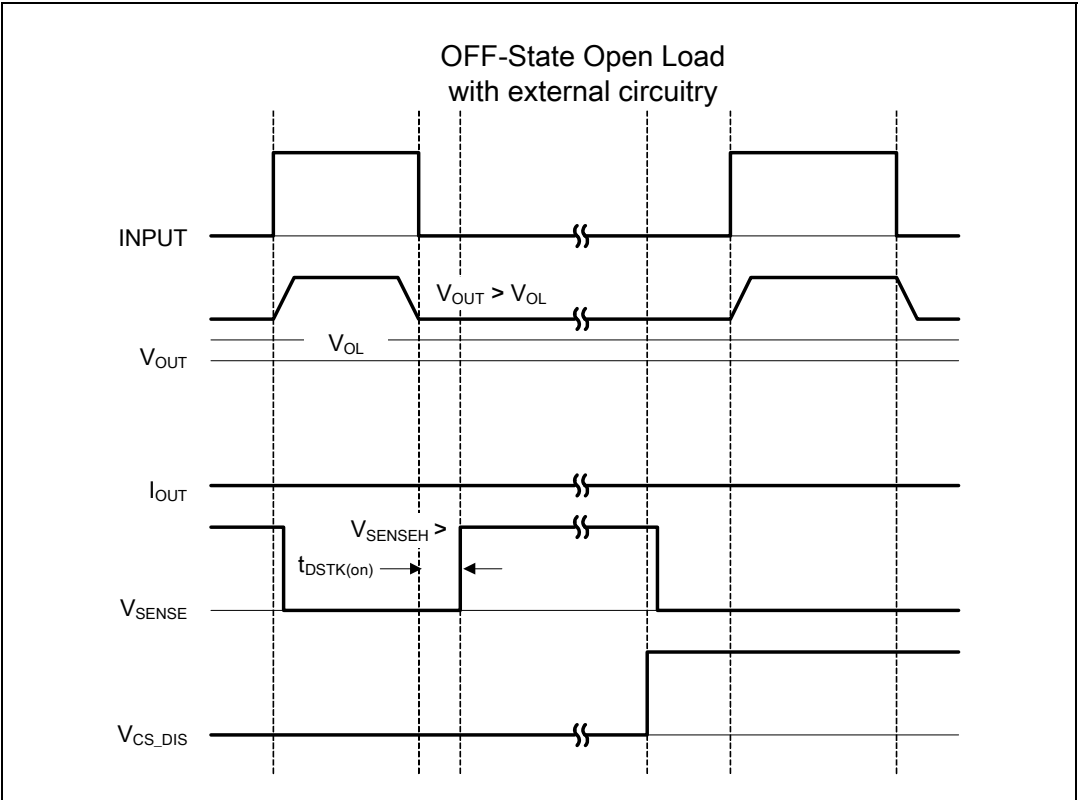


Figure 15. Short to V_{CC}

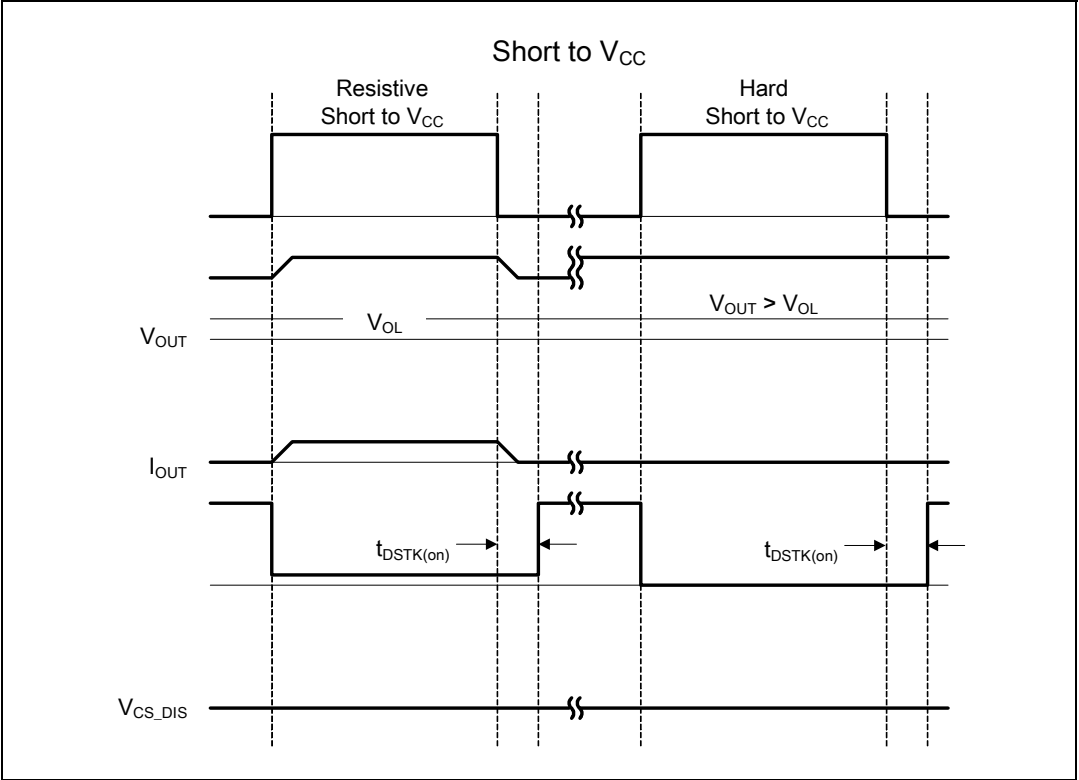
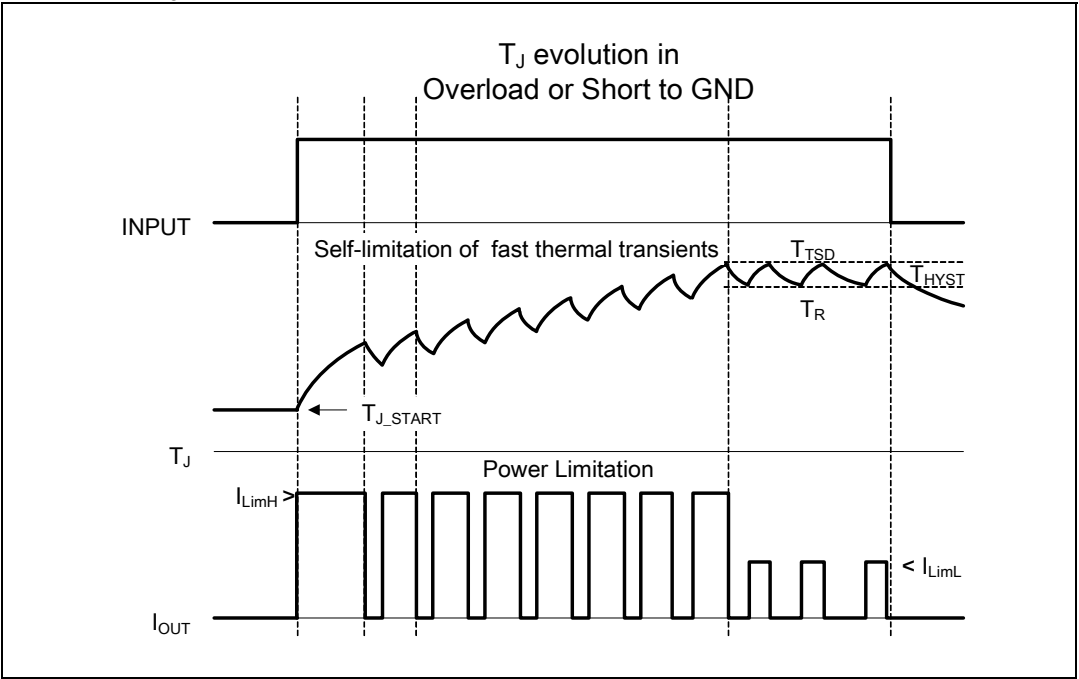


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

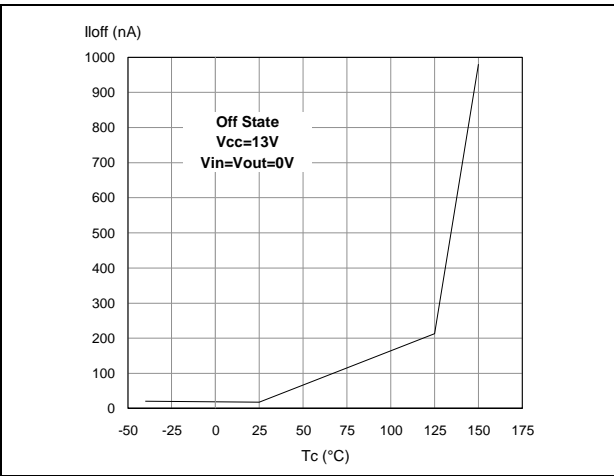


Figure 18. High level input current

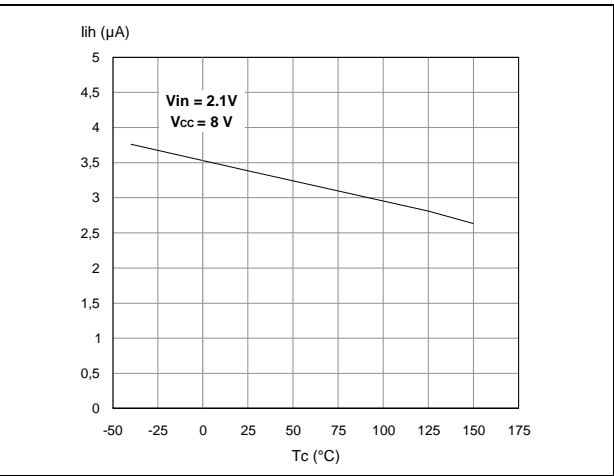


Figure 19. Input clamp voltage

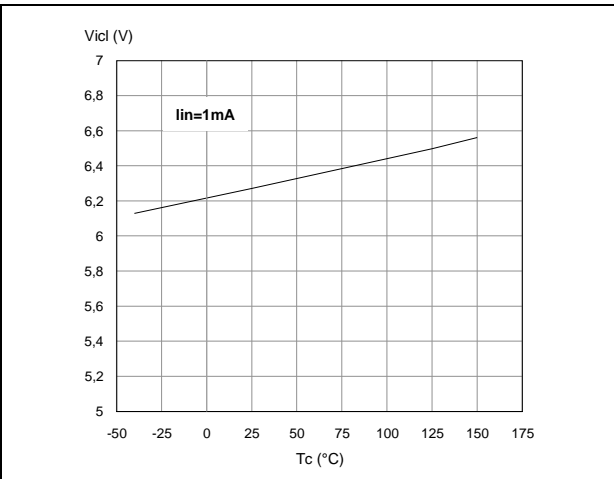


Figure 20. Input high level voltage

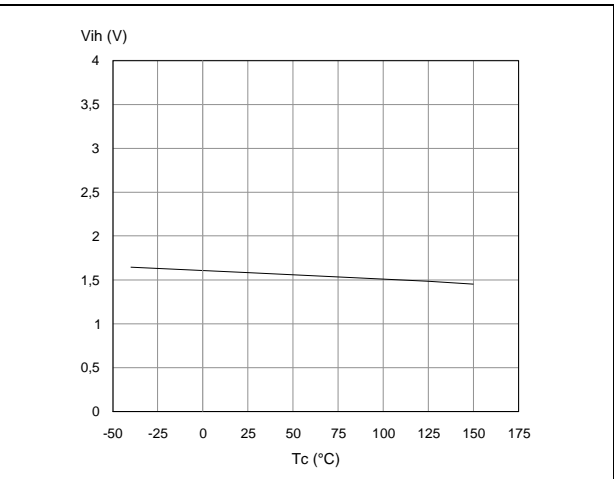


Figure 21. Input low level voltage

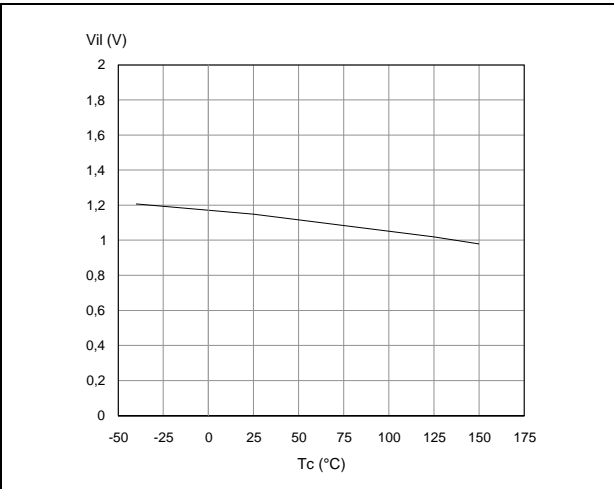


Figure 22. Input hysteresis voltage

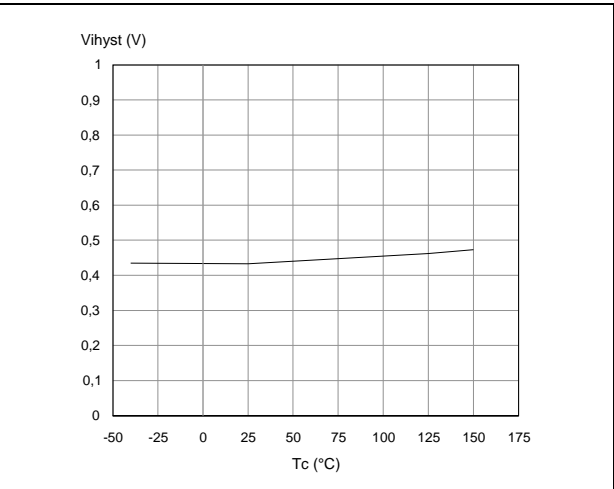


Figure 23. On-state resistance vs T_{case}

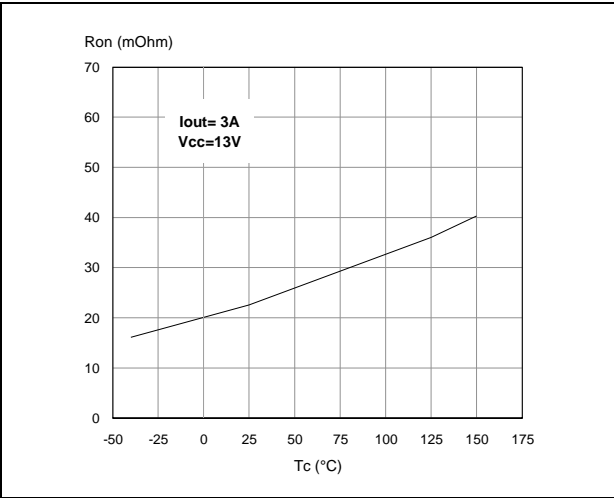


Figure 24. On-state resistance vs V_{cc}

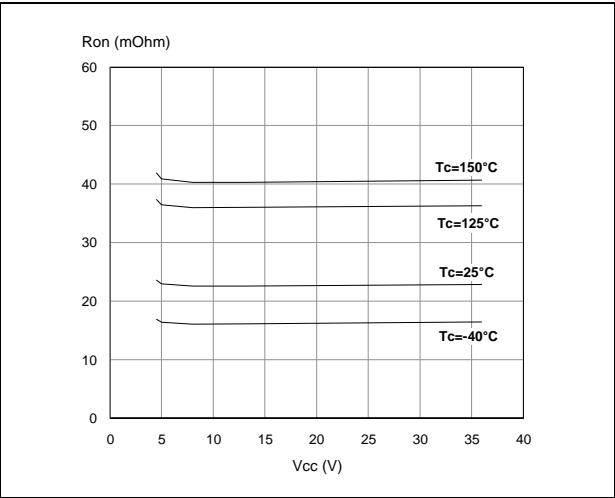


Figure 25. Undervoltage shutdown

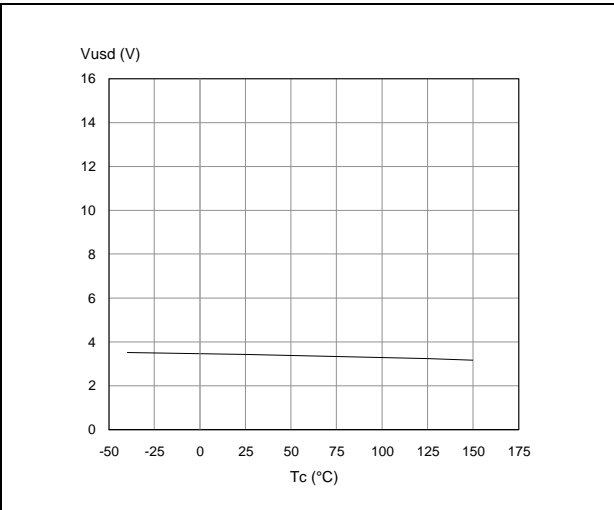


Figure 26. I_{LIMH} vs T_{case}

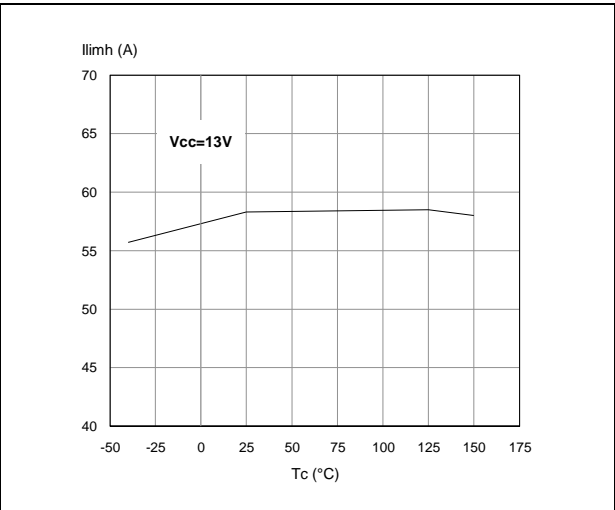


Figure 27. Turn-on voltage slope

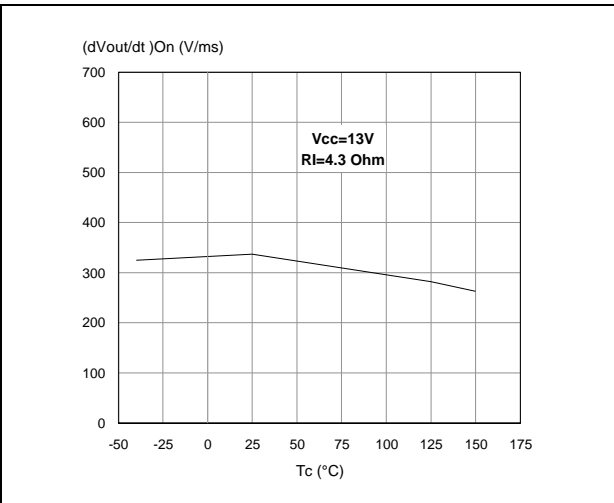


Figure 28. Turn-off voltage slope

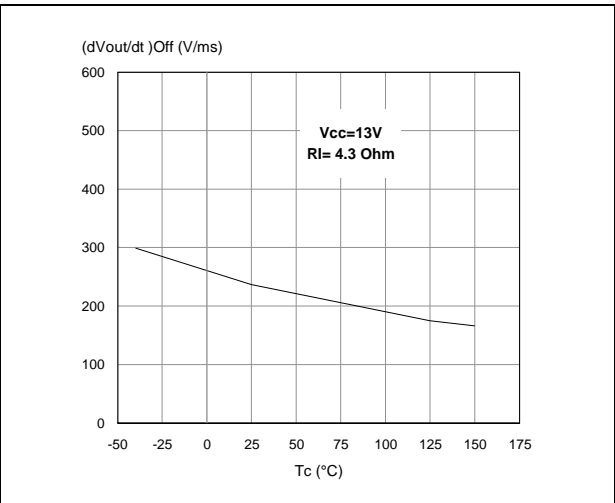


Figure 29. CS_DIS high level voltage

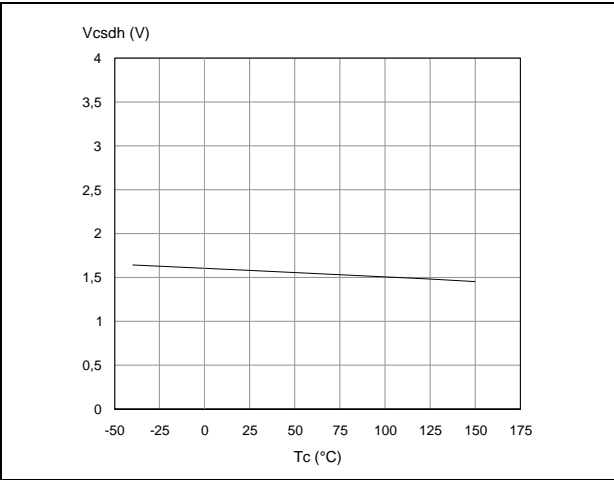


Figure 30. CS_DIS low level voltage

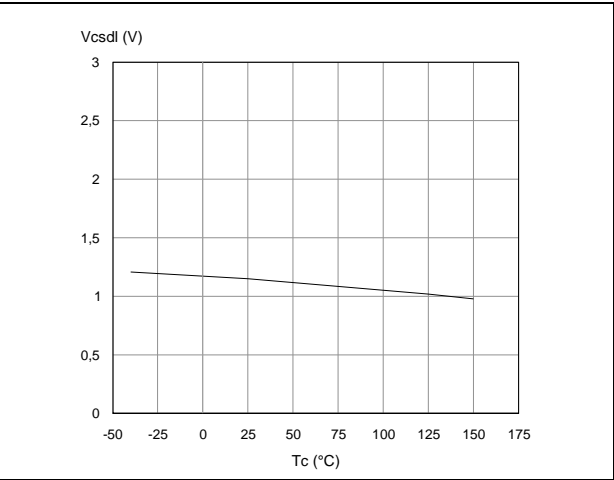
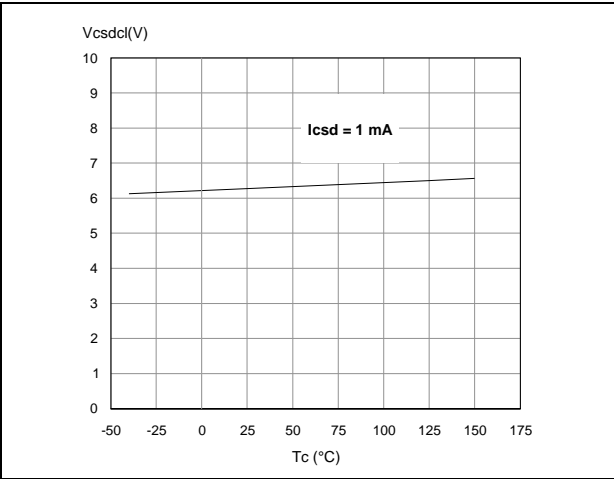
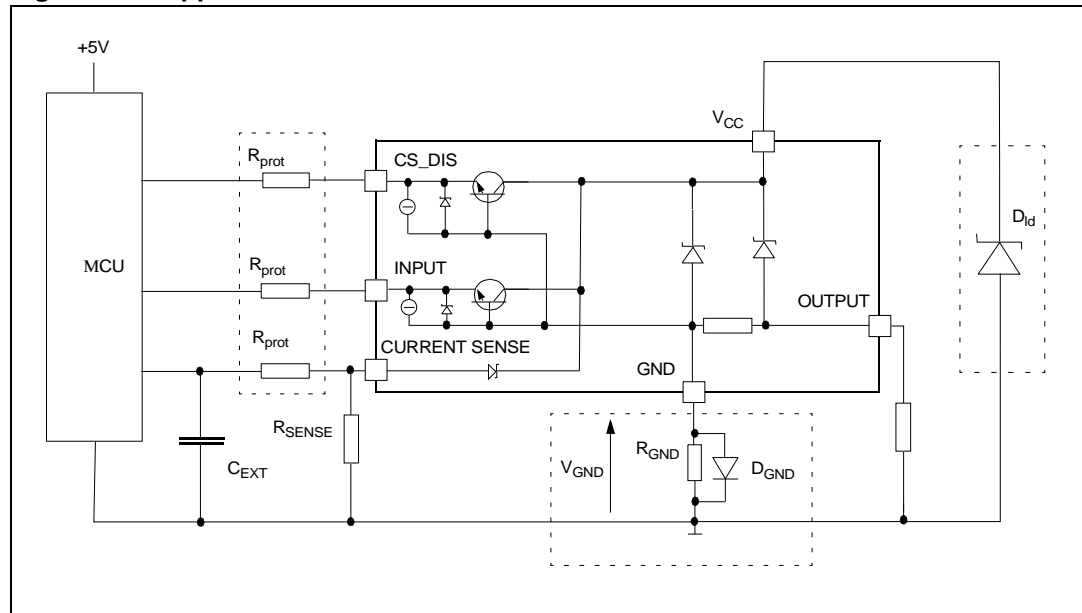


Figure 31. CS_DIS clamp voltage



3 Application information

Figure 32. Application schematic⁽¹⁾



1. Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{\text{GND}}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are On in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND}=1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift not varies if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values: $R_{prot}=10k\Omega$, $C_{EXT}=10nF$.

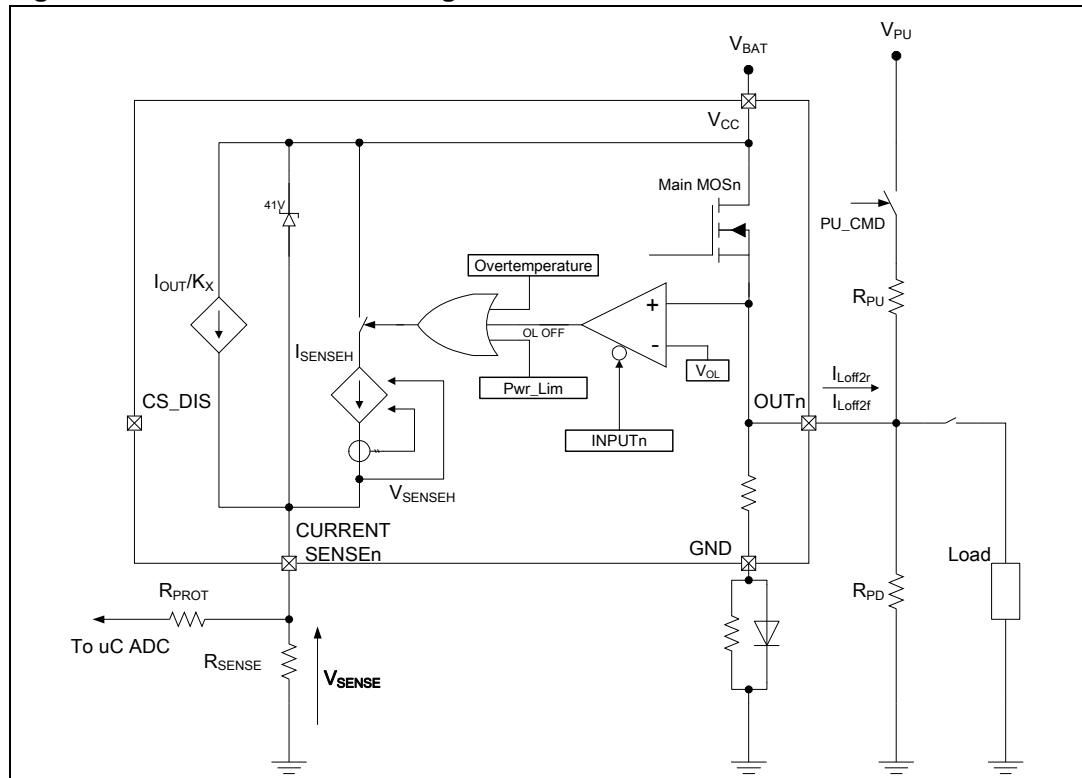
3.4 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 33: Current sense and diagnostic](#)):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load one according to a known ratio K_X . The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in [Table 9: Current sense \(\$8\text{ V} < V_{CC} < 18\text{ V}\$ \)](#)). The current sense accuracy depends on the output current (refer to current sense electrical characteristics [Table 9: Current sense \(\$8\text{ V} < V_{CC} < 18\text{ V}\$ \)](#)).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to [Table 11: Truth table](#)):
 - Power limitation activation
 - Overtemperature
 - Short to V_{CC} in off-state
 - Open-load in off-state with additional external components.

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostic



3.4.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

Off-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

An external pull down resistor R_{PD} connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see [Figure 33: Current sense and diagnostic](#)).

R_{PD} must be selected in order to ensure V_{OUT} < V_{OLmin} unless pulled up by the external circuitry:

$$V_{OUT}|_{Pull-up_OFF} = R_{PD} \cdot I_{L(off)2f} < V_{OLmin} = 2V$$

R_{PD} ≤ 22 KΩ is recommended.

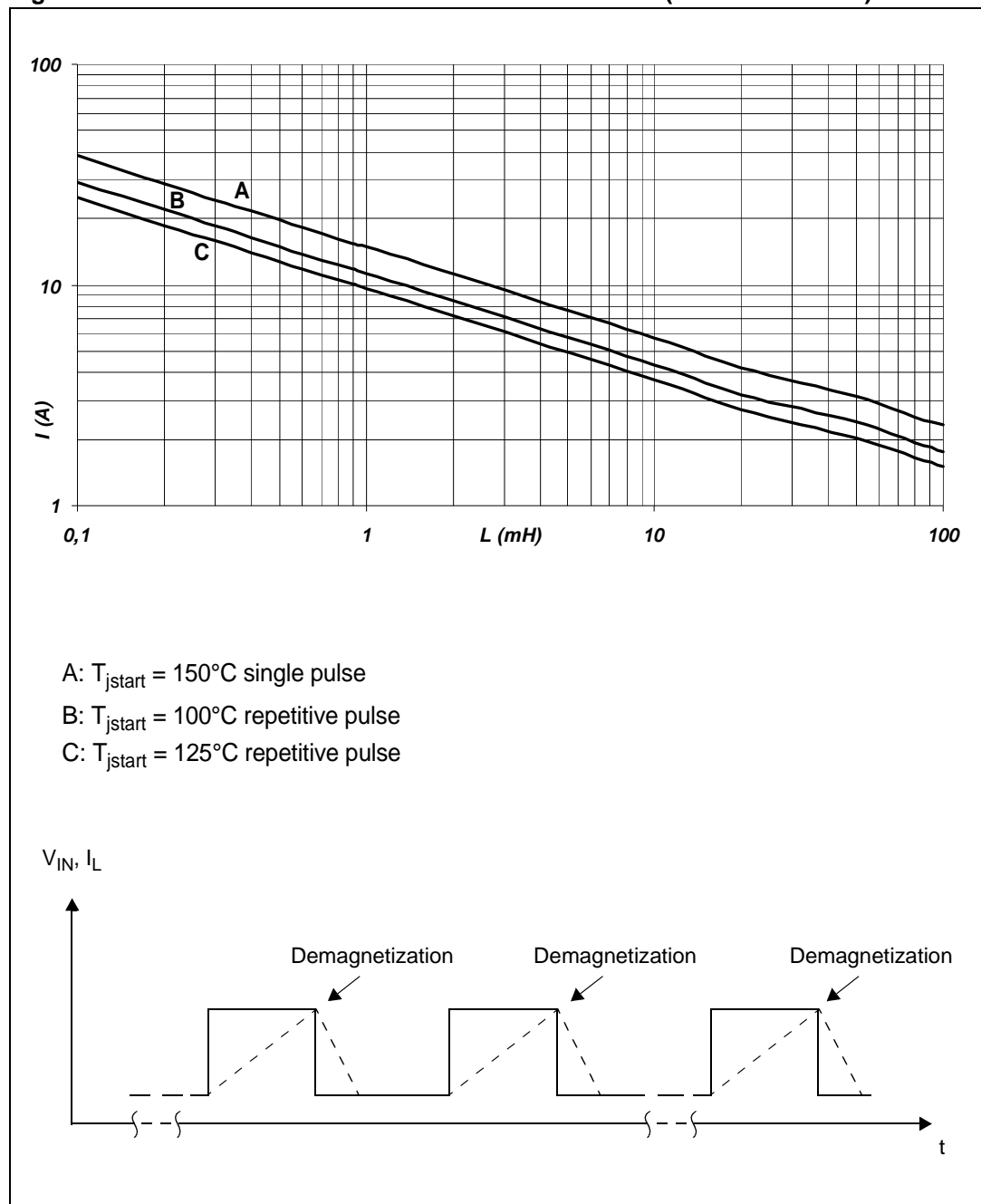
For proper open-load detection in off-state, the external pull-up resistor must be selected according to the following formula:

$$V_{OUT}|_{Pull-up_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off)2r}}{R_{PU} + R_{PD}} > V_{OLmax} = 4V$$

For the values of V_{OLmin}, V_{OLmax}, I_{L(off)2r} and I_{L(off)2f} see [Table 10: Open-load detection \(8 V < V_{CC} < 18 V\)](#).

3.5 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 34. Maximum turn-off current versus inductance (for each channel)⁽¹⁾

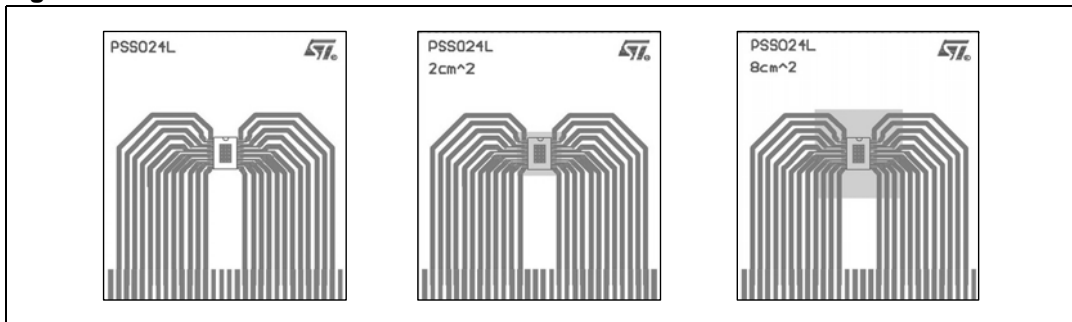


1. Values are generated with $R_L = 0\ \Omega$.
 In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and thermal data

4.1 PowerSSO-24 thermal data

Figure 35. PowerSSO-24 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area = 77 mm x 86mm, PCB thickness = 1.6 mm, Cu thickness = 70 μ m (front and back side), Copper areas: from minimum pad layout to 8 cm²).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

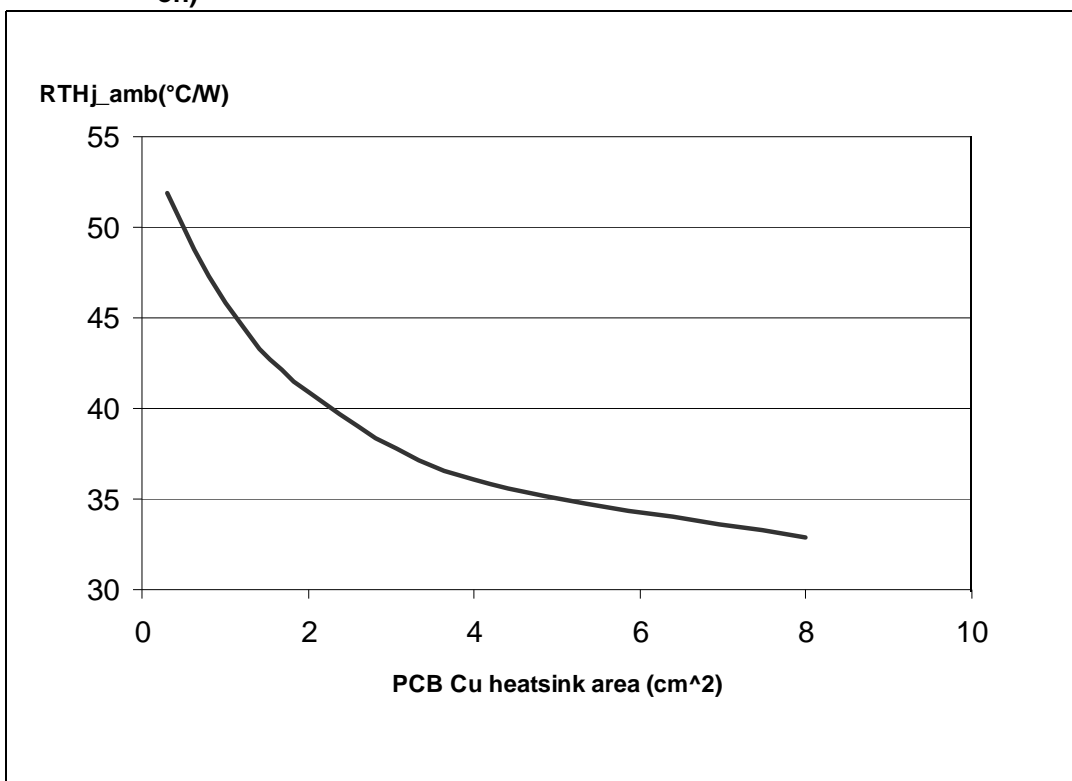
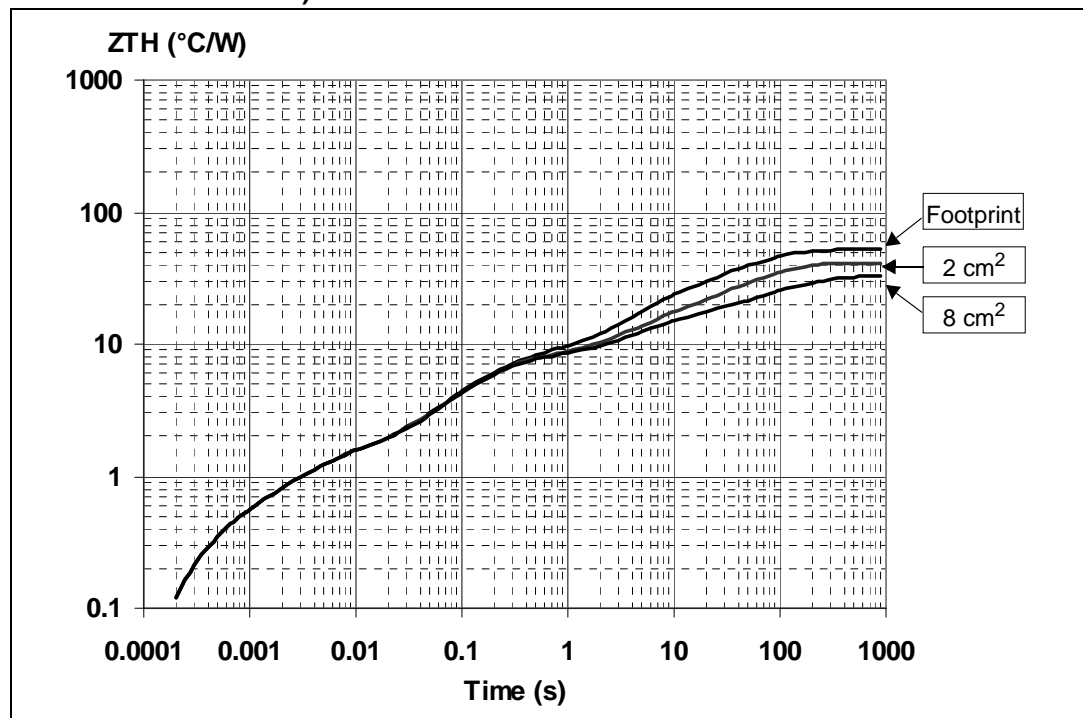


Figure 37. PowerSSO-24 thermal impedance junction to ambient single pulse (one channel on)

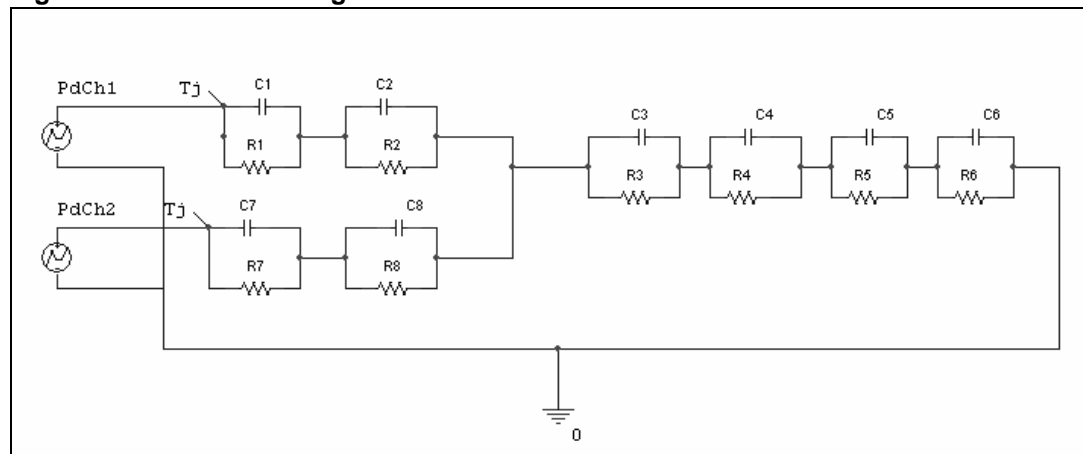


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-24⁽¹⁾



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area/Island (cm ²)	Footprint	2	8
R1 (°C/W)	0.28		
R2 (°C/W)	0.9		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
R7 (°C/W)	0.28		
R8 (°C/W)	0.9		
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.003		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17
C7 (W.s/°C)	0.001		
C8 (W.s/°C)	0.003		

5 Package and packing information

5.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 Package mechanical data

Figure 39. PowerSSO-24 package dimensions

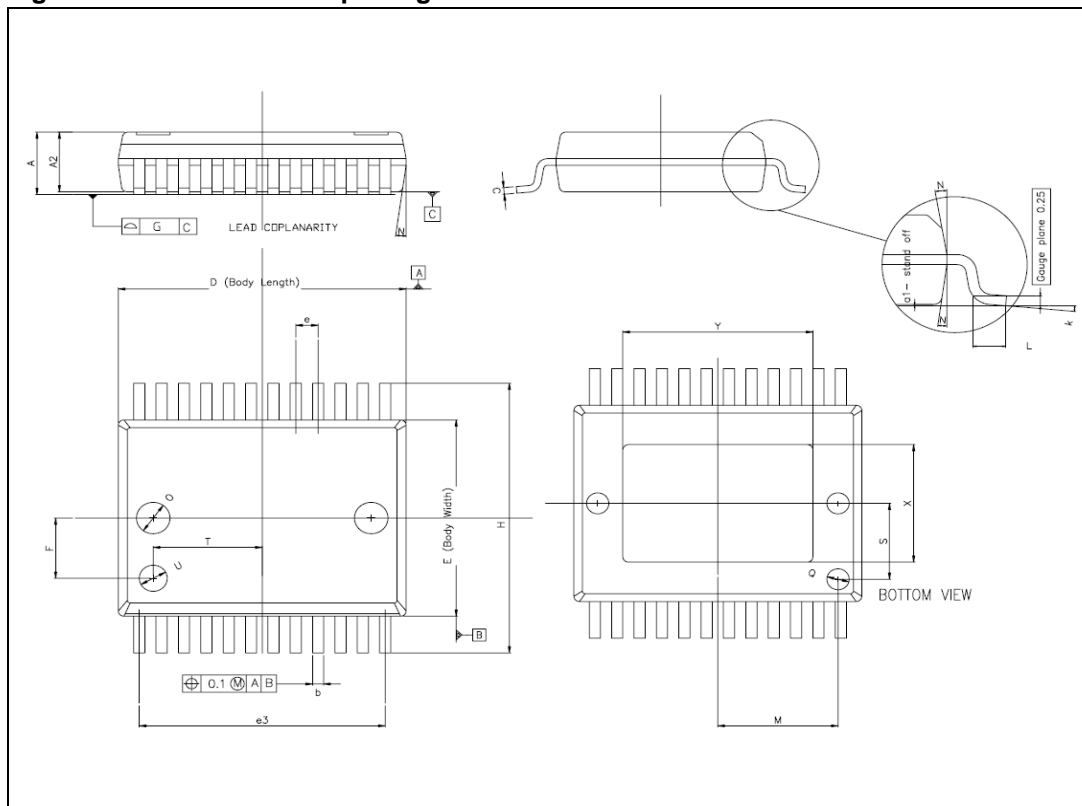


Table 16. PowerSSO-24™ mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			2.45
A2	2.15		2.35
a1	0		0.1
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
F		2.3	
G			0.1
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
N			10°
X	4.1		4.7
Y	6.5		7.1

5.3 Packing information

Figure 40. PowerSSO-24 tube shipment (no suffix)

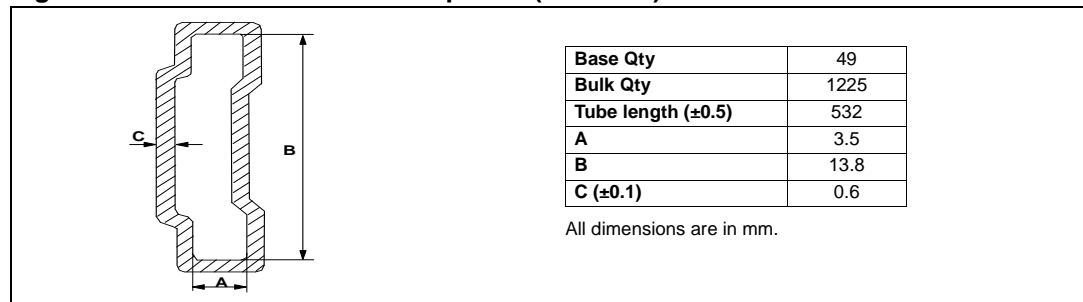
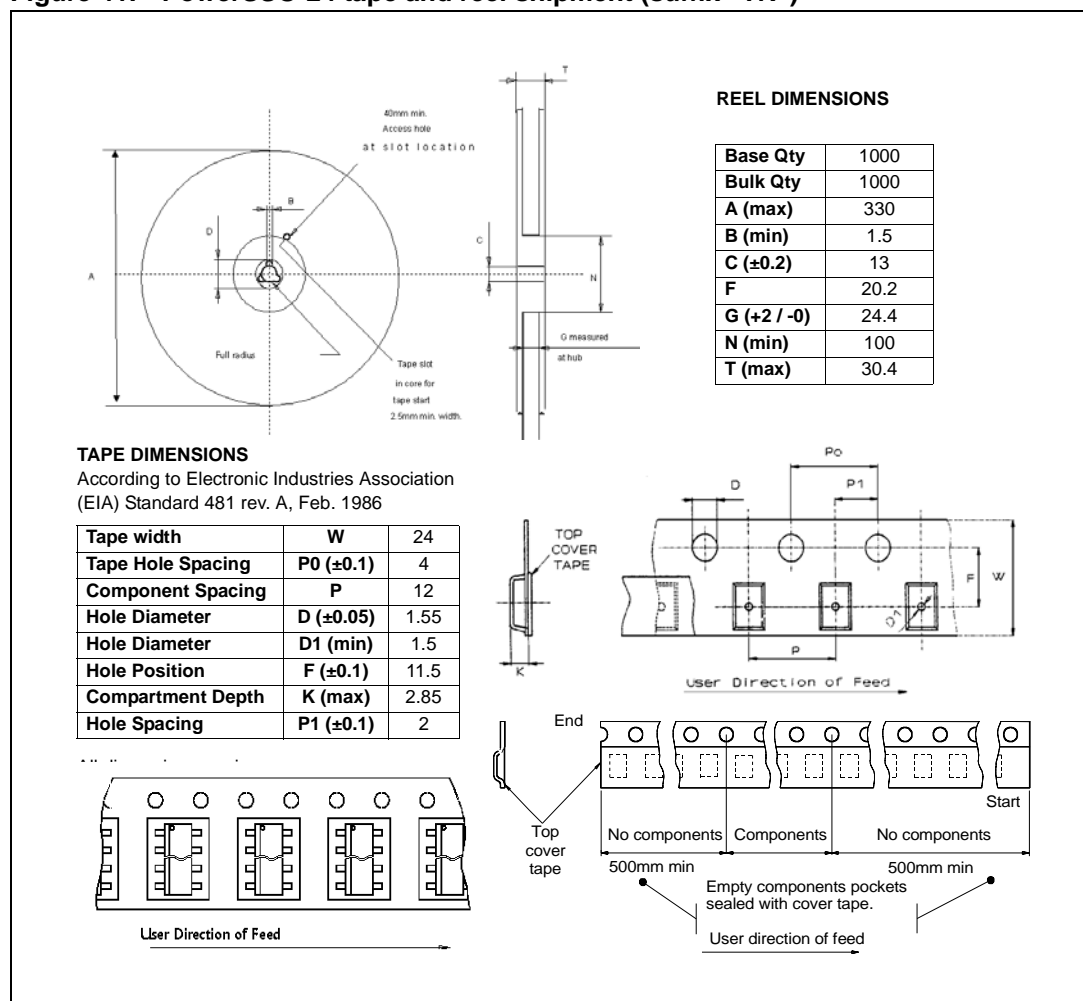


Figure 41. PowerSSO-24 tape and reel shipment (suffix “TR”)



6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VND5E025AK-E	VND5E025AKTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
01-Apr-2008	1	Initial release
19-Jun-2009	2	Table 16: PowerSSO-24 mechanical data: <ul style="list-style-type: none"> – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F row – Updated k row
22-Jul-2009	3	Updated Figure 39: PowerSSO-24 package dimensions. Updated Table 16: PowerSSO-24™ mechanical data: <ul style="list-style-type: none"> – Deleted G1 row – Added O, Q, S, T and U rows
28-May-2010	4	Updated Features list.
19-Sep-2013	5	Updated disclaimer.

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